

## DESIGN AND OPTIMIZATION OF A P+N+IN+ TUNNEL FET

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**Abstract-** Tunnel FETs are interesting devices for their steep sub-threshold slopes. In this paper a p+n+in+ tunnel FET is proposed and optimized for a high  $I_{on}/I_{off}$  ratio and suitable output characteristics. The proposed tunnel FET has p+in+ structure with a  $\delta$ -doped n+ region at the beginning of the channel. The proposed structure is extensively studied and the energy bands, transfer characteristics, and output characteristics are investigated. In this study, the width and the doping level of n+  $\delta$ -doped region are optimized aiming at increasing the  $I_{on}/I_{off}$  ratio and improving the output characteristics. Moreover, the channel doping is varied in order to improve on/off characteristics. Simulations show that the proposed transistor exhibits  $I_{on}/I_{off}$  ratio as high as  $10^9$ . Also, linear and saturation regions in the output characteristics are evident, much like a MOSFET.

**Keywords:** Tunnel FET,  $I_{on}/I_{off}$  Ratio, Band-to-Band Tunnelling, Off-Current.

### I. INTRODUCTION

Aggressive MOSFET scaling gives rise to a number of critical issues such as source/drain-to-channel electrostatic coupling, channel transport limitations, gate tunnelling current and parasitic effects [1]. Due to short-channel effects (SCEs) such as drain-induced barrier lowering (DIBL), surface scattering, and hot carrier effects, high  $I_{off}$  and reduced  $I_{on}/I_{off}$  ratio occurs for MOSFETs having channels smaller than 65 nm [2, 3]. This is because fundamental physics of MOSFETs limits the minimum of sub-threshold swing (SS) to 60 mV/dec. Moreover, with shrinking dimensions, power dissipation is becoming a major concern. As a result, reduction in  $I_{off}$  is necessary for low leakage current and low standby power systems. To overcome these problems, new engineering solutions like improving the structure of the device, considering different materials with various features (Si, SiGe, Ge, etc) in the channel region [4, 5, 6], and new dielectric (high- $k$ ) [7] are suggested, some of which are being used for a better exploitation of these devices. In recent years, different devices are studied to obtain a minimum  $I_{off}$  and a maximum ratio of  $I_{on}/I_{off}$  [7].

Tunnel FETs (TFETs) which can exhibit SS lower than 60 mV/dec [11, 12] are interesting candidates for low standby power applications [13-15]. TFETs turn to on

state based on band to band tunneling (BTBT) [15-19] and have the potential for very low off current with a sub-threshold swing beyond 60 mV/dec limit of conventional MOSFETs [12, 20]. Various TFETs are investigated in the literature, for example, with gate overlap/underlap [21], strained channel [22] and high- $k$  gate dielectric [23].

Although TFETs have low off-state current, but on-state current is not acceptably high [24, 13]. This results in low  $I_{on}/I_{off}$  ratio (on the order of  $10^3$ ~ $10^6$  [25]) which limits application of TFETs in digital circuits [21]. Therefore new TFET designs are needed in order to attain high  $I_{on}/I_{off}$  ratio. In order to increase on state current a SiGe delta layer at the edge of the source [26], SiGe [26], Ge [19] in the source region, double gate with a SiGe source [27] and high- $k$  dielectric [21] is used. Using high- $k$  gate dielectric improves on state current. Using Germanium with a lower band gap as the source material improves  $I_{on}/I_{off}$  ratio significantly [19]. In [28] in order to increase on state current, dual material gate TFET is studied. The double gate architecture has been reported in [27]. In this paper a p-i-n TFET with a delta-doped n+ at the source side is proposed and optimized for high  $I_{on}/I_{off}$  ratio and good output characteristics.

### II. DEVICE STRUCTURE

The tunnel FET structure in this paper has four regions (p+n+in+) in which the source region is p+ layer, the drain region is n+ and the channel is  $i$  region (lightly doped p). In order to enhance tunnelling, a  $\delta$ -doped n+ region is inserted at the beginning of the channel. The gate oxide and contact has a small overlap with the source and drain regions. Figure 1 depicts the tunnel FET structure studied in this paper. In this structure the width of the active layer is  $t_{si}=60$  nm, the gate oxide and buried oxide thicknesses are  $t_{ox}=2.5$  nm and  $t_{box}=100$  nm respectively. The  $\delta$ -doped n+ width is varied between  $W=1$  nm and 15 nm in order to pursue the best  $W$ . The channel length is considered  $L_{ch}=100$  nm, the source and the drain doping levels are  $2 \times 10^{20}$  /cm<sup>3</sup>, the channel doping  $10^{16}$  /cm<sup>3</sup>, and  $\delta$ -doped n+ region  $10^{19}$  /cm<sup>3</sup>. Table 1 summarizes the device parameters.

Simulations are performed using Atlas Silvaco device simulator, and analytic calculations according to tunnelling equations are performed in Matlab environment. Analytic calculations are based on band- to-

band tunnelling (BTBT) model [8, 9]. The gate and the drain voltages are swept from -0.5 to 2 V. The transfer and the output characteristics and  $I_{on}/I_{off}$  ratio are studied. To optimize the device characteristics, the width of  $\delta$ -doped n+ region is changed from  $W=1$  nm to 15 nm and the results are studied in order to optimize the width of this region. Also, the breakdown voltage in the output characteristics is studied.

After obtaining a suitable  $W$ , the value of the channel doping is optimized. Finally, extensive device simulations were performed using Atlas Silvaco device simulator coupled with analytical tunnelling calculations. The tunnelling calculations in our TFET were based on the well-known equations for tunnelling current [1].

$$I_t = I_{(C \rightarrow V)} - I_{(V \rightarrow C)} = A \int_{E_C}^{E_V} [F_c(E) - F_v(E)] \times T_t(E) n_c(E) n_v(E) dE \quad (1)$$

According to this equation, the drain current is proportional to the tunnelling probability  $T(E)$ , which is obtained as following [10]:

$$T(E) \propto \left( -\frac{4\sqrt{2m^* E_g^{3/2}}}{3|e|\hbar(E_g + \Delta\Phi)} \sqrt{\frac{\epsilon_{si}}{\epsilon_{ox}} t_{ox} t_{si}} \right) \Delta\Phi \quad (2)$$

In this equation  $m^*$  is the electron effective mass,  $E_g$  is band gap,  $\Delta\Phi$  is the energy range over which tunnelling can take place, and  $t_{ox}$ ,  $t_{si}$ ,  $\epsilon_{ox}$ ,  $\epsilon_{si}$  are the oxide and silicon films thickness and dielectric constants respectively, and  $\hbar$  is the reduced Planck's constant.

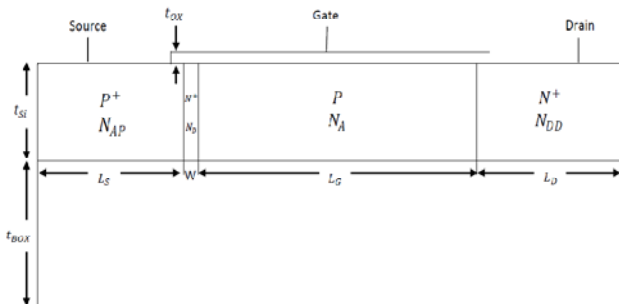


Figure 1. Device structure of the pnin tunnel FET

Table 1. Device parameters

$N_D$ (cm <sup>-3</sup> )	1e19	$N_A$ (cm <sup>-3</sup> )	1e16
$W$ (nm)	1-15	$N_{AP}$ & $N_{DD}$ (cm <sup>-3</sup> )	2e20
$T_{OX}$ (Å)	25	$L_{channel}$ (nm)	100
$T_{si}$ (nm)	60	$L_s$ & $L_D$ (nm)	50
$T_{BOX}$ (nm)	100	Gate work function	n-poly

### III. SIMULATION RESULTS

In Figure 2 conduction and valance bands of the tunnel FET are depicted with  $W=1$  nm,  $V_{DS}=1$  V, and  $V_{GS}=0$  & 1 V. As this figure shows when the gate voltage is 0 V, there is no region for tunnelling (i.e. there is no allowed energy levels for the electrons in the source valance band aligned with empty levels in the channel conduction band), but when the gate voltage is 1 V, the conduction band of the channel is lower than the valance band of the source. As a result, electrons of the source

valance band can tunnel to the channel conduction band through the energy gap. Figures 3 and 4 show the drain current versus gate voltage for the drain voltages of 0.2, 0.4, 0.5, 0.6, 1 V, and two values of  $W=1$  and 2 nm, respectively. According to these figures,  $I_{on}$  is the same for the two values of  $W$ , but  $I_{off}$  is lower for  $W=2$  nm.

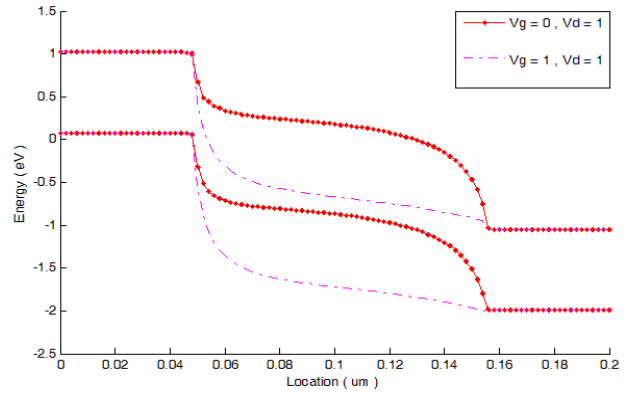


Figure 2. Energy bands for  $W=1$  nm,  $V_{DS}=1$  V,  $V_{GS}=0.1$  V

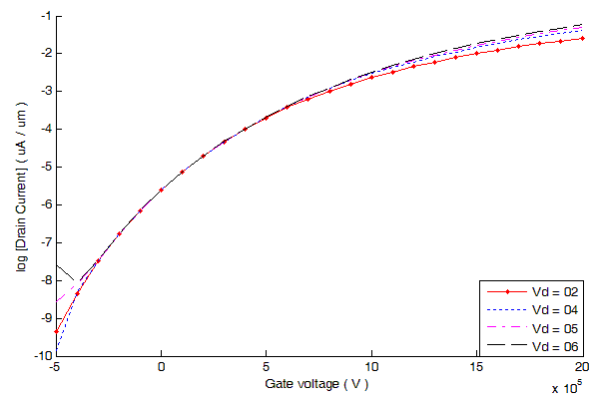


Figure 3. Drain current versus  $V_{GS}$  for  $W=1$  nm, with  $V_{DS}=0.2, 0.4, 0.5, 0.6$  and 1 V

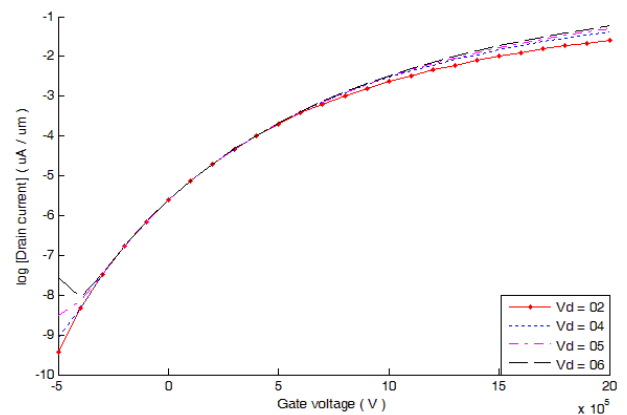


Figure 4. Drain current versus  $V_{GS}$  for  $W=2$  nm, with  $V_{DS}=0.2, 0.4, 0.5, 0.6$  and 1 V

In Figures 5 and 6 the output characteristics of the tunnel FET are depicted for  $-0.5 \text{ V} \leq V_{DS} \leq 2 \text{ V}$ , with the gate voltage as the parameter ( $V_{GS} = 0, 0.2, 0.4, 0.6, 0.8, 1 \text{ V}$ ) and two values of  $W=1$  and 2 nm. The output characteristics of this tunnel FET are very similar to the output characteristics of the MOSFETs and the linear and saturation regions are evident.

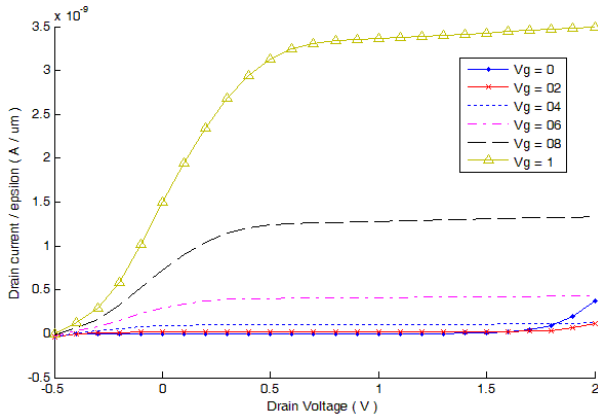


Figure 5. Output characteristics of the tunnel FET for  $W=1$  nm,  $V_{GS}$  is the parameter

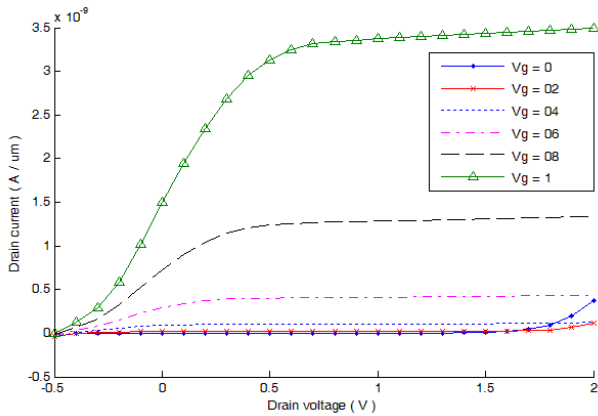


Figure 6. Output characteristics of the tunnel FET for  $W=2$  nm,  $V_{GS}$  is the parameter

In order to find breakdown voltages, the output characteristics are plotted in Figure 7 up to  $V_{DS}=3.5$  V and  $V_{GS}$  as the parameter. As this figure shows, increasing the gate voltage decreases the breakdown voltage. It must be noted that since the breakdown voltage occurs due to high electric field at the drain side,  $W$  has no effect on the breakdown voltage.

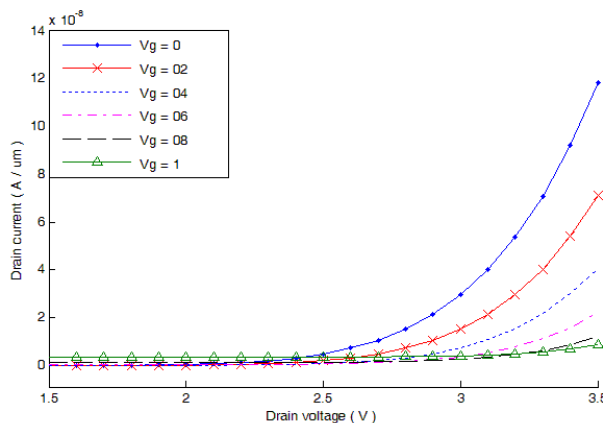


Figure 7. Output characteristics of the tunnel FET for  $W=1$  nm,  $V_{GS}$  is the parameter

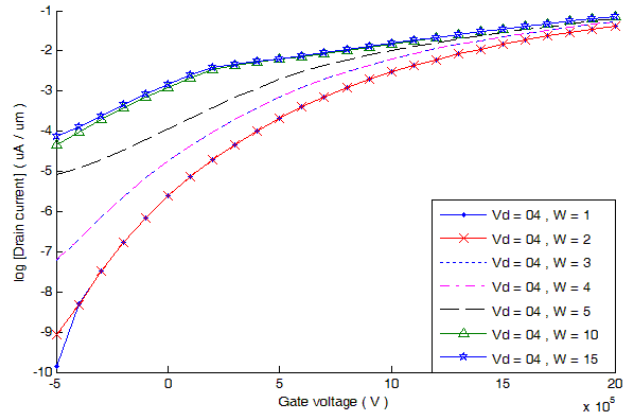


Figure 8. Drain current versus  $V_{GS}$  at  $V_{DS}=0.4$  V and  $W=1$  to 15 nm

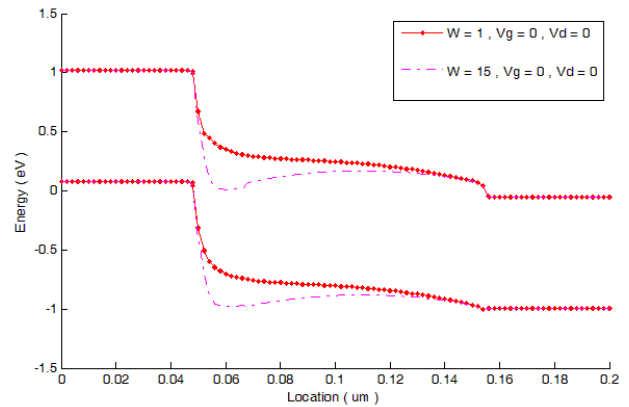


Figure 9. Energy bands at  $V_{DS}=V_{GS}=0$  for two values  $W=1$  and  $W=2$  nm

#### IV. OPTIMIZING W

The tunnelling probability depends considerably on the value of  $W$ . Figure 8 shows the drain current versus  $V_{GS}$  at  $V_{DS}=0.4$  and from  $W=1$  nm up to  $W=15$  nm. With a small  $W$ , the tunnelling probability decreases which results in low off-current. On the other hand, with a large  $W$ , the tunnelling probability increases which in turn increases the on-current. Increasing  $I_{on}$  is important in tunnel FETs [1]. But with increasing  $W$ , at the same time, the off-current increases substantially which results in a low  $I_{on}/I_{off}$  ratio. Low  $I_{on}/I_{off}$  ratio prevents proper switching of the transistor from on to off state. It seems that  $W=2$  nm is an optimum value for the  $\delta$ -doped region width.

Figure 9 depicts energy bands at  $V_{DS}=V_{GS}=0$  and two values  $W=1$  nm and  $W=15$  nm. At  $W=1$  nm, there is no region for tunnelling, which causes a low  $I_{off}$ , i.e. a good off state. On the other hand, at  $W=15$  nm, there exist a narrow tunnelling region at zero bias. This increases  $I_{on}$  which is desirable, but this tunnelling region increases  $I_{off}$  orders of magnitude, and consequently  $I_{on}/I_{off}$  ratio decreases substantially.

As figure 10 shows, the  $I_{on}/I_{off}$  ratio reveals monotonic decrease up to  $W=5$  nm, after which this ratio remains essentially constant. At  $W=1$  nm the  $I_{on}/I_{off}$  ratio is about  $10^9$ . This is comparable to conventional MOSFETs.

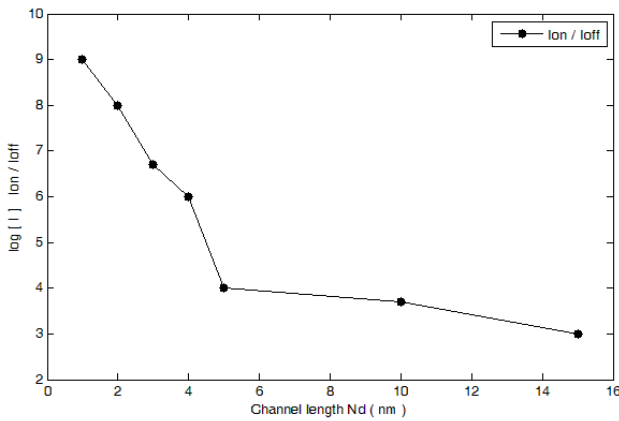


Figure 10.  $I_{on}/I_{off}$  ratio versus  $W$

### V. CONCLUSIONS

In this paper a p+n+in+ tunnel FET is proposed and its structure is optimized in the form of  $\delta$ -doped width and channel doping. The proposed structure has a high  $I_{on}/I_{off}$  ratio and proper output characteristics. The obtained  $I_{on}/I_{off}$  ratio is about  $10^9$  which is about 3 orders better than [1].

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