# Design and Performance of a Bidirectional Isolated DC–DC Converter for a Battery Energy Storage System

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*Abstract*—This paper describes the design and performance of a 6-kW, full-bridge, bidirectional isolated dc–dc converter using a 20-kHz transformer for a 53.2-V, 2-kWh lithium-ion (Li-ion) battery energy storage system. The dc voltage at the high-voltage side is controlled from 305 to 355 V, as the battery voltage at the lowvoltage side (LVS) varies from 50 to 59 V. The maximal efficiency of the dc–dc converter is measured to be 96.0% during battery charging, and 96.9% during battery discharging. Moreover, this paper analyzes the effect of unavoidable dc-bias currents on the magnetic-flux saturation of the transformer. Finally, it provides the dc–dc converter loss breakdown with more focus on the LVS converter.

*Index Terms*—Bidirectional isolated dc–dc converters, dc-bias currents, energy storage systems, lithium-ion (Li-ion) battery.

	LIST OF SYMBOLS
$B_{ m g}$	Air-gap flux density.
$B_{\rm max}$	Maximum dc-plus-ac flux density.
$F_{\rm net}$	Net magnetomotive force.
H	Magnetizing intensity.
$I_{1o}$	High-voltage-side (HVS) net dc-bias current.
$I_{21}, I_{22}$	Low-voltage-side (LVS) instantaneous switching
	currents at specific times.
$I_{2o}$	LVS net dc-bias current.
$i_{\rm CD2}$	LVS dc-link capacitor ripple current.
$I_{\rm m2}$	LVS magnetizing current.
$I_{RC}$	<i>RC</i> -snubber rms current.
$L_{\sigma 2}$	LVS stray inductance.
$L_{m1}$	HVS magnetizing inductance.
$L_{\rm m2}$	LVS magnetizing inductance.
N	Transformer turns ratio.
$N_1$	Transformer HVS turns number.
$N_2$	Transformer LVS turns number.
$P_{\rm B}$	Battery power.
$P_{\mathrm{D}}$	DC–DC converter power transfer.

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$P_{RC}$	<i>RC</i> -snubber loss.
100	
$R_{\rm CE}$	Insulated-gate bipolar transistor (IGBT) equiva-
	lent collector-emitter resistance.
$R_{ m dc1}$	Total HVS dc resistance.
$R_{ m dc2}$	Total LVS dc resistance.
$R_{\rm DS(ON)}$	MOSFET on-state resistance.
$R_{\rm FWD}$	HVS equivalent diode forward resistance.
$R_{ m wcml}$	MOSFET lead resistances.
$V_{\rm dc1}$	HVS net dc voltage.
$V_{ m dc2}$	LVS net dc voltage.
$\alpha, \beta, k$	PC40-core parameters.
$\phi_{ m ac}$	Maximum ac flux.

#### I. INTRODUCTION

I N JAPAN, photovoltaic (PV) systems with a power output capacity of 3–4 kW have been installed in some detached residential houses, whereas some schools and buildings have installed those with a power capacity of 10–30 kW [1]. Those PV systems are grid-connected and are usually without energy storage systems. Massive penetration of PV systems with the capability of exporting electric power into the grid, but without energy storage systems, can affect the grid due to their intermittent nature. Therefore, integration of energy storage systems is essential to make the output power of PV systems dispatchable in supply and demand control [2], [3].

High-efficiency power converters are indispensable to charging and discharging of energy storage devices. The single-phase, full-bridge bidirectional isolated dc-dc converter was first introduced in [4] for high-power-density power conversion systems. The converter realizes a low component count and a low device stress. High power transfer capability in the converter can be achieved by simple phase-shift modulation [4], [5]. This converter is the most efficient when the dc-voltage ratio between the HVS and the LVS is close to the transformer turns ratio. The overall efficiency of the 350-V, 10-kW dc-dc converter is 97% when the fifth-generation trench-gate IGBTs are used, and it is predicted to increase to 99%, if silicon carbide power switching devices are used in the near future [6]. The advantages of the converter have made it attractive for high-power automotive applications [7]–[9] and utility applications [10]–[12]. Three-port bidirectional isolated dc-dc converters are also proposed in [13] and [14].

The transformer used in an isolated dc–dc converter can experience magnetic-flux saturation due to a dc-bias current flowing in it [15], [16]. As a result, high-current pulses can be observed in

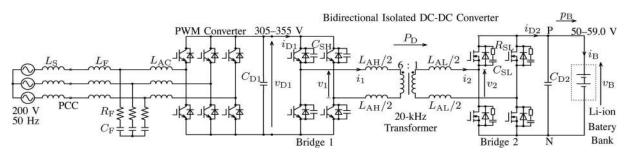


Fig. 1. Li-ion battery bank of 53.2 V, 40 A·h connected to the 6-kW bidirectional isolated dc–dc converter, where  $L_{\rm S}$  is the background system impedance (<1%).  $L_{\rm AC} = 280 \,\mu {\rm H} (1.3\%)$ ,  $L_{\rm F} = 44 \,\mu {\rm H} (0.2\%)$ ,  $R_{\rm F} = 0.2 \,\Omega (3\%)$ , and  $C_{\rm F} = 150 \,\mu {\rm F} (33\%)$  on a three-phase 200-V, 6-kW, and 50-Hz base.

the ac current. They cause additional current stress in the switching devices, reduce efficiency, and may damage the dc–dc converter in the worst case. The so-called "dc-blocking capacitors" are typically used to prevent the transformer from magneticflux saturation. However, available high-frequency capacitors may not meet high-current requirements. Parallel connections of multiple capacitors are accompanied by bulkiness, increased cost, and decreased reliability. Krismer and Kolar [9] designed a 100-kHz transformer with a low magnetic-flux density not only to achieve a low core loss but also to provide a large safety margin prior to the saturation flux density. However, they did not address any dc-bias current in the transformer. Klopper and Ferreira [17] proposed a sensor for measurement of flux below a saturation level.

This paper presents the 53.2-V, 2-kW·h Li-ion battery energy storage system based on the 6-kW full-bridge bidirectional isolated dc–dc converter using a 20-kHz transformer. The circuit configuration is similar to that in [6], [10], and [11]. However, this paper aims at demonstrating the performance of the bidirectional isolated dc–dc converter for low-voltage and high-current battery applications. It provides experimental and theoretical discussions concerning the effect of dc-bias currents on the magnetic-flux saturation of the high-frequency transformer. This consideration helps in designing an appropriate air-gap length in high-frequency transformers with different voltage and current ratings. The overall loss breakdown of the dc–dc converter compares the loss distribution of the low-voltage high-current converter with that of the high-voltage low-current converter.

# II. EXPERIMENTAL SYSTEM

#### A. System Configuration

Fig. 1 shows the experimental setup consisting of a threephase pulse-width-modulated (PWM) converter, the 6-kW bidirectional isolated dc–dc converter, and the 53.2-V, 40-A·h Li-ion battery bank. The PWM converter is connected at the point of common coupling to the 200-V, 50-Hz ac-side through the ac-link inductor  $L_{ac}$ , and the switching-ripple-filter circuit is represented by  $L_F$ ,  $C_F$ , and  $R_F$ . The battery bank consists of two 26.6-V, 40-A·h Li-ion battery modules connected in series. Note that both the nominal battery voltage of 53.2 V and the operating voltage range of 50–59 V are determined from a practical point of view, considering system-level safety, cost, and reliability. The high-voltage dc bus is adjusted between 305 and

 TABLE I

 CIRCUIT PARAMETERS OF THE BIDIRECTIONAL ISOLATED DC-DC CONVERTER

Transformer Core Material		Ferrite	
Transformer Turns Ratio	N	6:1	
Transformer Leakage Inductance (HVS)	$L_{\text{trans}}$	8.1 μH (6.2 %)	
Auxiliary Inductor (HVS)	$L_{\rm AH}/2$	10 µH (7.6 %)	
Snubber Capacitor (HVS)	$C_{\rm SH}$	10 nF	
DC Capacitor (HVS)	$C_{\rm D1}$	7 mF (58 ms)	
Auxiliary Inductor (LVS)	$L_{\rm AL}/2$	0.67 µH (18.4%)	
Snubber Capacitor (LVS)	$C_{\rm SL}$	141 nF	
Snubber Resistor (LVS)	$R_{\rm SL}$	1.67 Ω	
DC Capacitor (LVS)	$C_{D2}$	22 mF (5 ms)	
Switching Frequency	f	20 kHz	
HVS is based on single-phase 330 V, 6.6 kW, and 20 kHz.			

LVS is based on single-phase 550 V, 6.6 kW, and 20 kHz.

355 V to keep the dc-voltage ratio of the HVS to LVS close to the transformer turns ratio.

Table I summarizes the parameters of the electrical components in the bidirectional isolated dc–dc converter. The dc–dc converter with a symmetrical structure consists of two voltagesource converters that are referred to as bridge 1 and bridge 2 in this paper. To minimize stray inductances, the LVS uses laminated bus bars so that ripple currents can flow into the dc capacitor  $C_{D2}$  that is the combination of electrolytic capacitors and high-frequency film capacitors.

The dc–dc converter allows bidirectional power transfer by means of controlling the phase-shift angle  $\delta$  [rad] between square voltages  $v_1$  and  $v_2$  as follows [5]:

$$P_{\rm D} = \frac{V_{\rm D1} V_{\rm B} N}{\omega L} \delta \left( 1 - \frac{|\delta|}{\pi} \right) \tag{1}$$

where  $V_{D1}$  is the amplitude of  $v_1$ ,  $V_B$  is the amplitude of  $v_2$ ,  $\omega$  is the angular switching frequency, L is the sum of the transformer leakage inductance  $L_{trans}$  and the auxiliary inductances  $L_{AL}$  and  $L_{AH}$ , and N is the transformer turns ratio. Xie *et al.* [18] proposed a dc–dc converter power flow model that takes into account the switching-device voltage drop and dead time. However, this paper considers the power flow as shown in (1). The dc–dc converter is in the charging mode when voltage  $v_1$  leads voltage  $v_2$ , and  $\delta$  is denoted as positive. In the discharging mode, voltage  $v_2$  leads voltage  $v_1$ , and  $\delta$  is denoted as negative.

Bridge 1 consists of four 600-V, 200-A trench-gate IGBTs (CM200DY-12NF). Each IGBT module contains two devices in series. A lossless capacitor is connected in parallel with each of the IGBTs to achieve zero-voltage switching and to minimize

TABLE II DATA OF THE LI-ION BATTERY MODULE USED IN THE EXPERIMENTAL CIRCUIT SHOWN IN FIG. 1

Model Name	LIM40-7D1-S1
Capacity	40 Ah
Nominal Voltage	26.6 V (= $3.8 \text{ V} \times 7$ )
Rated Rapid Charging Current	120 A (3C)
Rated Discharge Current	200 A (5C)
Operating Temperature	0–45 °C
Weight	17 kg

Courtesy of GS Yuasa [19].



Fig. 2. Photo of the two Li-ion battery modules used for experiment, each of which is rated at 26.6 V and 40 A·h.

turn off overvoltage across the collector–emitter terminals of the IGBT.

Bridge 2 consists of four 100-V, 500-A MOSFETs (PDM5001). Each MOSFET module also contains two devices in series. From the datasheet by Nihon Inter Electronics Corporation, the on-state resistance,  $R_{\rm DS(ON)}$ , is as low as 0.5 m $\Omega$ . However, the sum of the wire bond resistance, contact resistance between the source and drain metallization and the silicon, and the contact resistance between the metallization and lead frame is not negligible because the total resistance  $R_{\rm wcm1}$  reaches 0.6 m $\Omega$ . Bridge 2 is operated in synchronous rectification mode to minimize conduction loss. A small-sized *RC* snubber is connected in parallel, with each of the four MOSFETs, to reduce its switching loss and to damp out an overvoltage and the resultant ringings.

#### B. Li-Ion Battery Modules

Table II presents the specifications of the Li-ion battery modules of the Li-ion battery bank shown in Fig. 1. Each of the modules consists of seven Li-ion battery cells connected in series, where the nominal voltage of each battery cell is 3.8 V. From the specifications given, the specific energy of the Li-ion battery module can be determined to be 63 W·h/kg, and its specific power to be 313 W/kg.

Fig. 2 shows the photo of the two Li-ion battery modules used in the experimental setup. No voltage-balancing circuit is required for the series-connected battery modules.

#### C. Control Method

The control method is based on an open-loop, feedforward control intended for investigating the basic operating performance of the dc–dc converter in the Li-ion battery energy storage system. Altera's Max 7000s complex programmable logic

 TABLE III

 Adjustment of HVS DC-Link Voltage With Battery Voltage

Charging		Discharging	
$v_{\rm B}$ [V]	$v_{\rm D1}$ [V]	$v_{\rm B} [V]$	$v_{\rm D1}$ [V]
54.7-55.5	330	55.9–55.2	340
55.9–57.6	340	55.3-54.2	330
58.0-58.4	345	53.9-53.1	320
58.5-59.0	355	53.1-52.1	315
-	-	51.7-50.0	305

device is used to generate eight gate signals for all the gate-drive circuits of the IGBTs in bridge 1 and the MOSFETs in bridge 2. The switching periods of bridges 1 and 2 are the same as 50  $\mu$ s (20 kHz). Due to the existence of finite turn on and turn off times of the IGBTs and MOSFETs, a dead time of 1.24  $\mu$ s is set for each leg in bridges 1 and 2. The time resolution of the controller is 40 ns/bit, i.e., 0.29°/bit.

Table III indicates the relation between the dc voltage at the HVS,  $v_{D1}$  and the battery voltage  $v_B$  during battery charging and discharging. The battery charging operation is carried out from an initial voltage of 54.7 V, and the discharging operation is carried out from an initial voltage of 55.9 V. The initial voltage is measured at  $i_B = 0$ . The dc voltage  $v_{D1}$  is controlled with the battery voltage  $v_B$  in such a way as to minimize the voltage change across the auxiliary inductors and transformer leakage inductor. Adjustment of  $v_{D1}$  is carried out by changing the reference voltage of the three-phase PWM converter.

# **III. EXPERIMENTAL RESULTS**

This section demonstrates the performance of the designed dc-dc converter in charging and discharging the Li-ion battery bank by adjusting the HVS dc voltage  $v_{D1}$ , as the battery voltage  $v_B$  at the LVS varies. The switching-frequency-based waveforms of Figs. 3–6 were observed through the Tektronix TDS3014B.

#### A. Experimental Waveforms

Fig. 3 presents the ac voltage and current waveforms of bridges 1 and 2 when the Li-ion battery is charged and discharged at  $P_{\rm B} = \pm 5.9 \,\mathrm{kW}$ . The effect of stray inductance at the LVS is seen as the following change in voltage  $v_2$ , where

$$v_2 = L_{\sigma 2} \frac{di_2}{dt} + v_B.$$
<sup>(2)</sup>

A nonnegligible stray inductance of a few tens of nanoHenries makes it difficult to achieve soft switching at turn off at the LVS. It may also cause MOSFET drain–source overvoltages and increase the switching loss.

In Fig. 3(a),  $v_1$  leads  $v_2$  because the Li-ion battery is charged. The high-voltage dc bus is 355 V, and the battery voltage (the low-voltage dc bus) is 59 V. The peak current of  $i_2$  is 153 A. The dc-bias current is 0.16 A in  $i_1$ , and -4.36 A in  $i_2$ . For the duration of a phase-shift angle of  $\delta = 5.78 \,\mu$ s, the rate of change of  $i_2$  (within the dotted lines) is calculated as  $di_2/dt =$  $-46.7 \,\text{A}/\mu$ s. The rate of change of current causes a voltage drop of  $\sim 4$  V across the stray inductance in bridge 2. This gives the stray inductance as  $L_{\sigma 2} = 85.6 \,\text{nH}$  from (2).

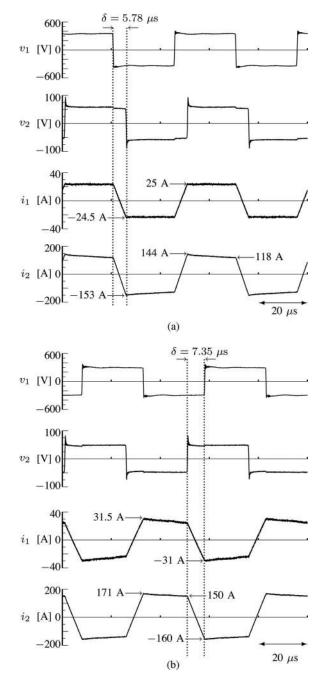


Fig. 3. Experimental waveforms with dc-voltage control at the HVS. (a) Charging mode at  $P_{\rm B}=5.9\,{\rm kW}$  ( $V_{\rm D\,1}=355\,{\rm V}$ ). (b) Discharging mode at  $P_{\rm B}=-5.9\,{\rm kW}$  ( $V_{\rm D\,1}=305\,{\rm V}$ ).

In Fig. 3(b),  $v_2$  leads  $v_1$  because the Li-ion battery bank is discharged. The high-voltage dc bus is 305 V, and the battery voltage is 50.5 V. The peak current of  $i_2$  is 171 A. The dc-bias current is 0.33 A in  $i_1$ , and 6.05 A in  $i_2$ . For the duration of a phase-shift angle of  $\delta = 7.35 \,\mu$ s, the rate of change  $i_2$  (within the dotted lines) is calculated as  $di_2/dt = -42.2 \,\text{A}/\mu$ s. The rate of change of current causes a voltage drop of ~3.5 V across the stray inductance in bridge 2. This gives the stray inductance as  $L_{\sigma 2} = 82.9 \,\text{nH}$ , which is nearly equal to the value from

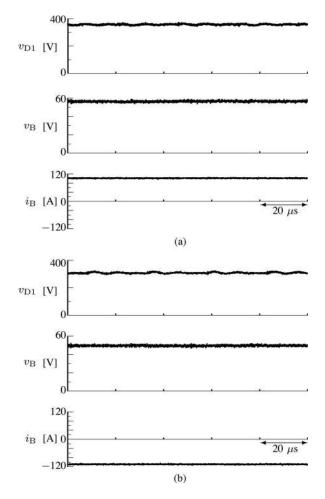


Fig. 4. Waveforms of  $v_{D1}$ ,  $v_B$ , and  $i_B$ . (a) Battery charging at  $P_B = 5.9$  kW. (b) Battery discharging at  $P_B = -5.9$  kW.

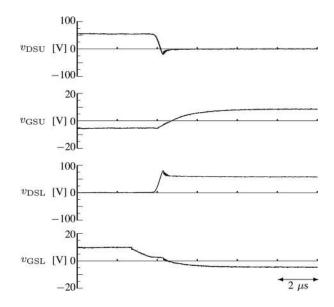


Fig. 5. Drain–source and gate–source voltages of a leg in bridge 2 at  $P_{\rm B}=5.9\,{\rm kW},\,V_{\rm D\,1}=355\,{\rm V},$  and  $V_{\rm B}=59\,{\rm V}.$ 

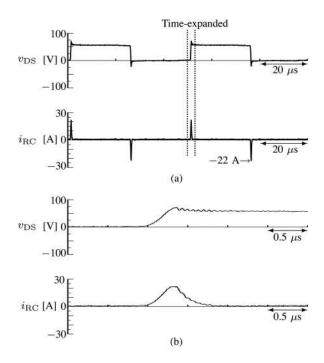


Fig. 6. Effects of the *RC*-snubber on a MOSFET in bridge 2 during battery charging at  $P_{\rm B} = 5.9 \, \rm kW$ . (a) Drain–source voltage and *RC*-snubber current. (b) Time-expanded waveform of  $v_{\rm DS}$  and  $i_{RC}$ .

Fig. 3(a). This stray inductance value is used to design the *RC* snubbers shown in Fig. 1 and Table I.

The adjustment of  $v_{D1}$  with the variation of  $v_B$  can minimize the rate of change of the currents  $i_1$  and  $i_2$  over the time interval of conduction. Therefore, a rather flat top ac current is observed in  $i_1$  and  $i_2$ . This method contributes to minimizing the peak switching current, especially during battery charging because a higher switching current causes a higher turn off overvoltage.

Fig. 4(a) shows the waveforms of the dc voltage at the HVS, the Li-ion battery voltage, and the battery current when the battery is charged at  $P_{\rm B} = 5.9$  kW. Fig. 4(b) shows those when the battery is discharged at  $P_{\rm B} = -5.9$  kW. In bridge 2, the current  $i_{\rm B}$  becomes a part of the rectified current of  $i_2$ . Since  $i_2$  has a frequency of 20 kHz,  $i_{\rm B}$  should contain a 40-kHz component. However, it is observed from Fig. 4 that the current  $i_{\rm B}$ , flowing into, or out of, the Li-ion battery bank have almost none of the 40-kHz ripples. The ripples in the battery voltage  $v_{\rm B}$ are also negligible. A 40-kHz ripple voltage exists at the HVS, which is 6% during battery charging and 9% during battery discharging.

Fig. 5 presents the time-expanded waveforms of the drainsource and gate-source voltages of a leg in bridge 2 at  $P_{\rm B} =$  $5.9 \,\mathrm{kW}$ ,  $V_{\rm D1} = 355 \,\mathrm{V}$ , and  $V_{\rm B} = 59 \,\mathrm{V}$ . The so-called "Miller effect" that lasts for approximately 400 ns is observed from the gate-source voltage of the lower MOSFET  $v_{\rm GSL}$ , which increases the turn off switching loss. On the other hand, voltages  $v_{\rm GSU}$  and  $v_{\rm DSU}$  show that zero-voltage switching at turn on is achieved in the upper MOSFET with a negligible turn on switching loss.

Fig. 6(a) shows the drain–source voltage  $v_{\rm DS}$  of a MOSFET in bridge 2 and the *RC*-snubber current  $i_{RC}$  of the corresponding snubber circuit during battery charging at  $P_{\rm B} = 5.9$  kW. The *RC* snubbers mitigate the overvoltages and ringings across the MOSFET drain–source terminals. The current flow in the *RC* snubber produces a snubber loss in bridge 2 that is estimated in Section V-A.

Fig. 6(b) presents the time-expanded waveforms of  $v_{\rm DS}$  and  $i_{RC}$ . The time taken to charge the snubber capacitor across the MOSFET to  $v_B$  (resonant-transition time), including the settling time of the voltage ringings (parasitic-resonance time) is approximately 0.9  $\mu$ s. During the resonant-transition time, the drain-source voltage of one diagonal MOSFET pair swings from 0 to  $v_B$ , and that of the other diagonal MOSFET pair swings from  $v_B$  to 0. Note that  $i_{\rm D2}$  is 0 during the resonant transition time, and that the ac current of bridge 2  $i_2$  circulates in the four *RC* snubbers, the transformer, and the LVS auxiliary inductors.

Moreover, Fig. 6(b) implies that the turn off switching loss in bridge 2 may not be negligible. This is deduced from the rise time of the MOSFET drain–source voltage, which is almost simultaneous to the rise time of the *RC*-snubber current, indicating that the snubber capacitor is not large enough to minimize the rate of change of the MOSFET drain–source voltage. Additionally, the peak current in the *RC* snubber is 22 A, which is less than half of the MOSFET peak turn off current. This means that an amount of current flows in the MOSFET during turn off, and that the current results in a nonnegligible turn off switching loss.

#### B. Converter Efficiency

Fig. 7 shows the measured plots of the dc–dc converter efficiency and the battery terminal voltage when the battery is charged and discharged between 500 W and 5.9 kW. Power at the HVS,  $P_{dc1}$  is calculated from measurements of  $v_{D1}$  and  $i_{D1}$ , and the battery power  $P_B$  is calculated from measurements of  $v_B$  and  $i_B$  by using the Hioki 3139 power meter having a moving average function. The losses in the Li-ion battery, the PWM converter, and the cables connecting the battery and PWM converter to the dc–dc converter are not considered. Therefore, this paper will consider the low-side dc-link voltage as the battery voltage  $v_B$ . The accuracies of the measuring instruments are listed in the Appendix.

The measured efficiency points in Fig. 7 are fitted with an exponential function, whereas the measured battery voltage points are fitted with a first-order polynomial function. Note that both functions use the least-mean-square approximation.

The efficiency of the dc–dc converter is less than 92% at low power levels (<1 kW). As bridge 2 is operated in synchronous rectification, the conduction loss in bridge 2 should not be significant at a low conduction current. The conduction loss in bridge 1, the snubber loss due to hard switching or incomplete zero-voltage switching, and the switching loss in bridges 1 and 2 would dominate the loss at this low-power level. At battery charging, the measured converter efficiency peaks at 96% at  $P_{\rm B} = 1.6$  kW. At battery discharging, measured converter efficiency averages at 96.8% between  $P_{\rm B} = -1.2$  kW and  $P_{\rm B} = -2.2$  kW. The maximum efficiency of the converter is achieved around the onset of zero-voltage switching. An observable decrease in converter efficiency exists when the battery

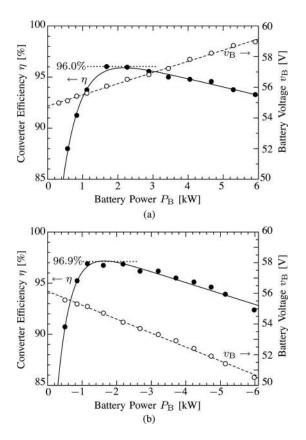


Fig. 7. Measured dc–dc converter efficiencies and battery voltages. (a) Battery charging. (b) Battery discharging.

power is between  $\pm 3$  and  $\pm 6$  kW. This is the result from an increase in conduction, copper, ohmic, and switching losses, as the operating current increases to 100 A during battery charging, and to 120 A during battery discharging at the LVS. The estimation of loss breakdown is shown in Section V.

# C. Power Transfer Versus Phase-Shift Angle

Fig. 8 compares the experimental and theoretical power transfer  $P_D$  versus phase-shift angle  $\delta$  during battery charging and discharging. The experimental phase-shift angle is the reference angle from the controller. The calculation of the theoretical phase-shift angle is derived from (1) to be

$$\delta = \frac{\pi}{2} - \sqrt{\frac{\pi^2}{4} - \frac{\omega \pi L P_{\rm D}}{V_{\rm D1} V_{\rm B} N}} \tag{3}$$

during battery charging, and

$$\delta = -\frac{\pi}{2} + \sqrt{\frac{\pi^2}{4} + \frac{\omega \pi L P_{\rm D}}{V_{\rm D1} V_{\rm B} N}}$$
(4)

during battery discharging. In order to calculate the theoretical phase-shift angle, the measured values of  $P_D$ ,  $V_{D1}$ , and  $V_B$  are substituted into (3) or (4). When charging, the power transfer  $P_D$  is equal to the battery power  $P_B$  and it is denoted as positive. When discharging,  $P_D$  is equal to the power at the HVS  $P_{dc1}$  and it is denoted as negative. Note that the theoretical calculation is not entirely idealized due to the usage of the experimental values

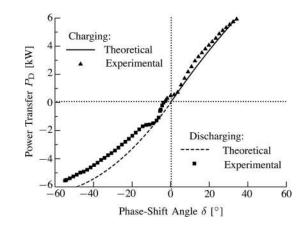


Fig. 8. Bidirectional power transfer versus phase-shift angle.

in the calculation, but it is considered reasonable in making the comparison. The curves for the theoretical and experimental points are fitted with the function in (1) using the least-mean-square approximation. The absolute value of the power transfer increases, as the phase-shift angle increases in the positive and negative directions.

For the charging and discharging modes of operation, the theoretical and measured curves are seen to be in good agreement because the dc-voltage ratio of the HVS to the LVS is kept close to the transformer turns ratio. Based on the experimental results, at  $\delta = 0$ , the power transfer is not zero, but is 500 W. Almost no power flows when the reference phase-shift angle is about  $-4^{\circ}$ . The dead time in the converter causes a phase difference between voltages  $v_1$  and  $v_2$ , resulting in a power transfer that deviates from the converter power transfer model in (1). The deviation is more severe when the dc-voltage ratio of the HVS to the LVS is not equal to the transformer turns ratio. Xie *et al.* [18] have proposed a more accurate power transfer model for the dc-dc converter, which is divided into eight different regions of operation. The model is useful for accurate power management when  $v_{D1} \neq Nv_B$ .

## IV. TRANSFORMER OF 20 KHz

This section discusses the dc-bias current phenomenon observed in the transformer. An air-gap length of 1 mm is inserted to prevent the transformer from magnetic-flux saturation, even in the worst case that considers transient conditions and a margin of manufacturing and component tolerances.

#### A. Maximum AC-Flux Density and Magnetizing Current

Table IV presents the specifications of the 20-kHz transformer with an air-gap length of 1 mm, where the core material is ferrite PC40. The maximum ac-flux density  $B_{\rm ac}$  can be calculated as

$$B_{\rm ac} = \frac{V_{\rm D1}}{4N_1 A_{\rm e} f} = 0.104 \,\rm T \tag{5}$$

where  $V_{D1} = 360 \text{ V}$  is the rated voltage at the HVS. The magnetizing inductance at the LVS is equivalent to 48.9  $\mu$ H (=1.76 mH/36). The magnetizing current is triangular, and at the battery voltage of 59 V, its LVS-referred peak and rms

TABLE IV Specifications of the 20-KHz Transformer Used in Experiment

Core Material		Ferrite PC40
Effective Cross-Section Area	$A_{ m e}$	12 cm <sup>2</sup>
Core Effective Path Length	$l_{ m c}$	36.3 cm
Magnetizing Inductance (HVS)	$L_{ m m1}$	1.76 mH
Turns Number	$N_1/N_2$	36/6
Maximum AC-Flux Density	$B_{ m ac}$	0.104 T
Air-Gap Length	$l_{\rm g}$	0.5 mm×2

currents are 15.3 and 8.9 A, respectively. An optimal design in the air-gap length results in a reasonable magnetizing current in the transformer.

#### B. DC-Bias Currents at the HVS and LVS

The bidirectional isolated dc–dc converter produces squarewave ac voltages that are applied to the HVS and LVS of the 20-kHz transformer. An unequal voltage–time area in each ac voltage would result in a net dc voltage in either side of the transformer. A dc-bias current can cause magnetic-flux saturation that produces high current pulses in the transformer. This burdens the switching devices with additional current stress, reduces converter efficiency, and may damage the dc–dc converter.

There are several factors that can cause dc-bias currents in the transformer. These include the following:

- 1) unequal gate-drive circuits;
- 2) unequal saturation voltage in the IGBTs;
- 3) unequal on-state resistance of the MOSFETs;
- asymmetry in transient overvoltages across the IGBTs and MOSFETs;
- unequal turn on and turn off times of the IGBTs and MOS-FETs.

Manufacturing and component tolerances make it impossible to predict accurate degrees of mismatches in the IGBTs/MOSFETs and their gate-drive circuits at the stage of system design. As shown in Fig. 3, an amount of dc-bias current was observed in the experimental waveforms.

Fig. 9 shows the theoretical digital control signals for the two diagonal-pair MOSFETs, and the ensuing square-wave ac voltage  $v_2$  at the LVS under both ideal and practical conditions. Note that the on-state resistance across each MOSFET is assumed equal, and no transient overvoltage is considered in Fig. 9. The dash-line waveform of  $v_2$  represents the ac voltage at the LVS under the ideal condition. It shows that at times  $t_a$ and  $t_c$ , the polarity of  $v_2$  changes from negative to positive when the gate signal for diagonal-pair 2 changes from high to low. At the time  $t_b$ , the polarity of  $v_2$  changes from positive to negative when the gate signal for diagonal-pair 1 changes from high to low. In this case, the voltage-time area for one half of a switching cycle is equal to that for the other half of the switching cycle. However, possible delays in the turn on and turn off times of the MOSFETs and the output signals from their gate-drive-circuits can defer the polarity change in  $v_2$ . The solid-line waveform of  $v_2$  shows the following difference caused by the delays: The diagonal-lined voltage-time area is larger than the gray-shaded voltage-time area. Hence, the presence of the delay-time differ-

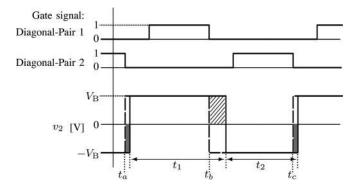


Fig. 9. Theoretical MOSFET gate signals and the resultant ac voltage  $v_2$  at the LVS that emphasizes on the time delay during the dead time.

ence defined by  $\Delta t(=t_1 - t_2)$  yields a net positive dc voltage in the LVS every switching cycle. A net negative dc voltage is also possible. The same situation can appear in square-wave voltage  $v_1$  at the HVS, resulting in a positive or negative net dc voltage every switching cycle.

Table V presents the measured dc-resistance values of the passive components and connecting cables in the dc–dc converter. A constant current source of  $I_{\rm dc} = 5$  A was connected across the transformer HVS, whereas  $I_{\rm dc} = 25$  A was connected across the transformer LVS, other components, and cables, and the terminal dc voltage of each of them was measured. The total dc resistance at the LVS in the charging and discharging modes  $R_{\rm dc2}$  is expressed as

$$R_{\rm dc2} = 2R_{\rm DS(ON)} + 2R_{\rm wcml} + R_{\rm ALo} + R_{\rm 2o}$$
  
= 3.16 m \Omega. (6)

The total dc resistance at the HVS in the charging and discharging modes  $R_{dc1}$  is expressed as

$$R_{\rm dc1} = 2R_{\rm FWD} (\text{or } 2R_{\rm CE}) + R_{\rm AHo} + R_{\rm 1o} + R_{\rm CBLo}$$
$$= 42 \,\mathrm{m}\Omega (\text{or } 33.9 \,\mathrm{m}\Omega) \tag{7}$$

where  $R_{\rm FWD}$  is the equivalent diode forward resistance in the discharging mode, which excludes the threshold voltage from the  $i_A-v_{\rm AK}$  curve of the diode, and it is estimated as 7.8 m $\Omega$  from the datasheet by Mitsubishi Electric. Similarly,  $R_{\rm CE}$  is the equivalent collector–emitter resistance in the charging mode, which excludes the threshold voltage from the  $i_C-v_{\rm CE}$  curve of the IGBT, and it is estimated as 3.75 m $\Omega$  from the same data sheet. Note that the MOSFET on-state resistance, the IGBT equivalent collector–emitter resistance, and the equivalent diode forward resistance have a role in reducing the dc-bias currents in the dc–dc converter.

The dc-bias current in the LVS was measured as 6.05 A at the rated power in the discharging mode. Based on the calculated dc resistance  $R_{dc2}$ , the net dc voltage of  $v_2 V_{dc2}$  is deduced as 19.1 mV. From Fig. 9, the delay-time difference  $\Delta t$  is calculated as

$$\Delta t = \frac{V_{\rm dc2}T}{V_{\rm B}} = 19\,\rm ns \tag{8}$$

where  $T = 50 \,\mu \text{s}$  and  $V_{\text{B}} = 50.5 \,\text{V}$ .

		DC Resistance $[m\Omega]$
Transformer Winding (HVS)	$R_{1o}$	19.2
Auxiliary Inductor (HVS)	$R_{\rm AHo}$	3.6
Connecting Cables (HVS)	$R_{\rm CBLo}$	3.6
Transformer Winding (LVS)	$R_{2o}$	0.58
Auxiliary Inductor (LVS)	$R_{\mathrm{ALo}}$	0.38

CONVERTER

The dc-bias current in the HVS was measured as 0.33 A at the rated power in the discharging mode. Based on the dc resistance  $R_{dc1}$ , the net dc voltage of  $v_1 V_{dc1}$  is deduced as 13.9 mV. The delay-time difference  $\Delta t$  is calculated as

$$\Delta t = \frac{V_{\rm dc1}T}{V_{\rm D1}} = 2.3\,\rm{ns} \tag{9}$$

where  $V_{D1} = 305 \text{ V}$ . Note that  $V_{D1}$  is much higher than  $V_{dc1}$ , and that measurements of the net dc voltages  $V_{dc1}$  and  $V_{dc2}$  cannot be carried out because reasonable accuracy is unachievable as  $v_1$  and  $v_2$  also include transient overvoltages.

The delay-time differences are seen to be less than the controller resolution (40 ns). This means that the controller resolution is not responsible for the dc-bias currents. Since the delaytime differences are very small, measurements with reasonable accuracy are challenging. Therefore, the delay-time differences in (8) and (9) are calculated based on the measured dc-bias currents in the HVS and LVS and the measured dc resistances that are shown in Table V. Considering that the measured values are subjected to the accuracies of the measuring instruments (0.5% to 2% of reading), the calculated delay-time differences are only approximations.

#### C. Net DC Magnetomotive Force

In the discharging mode of Fig. 3(b), the positive dc-bias currents at both HVS and LVS produce a dc flux that has a slight cancellation effect. As a result, the net magnetomotive force can be expressed as

$$F_{\rm net} = N_2 I_{20} - N_1 I_{10} = 24.4 \,\text{A} \cdot \text{turns} \tag{10}$$

where  $I_{1o}$  and  $I_{2o}$  are the dc-bias currents at the HVS and LVS, respectively.

The dc-bias currents can also be of opposite polarity, as shown in the charging mode of Fig. 3(a). Each dc-bias current produces a dc flux that has a slight cumulative effect. The net magnetomotive force is expressed as

$$F_{\rm net} = -(N_2 I_{2\rm o} + N_1 I_{1\rm o}) = -31.9 \,\mathrm{A} \cdot \mathrm{turns.}$$
 (11)

Fig. 10 shows the relationship of the magnetic flux density and flux with the magnetomotive force of the transformer with no air gap and air-gap lengths of 0.2, 0.5, 1.0, and 2.0 mm at a temperature of 120 °C. The saturation flux density of the core reduces to 0.35 T at 120 °C. These curves are derived based on the B–H curve obtained from the datasheet of ferrite PC40 with the help of the following basic relationship between

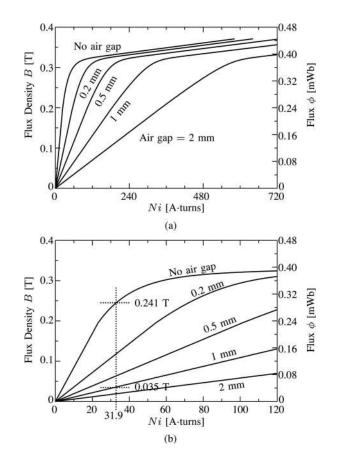


Fig. 10. Ferrite-core (PC 40) flux density and flux versus magnetomotive force at  $120 \,^{\circ}$ C. (a) Comparison between the transformer with no air gap and four different air-gap lengths. (b) The magnetomotive force is expanded.

magnetomotive force and magnetic flux density:

$$F = Hl_c + \frac{l_{\rm g}B_{\rm g}}{\mu_0} \tag{12}$$

where *H* is the magnetizing intensity,  $B_g$  is the air-gap flux density, and  $\mu_0$  (=4 $\pi \times 10^{-7}$  H/m) is the permeability of air. The following assumption is made: Neither fringing effects at the air gap nor leakage flux exists.

Fig. 10(b) indicates that the change in flux with current is approximately 0.008 mWb/A in the transformer with the air-gap length of 1 mm. This theoretical value is in good agreement with the one calculated from the measured magnetizing inductance value as follows:

$$\frac{d\phi}{di} = \frac{(L_{\rm m1}/N^2)}{N_2} = 0.008\,\rm{mWb/A}$$
(13)

where N = 6 from Table I, and  $L_{m1} = 1.76$  mH and  $N_2 = 6$  from Table IV.

#### D. Design of an Optimal Air-Gap Length

In the worst case of the experimental results, the dc-bias currents at the HVS and LVS accumulate to produce a net magnetomotive force of 31.9 A turns in the charging mode, as shown in (11). From Fig. 10(b), the initial dc-flux density  $B_{\rm dc}$  is 0.241 T for the transformer with no air gap. This means that the operating condition is almost at the saturation flux density because

TABLE VI CALCULATED MAGNETIZING INDUCTANCE AND CURRENT AT THE LVS, AND DC-FLUX DENSITY FOR VARIOUS AIR-GAP LENGTHS AT 120 °C

$l_{\mathbf{g}}$	$L_{m2}$	Magnetizing Current		DC-Flux Density
[mm]	$[\mu H]$	<i>I</i> <sub>m2</sub> [A]	$I_{m2(rms)}$ [A]	B <sub>dc</sub> [T]
0	360	2.0	1.2	0.241
0.2	153	4.8	2.8	0.114
0.5	81	9.0	5.2	0.061
1	48	15.3	8.6	0.035
2	25	29.3	16.9	0.018
A . 17	055 17		501111 1.0	91 0 A 4

At  $V_{D1} = 355$  V,  $V_B = 59$  V,  $P_D = 5.9$  kW, and  $F_{net} = 31.9$  A  $\cdot$  turns.

the maximum dc-plus-ac flux density reaches 0.345 T. However, the transformer with an air-gap length of 1 mm has an initial dc-flux density of 0.035 T. The maximum dc-plus-ac flux density reaches 0.139 T, leaving a decent margin prior to the saturation flux density. Note that the maximum dc-plus-ac flux density in the possible worst case for the transformer with an air-gap length of 1 mm,  $B_{\rm max}$  is given by

$$B_{\rm max} = (0.104 \times 2) + (0.035 \times 2) = 0.278 < 0.3 \,\mathrm{T}$$
 (14)

where the doubling factor for the ac-flux density could come from start-up and transient conditions, and that for the dc-flux density could come from a margin of manufacturing and component tolerances.

Table VI summarizes the peak and rms magnetizing currents, the magnetizing inductance, and the dc-flux density that would be present when the net magenetomotive force is 31.9 A·turns, for various air-gap lengths. The peak magnetizing current at the LVS is calculated as

$$I_{\rm m2} = \frac{N_2 \phi_{\rm ac}}{L_{\rm m2}}$$
(15)

where  $\phi_{ac}$  is the maximum ac flux, and  $L_{m2}$  is the magnetizing inductance at the LVS, which is obtained from the curves in Fig. 10. For an air-gap length of 0.5 mm, the maximum dc-plusac flux density in the possible worst case would be 0.33 T, which is close to the saturation flux density. For an air-gap length of 2 mm, the rms magnetizing current would be 14.4% of the rated current, which could increase the copper loss. Finally, Table VI suggests that the acceptable air-gap length would be in the range of 0.5 to 1 mm. However, in consideration of the possible worst case, the air-gap length of 1 mm is concluded to be optimal for this system.

Manufacturing and component tolerances are unavoidable in any practical bidirectional isolated dc–dc converter. Slight component mismatches in bridges 1 and 2 produce a net dc magnetomotive force in the transformer with different voltage and current ratings in the primary and secondary sides. The component mismatches are due to the dc–dc converter employing different switching devices and gate-drive circuits. The dc–dc converter in [6], [10], and [11] had a toroidal-core transformer with a turns ratio of 1:1, in which the nanocrystalline soft-magnetic material with a saturation flux density of 1.3 T, named Finemet, was used and the ac magnetic flux density was designed as 0.86 T. This transformer with no air gap did not experience any magneticflux saturation. This would result from using the same IGBTs and gate-drive circuits, where good matches in the IGBTs and the gate-drive circuits could aid in minimizing or even canceling the dc magnetomotive force at the primary and secondary sides with the same voltage and current ratings.

The effect of dc-bias currents on the transformer would become more severe when SiC-MOSFETs are employed in the HVS, because the on-state resistance of the SiC-MOSFETs is expected to be one-fifth as low as that of the Si-MOSFETs [6], [20]. Therefore, inserting an appropriate air gap into the transformer ensures stable operation of the dc–dc converter without causing magnetic-flux saturation.

#### V. LOSS BREAKDOWN

This section presents the estimated loss distribution in the dc-dc converter under the following two battery charging conditions: One is at  $P_{\rm B} = 4.1 \,\mathrm{kW}$ ,  $V_{\rm D1} = 340 \,\mathrm{V}$ ,  $V_{\rm B} = 57.8 \,\mathrm{V}$ , and  $I_{\rm B} = 70 \,\mathrm{A}$ , and the other is at  $P_{\rm B} = 5.9 \,\mathrm{kW}$ ,  $V_{\rm D1} = 355 \,\mathrm{V}$ ,  $V_{\rm B} = 59 \,\mathrm{V}$ , and  $I_{\rm B} = 100 \,\mathrm{A}$ . Although the method of loss breakdown is the same as that in the previous papers [6], [10], the following differences exist: This paper takes into account the *RC*-snubber and dc-capacitor losses at the LVS, and calculates the auxiliary-inductor core loss using an improved generalized Steinmetz equation [21] that is suitable for nonsinusoidal excitation waveforms.

#### A. RC-Snubber Loss

Zero-voltage switching is achieved in both the HVS and LVS at  $P_{\rm B} = 5.9$  kW and  $P_{\rm B} = 4.1$  kW. However, the *RC* snubbers in the LVS produce an amount of loss. From the measured waveform of  $i_{RC}$  in Fig. 6(b), the rms current  $I_{RC}$  is 2.27 A at  $P_{\rm B} = 5.9$  kW. Assuming that the same rms current flows in the other three *RC* snubbers, the total loss in the four *RC* snubbers is given by

$$P_{RC} = 4I_{RC}^2 R_{\rm SL} = 34.4 \,\rm W. \tag{16}$$

At  $P_{\rm B} = 4.1 \,\text{kW}$ ,  $P_{RC} = 30.6 \,\text{W}$ , since  $I_{RC} = 2.14 \,\text{A}$ .

The total loss can also be calculated from its energy loss for one switching cycle as follows:

$$P_{RC} = 4C_{\rm SL}V_{\rm B}^2 f. \tag{17}$$

The total loss at  $P_{\rm B} = 5.9 \,\mathrm{kW}$  and  $P_{\rm B} = 4.1 \,\mathrm{kW}$  are 39.3 and 37.6 W, respectively. These *RC*-snubber losses agree fairly well with those calculated from the measured *RC*-snubber current.

## B. Core Loss in Auxiliary Inductors

The voltage drop across the high-voltage and LVS inductors are deduced from the rate of change of currents  $i_1$  and  $i_2$  per switching cycle. The Steinmetz parameters of ferrite PC44 are  $\alpha = 1$ ,  $\beta = 2$ , and  $k = 150 \text{ W} \cdot \text{Hz}^{-1} \cdot \text{T}^{-2} \cdot \text{m}^{-3}$  from the datasheet. Using the Steinmetz parameters and the improved generalized Steinmetz equation, the inductor core losses in the HVS and LVS at  $P_{\text{B}} = 5.9 \text{ kW}$  are 3.2 and 20.2 W, respectively.

At  $P_{\rm B} = 4.1$  kW, the inductor core losses in the HVS and LVS are 1.6 and 4.8 W, respectively.

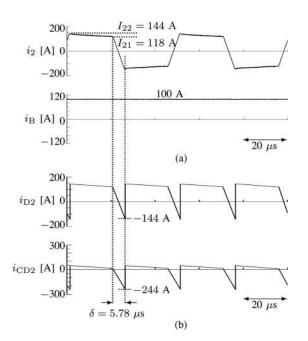


Fig. 11. Observed and simplified theoretical current waveforms at  $P_{\rm B} = 5.9 \, \rm kW$ . (a) Observed waveforms of  $i_2$  and  $i_{\rm D2}$ . (b) Simplified waveforms of  $i_{\rm D2}$  and  $i_{\rm CD2}$ .

### C. DC-Capacitor Loss at the LVS

Fig. 11(a) shows the experimental waveforms of  $i_2$  and  $i_B$ at  $P_B = 5.9$  kW. As specially designed laminated bus bars are used at the LVS, measurements of the currents  $i_{D2}$  and  $i_{CD2}$  are restricted. Therefore, Fig. 11(b) shows the simplified waveforms of  $i_{D2}$  and  $i_{CD2}$ , where  $i_{D2}$  can be analyzed from the charging operation, and  $i_{CD2}$  is the ripple current flowing in the dc capacitors at the LVS. The ripple current is obtained as  $i_{CD2} = i_{D2} - i_B$ .

The analysis of  $i_{D2}$  and  $i_{CD2}$  are based on the following assumptions: Since Fig. 6(c) shows that the resonant transition time of  $i_2$  is less than 0.9  $\mu$ s, this time in which  $i_{D2}$  is 0 is negligible with respect to its fundamental frequency (40 kHz). In addition, only the dc and fundamental components are considered in the simplified waveforms. Because the waveform of  $i_B$  contains almost no 40-kHz ripple, it can be assumed that the ripple current flows into the dc capacitors  $C_{D2}$ .

Referring to the datasheets, the equivalent series resistance (ESR) of the film and electrolytic capacitors can be approximated to be 3.2 m $\Omega$ . At  $P_{\rm B} = 5.9$  kW, the rms current of  $i_{\rm CD2}$  can be calculated from Fig. 11(b) to be 71.1 A. Hence, the ESR loss in  $C_{\rm D2}$  is 16 W. At  $P_{\rm B} = 4.1$  kW and  $\delta = 3.52 \,\mu$ s, the currents  $I_{21}$  and  $I_{22}$  are measured to be 99 and 73 A, respectively. Hence, the rms current of  $i_{\rm CD2}$  is 5 W. Note that  $I_{21}$  and  $I_{22}$  are defined as the instantaneous switching currents of bridge 2 at specific times. While the values of  $I_{21}$  and  $I_{22}$  in this section are obtained from experiments, the calculation for the switching currents can be found in [6] and [22].

## D. HVS Switching Loss and Ohmic Loss

Fig. 12 shows the experimental results relating the dc-dc converter loss with the switching frequency between 10 and

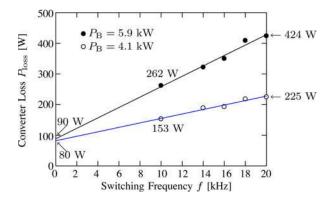


Fig. 12. Relationship between the dc-dc converter loss and switching frequency at  $P_{\rm B} = 4.1$  kW,  $V_{\rm D1} = 340$  V, and  $V_{\rm B} = 57.8$  V, and at  $P_{\rm B} = 5.9$  kW,  $V_{\rm D1} = 355$  V, and  $V_{\rm B} = 59$  V.

20 kHz for battery powers of 5.9 and 4.1 kW. The experimental data were fitted with a first-order polynomial and extrapolated to zero switching frequency. The frequency-dependent losses at  $P_{\rm B} = 5.9$  kW and  $P_{\rm B} = 4.1$  kW are estimated as 334 W (424 W - 90 W) and 145 W (225 W - 80 W), respectively. They include LVS snubber loss, transformer-core and inductorcore losses, and switching loss. Based on the estimated losses in earlier sections, the switching loss is the most dominant of the frequency-dependent loss.

Inoue and Akagi [6] showed that the total switching loss for the 350-V bidirectional isolated dc–dc converter using IGBTs was estimated as 90 W at 10 kW. Assuming that the switching loss is proportional to the power transferred, the switching loss in bridge 1 is 27 W at  $P_{\rm B} = 5.9$  kW, and 18 W at  $P_{\rm B} = 4.1$  kW.

The ohmic loss is considered to be mainly contributed by the contact points and laminated bus bars at the LVS. The contactpoint ohmic losses can be estimated to be in the range of 2–5 W. The total ohmic loss in the dc–dc converter is deduced to be in a range of 4–10 W at  $P_{\rm B} = 4.1$  kW or  $P_{\rm B} = 5.9$  kW.

#### E. Estimated Loss Distribution and Considerations

Fig. 13 shows the estimated overall loss breakdown at battery charging powers of 4.1 and 5.9 kW. At  $P_{\rm B} = 5.9$  kW,  $V_{\rm D1} = 355$  V,  $V_{\rm B} = 59.0$  V, and  $I_{\rm B} = 100$  A, the measured dcdc converter loss and efficiency are 424 W and 93.3%. The estimated loss, including the conduction, *RC*-snubber, transformercore, inductor-core, copper, ESR, HVS switching loss, and ohmic loss, is 224 W. Therefore, the LVS switching loss is 200 W. At  $P_{\rm B} = 4.1$  kW,  $V_{\rm D1} = 340$  V,  $V_{\rm B} = 57.8$  V, and  $I_{\rm B} = 70$  A, the measured dc-dc converter loss and efficiency are 225 W and 94.8%. The estimated loss excluding the LVS switching loss is 132 W. Therefore, the LVS switching loss is 93 W.

Fig. 14 presents the loss distribution in bridges 1 and 2, and the magnetic components, which include the transformer and auxiliary inductors at the rated power. The figure illustrates that the switching loss of 200 W in bridge 2 is the largest portion (47%) of the loss in the dc–dc converter. The total loss in the switching devices, which include conduction and switching

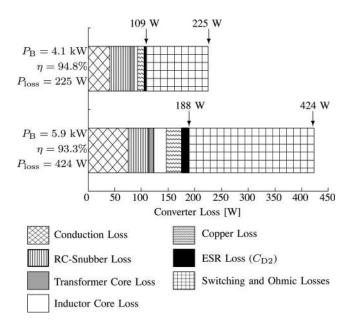


Fig. 13. Estimated loss breakdown at  $P_{\rm B} = 4.1$  kW,  $V_{\rm D1} = 340$  V,  $V_{\rm B} = 57.8$  V, and  $I_{\rm D2} = 70$  A, and that at  $P_{\rm B} = 5.9$  kW,  $V_{\rm D1} = 355$  V,  $V_{\rm D2} = 59$  V, and  $I_{\rm B} = 100$  A.

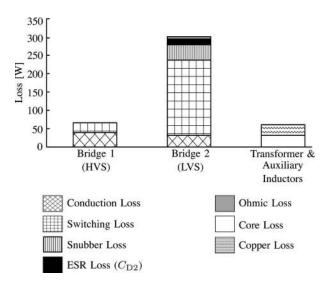


Fig. 14. Estimated loss distribution in bridges 1 and 2, and the magnetic components at  $P_{\rm B}=5.9\,{\rm kW},\,V_{\rm D1}=355\,{\rm V},\,V_{\rm D2}=59\,{\rm V}$ , and  $I_{\rm B}=100\,{\rm A}$ .

losses, is 71% of the loss in the dc-dc converter at the rated power.

The MOSFET employed in bridge 2 has a very low on-state resistance (0.5 m $\Omega$ ). As a result of a tradeoff, the very low on-state resistance compromises the switching loss in the MOS-FET. Therefore, this class of MOSFET is more optimal at lower switching frequencies to minimize the switching loss.

Fig. 12 indicates that the efficiency of the 6-kW bidirectional isolated dc–dc converter at the rated power can be improved when the switching frequency of the dc–dc converter is reduced. For example, at a switching frequency of 10 kHz, the overall efficiency of the dc–dc converter can be improved by 2-3% at the rated power. The extrapolation based on the experimental results shows that at the rated power, the dc–dc converter can

achieve an efficiency as high as 97% at a switching frequency of 5 kHz at the expense of generating acoustic noise and requiring a bulky transformer.

## VI. CONCLUSION

This paper has presented the experimental results from the combination of a 53.2-V, 40-A h Li-ion battery bank with a single-phase full-bridge bidirectional isolated dc-dc converter. The results have verified the proper operation of the Li-ion battery energy storage system. Discussions focusing on magneticflux saturation due to unavoidable dc-bias currents at the highvoltage and LVSs have been carried out. The transformer with an air-gap length of 1 mm has been shown experimentally to be robust against magnetic-flux saturation, even in the worst cases. The bidirectional isolated dc-dc converter exhibits high efficiency in the low-voltage and high-current operation. From the estimation of loss distribution in the dc-dc converter, a large portion of the loss at the rated power is caused by the turn off switching loss at the LVS. One of the best methods of improving the efficiency of the dc-dc converter is to operate it at a lower switching frequency. However, this method is accompanied by acoustic noise generation and a bulky transformer.

#### APPENDIX

The 9602 ac/dc clamp-on meters of Hioki 3139 have the following specifications:

- 1) Voltage meter
  - a) DC-voltage measurement range: 0–600 V;
  - b) accuracy:  $\pm 0.2\%$  of full scale.
- 2) Current meter
  - a) DC-current range: 0–500 A (depending on the rating of the clamp-on current transducer);
  - b) accuracy:  $\pm 0.2\%$  of full scale.

The dc-current ranges for the 9278 universal clamp-on current transducer at the HVS and LVS are 0–50 and 0–200 A, respectively. Their accuracies are  $\pm 0.05\%$  of full scale.

#### REFERENCES

- New Energy and Industrial Technology Development Organization (NEDO). (2008). Global warming counter measures: Japanese technologies for energy savings/GHG (greenhouse gases) emissions reduction (Revised ed.), [Online]. Available: http://www.nedo.go.jp
- [2] S. C. Smith, P. K. Sen, and B. Kroposki, "Advancement of energy storage devices and applications in electrical power system," in *Proc. IEEE Power Energy Soc. General Meeting*, Jul. 2008, pp. 1–8.
- [3] P. F. Ribeiro, B. K. Johnson, M. L. Crow, A. Arsoy, and Y. Liu, "Energy storage systems for advanced power applications," *Proc. IEEE*, vol. 89, no. 12, pp. 1744–1756, Dec. 2001.
- [4] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A threephase soft-switched high-power-density dc/dc converter for high power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Feb. 1991.
- [5] M. H. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge dc-todc converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, Nov./Dec. 1992.
- [6] S. Inoue and H. Akagi, "A bidirectional isolated dc-dc converter as a core circuit of the next-generation medium-voltage power conversion system," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 535–542, Mar. 2007.

- [7] J. Walter and W. W. De Doncker, "High-power galvanically isolated dc-dc converter topology for future automobiles," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, Jun. 2003, vol. 1, pp. 27–32.
- [8] L. Zhu, "A novel soft-commutating isolated boost full-bridge ZVS-PWM dc-dc converter for bidirectional high power applications," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 422–429, Mar. 2006.
- [9] F. Krismer and J. W. Kolar, "Accurate power loss model derivation of a high-current dual active bridge converter for an automotive application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 881–891, Mar. 2010.
- [10] S. Inoue and H. Akagi, "A bidirectional dc-dc converter for an energy storage system with galvanic isolation," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2299–2306, Nov. 2007.
- [11] N. M. L. Tan, S. Inoue, A. Kobayashi, and H. Akagi, "Voltage balancing of a 320-V, 12-F electric double-layer capacitor bank combined with a 10kW bidirectional isolated dc-dc converter," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2755–2765, Nov. 2008.
- [12] H. Zhou and A. M. Khambadkone, "Hybrid modulation for dual-activebridge bidirectional converter with extended power range for ultracapacitor application," *IEEE Trans. Ind. Appl.*, vol. 45, no. 4, pp. 1434–1442, Jul./Aug. 2009.
- [13] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, "Transformercoupled multiport ZVS bidirectional dc-dc converter with wide input range," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 771–781, Mar. 2008.
- [14] C. Zhao, S. D. Round, and J. W. Kola, "An Isolated Three-Port Bidirectional DC-DC Converter With Decoupled Power Flow Management," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2443–2453, Sep. 2008.
- [15] H. R. Weischedel and G. Westerman, "A symmetry correcting pulsewidth modulator for power conditioning applications," *IEEE Trans. Ind. Appl.*, vol. IA-9, no. 3, pp. 318–322, May/Jun. 1973.
- [16] D. Vinnikov, J. Laugis, and I Galkin, "Middle-frequency isolation transformer design issues for the high-voltage dc-dc converter," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, Jun. 2008, pp. 1930–1936.
- [17] S. Klopper and J. A. Ferreira, "A sensor for balancing flux in converters with a high-frequency transformer link," *IEEE Trans. Ind. Appl.*, vol. 33, no. 3, pp. 774–779, May/Jun. 1997.
- [18] Y. Xie, J. Sun, and S. Freudenberg, "Power flow characterization of a bidirectional galvanically isolated high-power dc/dc converter over a wide operating range," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 54–66, Jan. 2010.
- [19] G. S. Yuasa. (2007). Industrial Use Lithium-Ion Battery (LIM40/LIM80 Series) (in Japanese). [Online]. Available: http://home.gyps.gsyuasa.com/products/li/lim40.html
- [20] N. Miura, K. Fujihira, Y. Nakao, T. Watanabe, Y. Tarui, S.-I. Kinouchi, M. Imaizumi, and T. Oomori, "Successful development of 1.2 kV 4H-SiC MOSFETs with the very low on-state resistance of 5 mΩcm<sup>2</sup>," in *Proc. Int. Symp. Power Semicond. Devices Ics (ISPSD)*, Jun. 2006, pp. 1–4.
- [21] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," in *Proc. IEEE Workshop Comput. Power Electron.*, Jun. 2002, pp. 36–41.
- [22] N. M. L. Tan, T. Abe, and H. Akagi, "A 6-kW, 2-kWh lithium-ion battery energy storage system using a bidirectional isolated dc-dc converter," in *Proc. Int. Power Electron. Conf. (IPEC)*, Jun. 2010, pp. 46–52.



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