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Design and Performance of High T_c Superconducting Coplanar Waveguide Matching Circuit for RF-CMOS LNA

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SUMMARY As an RF high T_c superconducting (HTS) front end for a microwave receiver, we propose a new design method for the broadband matching circuit composed of coplanar waveguide (CPW) meanderline resonators connecting a slot antenna with CMOS low noise amplifier (LNA). The parameters of the antenna sections with matching circuit are calculated and simulated with the circuit simulator and electromagnetic field simulator. CMOS LNA was designed and its input and output impedances and noise figure were obtained by SPICE simulation.

key words: *microwave device, CMOS low noise amplifier, matching circuit, coplanar waveguide, HTS device*

1. Introduction

With the remarkable demands of data transmissions, such as wireless LAN, bluetooth, IMT-2000 and satellite telecommunications, there are many investigations of RF devices such as antenna, bandpass filter (BPF) and so on. Moreover, there are many reports on high T_c superconducting (HTS) BPF [1]–[4] and HTS BPF based cryogenic receiver front-end [5] is being fabricated for commercial use. For active devices, there are great expectations of RF-CMOS devices such as low noise amplifier (LNA) [6]. Coplanar waveguide (CPW) configuration is easy to connect the CMOS chip because the signal line and ground plane exist on the same side [7]. Beside, it is particularly well suitable for HTS films because only one side of the substrate needs to be coated before patterning. Figure 1 shows the typical block diagram of wireless terminal and RF section. Impedance matching circuit is necessary for interconnecting antenna and LNA. Although the lumped element such as the spiral inductor and MIM capacitor are adopted for matching circuit, it cannot be used at high frequency range because of the self-resonances and stray impedances. On the other hand, distributed element made of CPW transmission line is particularly effective because its size becomes smaller, as the frequency is higher, and it is easy to interconecction.

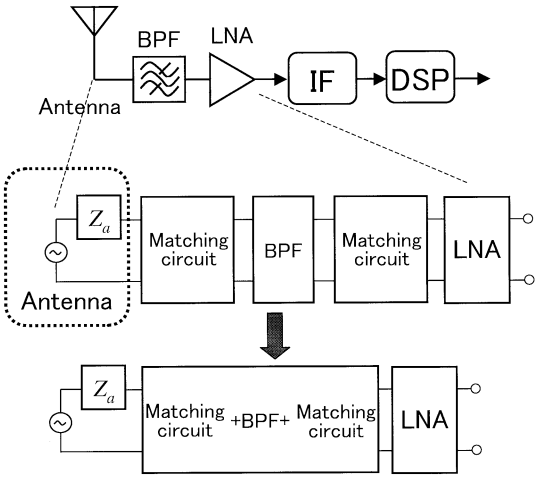

Fig. 1 Block diagram of wireless terminal and RF section.

In our previous paper [8], we proposed a new design method for the broadband impedance matching circuit for the small antenna, which is based on the conventional design theory of n-pole BPF [9]. In this paper, we generalize the design method to the CPW matching circuit connecting the slot antenna with the CMOS LNA (see Fig. 1). By obtaining the radiation resistance and the antenna reactance, and input impedance of the CMOS LNA for the susceptance slope parameters, we can design the fractional bandwidth and return loss in the passband of the matching circuit. The circuit simulator and electromagnetic field simulator studies provide the expected performances of the slot antenna and CMOS LNA with the impedance matching circuit designed with the present method.

2. Design Theory of Broadband Impedance Matching Circuit

The present theory is based on the conventional design theory for the n-pole Chebyshev BPF [9]. BPF can be realized by using the opened resonators connected with J-inverters ($J_{i,i+1}$). Figure 2 shows the circuit model of the LNA section, which is assumed to have load impedance Z_L=R_L+jX_L. At first, we propose

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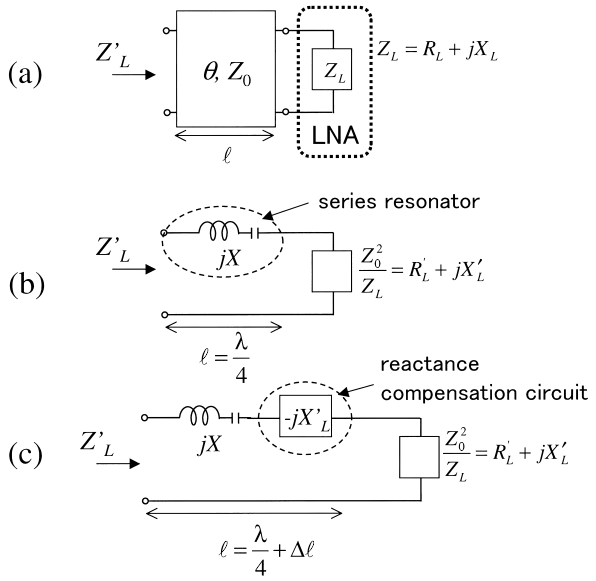

Fig. 2 Equivalent circuit model of matching circuit of LNA section: (a) circuit model, (b) equivalent circuit for $\ell = \lambda/4$ and (c) equivalent circuit for $\ell = \lambda/4 + \Delta\ell$.

the method for conjugate matching. In order to make impedance inversion, we insert the quarter wavelength transmission line, which has length (ℓ), electrical length (θ) and characteristic impedance (Z_0) (see Fig. 2(a)).

When $|Z_L| \gg Z_0$ and

$$\ell \cong \frac{\lambda}{4} \ \left(\theta \cong \frac{\pi}{2}\right), \tag{1}$$

it can be easily shown that the input impedance Z'_L seen from the left of the transmission line is approximately given by,

$$Z'_L \cong jX' + \frac{Z_0^2}{Z_L} = j\left(X + \omega_0 L \Delta\ell\right) + \frac{Z_0^2}{Z_L}, \tag{2}$$

where X' is the reactance for the $\lambda/4$ line and L is the inductance per unit length of the transmission line.

$$X = -Z_0 \cot\theta \cong x\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right), \tag{3}$$

and

$$x = \frac{\omega_0}{2}\frac{\partial X}{\partial \omega}\ |_{\omega=\omega_0} = \frac{\pi}{4} Z_0, \tag{4}$$

are the reactance and the reactance slope parameter of the series resonance circuit at $\omega = \omega_0$, respectively, as shown in Fig. 2(b). Inverted Z_L can be expressed as,

$$\frac{Z_0^2}{Z_L} = \frac{Z_0^2 R_L}{R_L^2 + X_L^2} - j\frac{Z_0^2 X_L}{R_L^2 + X_L^2} \equiv R'_L + jX'_L. \tag{5}$$

In order to compensate the jX'_L, we adjust the length by $\Delta\ell$ as (see Fig. 2(c)),

$$\Delta\ell = -\frac{X'_L}{\omega_0 L} = \frac{Z_0^2 X_L}{\omega_0 L\left(R_L^2 + X_L^2\right)}, \tag{6}$$

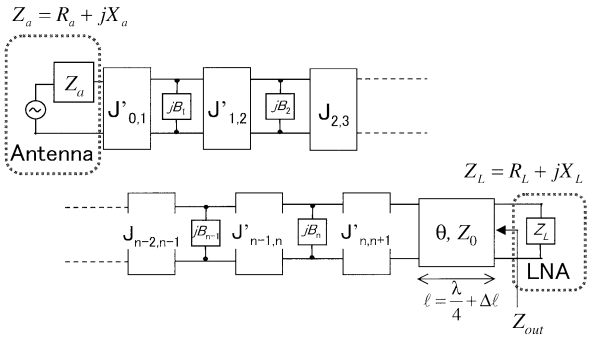

Fig. 3 Circuit model of n-pole matching circuit with antenna and LNA.

In the case of noise matching, it is easy to show Z_L=Z^*_{opt} (Z_{opt}=R_{opt}+jX_{opt} is the impedance which minimize the noise figure), and $\Delta\ell$ is given by,

$$\Delta\ell = -\frac{Z_0^2 X_{opt}}{\omega_0 L\left(R_{opt}^2 + X_{opt}^2\right)}. \tag{7}$$

Figure 3 shows the circuit model of n-pole broadband matching circuit with the antenna and LNA, where antenna impedance is Z_a=R_a+jX_a. The proposed design values for the admittance inverters (J-inverters) are given by,

$$J'_{0,1} = \sqrt{w}\sqrt{\frac{b'_1}{R_a g_1}}, \tag{8}$$

$$J'_{1,2} = w\sqrt{\frac{b'_1 b_2}{g_1 g_2}}, \tag{9}$$

$$J_{i-1,i} = w\sqrt{\frac{b_{i-1,i}\, b_i}{g_{i-1,i}\, g_i}}\ (i = 3, 4, \cdots, n-1), \tag{10}$$

$$J'_{n-1,n} = w\sqrt{\frac{b_{n-1,n}\, b'_n}{g_{n-1,n}\, g_n}}, \tag{11}$$

$$J'_{n,n+1} = \sqrt{w}\sqrt{\frac{b'_n}{R'_L g_n}}, \tag{12}$$

with,

$$b'_1 = \frac{b_1}{1 - \frac{w x_a}{R_a g_1}}, \tag{13}$$

$$b'_n = \frac{b_n}{1 - \frac{wx}{R'_L g_n}}, \tag{14}$$

where, x_a is the reactance slope parameter at the series resonance of the antenna impedance (see Ref. [8]), and b_n is the susceptance slop parameter of the $\lambda/2$ resonator which has susceptance B_n. g_i and w are normalized filter elements and fractional bandwidth, respectively. Substituting x of $\lambda/4$ line and R_L into b'_n,

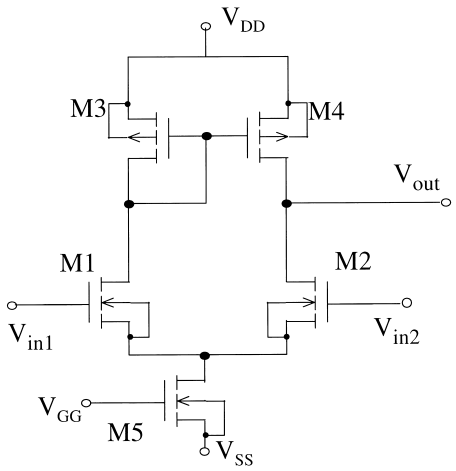

Fig. 4 Schematic diagram of CMOS differential amplifier.

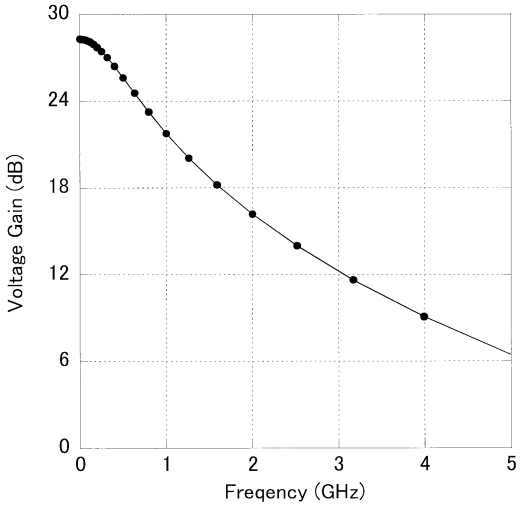

Fig. 5 Voltage gain of the CMOS LNA.

we can design the matching circuit with high impedance element. From Eqs. (8) to (14), the minimum constriction is n=2, where the total length of the matching circuit is as small as $5\lambda/4$.

3. Design of CMOS LNA

Figure 4 is the schematic diagram of CMOS differential amplifier. The voltage gain and Z_L is simulated by the HSPICE (Avanti!). The gate length and width are 0.6 μm and 10 μm, respectively (Rohm 0.6 μm process). We chose the typical MOSFET model and simulation temperature is 25°C. VDD is 5 V. g_m of nMOSFET and pMOSFET are 1.3 mA/V and 0.52 mA/V, respectively. Figures 5 and 6 show the simulated results of voltage gain and Z_L of the CMOS LNA. At 2 GHz, we obtained voltage gain =16 dB and $Z_L = 3.0 - j3.3$ (kΩ), respectively. The common-mode rejection ratio (CMRR) is 30 dB at 2 GHz.

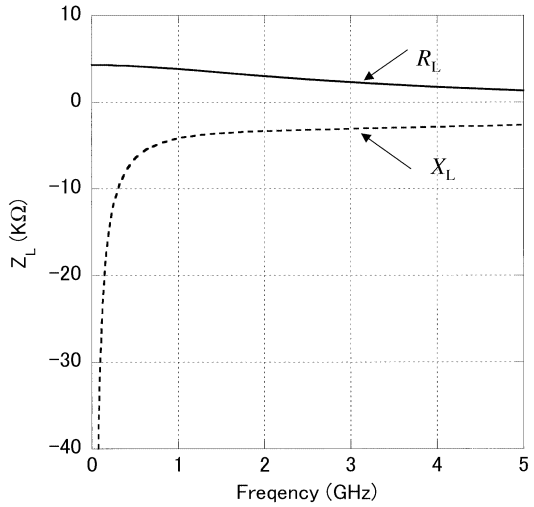

Fig. 6 Frequency dependence of Z_L of the CMOS LNA.

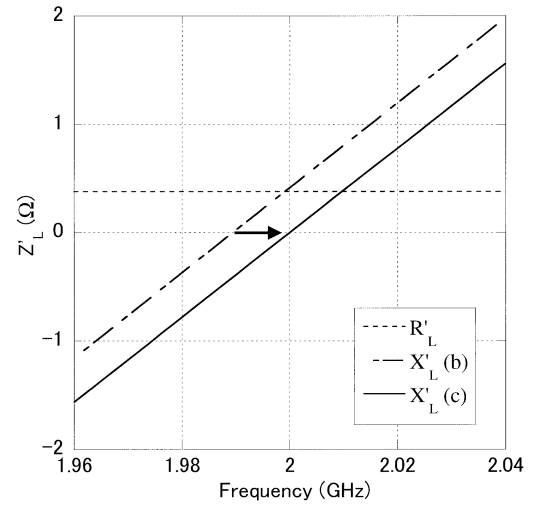

Fig. 7 Frequency dependence of Z'_L.

4. Simulation Results of Broadband Matching Circuit

Figure 7 shows the frequency dependence of Z'_L. In the figure, X'_L(b) shows the reactance in the case of Fig. 2(b). Also, X'_L(c) shows the reactance including the compensation reactance at 2 GHz (see Fig. 2(c)). We assume that the lossless conductor is placed on the MgO substrate with thickness on 0.5 mm and relative dielectric constant = 9.6, so that, $\Delta\ell$ is calculated as −85.8 mm at 2 GHz from Eq. (6).

At first, we discuss the properties of matching circuit connecting LNA with 50 Ω line, namely, in the case of Z_a=R_a=Z_0 in Eqs. (8) and (9). So that, $J_{0,1}$ and $J_{1,2}$ are rewritten by,

$$J_{0,1} = \sqrt{w}\sqrt{\frac{b_1}{Z_0 g_1}}, \tag{15}$$

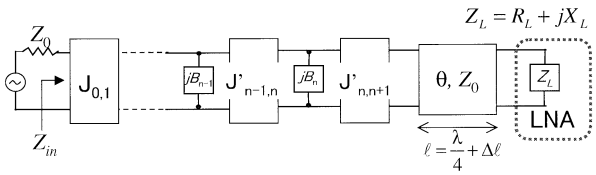

Fig. 8 Circuit model of $\lambda/2$ n-pole matching circuit with LNA and Z_0.

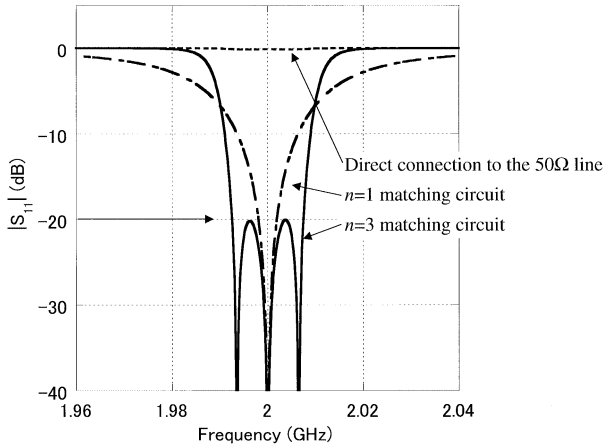

Fig. 9 Input return loss of the LNA with the matching circuit.

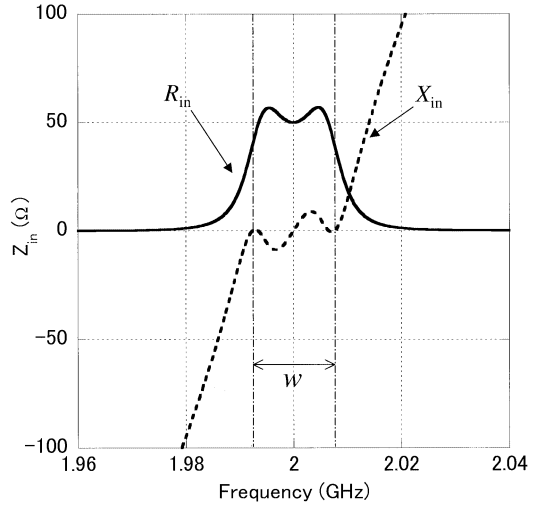

Fig. 10 Frequency dependences of the input impedance Z_{in}.

$$J_{1,2} = w\sqrt{\frac{b_1 b_2}{g_1 g_2}}. \tag{16}$$

Figure 8 shows the circuit model of $\lambda/2$ matching circuit connecting LNA with Z_0 line. The design parameters are: f_0=2 GHz, w=15 MHz and return loss in the passband =20 dB. Figure 9 shows the input return losses of the LNA with the n=3 and n=1 matching circuit. In the figure, the response of the direct connection of the LNA with the 50 Ω line is also plotted. It is shown the bandwidth at 20 dB return loss increases

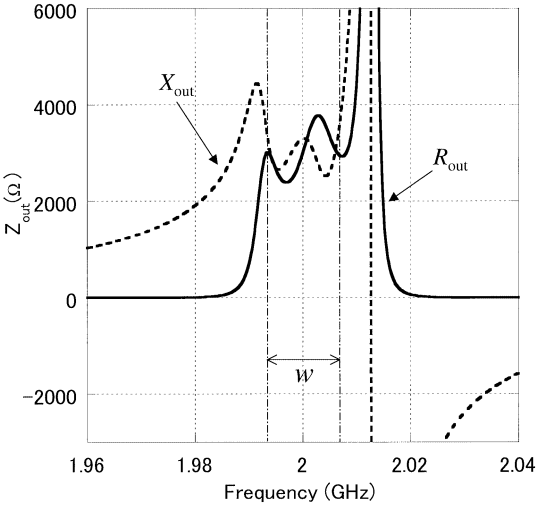

Fig. 11 Frequency dependences of the output impedance seen toward the antenna.

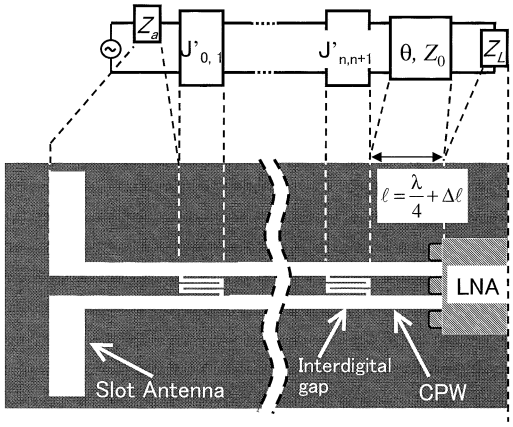

Fig. 12 Schematic diagram of the matching circuit of the antenna and LNA section.

and skirt characteristic become sharper as n decreases. Figure 10 shows the frequency dependence of the input impedance Z_{in} seen from the left of the inverter $J_{0,1}$ as shown in Fig. 8. R_{in} and X_{in} are almost matched to Z_0 (50+j0 Ω) in the passband. These frequency dependences have the Chebyshev properties.

Next, we discuss the matching circuit connecting the LNA with the antenna instead of 50 Ω line (see Fig. 3). Figure 11 shows the frequency dependence of the Z_{out} seen from the LNA towards antenna as shown in Fig. 3. R_{out} and X_{out} are almost matched to Z_L^* (=3.0+j3.3 (kΩ)) in the passband. They also have the Chebyshev properties. Figure 12 shows the schematic diagram of the CPW broadband matching circuit connecting with LNA and slot antenna, where J-inverters are realized by the interdigital gaps. Figure 13 shows the EM-simulation (Agilent: Momentum) layout of the n=3 broadband matching circuit connecting with 50 Ω line and LNA. For the size reduction, we adopt the mender line structure. For EM-simulation, we assume

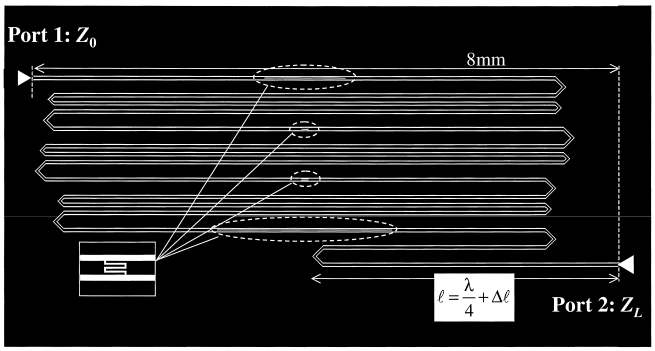

Fig. 13 EM-simulation pattern of the 2 GHz n=3 meander line CPW matching circuit.

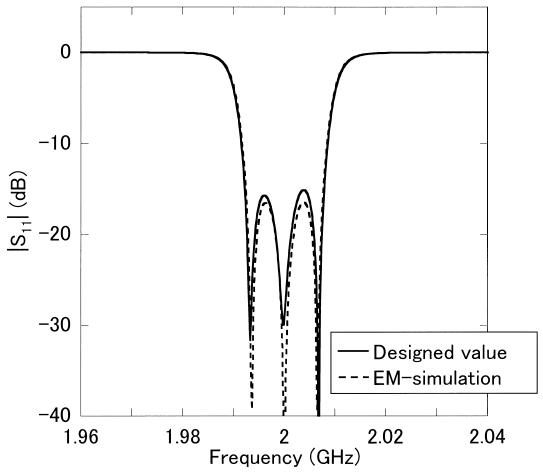

Fig. 14 Simulation results of n=3 matching circuit.

that the loss less conductor is placed on MgO substrate with a thickness of 0.5 mm and relative dielectric constant of 9.6. The width of the center conductor is 35 μm, and the width between the ground conductors is 66 μm. Figure 14 shows the EM-simulation result of the n=3 matching circuit (Design ripple = 0.1 dB). In the figure, the designed value (theoretical value) is also plotted. The simulation result is in good agreement with the designed value.

5. Conclusion

We present a design theory for the broadband impedance matching circuit connecting the slot antenna with LNA, which incorporates the radiation resistance and the antenna reactance, and input impedance of the CMOS LNA into the susceptance slope parameters of the conventional filter theory. The prototype HTS practical device, which integrates the slot antenna and the CPW matching circuit, is now fabricating on the YBCO thin film. Design of the on chip matching circuits for RF-CMOS is also in progress.

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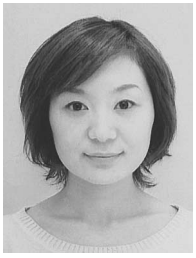

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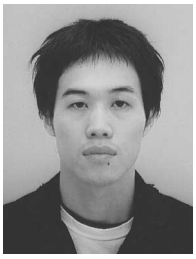

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