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Design and Simulation of a 2.4 GHz VCO with High Q MEMS Inductor and CMOS Varactor

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***Abstract*—This paper presents design of high-performance MEMS inductor and CMOS varactor for use in CMOS voltage controlled oscillators (VCO) operating at 2.4 GHz. The high-Q air suspended inductor has been designed by inductance of 2.87 nH using MEMS technology to reduce the resistive loss and the substrate loss. A CMOS varactor has been designed. The DC voltage is 2.5v which is applied to the CMOS and the results of 0.6 pF could be achieved. Through this optimization, less phase noise (-117.7 dBc / Hz at 100 KHz) and lower power consumption (11 mW) have been obtained.**

***Index Terms*— VCO; MEMS; CMOS; Inductor; Varactor; Q factor**

I. INTRODUCTION

A voltage controlled oscillator can be controlled its frequency of oscillation by an input voltage. Tuned oscillators need some kind of frequency-selective or tuned circuit in a feedback configuration and they generate sinusoidal output. Tuned oscillators usually place switched-capacitor circuits, LC circuit, RC circuit or crystal into a feedback loop when the loop gain should becomes positive and equal to unity[1].

In an LC oscillator L and C could be in parallel or series, but the most important factor which is caused a low power and low noise oscillator is quality factor of inductor and varactor of LC-tank. It means a Q factor is a Figure of merit to evaluate the inductor and varactor.

The needs for low phase noise VCO are High Q factor inductor and varactor. The Q of inductor has been improved due many researches on it [1-7]. Among those investigations using MEMS technology is the best solution to design an inductor with high Q factor.

While the reasons for low- factors come from thin metal layers (ohmic loss) and high substrate coupling (eddy-current loss) in standard silicon processes. MEMS techniques have been developed to reduce the substrate loss.

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On the other hand using a CMOS varactor allows a larger tuning range, for a given applied voltage. Therefore the phase noise of VCO can be improved by using MEMS inductor when the power consumption still remains low [8, 9].

This paper concerns on designing of LC oscillator because of the advantages of using in RF frequency (2.4 GHz), sinusoidal output and ability to improve specification of LC-tank with MEMS technology which will be describing. The main aim of this investigation is to enhance the understanding of VCO operation while MEMS inductor has been optimized. To the best of author's knowledge, this work has been reported the lowest value for phase noise by keeping the power consumption low. After the design and modeling of MEMS inductor the VCO circuit presented and the characteristic of VCO such as phase noise and power consumption have been discussed.

II. PHASE NOISE IN VCO P

The performance of an oscillator is measured by phase noise and power. The output of oscillator in a typical transceiver of wireless system is important when the oscillator provides the carrier signal for both the receiver and the transmitter. If the VCO has high phase noise, both down-converted and up-converted signals are disturbed. A simple model of the oscillator noise spectrum has been developed by Leeson to find out the phase noise of the oscillator [10].

There are two sources of noise in an oscillator, thermal and flicker noise. Thermal noise is proportional to T as an absolute temperature. Flicker noise happens because of the structure of MOSFETs and is proportional to $1/f$ because of that it has been called as a $1/f$ noise also.

The total phase noise of the closed loop system of an oscillator normalized to a 1 Hz bandwidth is given by:

$$S_f(f_m) = 10\log_{10}\left[\left(1+\frac{f_0^2}{(2f_mQ_L)^2}\right)\left(1+\frac{f_c}{f_m}\right)\left(\frac{KTF}{P_0}\right)\right] \quad (1)$$

Where K is the Boltzmann's constant, K=1.38*10-23 J/k, F is the noise Figure of the amplifier and P0 is the power of the oscillator at the output. Offset frequency is shown by fm and corner frequency is fc. In this case KTF/P0 is the thermal noise versus signal power, fc /fm is signal symmetry term which these two terms are circuit design issues and QL is the fundamental limitation of PN. It is clear the high Q of resonator is needed for better results of phase noise [11, 12].

III. POWER DISSIPATION

Oscillators are required to have long stability, so the low power consumption in oscillator is needed. In a VCO, it is difficult to obtain low phase noise with low power

consumption at the same time because the tank voltage amplitude is proportional to the current flowing. Therefore, there is a compromise between phase noise and power consumption [10]. As the tank voltage changes, the direction of the current flow through the tank will also change. The differential pair can be modeled as a current source switching between *Itotal* and *–Itotal* in parallel with an *RLC* tank. *Req* is the equivalent parallel resistance of the tank. The tank amplitude can be approximated as:

$$V \approx I_{total}.R_{eq} \quad (2)$$

This is referred to as the current-limited operation because tank amplitude mainly depends on the total current flowing and the tank's equivalent resistance. However, Equation (2) becomes invalid when the tank amplitude becomes equal to the supply voltage through an increase of *Itotal*. This operation is called the voltage-limited operation [13]. With current limited operation, as the current increases (consuming more power), the phase noise lowers because the tank amplitude is increasing simultaneously. Finally when total DC supply current will be I_0 the average power consumption at the supply V_{dd} will be [14]:

$$P_{av} = 2V_{dd}.I_0 \quad (3)$$

I_0 is obtained from:

$$I_o = (b/p)*\begin{pmatrix}(-V_1^2/2)\sin 2j_1 - (V_1^2+V_{th}^2/2)j_1 + 2V_1V_{th}\sin j_1 \\ +(V_1^2/8)\sin 2j_2 + (V_1V_{dd}/2 - V_1Vth)\sin j_2 \\ +(V_1^2/4 + V_{dd}^2/8 - V_{th}V_{dd}/2 + V_{th}^2/2)j_2\end{pmatrix} \quad (4)$$

Where φ_1, φ_2 and V_1 are as below:

$$j_1 = \cos^{-1}(V_{th}/2V_1) \quad (5)$$

$$j_2 = \cos^{-1}((V_{th} - V_{dd}/2)/V_1) \quad (6)$$

$$V_1 \quad V_{dd}/2 \quad (7)$$

IV. DESIGN OF MEMS INDUCTOR

A high quality spiral inductor can be designed by taking into considerations following points [4, 15]:

It should be hollow at high frequencies because the innermost turns of the coil suffer from enormous increase in resistance when it is not hollow.

- Opposing sets of coupled lines in hollow part of the spiral should be separated at least 5 times the width of the wire segment (*w*) to allow enough magnetic flux to pass through it.
- The width of the metal inductors should be about 10 to 15 μm for an optimum *Q* factor.
- Using minimum allowable spacing between metal segments causes the maximum magnetic coupling to achieve maximum of *Q* factor and reduces the chip area.
- The space between the outer spiral turn and any other surrounding metal structures should be at least 5*w* to avoid any unwanted coupling.
- More turns and smaller outer dimension increase the self inductance and mutual inductance.

A. Layout Design

The layout of the square spiral inductor is shown in Figure 1. For the given shape the inductor parameters are completely specified by the numbers of turns n, the metal width w, the metal spacing s, and the outer and inner diameter dout and din respectively. The thickness of the inductor (t) has very small effect on inductance [16].

The starting point for the designing of the layout is Greenhouse theory [17]. Greenhouse decomposed inductor into its constituent segments. Thus the spiral inductor is divided into straight conductive segments.

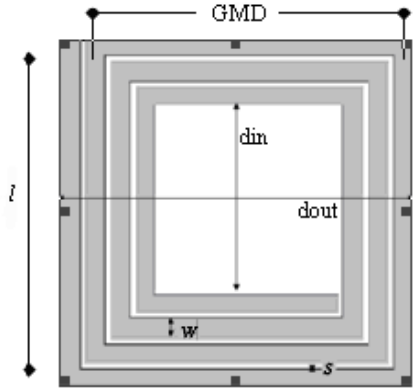

Figure1: The layout of inductor

The total inductance of the spiral inductor is a sum of self-inductances of all segments and the negative and positive mutual inductances between all combinations of straight segments. However in this theory the fringe effect of the corners has been neglected. The expression for self-inductance (Ln) mutual inductance (M) and total inductance (LT) of the conductive segment are given as following:

$$L_n = 2l_n\{\ln[2l_n/(w+t)] + 0.50049 + [(w+t)/3l_n]\} \quad (8)$$

$$M = 2*l*Q \quad (9)$$

$$L_T = L_n + M_+ - M_- \quad (10)$$

$$l_{2y} = l_2 - (y-1)(w+s), \; y \geq 2 \quad (11)$$

$$l_{2y-1} = l_1 - (y-2)(w+s), \; y \geq 2 \quad (12)$$

where Ln and ln are inductance and length of nth segment respectively. n is number of turns of inductor.

$$Q = \ln\{(l/GMD) + [1 + (l^2/GMD^2)]^{1/2}\} - [1 + (GMD^2/l^2)]^{1/2} + (GMD/l) \quad (13)$$

$$\ln GMD = \ln d - \{[1/12(d/w)^2] + [1/60(d/w)^4] + [1/168(d/w)^6] + [1/360(d/w)^8] + [1/660(d/w)^{10}] + ...\} \quad (14)$$

The geometric mean distance (GMD) is the distance between the centers of two arbitrary cross-sections of the conductors.

A procedure for calculating inductance value for a single turn rectangular inductor is presented now. The same procedure can be extended for inductors with more number of turns. A single turn inductor is shown in Figure 2. It has five segments (segment 1 – segment 5) having inductance value L1 – L5 respectively. M1,5 is positive mutual inductance and M1,3 and M2,4 are negative mutual inductances. For a given length of segment 1 and segment 2, the length of other segments in the spiral has been calculated

using Equations (11) and (12). The GMD for each segment is calculated from the dimensions of each segment. Equation (8) is used to calculate the inductance of each segment. The mutual inductance is calculated using Equation (9). The total inductance of the single turn coil is given by following Equation:

$$L = L1 + L2 + L3 + L4 + L5 + M1,5 - M1,3 - M2,4 \quad (15)$$

It is observed that the length of segment 1 and segment 2 are very critical in determining the area of the spiral inductor.

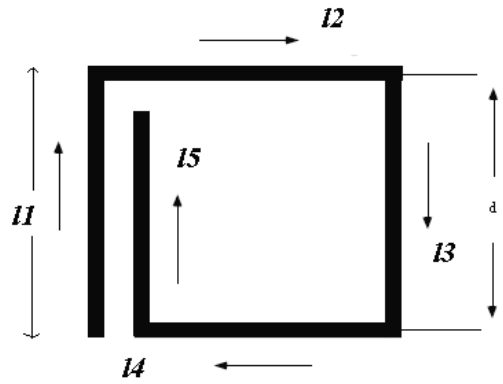

Figure 2: The current direction in each segment of inductor

MATLAB program has been used to compute the dimensions of inductor. The results of the program output are given in Table 1 for t = 15×10-4 cm, w = 1×10-3 cm, s = 3×10-4 cm and l1 = l2 = 18×10-3 cm.

TABLE 1: CALCULATED VALUE OF INDUCTOR USING MATLAB

Ln (nH)	M+ (nH)	M- (nH)	LT (nH)
1.245323	2.484299	0.795743	2.933879

Design and Simulation Process

CoventorWare software has been used in this work for MEMS design and simulation. The design process of integrable MEMS inductor, which allows fabricating CMOS compatible highly suspended metal microstructures, is presented in this section. Silicon substrate has been used to design high-Q inductor compatible with CMOS technology.

The inductor has been fabricated on oxidized silicon substrate for thick insulation layer. To avoid the resistive loss that results from use of relatively thin (0.5~2 μm) metal layer, low resistivity material has been used and the thickness of metal layers has been made much larger than the skin depth. In this research, the electroplated thick copper layers, which have a low resistivity of 1.7 μΩcm has been used. The other loss mechanism to be minimized is substrate-induced loss, which comes from electromagnetic coupling between substrate and metal on top of it. The substrate coupling can be significantly reduced by using a suspended metal structure from the substrate. In this study, we design MEMS inductors suspended by 30 μm from the top most layers.

The fabrication processes include oxidation, etching and metallization. The first step in the fabrication is to oxidize the top layer for the silicon substrate to provide an insulating layer (Figure 3). This layer is deposited to isolate substrate from conductor. The etch process is applied to this layer as first mask to provide the pads of inductors. Then the copper would be deposited for pads. A sacrificial Titanium layer is deposited now to provide a gap between substrate and conductor. This layer would be removed after all the processing steps have been completed. In order to support the suspended inductor, the copper should be substituted with Titanium in the holes on pads which are made after etching. Finally, the sacrificial layer is removed to suspend the conductor from substrate.

Meshing is needed to divide the device to small elements and obtain the solution for each filaments of the device. After integrating of each element's solution, the final results will be obtained. For meshing the solid model has been meshed and the geometry of the structure has been reduced to a group of simpler finite element bricks and presented to the solver for finite element analysis.

TABLE 2: THE INDUCTANCE AND RESISTANCE OBTAINED FROM COVENTORWARE ANALYSIS

Frequency (Hz)	Resistance (Ohm)×10-1	Inductor (nH)×10-9
1.0×105	9.298823	2.929822
1.3895×106	9.298829	2.929822
1.2452×107	9.299335	2.92982
1.11588×108	9.339886	2.929547
1×109	12.08181	2.912387
1.55052×109	14.94953	2.896092
2.4041×109	19.55385	2.872307
3.72759×109	25.63956	2.84479
5.77969×109	32.3385	2.819353
8.96151×109	38.74896	2.799873

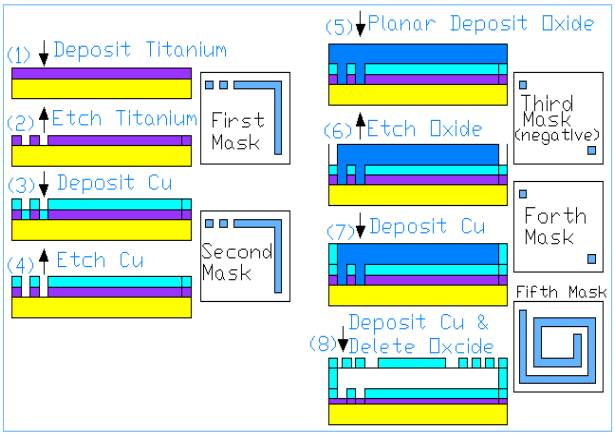

Figure 3: The fabrication process of inductor

After completing the layout, a 3-D model has been built using thickness and etches profile information from the process file and the 2-D layout mask information.

We have used the manhattan model mesh which has orthogonal geometry for inductor; this implies that all model faces (patches) are planar and joined at 90 degrees angles. The solid model after applying mesh is shown in Figure 4.

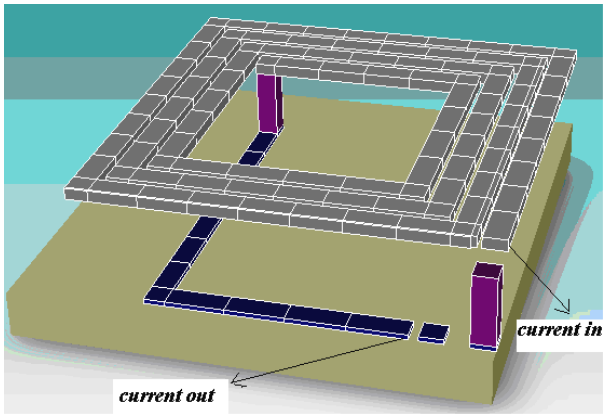

Figure 4: Mesh model of inductor

The gaps between not joined parts of inductor will be connected in the analyzer part of inductor.

As seen in Table 2 the inductance and resistance of the inductor are 2.86 nH and 2.01 Ω at 2.4 GHz.

In comparison the results which are obtained from simulation with the results which we expected from theoretical computation (Greenhouse method) good agreement could be seen. 2.934nH and 2.87nH are the amounts for inductance from Greenhouse and CoventorWare respectively.

C. Modeling and Q Factor of inductor

The designed inductor modeled based on lumped parameter model given by Yue [18] is shown in Figure 5. In this model Ls is the spiral inductance, Cox is the oxide capacitance from the metal layer to the substrate, Rs is the resistance of the metal layer that is frequency dependent, Rsi and Csi are substrate resistance and substrate capacitance respectively and Cs is the underpass capacitance between wires.

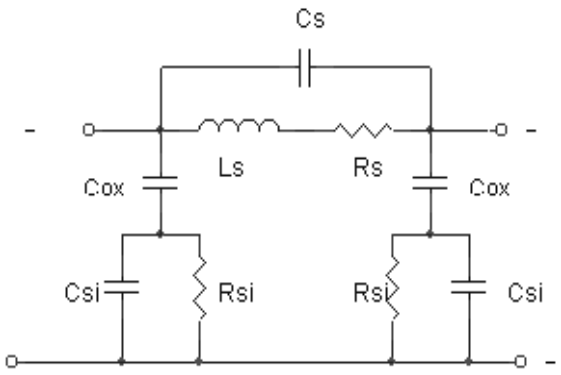

Figure 5: Lamped inductor model (Yue's model)

the Q of on chip inductors is given by:

$$Q_{ON-CHIP} = \frac{wL_s}{R_s} \times \frac{R_p}{R_p + \left[\left(\frac{wL_s}{R_s}\right)^2 + 1\right].R_s} \times \left(1 - \frac{R_s^2 C_o}{L_s} - w^2 L_s C_o\right) \quad (16)$$

where

$$R_p = \frac{1}{w^2 C_{OX}^2 R_{si}} + \frac{R_{si}\left(C_{OX} + C_{si}\right)^2}{C_{OX}^2} \quad (17)$$

Co = Cp + Cs,

and

$$C_p = C_{OX} \cdot \frac{1 + w^2\left(C_{OX} + C_{si}\right) C_{si} R_{si}^2}{1 + w^2\left(C_{OX} + C_{si}\right)^2 R_{si}^2} \quad (18)$$

The results for parameter calculation of inductor have been summarized in Table 3.

TABLE 3: THE CALCULATED PARAMETERS OF INDUCTOR

R_s (Ω)	C_s (fF)	C_{ox} (fF)	R_{si} (Ω)	C_{si} (fF)
2.23	81.99	288.94	844.17	86.54

The results show the good agreement in a value of series resistance of inductor between simulation and calculation results. This could be validated the achieved results. Using Equations (16) led us to achieve the Q factor of an inductor about 27 which is good enough value in comparison with other previous works.

V. CMOS VARACTOR DESIGN

The configuration of MOSFET as a varactor in this work is leaving drain and source open and applying voltage across the gate and bulk only. This type of varactor is known as an accumulation varactor. The capacitance always decreases with increasing control voltage. Figure 6 shows the behavior of varactor. In this Figure the capacitance versus Vgs (Vcontrol –Vg =Vgs) has been plotted.

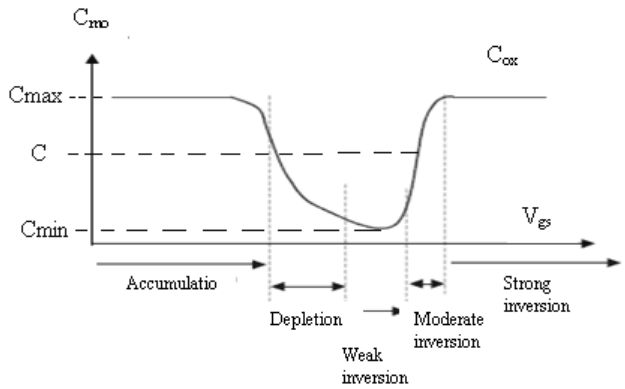

Figure 6: The response of the B-S-D varactor by applying voltage to the gate

MOSFET model PMOS BSIM3 from HP 14TB has been used to determine minimum (Cmin) and maximum (Cmax) value of capacitor. The Cmin and Cmax are given by following Equations:

$$C_{\min} = C_{gdo}.W \quad (19)$$

$$C_{\max} = \frac{3.9 e_0 WL}{T_{ox}} N \quad (20)$$

Where C_{gdo} is the gate-drain capacitance (= 2.41E-10 F/m) for above model. W is the width of channel, L is the length of channel, N is the number of gate fingers (=1) for this model. $e_0 = 8.84542 * 10^{-12} F/m$ and $T_{ox} = 9.8\text{E-}9$. The average value of capacitor (C) is given as:

$$C = \frac{C_{\max} + C_{\min}}{2} \quad (21)$$

In order to maximize the Q, we should choose L as short as possible and this will be determined by the process technology. For $W = 500mm$ and $L = 0.6mm$ we have

$C_{\max} = 1.05pF, C_{\min} = 0.12pF$ and $C = 0.585pF$.

Figure 7 shows the circuit to simulate the behavior of varactor with variable bias voltage in ADS software. The value of control voltage is 2.5v. The variation of varactor capacitance against the bias voltage is shown in Figure 8. The minimum and maximum value of the capacitor are $C_{\min} = 0.11pF$ and $C_{\max} = 0.72pF$, the closely matches with the expected value.

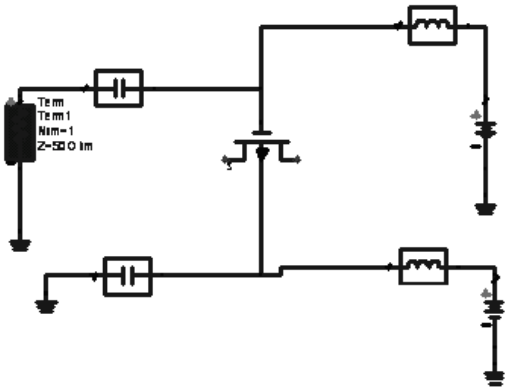

Figure 7: Circuit to characterize the varactor

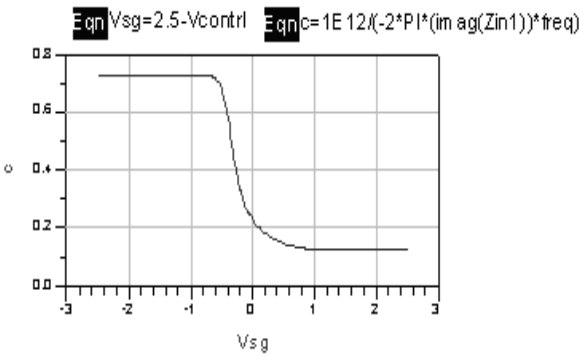

Figure 8: Varactor capacitance versus bias voltage characterize

A.. Q of the varactor diode

The Q of the MOS varactor is given by [19]:

$$Qmos = \frac{12}{w.C_{ox}.W.L}.K_p.\frac{W}{L}(Vgs - |V_T|) \quad (22)$$

Where w is the frequency, C_{ox} is (= $\frac{3.9.e_0}{T_{ox}}$), K_p gain factor ($= MUZ.C_{ox}$), Vgs is gate-source voltage and V_T is theroshold voltage. For the model chosen, we have $C_{ox} = 0.0035\,\mathrm{F/m^2}$ and $K_p = 51.35mA/V^2$. The Q factor for $Vgs - |V_T| = V_{dd}/2$ is 40.53. This is in good agreement with the desired value of Q=40.

VI. QUALITY FACTOR OF AN LC-TANK

The LC-tank which has been used in this work is a parallel inductor and capacitor. The loaded Q in the LC-tank is a measure of the Q factor of the elements and computed as below:

$$\frac{1}{Q_T} = \frac{1}{Q_L} + \frac{1}{Q_C} \quad (23)$$

Whereas the obtained Q of inductor in this work is 27 and the Q factor of capacitor is about 39 the total Q of the LC-tank is 15.95, which is good enough to get acceptable results from VCO.

VII. CROSS-COPLED PAIR VCO DESIGN

Cross-coupled pair VCO is the best topology for RF oscillator circuit. It has large voltage swing, Symmetric structure and Differential output. These circuits can be easily integrated with baseband CMOS digital circuits. Two NMOS transistors which have been used in the circuit are coupled in positive feedback to provide a negative resistance. The minimum power supply needed for operating this circuit is VD,sat PMOS +VGS NMOS. The dimensions of the transistors are very important to minimize the noise. The ratio of NMOS and PMOS transistors has been optimized for reducing the flicker noise. The actual NMOS transistor widths have been determined for thermal noise reduction. We have used ratio for NMOS to PMOS transistors to be about 1:2.5. this is the best ratio reported on the literature review [8].

One role of an active part of the oscillator circuit is to compensate for the losses in the LC-tank for a stable oscillation. Figure 9 shows the positive and negative resistance between active part and LC-tank circuit. The cross-coupled pair has a negative resistance around -2 / gm. If all losses in the LC-tank are equal to RP, then for the oscillation to start the negative resistance should be equal to the positive resistance. The minimum value of transconductance (gm) of cross-coupled transistors for oscillation is obtained from the condition that:

$$2/g_m \geq R_p \quad (24)$$

Where RP is series resistance of inductor and is given by:

$$R_p = \frac{2p.f.L}{Q_{ind}} \quad (25)$$

L is the inductance; f is the frequency and Qind is the Q of the inductor. The gm of the transistor is given by:

$$g_m = \frac{I_D}{Vgs - V_T} = \left[2K'\frac{W}{L}I_D\right] \quad (26)$$

Where ID is the DC bias current and can be substitute by RP to give us the desired bias current.

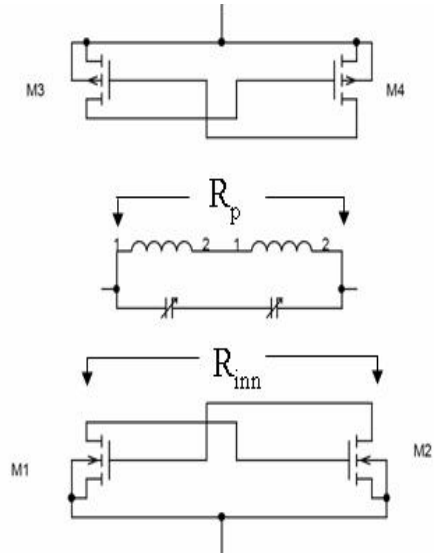

Figure 9: VCO circuit with positive and negative resistance

The dimensions of the transistors of active part have been computed and it is given as:

$$\frac{W}{L} = \frac{g_m^2}{2KI_D} \quad (27)$$

Equation (27) gives the minimum W/L ratio required to give oscillation. In this work ID assumed as 3.5 mA so the K of each transistor will be calculated from Equation (26). All the Equations above lead to calculate the specification of the oscillator for designing of active part.

The schematic of the oscillator is shown in Figure 10 and simulation has been done by ADS software.

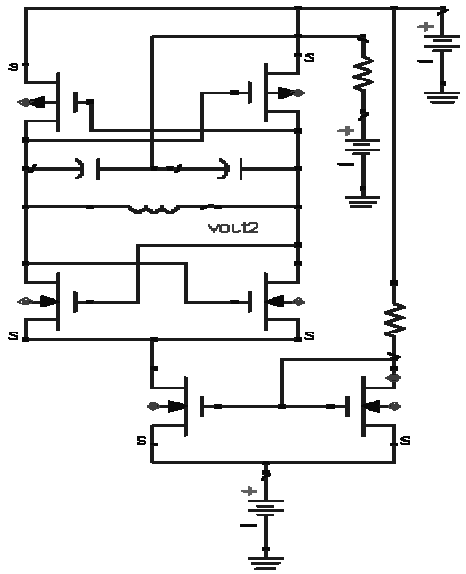

Figure 10: The schematic of the oscillator using ADS

The calculated value of gm is about 1.4 mS where as the minimum value to start oscillation is about 2.3 mS. This is obtained based on model of transistors and Kn and Kp to be equal to 150.85*10-6 A/Vs and 51.3514*10-6 A/Vs respectively. We have calculated W of PMOS and NMOS about 14.7 μm and 5.0095 μm respectively. L has been taken as 1 μm. Phase noise obtained in our design is -117.5 dBc / Hz at 10 KHz. The power consumption is about 11 mW.

Figure 11 shows the out put signal of oscillator which is oscillating at 2.4 GHz. We observe that the output signal is symmetrical. Figure 12 illustrates the phase noise plot obtained using ADS simulation. The measured phase noise was at 100 KHz is -117.7 dBc/Hz. It can be noted the phase noise in comparison with the other works is in very good situation especially when the power consumption is not very high.

TABLE 4: COMPARISON FOR DIFFERENT VCOS

References	LC-tank	Frequency GHz	Phase noise dBc/Hz	Supply voltage V	Current mA
Young and boser[20]	MEMS varactor, Wire bonding inductor	0.714	-107@100KHz	3.3	15
Dec and suyama[21]	MEMS varactor, Wire bonding inductor	2.4	-93@100KHz	2.7	5
Ramachand[9]	MEMS inductor, Varactor diodes	2.45	-104@100KHz	N.C.	2
Park [8]	MEMS inductor, MOS varactor	2.6	-117@600KHz	3	5
Chen [22]	MEMS inductor, MOS varactor	2.78	-121@600KHz	3	2.1
This work	MEMS inductor, MOS varactor	2.4	-117.7@100KHz	2.5	3.5

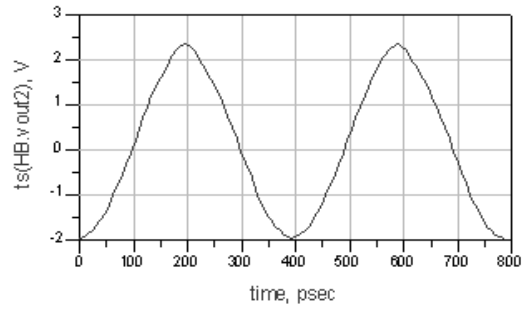

Figure 11: Output of oscillator

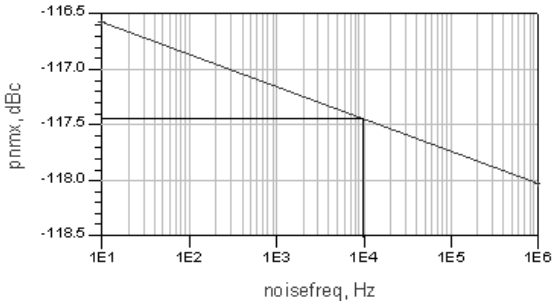

Figure 12: Phase noise measurement of oscillator

VIII. VALIDATION OF THE SOLUTION

It should be noted the verification for the value of Q factor in inductor which comes from Equation (16) depends on the values of inductance of inductor, the material properties and center frequency. The value of inductance is verified by two methods, the analytical calculation of greenhouse and simulation results of CoventorWare and the results are in good agreement. The center frequency is defined 2.4GHz and the material properties got from handbooks. Park [8] reported an inductor about 1.8 nH and 400*400 μm2 area, the Q factor achieved about 25. It should be noted in this work the area has been reduced and Q factor has been increased.

Table 4 shows some recently published VCOs as can be found this work has the best results using the optimization in design of LC-tank to reduce phase noise by keeping power consumption low.

IX. CONCLUSION

In this paper the spiral inductor designed and simulated. The inductance computed using Greenhouse equations about 2.93 nH, the specification of inductor assumed using the review points. The layout and 3-D model of inductor designed by CoventorWare software about 2.87 nH, so the value of inductance verified using simulation. Modeling the inductor is based on Yue's model to find the parameters of equivalent circuit and the Q factor of inductor. The series resistance of inductor is calculated about 2 Ω which is in good agreement to the results of simulation. The high Q factor achieved about 27.

CMOS varactor has been designed in this work as well; the Q factor of varactor has been achieved about 39.

Finally the major steps of designing VCO circuit have been investigated. The basic topology of oscillator has been described. VCO circuit simulated using ADS software. The dimensions of transistors have been achieved about 15/1 μm for PMOS and 5/1 μm for NMOS transistor.

The results in phase noise are about -117.7 dBc / Hz at 100 KHz and the power consumption is 11 mW. The results are pleased enough in comparison with other previous works and the phase noise has been decreased by applying optimization in LC-tank.

REFERENCES

[1] D. A. Johns and K. Martin, Analog integrated circuit design, 1997.
[2] L. E. Larson, M. Case, S. Rosenbaum, D. Rensch, P. Macdonald, M. Matloubian, H. Chen, J. Malinowski, B. Meyerson, and S. Gilbert, Si/SiGe HBT Technology for low-cost monolithic microwave integrated circuits, In Proceeding International Solid circuits Conference (1996), 80-81.
[3] K. B. Ashby, I. A. Koullias, W. C. Finley, J. J. Bastek, and S. Moinian, "High Q inductors for wireless applications in a complementary silicon bipolar process," IEEE Journal of Solid-State Circuits 31 (1996), 4-9.
[4] J. R. Long and M. A. Copeland, The modeling, characterization and design of monolithic inductors for silicon RF IC's, IEEE Journal of Solid State Circuits 32 (1997), 357-369.
[5] C. Yue, C. Ryu, J. Lau, T. Lee, and S. A. Wong, physical model for planar spiral inductors on silicon, IEEE International Electron Devices Meeting (1996) 8-11.
[6] B. K. Kim, B. K. Ko, and L. K, Monolithic planar RF inductor and waveguide structures on silicon with performance comparable to those in GaAs MMIC, In IEDM Technology Digest (1995), 717-720.
[7] H. Jiang, Y. Wang, J. Yeh, and N. Tien, ON-Chip Spiral Inductors Suspended over Deep Copper-Lined Cavities, IEEE Journal of Transactions on Microwave theory and Techniques 48 (2000), 2415-2423.
[8] E.-C. Park, Y.-S. Choi, J.-B. Yoon, S. Hong, and E. Yoon, "Fully integrated low phase-noise VCOs with on-chip MEMS inductors, IEEE Journal of Transactions on Microwave Theory and Techniques 51 (2003) 289-296.
[9] D. Ramachandran, A. Oz, V. K. Saraf, G. K. Fedder, and T. Mukherjee, MEMS enabled reconfigurable VCO and RF filter, In IEEE Radio Frequency Integrated Circuits (RFIC) Symposium Digest of Papers 94 (2004), 251-254.
[10] D. B. Leeson, A simple model of feedback oscillator noise spectrum, Proceedings of the IEEE Letters 54 (1996), 329-330.
[11] B. Goldberg, Phase noise theory and measurements: A short review, Microwave Journal (2000), 112-122.
[12] G. Sauvage, Phase noise in oscillators: A mathematical analysis of leeson's model, IEEE Transaction on Instrumentation and Measurement, 26 (1997), 408-410.
[13] T. H. L. Ali Hajimiri, the Design of Low Noise Oscillators, 1999.
[14] R. Dehghani, Design of an Optimized 2.5 GHz CMOS Differential LC Oscillator with Nonlinear Analysis for MOS Varactor, Journal of Analog Integrated Circuits and Signal Processing 45 (2005), 5-25.
[15] J. Craninckx and M. steyaert, A 1.8 GHz low phase noise CMOS VCO using optomized hollow inductors1997, IEEE Journal of Solid State Circuits 32 (1997), 736-745.
[16] S. S. Mohn, M. Hershenson, S. P. Boyd, and T. H. Lee, Simple accurate expressions for planar spiral inductances, IEEE Journal of Solid-State Circuits 34 (1999), 1419-1424.
[17] H. M. Greenhouse, Design of planar rectangular microelectronic inductor, IEEE Transaction of parts, hybrids and packaging PHP-10 (1974), 101-109.
[18] C. P. Yue and S. S. Wong, Physical modeling of spiral inductors on silicon, IEEE Journal of Transaction on Electron Devices 47 (2000), 560-568.
[19] S. M. P Andreani, A 2.4-GHz CMOS Monolithic VCO with an MOS Varactor, Journal of Analog Integrated Circuits and Signal Processing 22 (2000), 17-24.
[20] D. J. Young and B. E. Boser, A micromachine-based RF low-noise voltage- controlled oscillator, In Proceedings IEEE Custom Integrated Circuits Conference (1997), 431-434.
[21] A. Dec and K. Suyama, Microwave MEMS-based voltage-controlled oscillators, IEEE Journal of Transactions on Microwave Theory and Techniques 48 (2000), 1943-1949.
[22] H.-C. Chen, C.-H. Chien, H.-W. Chiu, S.-S. Lu, K.-N. Chang, K.-Y. Chen, and S.-H. Chen, A low-power low-phase-noise LC VCO with MEMS Cu inductors, IEEE Journal of Microwave and Wireless Components Letters 15 (2005), 434-436, 20