

## Design and Simulation of a High Speed CMOS Comparator

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### Abstract

Analog-to-Digital conversion process is an electronic process in which an analog signal is changed, without changing its necessary contents, into a digital signal. Latched comparators use positive feedback mechanism (aids in the input signal) to re-generates (amplifies) the analog input signal into a Full-scale digital level output signal [2]. This paper presents a CMOS comparator that reduces the overall propagation delay and hence provides higher speed. The design is simulated in 0.25 $\mu$ m CMOS Technology using Tanner EDA Tools. CMOS Comparator shows that the overall propagation delay of the comparator, TPD, is 1.7872e-9 seconds, with a 1.0 V supply voltage.

**Keywords:** Comparator, CMOS, Dynamic Latched Comparator.

### Introduction

Cmos fully dynamic latched comparators are majorly used in Analog to Digital converters (ADCs), data receivers and Memory Sense Amplifiers (SAs) because they provide high speed, reduced power consumption, full swing output and high input impedance. Dynamic latched comparators employ re-generative stage, which consist of cross coupled inverters, to provide a positive feedback mechanism. This regenerative stage is used to convert a differential voltage, from the input stage, into a full swing digital output state at a very fast rate [8].

### Literature review and objectives

D. Y. Kim *et. al.* [3] presented “The Design of the High Speed Amplifier Circuit for Using in the Analog Subsystems” a high speed cmos based an amplifier circuit and this amplifier circuit is further used to design a high speed cmos comparator, which is further applied in different analog to digital converters. The designed amplifier and

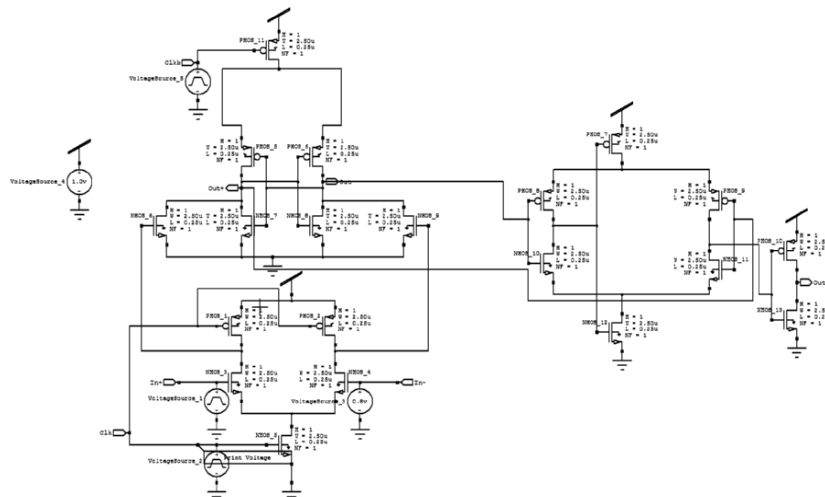
comparator circuit is connected in complementary fashion to provide the gain stage to increase speed.

Daniel Schinkel *et. al.* [6] investigated “A Double-Tail Latch-Type Voltage Sense Amplifier” a latch type voltage sense amplifier that has one tail transistor which limits the total current flowing through the both of the output branches; it shows strong dependency on speed and offset voltage with different common-mode input voltage  $V_{com}$ . To mitigate this drawback, the comparator with separated input-gain stage and output-latch stage was introduced. This separation made this comparator have a lower and more stable offset voltage over wide input common-mode voltage ( $V_{com}$ ) ranges and operate at a lower supply voltage ( $V_{DD}$ ) as well.

Heung Jun Jeon *et. al.* [3] investigated “A CMOS low-power low-offset and high-speed fully dynamic latched comparator” that a novel dynamic latched comparator has lower offset voltage and higher load drivability than the conventional dynamic latched comparators. With two additional inverters inserted between the input- and output-stage of the conventional double-tail dynamic comparator, the gain preceding the regenerative latch stage is improved. The complementary version of the regenerative latch stage, which provides larger output drive current than the conventional one at a limited area, is implemented.

### Existing CMOS Comparator

Figure1 shows the double tail fully dynamic comparator is designed in CMOS Technology using Tanner EDA Tools. It consists of an input stage followed by a regenerative latch stage and an output buffer stage. Comparator utilizes two tail transistors, one transistor is used for input stage and second tail transistor is used for latching or re-generative stage. His comparator can be used for lower operating voltages.



**Figure 2:** Dual Tail fully dynamic CMOS comparator[6].

The double tail comparator offers a large current in the re-generative stage for fast re-generation and enables less current in the input differential stage to reduce offset.

During the reset phase when  $Clk=0$ , nmos transistor NMOS\_5 is off or in cut-off mode, nmos transistors NMOS\_3 and NMOS\_4 are off whereas pmos transistors PMOS\_1 and PMOS\_2 are on, these pmos transistors will charge the drains of PMOS\_1 and PMOS\_2 transistor towards  $V_{DD}$ . And subsequently NMOS\_6 and NMOS\_9 will cause the output nodes out+ and out- to discharge towards ground since  $Clkb=1$  so pmos transistor PMOS\_11 will be in cut-off mode.

During the re-generation phase when  $Clk=V_{DD}$  the tail transistors NMOS\_5 and PMOS\_11 will turn on and the voltages at the drain terminals of PMOS\_1 and PMOS\_2 drops down. Nmos transistors NMOS\_3 and NMOS\_4 are on whereas pmos transistors PMOS\_1 and PMOS\_2 are off. The transistors NMOS\_6 and NMOS\_9 are then used to pass the differential voltage from the input nodes to the re-generating stage. The cross coupled inverters start to re-generate the differential voltage as NMOS\_6 and NMOS\_9 can't clamp the outputs to ground.

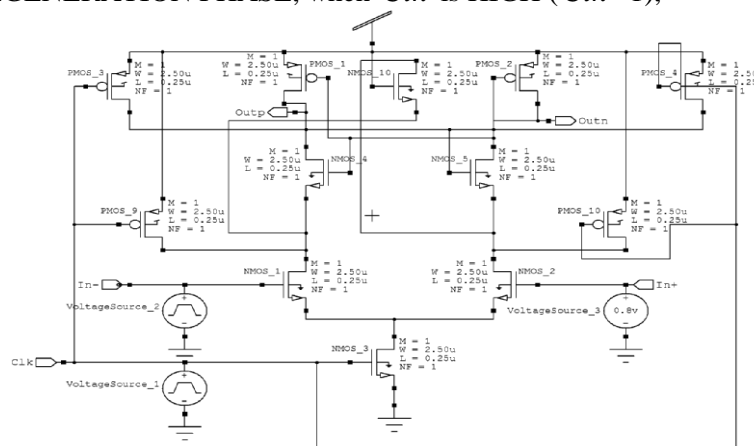
The design is simulated using  $0.25\mu\text{m}$  CMOS Technology using Tanner EDA Tools, with a 1.0 V supply.

### Design Process of this Work

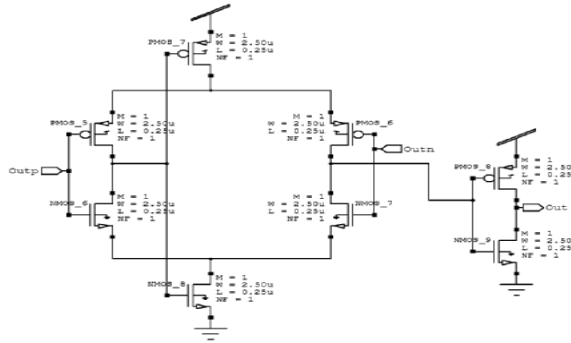
A high speed latched comparator using positive feedback based back to back latch stage, suitable for pipelined Analog to Digital converter, with reduced delay and high speed is proposed

During the RESET PHASE, when  $Clk$  is LOW ( $Clk=0$ ), transistor NMOS\_3 is in off state and pmos transistors PMOS\_3, PMOS\_9, PMOS\_4, PMOS\_10 are in on state. Transistors NMOS\_1 and NMOS\_2 are in cutoff mode. Switch transistors PMOS\_3, PMOS\_9, PMOS\_4, and PMOS\_10 will charge the drains of transistors NMOS\_1 and NMOS\_2 and the output nodes Outp and Outn towards  $V_{DD}$ .

During the REGENERATION PHASE, when  $Clk$  is HIGH ( $Clk=1$ ),



**Figure 3:** High speed CMOS comparator.



**Figure 4:** High speed CMOS comparator Output Stage.

The process starts by turning the transistor NMOS<sub>3</sub> on and immediately an current 'I' starts to flow and the drain of transistor NMOS<sub>3</sub> starts to discharge towards ground (Gnd).

In this succession the differential input transistors NMOS<sub>1</sub> and NMOS<sub>2</sub> are turned on. The currents of transistors NMOS<sub>1</sub> and NMOS<sub>2</sub>, (at the drain terminal) will start to pull the output nodes Outp and Outn towards Gnd. Due to the difference of voltages between the input signals, the current at the drain terminals of transistors NMOS<sub>1</sub> and NMOS<sub>2</sub> will be different.

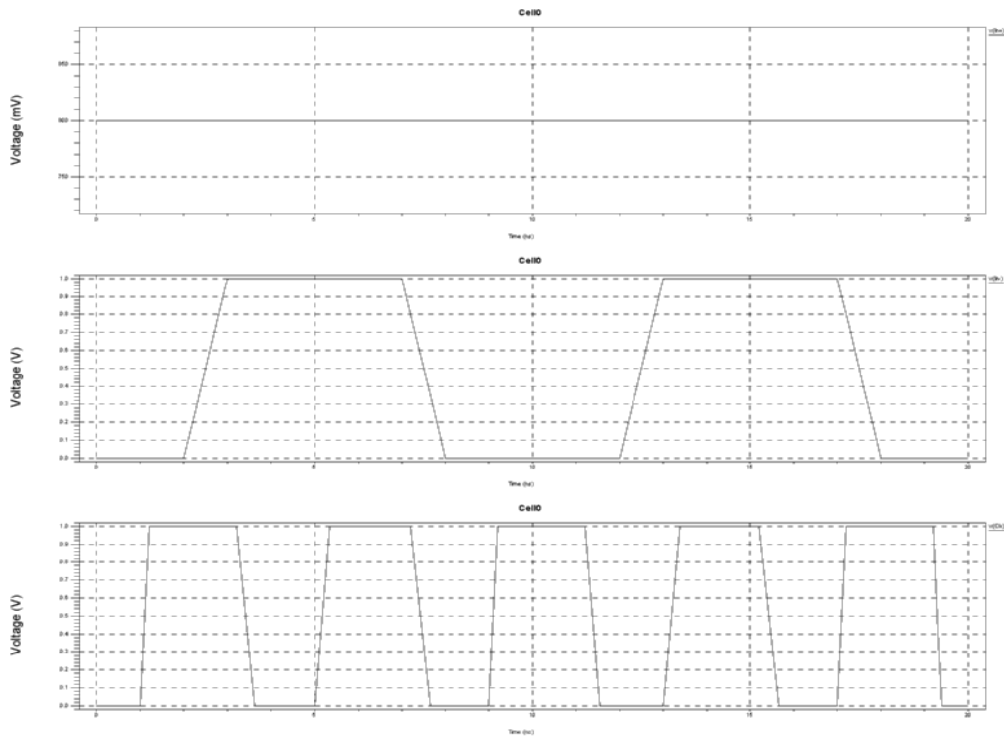
Now in the regeneration mode the output node are discharging towards Gnd and pmos transistors PMOS<sub>1</sub> and PMOS<sub>2</sub> will come in saturation mode as the voltage at output nodes falls below  $V_{DD} - |V_p|$ . So a strong positive feedback will enhance the output signal. This regeneration process is completed when one Nmos transistor comes in cutoff mode.

The design is simulated using 0.25 $\mu$ m CMOS Technology using Tanner EDA Tools. Proposed design exhibits reduced delay and high speed with a 1.0 V supply. This design can be used where high speed and low propagation delay are the main parameters.

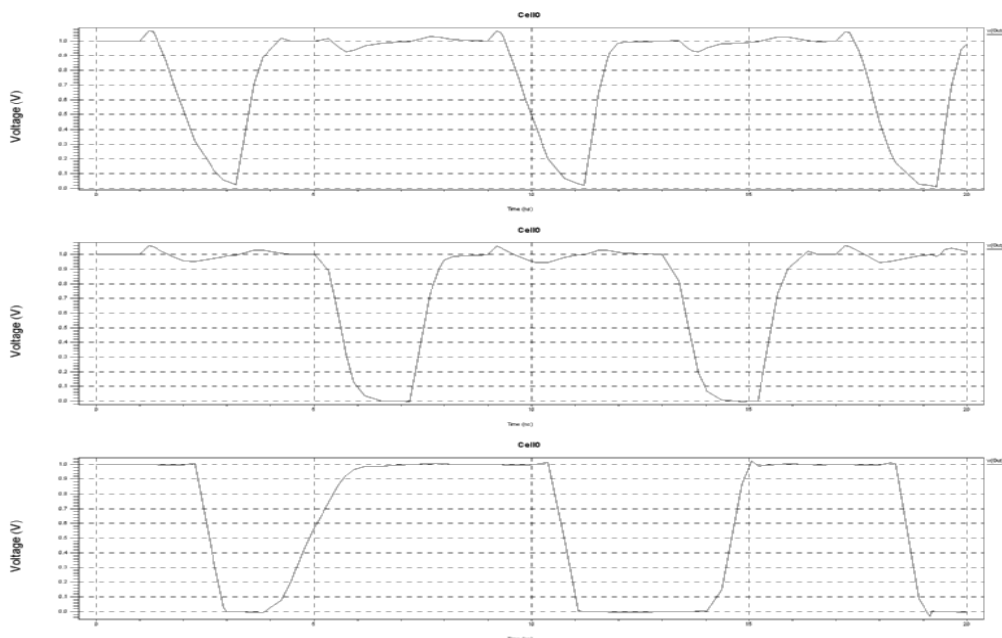
### Simulation

The design is simulated in the design is simulated in 0.25 $\mu$ m CMOS Technology using Tanner EDA Tools. Comparator design shows reduced delay and high speed with a 1.0 V supply.

Finally simulation results of the comparator are given below, when a differential signal is applied as an input to the latched comparator. The simulated results are shown below:



**Figure 5:** Simulation Results (waveform 1 and waveform 2 shows the analog input applied to the comparator, waveform 3 shows the clock signal applied).



**Figure 6:** Simulation Results (waveform 1 shows the output at node Outn, waveform 2 shows the output at node Outp, waveform 3 shows the output at node Out).

## Results and Future Scope

The shorter propagation delay, the higher the speed of the circuit and vice-versa. Delay time is measured at 90% transition of the point. The propagation delay is determined using two basic time intervals, which is T<sub>PHL</sub> and T<sub>PLH</sub>. T<sub>PLH</sub> is the delay time measured when output is changing from logic 0 to logic 1 and T<sub>PHL</sub> is from logic 1 to 0. The overall propagation delay of the above circuit (Fig 3 and Fig 4) comes out to be 1.7872e-009 seconds.

**Table 1:** Results Obtained.

Comparators	Existing Comparator	This Work
Parameters	A	B
Total Propagation Delay	5.954 ns	1.787ns

The Total Propagation Delay of the proposed comparator comes out to be 1.7872ns which is less than delay of Comparator A having a delay of 5.954 ns. So the Proposed Comparator shows reduced delay and hence it will show better speed as compared to the comparators discussed in [4].

In the future one can reduce the input referred latch offset voltage, power consumption, Hysteresis response.

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