SCISPACE
formerly Typeset

Open access • Journal Article • DOI:10.1007/S12633-021-01145-W

Design and Temperature Assessment of Junctionless Nanosheet FET for Nanoscale Applications — Source link

V. Bharath Sreenivasulu, Vadthiya Narendar

Institutions: National Institute of Technology, Warangal

Published on: 18 May 2021 - Silicon (Springer Netherlands)

Topics: Nanosheet and Drain-induced barrier lowering

Related papers:

- Junctionless Gate-All-Around Nanowire FET with Asymmetric Spacer for Continued Scaling
- A Comprehensive Analysis of Junctionless Tri-Gate (TG) FinFET Towards Low-Power and High-Frequency Applications at 5-nm Gate Length
- Parametric Investigation and Design of Junctionless Nanowire Tunnel Field Effect Transistor
- 3-D Simulation of Novel High Performance of Nano-Scale Dual Gate Fin-FET Inserting the High-K Dielectric TiO2 at 5 Nm Technology
- Virtually Doped Schottky Buried Metal Layer Planar Junctionless FET for SCE Suppression at sub-28nm Technology Nodes

Share this paper:

View more about this paper here: https://typeset.io/papers/design-and-temperature-assessment-of-junctionless-nanosheet-47rtzkzew1

Preprints are preliminary reports that have not undergone peer review. They should not be considered conclusive, used to inform clinical practice, or referenced by the media as validated information.

Design and Temperature Assessment of Junctionless Nano-Sheet FET for Nanoscale Applications

Bharath Sreenivasulu Vakkalakula (vbharathsree818@gmail.com)
National Institute of Technology Warangal https://orcid.org/0000-0003-3064-1522
Narendar Vadthiya
National Institute of Technology Warangal

Research Article

Keywords: Nano-sheet, Temperature, analog/RF, High-K Metal Gate, Dynamic Power, Power Consumption

Posted Date: April 12th, 2021

DOI: https://doi.org/10.21203/rs.3.rs-302409/v1

License: This work is licensed under a Creative Commons Attribution 4.0 International License.
Read Full License

Design and Temperature Assessment of Junctionless Nano-Sheet FET for Nanoscale Applications

V. Bharath Sreenivasulu and Vadthiya Narendar

Department of Electronics & Communication Engineering

National Institute of Technology Warangal

E-mail: vbharathsree818@gmail.com and narendarv@nitw.ac.in

Abstract

Nano-sheets are the revolutionary change to overcome the limitations of FinFET. In this paper, the temperature dependence of 10 nm junctionless (JL) nano-sheet FET performance on DC, analog and RF characteristics are investigated for the first time using extended source/drain and with high-*k* gate stack. The detailed DC performance analysis like transfer characteristics (I_D-V_{GS}), output characteristics (I_D- V_{DS}), DIBL, SS and I_{ON}/I_{OFF} ratio are evaluated from 200 K to 350 K. We also analyzed the temperature effect on the ON-OFF performance metric (Q), dynamic power, and power consumption. Furthermore, to understand the device performance on various process parameters like doping, and work function variations are presented at 300 K. The proposed device exhibits good I_{ON}/I_{OFF} switching behaviour with I_{OFF} reaching less than nA for all temperatures. The cut-off frequency (f_t) is determined to be in the THz range and the ON-OFF performance metric (Q) ranges between 1.5 to 2.2 µS-dec/mV at L_G of 10 nm. Furthermore, the scaling effect of nano-sheet at various gate lengths (L_G = 5 nm, 8 nm, 10 nm, 14 nm, and 20 nm) are also presented. From simulation analysis we notice that analog/RF performance parameters of a JL nano-sheet FET are less sensitive to temperature variations. At extremely scaled L_G the nano-sheet FET exhibits lower power consumption and dynamic power and comparatively decreases with increase in temperature. The proposed nano-sheet FET demonstrates as a strong potential contender for low-power and high-frequency applications at nano-regime.

Keywords: Nano-sheet, Temperature, analog/RF, High-K Metal Gate, Dynamic Power, Power Consumption.

1. Introduction

Due to a wide range of applications in electronic fields like military, automobiles, nuclear sector, satellite communications, space, infrared detectors, and terrestrial systems which are highly temperature dependent [1-3]. In most of the aforementioned applications, the basic building blocks are transistors, logic gates, static RAM cells, and operational amplifiers. The miniaturization of the device is the primary driving force for CMOS transistors to reach more density and high performance for IC applications. But on the other side deep scaling invites adverse short channel effects (SCEs) and severe second order effects which are diminishing the technological outreach. In order to counter these SCEs metal oxide semiconductor field effect transistor (MOSFET) with more than one gate is a viable option for future nano transistors.

One such device is FinFET in which short channel effects (SCEs) have been reduced by wrapping the channel from three sides. But in the contrary, the FinFETs are facing several challenges in terms of device performance, layout, patterning, and effective cost to continue scaling [4-6]. Since all pitches are decreasing, taller, thinner, and tighter fin structures are required for optimum performance and process. However, for sub-10 nm technology nodes more robust structure that can control the channel from all directions is highly essential in order to control the channel to avoid SCEs. The gate-all-around structures like GAA nanowire, GAA nanoplate and nano-sheet are the suitable candidates that can replace FinFET at sub-10 nm regime [7]. But the limiting factors of GAA nanowire transistor is lower drive current due to lower effective channel widths.

To continue scaling and to have high performance devices nano-sheet transistors are suggested. Since nano-sheet FET is not limited by fin pitch, fin quantization and have optimum effective width. The nano-sheet also offers a larger channel area by vertically stacking the channels in

the same metal gate area. The stacked nano-sheets get 30% more effective width compared to FinFETs within the same footprint [8,9]. For nano-scale devices it is very difficult to manufacture sharp junctions and have fabrication difficulties. To counter these manufacturing difficulties, Junctionless structures are formed through uniform doping throughout the silicon fin [10-12]. This uniform doping behaves like a resistor whose resistivity can be controlled by gate bias. To enhance the performance of 3D nano-sheet, high-*k* gate stack is used by reducing the oxide thickness. Although the oxide thickness is less the high-*k* dielectric enhances the gate controllability. The metal gate electrode is placed for the gate stack over polysilicon which induces phonon scattering and fermi level pinning [13].

In this paper the simulation of nano-stack FET is carried out by high-*k* gate stack to have good electrostatic gate control and the whole device is isolated with SiO_2 along with spacer to reduce the series resistance effect due to underlap formation. The result analysis of section-II presents DC simulation characteristics of 10-nm nano-sheet FET. The section-III presents the analog/RF performance and power characteristics of JL nano-sheet FET with temperature variation. The section-IV presents the gate length (L_G) variation and process variation effects at 300 K.

2. Device Structure and Simulation Setup

The device structure is generated through cogenda visual TCAD simulator [14]. The 3D and 2D view of nano-sheet FET is depicted in Fig.1(a, c and d). The nano-sheet FET with gate length (L_G) = 10 nm, each fin width (F_W) = 10 nm, and fin height (H_{SN}) = 10 nm (with total fin height (H_{Si}: $3 \times 10 = 30$ nm) is generated. The device with a uniform doping concentration of 1×10^{19} cm^{-3} is maintained to avoid junction formation at nano-regime.

The gate stack with SiO_2 of 0.5 nm and HfO_2 of 1.28 nm to get equivalent oxide thickness (EOT) of 0.75 nm is considered to have good electrostatic integrity [15]. The metal gate work function of 4.8 eV is fixed for all the device simulations in order to have individual threshold

voltages (V_{th}). An optimized spacer distance of 15 nm is maintained between source and drain potential terminals to have good subthreshold behaviour.

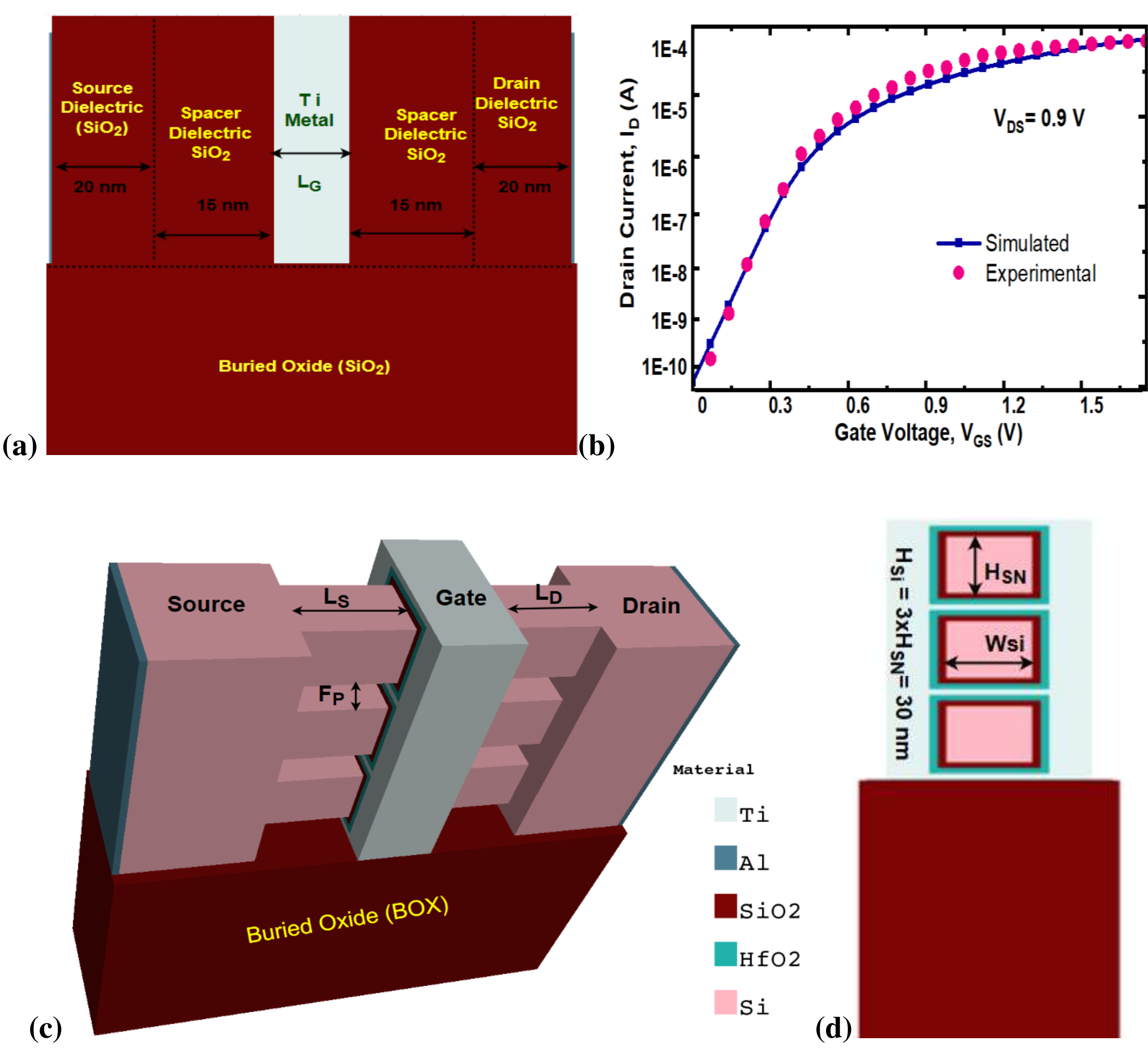


Fig. 1. (a)The 3D schematic view of n-channel SOI nano Sheet with isolation oxide and Spacer dielectric (b) Calibration with experimental data [16] (c) 3D View of SOI FinFET without spacer dielectric and outer isolation oxide (d) 2D cross sectional view of n-channel SOI FinFET.

An increase in series resistance with spacer distance can be reduced by adopting a spacer dielectric which enhances both ON current and reduces drain influence on the channel. Initially

uniform doping concentration of $1\times10^{-19}cm^{-3}$, and L_G are set to10 nm respectively for temperature variations.

The physical models used in the simulation are Fermi Dirac statistics to account for heavily doped JL nano-sheet FET. To account for generation and recombination phenomena SRH recombination model is activated. To account for various scattering phenomena like surface roughness, and acoustic phonons Lombardi mobility model is incorporated. The bandgap narrowing model is involved due to the higher doping of JL nano-sheet FET. The quantum density gradient model for quantum correction effect is also included. The geometrical parameters and materials used for device simulation are depicted in Table I. The TCAD device physics is welly calibrated with experimental results used for demonstration of nano-sheet FET. The threshold voltage (V_{th}) is extracted at 100 nA × (W_{eff}/L_G), where W_{eff} is the effective device width [$W_{eff} = n \times (2 \times H_{SN} + W_{Si})$].

Table I. Parameter Description.

Parameter	**SOI n-FinFET**
Gate Length (L_G) = Fin width (W_{Si}) = Fin height (H_{SN}).	10 nm
Gate oxide thickness (t_{OX}) - SiO_2	0.5 nm
Gate high-*k* dielectric oxide thickness – HfO_2	1.28 nm
EOT (Equivalent Oxide Thickness)	0.75 nm
Spacer dielectric	SiO_2
Source/drain Length (L)	20 nm
Length of source/drain spacer $L_S = L_D$	15 nm
Source/channel/drain doping	1×10^{19}
Gate work function	4.8 eV

III. Simulation Results and Discussion with Temperature Variations.

The device log transfer characteristics of nano-sheet FET with various temperature variations are shown in Fig. 1. With an increase in temperature the leakage current increases i.e., the OFF-state leakage current increases. This increase in OFF current (I_{OFF}) with the rise in temperature is due to diffusion current and SRH recombination's which are dependent factors of temperature. The intrinsic carrier concentration (n_i) is a dependent factor of temperature and the expression for n_i is given as [17].

$$n_i = \exp(-Eg/2kT) \quad (1)$$

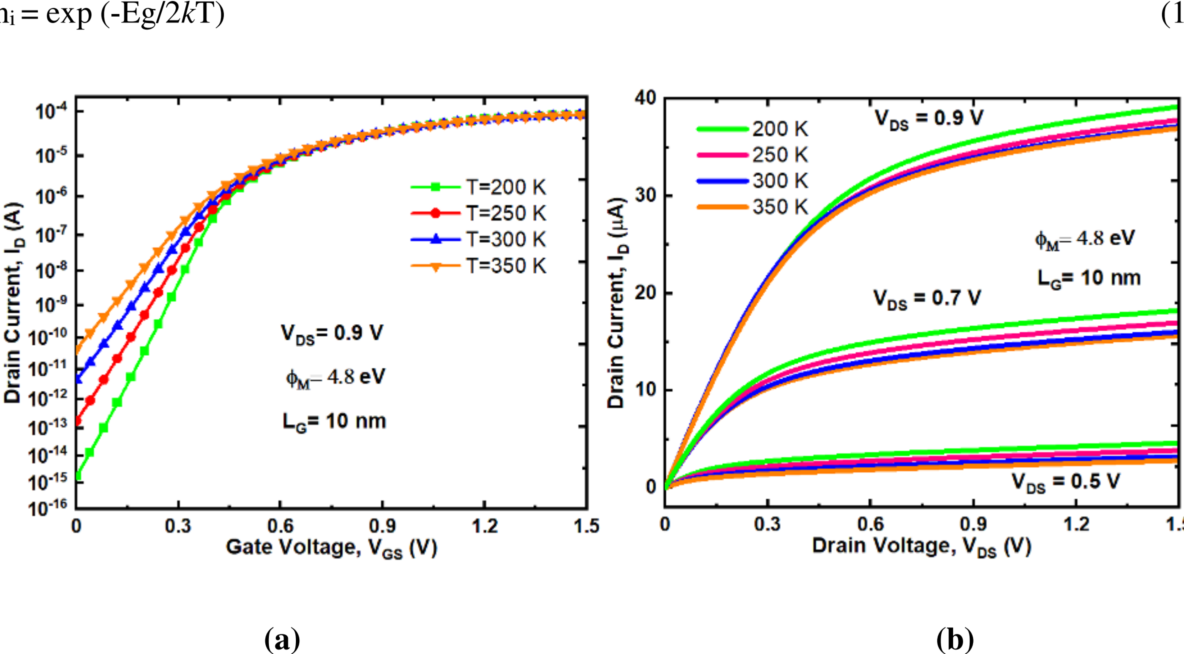


Fig. 2. (a) Transfer (I_D-V_{GS}) (b) Output characteristics of nano-sheet FET with variation of temperature.

Here 'k' is the boltzmann constant and 'T' is the absolute temperature. At V_{GS} = 0.6 V the temperature variation is almost negligible i.e., the temperature coefficient (TC) is zero. The leakage current increases with a rise in temperature due to reduced V_{th}. From Fig. 4b it is noticed that the DIBL effect is more at 350 K and eventually decreases when the device temperature reaches 200 K. As shown in Table. II, the OFF current (I_{OFF}) decreases with a decrease in temperature, and the ON current (I_{ON}) will be in constant comparatively due to flat

band voltage i.e., zero vertical electric field [18]. The I_{ON}/I_{OFF} ratio is higher for 200 K and is least for 350 K. The variation in I_{ON}/I_{OFF} ratio is due to a change in OFF current (I_{OFF}) only.

Fig. 3a shows the potential distribution of JL nano-sheet FET in ON state (V_{GS} = 1.5 V, V_{DS} = 0.9 V). The potential distribution is more towards the drain and is minimal towards the channel and source side which reduces SCEs. Fig. 3b and 3c shows the conduction and valence band energy contour distributions. Both of them have high energy at source and energy falls in the channel and drain sides due to band bending.

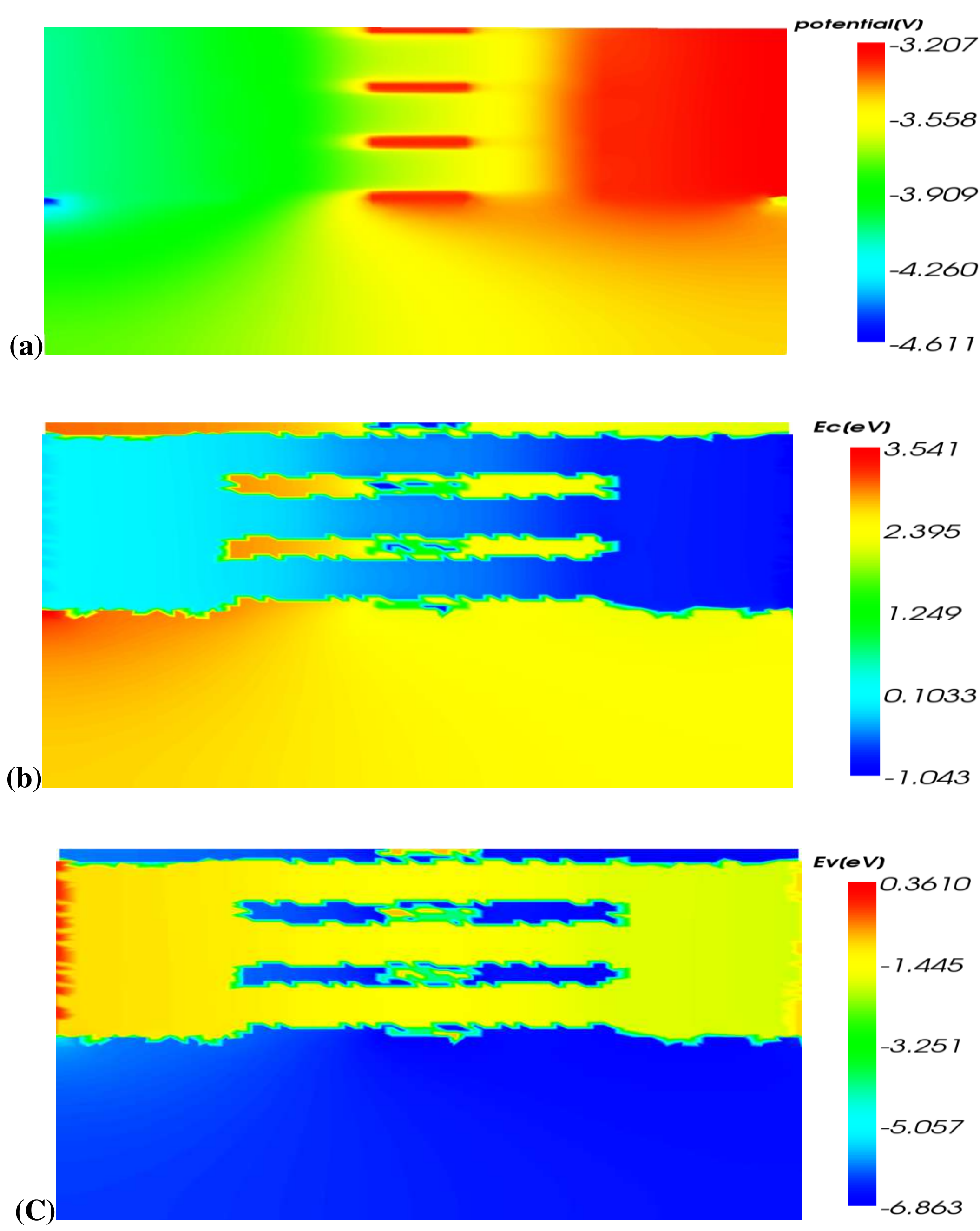


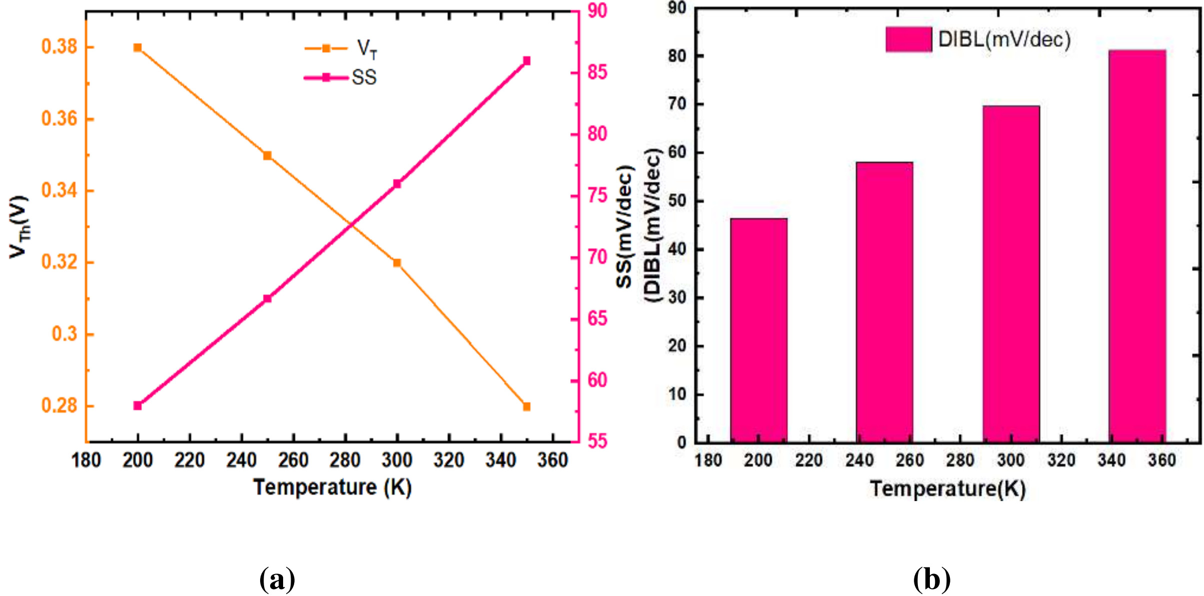
Fig. 3. The (a) Potential distribution (b) Conduction band energy (C) Valence band energy of nano-sheet FET at 300 K with V_{DS}= 0.9 V and V_{GS} = 1.5 V i.e., ON state.

The drain induced barrier lowering (DIBL) and subthreshold swing (SS) evaluates the device efficiency towards subthreshold performance. The threshold voltage is extracted at 100 nA × W_{eff}/L_{eff}, where W_{eff} is the effective width and L_{eff} is the effective gate length. The DIBL and SS are given by the following expressions [19, 20].

$$\text{DIBL (mV/V)} = \left|\frac{(V_{th1}-V_{th2})}{(V_{DS1}-V_{DS2})}\right| \quad (2)$$

$$\text{SS (mV/dec)} = \left[\frac{\partial \log_{10}(I_D)}{\partial V_{GS}}\right]^{-1} \quad (3)$$

where V_{th1} and V_{DS1} is the voltage taken at supply voltage of 0.04 V and V_{th2} and V_{DS2} is the voltage taken at supply voltage of 0.9 V.



(a) (b)

Fig. 4. The nano-sheet FET subthreshold characteristics (a) Threshold voltage (V_{th}) and subthreshold swing (*SS*) (b) Drain induced barrier lowering (DIBL) with variation of temperature.

From Fig. 4a. reduction in threshold voltage (V_{th}) leads to the increment of subthreshold swing (SS). With an increase in temperature the drain current increases due to decrease of V_{th} with the rise in temperature. The SS value increases with a rise in temperature.

Table II. Electrical characteristics of nano-sheet FET.

Temperature in K	**V_{th}@ 0.9 V**	**V_{th}@ 0.04V**	**DIBL**	***SS* (mV/dec)**	**I_{ON}(A)**	**I_{OFF}(A)**	**I_{ON}/I_{OFF} Ratio**
200	0.39	0.43	46.5	48	8.65 x10^{-5}	1.78 x10^{-15}	4.85x10^{10}
250	0.35	0.41	58.13	66.7	8.51 x10^{-5}	1.81 x10^{-13}	4.70×10^{8}
300	0.31	0.37	69.76	76	8.54 x10^{-5}	4.38 x10^{-12}	1.94×10^{7}
350	0.28	0.35	81.39	86	8.64 x10^{-5}	4.6 x10^{-11}	1.87×10^{6}

3. Analog and RF performance metrics.

The g_m is an important parameter for building operational amplifiers and transconductance amplifiers. The g_m also specifies bandwidth, DC gain of an amplifier, noise performance and offset. To evaluate g_m the mathematical expression can be given as $g_m = \partial I_D/\partial V_{GS}$. The g_m value increases with decrease in temperature due to a rise in drive current (I_D). The improvement in g_m is observed in the weak moderate inversion region and it falls at higher gate bias due to mobility reduction. Fig. 5a depicts the temperature variation of g_m with respect to gate bias. The g_m shows significant rise in weak-moderate inversion region, and at high V_{GS} the g_m falls due to mobility degradation. The g_m reaches to highest peak to 115 µS at temperature of 200 K and with increase in temperature g_m decreases due to downfall in drain current. The g_m shows negligible increment with effect to temperature for JL nano-sheet FET at L_G = 10 nm.

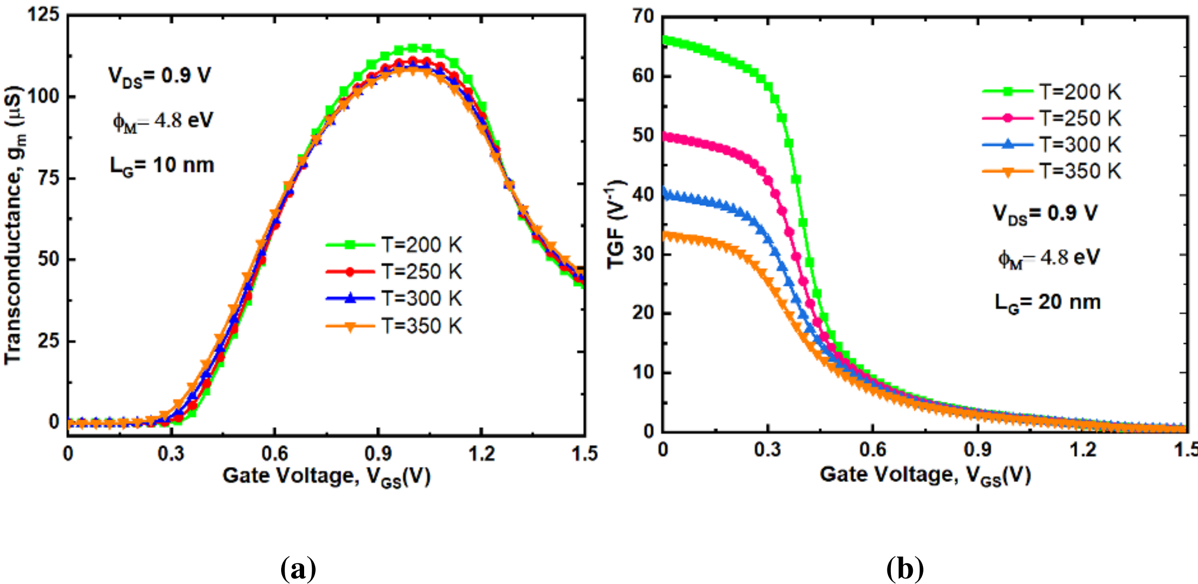


Fig. 5. The analog characteristics of nano-sheet FET(a) Transconductance (g_m) (b) Transconductance generation Factor (TGF) with variation of temperature.

The transconductance generation factor (TGF) is the property of a device that converts DC power into AC frequency. Higher the g_m for a device more will be the TGF, higher TGF for device indicates better analog performance. The mathematical expression for TGF can be given as TGF = g_m/I_D. The TGF value will be higher with a decrease in temperature and its value decreases with a raise in temperature. Since the reduction in I_D is more significant in the weak-moderate inversion region than increase in g_m with temperature, leading to an increase in the g_m/I_D ratio. Moreover, there is a negligible impact of TGF, as anticipated at higher V_{GS} with temperature.

The early voltage V_{EA} ($\approx \frac{I_D}{g_d}$) is another important parameter for analog performance evaluation. Higher V_{EA} ensures higher output resistance. From Fig. 6a, at moderate gate bias V_{EA} is comparatively higher at T = 200 K. The device achieves V_{EA} of ~9 V for all temperatures and ensures good analog perspective. From results it is noticed that JL nano-sheet FET exhibits marginal increment in V_{EA} for temperature variations due to marginal variation in g_d.

The output conductance (g_d) is an important figure of merit to calculate the intrinsic gain of a device. The output conductance is represented as (g_d) and expressed as $g_d = \partial I_D / \partial V_{DS}$.

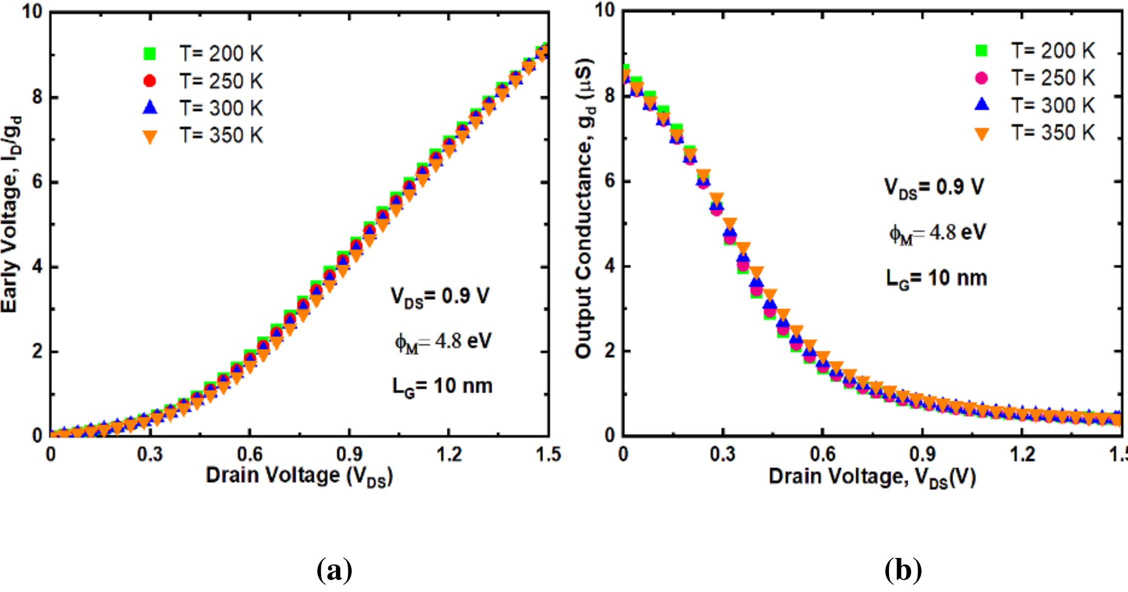


Fig. 6. The output characteristics of nano-sheet FET (a) Early voltage (V_{EA}) (b) Output conductance (g_d) with variation of temperature.

The output conductance variation with respect to temperature is depicted in Fig.6b and noticed that increase in temperature, g_d decreases and leads to a reduction of output resistance which ensures the better driving capability of the devices. Both the early voltage and output conductance have minimal impact with respect to temperature variation.

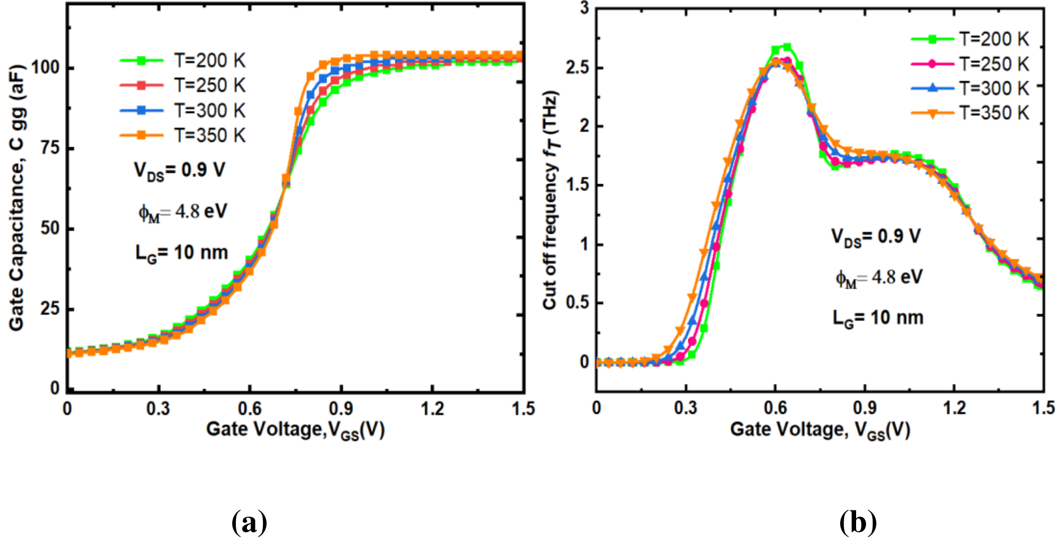


Fig. 7. The nano-sheet FET characteristics (a) Gate capacitance (Cgs) (b) Cut-off frequency (f_t) with variation of temperature.

The total gate capacitance (C_{gg}) is the capacitance combination between source and drain terminals i.e., Cgg = Cgs+Cgd. The total capacitance is an important metric to evaluate the parameters like cutoff frequency (f_t) and delay (τ). The response of total gate capacitance (C_{gg}) for various temperature range with gate bais variation is depicted in Fig. 7a. From results it is noticed that raise in temperature the (C_{gg}) values increases due to reduction in energy bandgap lowers the energy barrier which simultaneously increases the charge carriers in the channel. Since the increase of charge carriers in channel results in an increase of charge carriers under the gate region which increases gate capacitance [21].

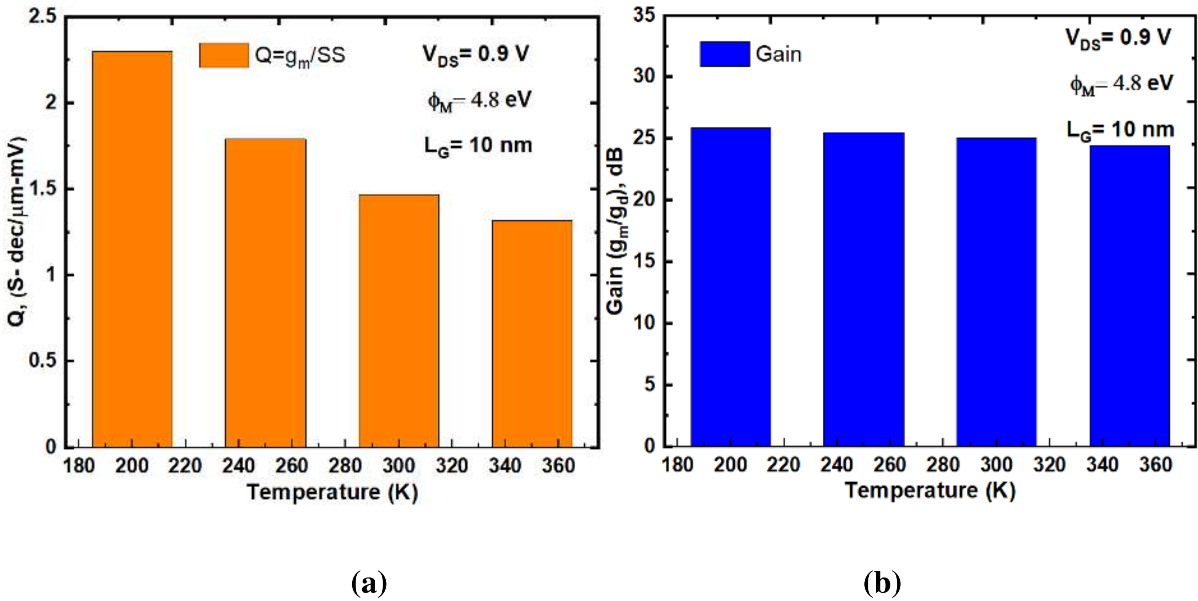
The cutoff frequency ($f_t = g_m/2\pi(C_{gs}+C_{gd})$) is the frequency at which the current gain is 1 and it indicates its high frequency operation capability to obtain optimum gain [20]. The f_t value increases with decreases in temperature i.e., lower at T = 350 K and its value is higher at T = 200 K. The marginal increment of f_t as a function of temperature is due to marginal variation in g_m and Cgg.

Table III. Analog characteristics of nano-sheet FET.

Temperature in K	**TGF**	g_m **(μS)**	g_d **(μS)**	V_{EA}	C_{gg} **(aF)**	f_t **(THz)**
200	66.25	115.08	8.6	9.14	96.5	2.68
250	49.98	111.13	8.43	9.15	98.4	2.54
300	40.70	109.39	8.4	9.11	99.5	2.53
350	33.24	108.44	8.4	9.11	102	2.51

The ON-OFF performance metric ‘Q’ evaluates the device switching capacity and measures the qualitative behaviour of a device. The expression for ‘Q’ is defined as Q = g_m/SS [23] and is detrimental in evaluation of device performance for mixed-signal applications. The ‘Q’ value is higher with lower temperature i.e., its value is higher at 200 K and lower at 350 K.

The gain of a device evaluates the overall performance of a device. The expression of gain is given as $A_V = g_m/g_d$. The A_v is higher with 200 K and comparatively lower with 350 K due to g_m.



(a) **(b)**

Fig. 8. The nano-sheet FET characteristics (a)The ON-OFF performance characteristics (Q) (b) Gain (A_V) with variation of temperature.

The dynamic power and power consumption at V_{DD} = 0.7 V of 10 nm SOI nano-sheet FET is shown in Fig.9. The expression for dynamic power (DP) is given as $\left(C_{OX}V_{DD}^2\right)$ and the power consumption (PC) is given as $\left(\frac{1}{2}C_{OX}V_{DD}^2\right)$ per W at V_{DD} of 0.9 V [24]. Here C_{OX} is the intrinsic capacitance i.e., without any parasites. Both DP and PC decrease with an increase in temperature at L_G =10 nm. Both DP and PC are essential to estimate the device flexibility for low power and high-performance applications.

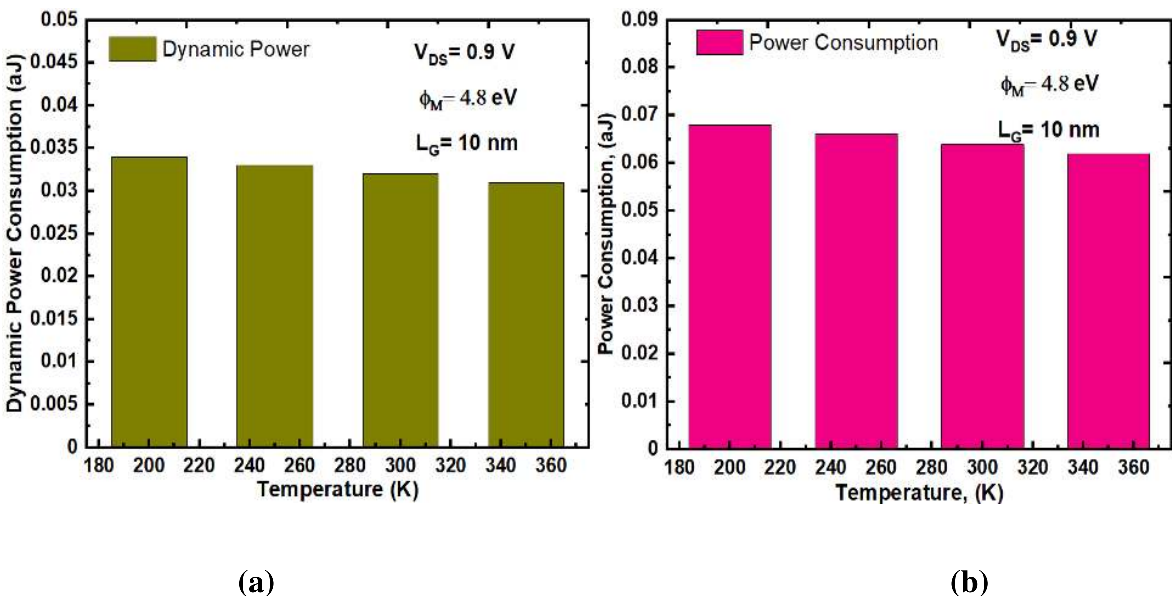


Fig. 9. The nano-sheet FET characteristics (a)The dynamic power characteristics (DP) (b) Power consumption (PC) with variation of temperature.

4. Impact of Various Parameter Variations:

4.1 Impact of Doping and Work function.

From Fig. 10a, depicts the doping variations of nano-sheet FET at fixed work function of 4.8 eV, V_{GS} = 1.5 V, and V_{DS} = 0.7 V respectively. Lower doping concentration exhibits lower leakages but with a decrease of I_{ON}, higher doping shows moderate I_{OFF} but with enhanced I_{ON}.

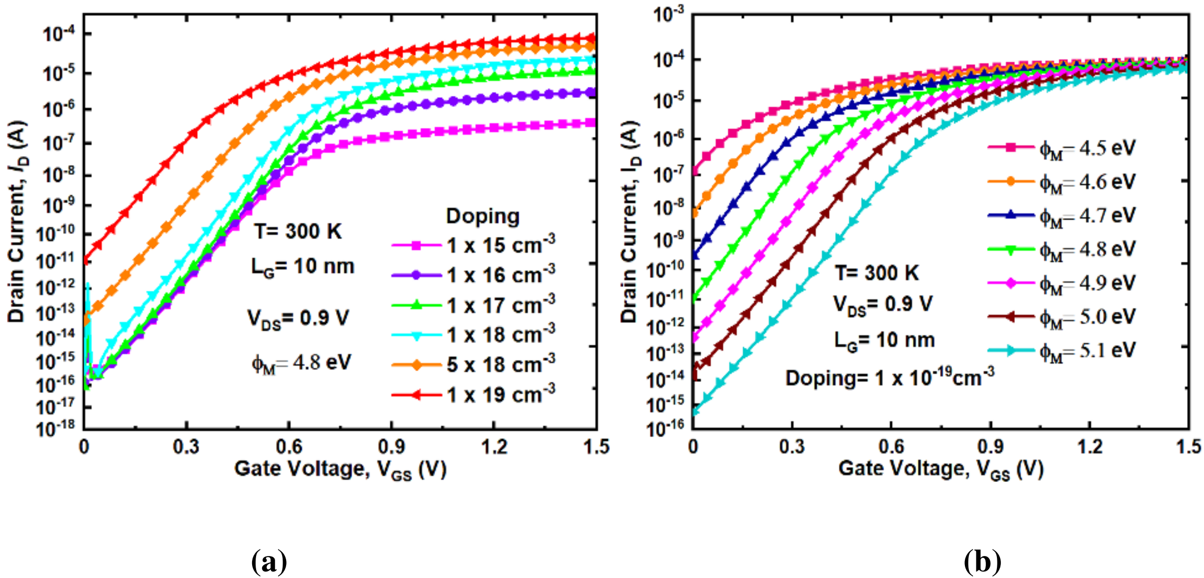
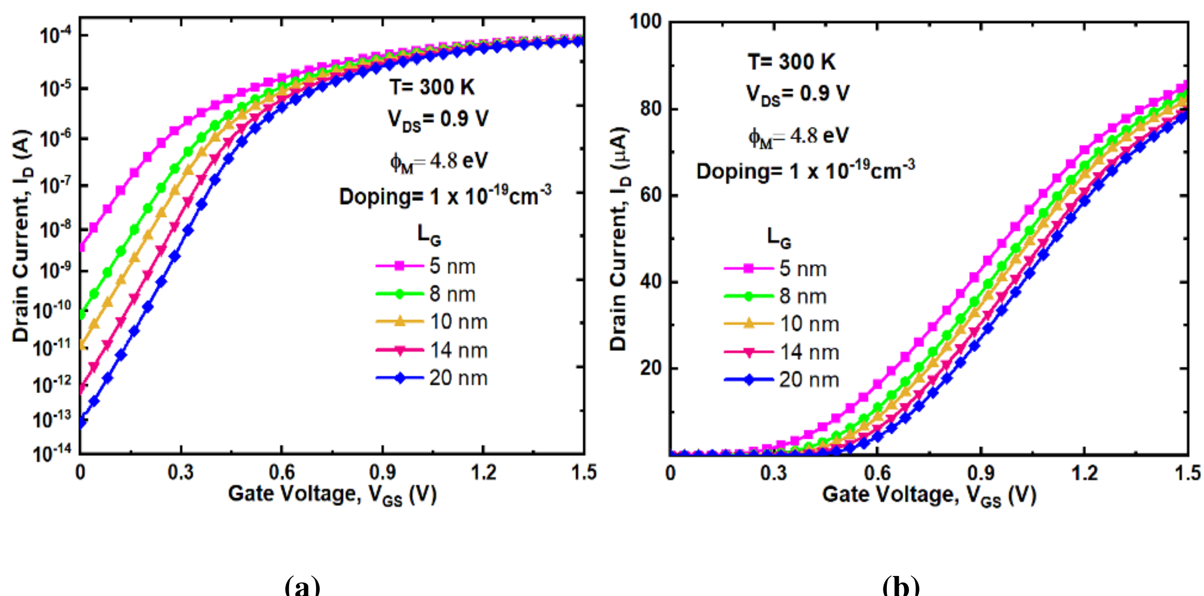


Fig. 10. The nano-Sheet FET characteristics (a)The Doping Characteristics (b) Work Function (WF) variation with variation of temperature.

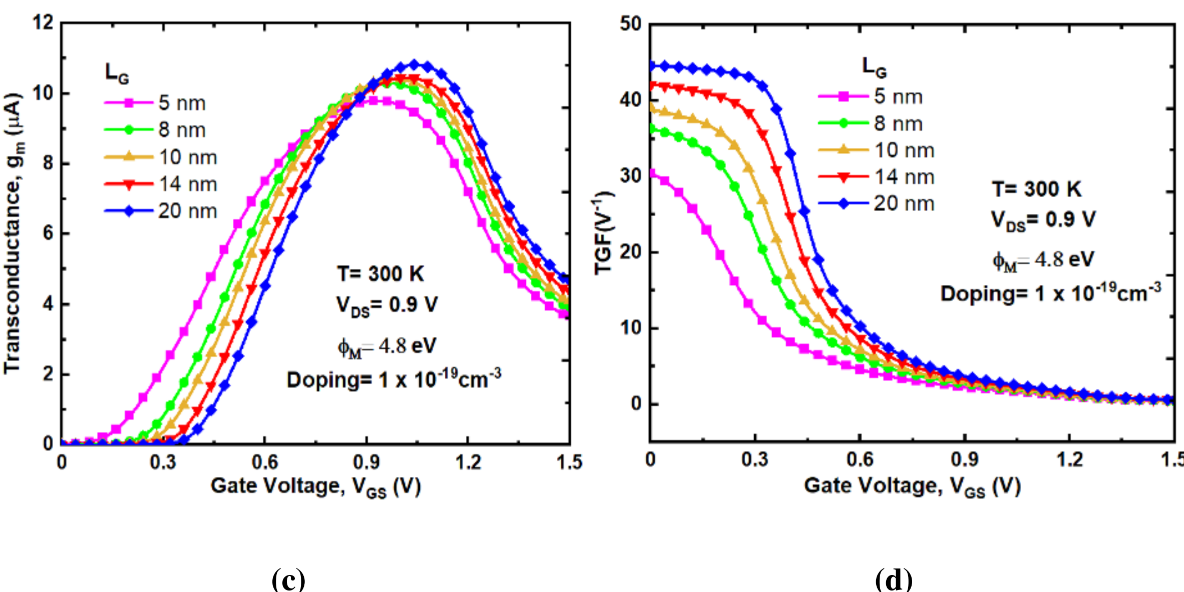
With an increase in doping both I_{ON} and I_{OFF} increases. At doping concentration of 1×10^{-19} cm^{-3} the device achieves the highest I_{ON} and lower threshold voltage (V_{th}) and at 1×10^{-15} cm^{-3} the device achieves lower I_{OFF}. The work function (WF) variation of nano-sheet FET is depicted in Fig. 10.b and noticed that increase in WF device leakage decreases and threshold voltage increases. The work function range between 4.7 eV to 4.8 eV ensures moderate ON-OFF characteristics at 10 nm L_G.

4.2 Impact of Gate Length Variation.

The investigation of scaling leverage on nano-sheet FET from 20 nm down to 5 nm respectively is carried for evaluation of different short channel characteristics like threshold voltage (V_{th}), DIBL, SS. The Fig. 11. a, shows the transfer characteristics of nano-sheet FET with various gate lengths (L_G) at V_{GS} = 1.5 V and V_{DS} = 0.9 V. Scaling (L_G) increase leakages due to a shortage of gate control. The high leakages are dominant in nano-regime and occupy a significant portion of power dissipation due to reduction of the power of gate through the channel.



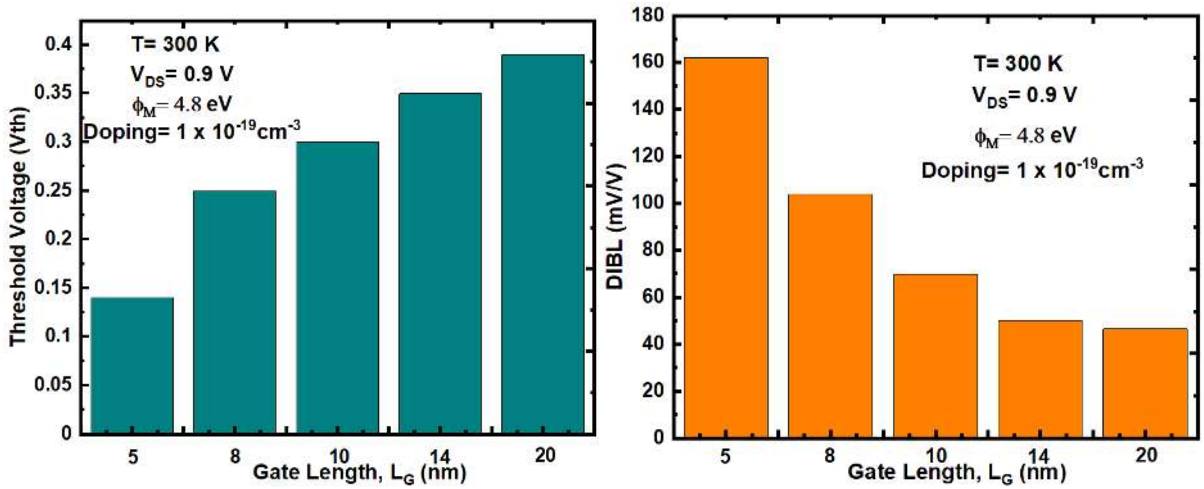
(a) **(b)**



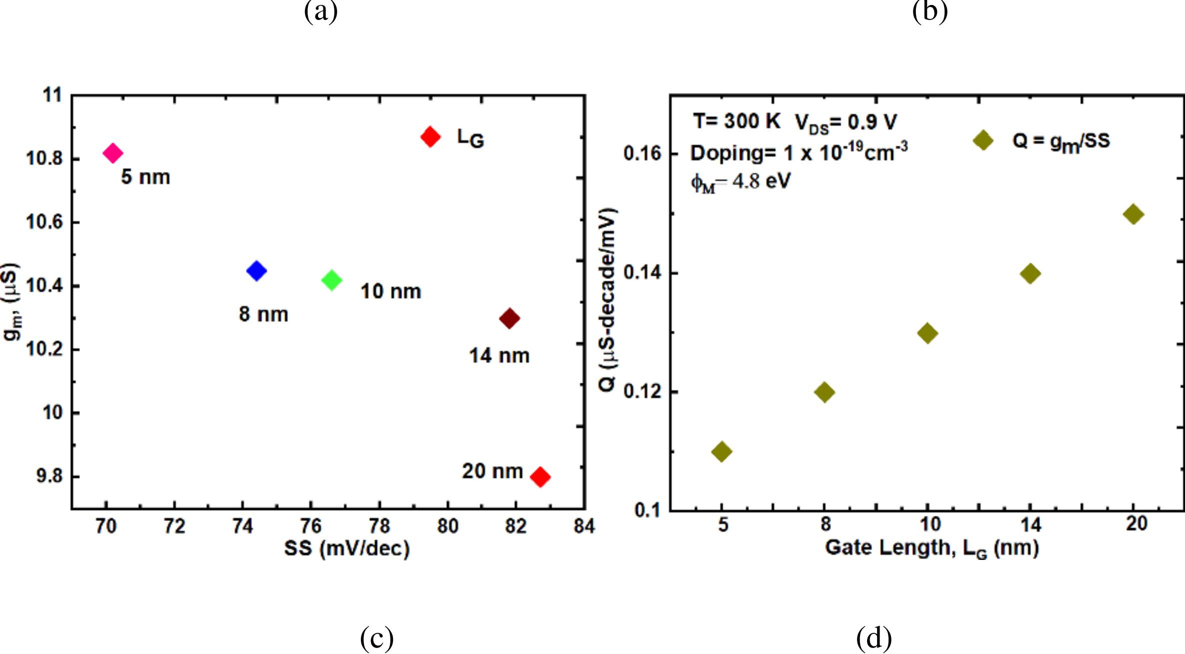
(c) (d)

Fig. 11. The nano-sheet FET characteristics (a) Gate length (L_G) scaling in log scale (b) (b) Gate length (L_G) scaling in linear scale (c) Transconductance variation (g_m) (d) Transconductance generation factor (TGF) variation with gate length (L_G).

The device shows decent performance in all gate lengths with I_{ON}/I_{OFF} ratio higher than 10^6 except at 5 nm L_G. Both TGF and g_m shows significant increment with L_G scaling, the TGF and g_m are the highest for 20 nm and significantly decreases with L_G scaling due to reduction of gate control over the channel. The DC characteristics like g_m,TGF and SS are depicted in Table IV.



(a) (b)



(c) (d)

Fig. 12. The nano-sheet FET characteristics (a) Threshold voltage (V_{th}) roll-off (b) DIBL (c) g_m and SS and (d) ON-OFF performance metric (Q).

The short channel performance estimation of nano-sheet FET is examined in Fig. 12. a and b. The threshold voltage decreases with L_G scaling. With increase in L_G the short channel effects gets minimised and exhibits better performance due to better gate control and improved gate electrostatics. From the result analysis it is inferred that the device achieves better V_{th} with greater than 100 mV for all L_G except at 5 nm. From Fig.12b, it is observed that DIBL increases with L_G scaling due to reduced gate control over channel.

The device exhibits moderate DIBL up to 10 nm L_G, but below 10 nm L_G the higher DIBL is noticed due to diminished gate control over the channel. The variation of g_m as a function of SS is depicted in Fig. 12.c, lower SS has higher g_m and reduction of g_m the SS value diminishes. The variation of Q with L_G is depicted in Fig. 12.d and noted that Q value significantly decreases due to reduction of SS wit L_G scaling.

Table IV. Nano-Sheet FET simulation results for different gate lengths at 300 K.

L_G (nm) Parameters at 300 K	**5**	**8**	**10**	**14**	**20**
Vth (V)	0.14	0.25	0.3	0.35	0.39
SS (mV/dec)	82.7	81.8	76.6	74.4	70.2
DIBL (mV/V)	162	104	69.76	50	46.5
I_{ON}/I_{OFF}	2.2×10^4	1×10^6	1.9×10^7	9.7×10^7	9.4×10^8
Transconductance, g_m (µm)	9.8	10.3	10.42	10.45	10.82
TGF (V^{-1})	30.49	36.38	39.11	42.08	44.62

Conclusion

The temperature simulation of analog/RF and power consumption analysis is performed on JL SOI nano-sheet FET. The results analysis reveals that analog/RF parameters like transconductance (g_m), TGF, gate capacitance (C_{gg}), and cut-off frequency (f_t) degrade with rise in temperature. The temperature dependence of analog/RF parameters of JL SOI nano-sheet FET is minimal. The dynamic power (DP) and power consumption (PC) decrease with rise in temperature. The switching performance metric (Q) and gain (A_v) decrease with increase in temperature. The nano-sheet FET not only ensures optimum realization of digital logic but also analog/RF metrics with THz operational band frequency regime and ensures further scaling. The reduction of DP and PC ensures device driving capability for low power and high frequency applications at nano-regime.

Author Contributions

V. Bharath Sreenivasulu: Writing- Original draft preparation, Formal Analysis, Investigation, Simulation, Data Curation.

V. Narendar: Conceptualization, Methodology, Supervision.

Financial interests: The authors declare they have no Financial interests.

Funding: No Funding Received.

Conflict of Interest: The author has no conflicts of interest to declare that are relevant to the content of this article.

Compliance with Ethical Standards:

- The contents of this manuscript are not now under consideration for publication elsewhere;
- The contents of this manuscript have not been copyrighted or published previously
- The contents of this manuscript will not be copyrighted, submitted, or published elsewhere, while acceptance by the Journal is under consideration.

Availability of data and material: Not applicable.

Consent to Participate: Not applicable.

Consent for Publication: Not applicable.

Acknowledgements: The authors thank to the department of Electronics and Communications Engineering, NIT Warangal for providing the TCAD Tools.

Declaration of interests

☑ The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

☐ The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

N.A.

V. Bharath Sreenivasulu

Dr. Vadthiya Narendar

References

[1] E. A. Gutierrez, M. J. Dean, and C. Claeys, Low Temperature Electronics: Physics, Devices, Circuits and Applications. New York, NY, USA: Academic, 2001.

[2] R. L. Patterson, J. E. Dickman, A. Hammoud, and S. Gerber, Electronic components and circuits for extreme temperature environments. Proc. IEEE Aerosp. Conf. **6**, 6_2543–6_2548 (2003).

[3] M. Elbuluk, A. Hammoud, and R. Patterson, Power electronic components, circuits and systems for deep space missions. Proc. IEEE 36th Power Electron. Specialists Conf., Jun. pp. 1156–1162 (2005).

[4] Srivastava, N.A., Priya, A. & Mishra, R.A. Design and analysis of nano-scale SOI MOSFET-based ring oscillator circuit for high density ICs. Appl.phys. A **125**, 533 (2019).

[5] R. Divakaruni and V. Narayanan, Challenges of 10 nm and 7 nm CMOS for server and mobile applications. ECS Trans. **72**, 3–14(2016).

[6] M. G. Bardonet al., Dimensioning for power and performance under 10 nm: The limits of FinFETs scaling. Proc. ICICDT. pp. 1–4(2015).

[7] N. Thoti and Y. Li, Influence of Fringing-Field on DC/AC Characteristics of $Si_{1-x}Ge_x$ Based Multi-Channel Tunnel FETs. IEEE Access. **8**, 208658-208668 (2020). doi: 10.1109/ACCESS.2020.3037929.

[8] N. Loubet et al., Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET. Symposium on VLSI Technology, Kyoto, pp. T230-T231(2017). doi: 10.23919/VLSIT.2017.7998183.

[9] Y. Lin et al., Performance of Junctionless and Inversion-Mode Thin-Film Transistors With Stacked Nanosheet Channels. IEEE Transactions on Nanotechnology. **19**, 84-88 (2020). doi: 10.1109/TNANO.2019.2960836.

[10] Kumar, R., Kumar, A. “Hafnium based high-k dielctric gate-stacked (GS) gate material engineered (GME) junctionless nanotube MOSFET for digital applications. Appl. phys. A **127**, 26 (2021).

[11] Bharath Sreenivasulu V. and Narendar V “Design and Insights into Sub-10 nm Spacer Engineered Junctionless FinFET for Nanoscale Applications.” ECS J. Solid State Sci. Technolo. **10**, 013008 (2021).

[12] Sreenivasulu, V.B., Narendar, V. A Comprehensive Analysis of Junctionless Tri-gate (TG) FinFET Towards Low-power and High-frequency Applications at 5-nm Gate Length. Silicon (2021). https://doi.org/10.1007/s12633-021-00987-8.

[13] Bha, J.K.K., Priya, P.A., Joseph, H.B.et al. 10 nm TriGate High k Underlap FinFETs: Scaling Effects and Analog performance. Silicon **12**, 2111-2119 (2020).

[14] Genius, 3-D Device Simulator, Version1.9.0, Reference Manual, Cogenda, Singapore, 2008.

[15] Samal, A., Pradhan, K.P.& Mohapatra, S.K. Improvising the Switching Ratio through Low-k/High-k Spacer and Dielectric Gate Stack in 3D FinFET- a Simulation perspective Silicon (2020).

[16] V. Jegadheesan, K. Sivasankaran, Aniruddha Konar, Improved statistical variability and delay performance with junctionless inserted oxide FinFET, AEU – International Journal of Electronics and Communications.**115**, 153030 (2020).

[17] Datta, E., Chattopadhyay, A.& Mallik, A. Relative Study of Analog Performance, Linearity, and Harmonic Distortion Between Junctionless and Conventional SOI FinFET at Elevated Temperatures. Journal of Elec Materi **49**, 3309-3316 (2020).

[18] Baruah, R.K., Paily, R.P. The Effect of high-k gate dielectrics on device and circuit performance of a junctionless transistor. J Comput Electron **14**, 492-499 (2015).

[19] Narendar, V., Narware, P., Bheemudu, V.et al. Investigation of short Channel Effects (SCEs) and Analog/RF Figure of Merits (FOMs) of Dual-Material Bottom-Spacer Ground-Plane (DMBSGP) FinFET. Silicon **12**, 2283-2291 (2020).

[20] S. K. Mohapatra, K. P. Pradhan, D. Singh and P. K. Sahu. The Role of Geometry Parameters and Fin Aspect Ratio of Sub-20nm SOI-FinFET: An Analysis Towards Analog and RF Circuit Design. IEEE Transactions on Nanotechnology. **14**, 546-554 (2015). doi: 10.1109/TNANO.2015.2415555.

[21] Saha, R., Bhowmick, B.&Baishya, S. Temperature effect on RF/Analog and linearity parameters in DMG FinFET. Appl.Phys A **124**, 642 (2018).

[22] Narendar Vadthiya, pallavi Narware, V. Bheemudu, bhukya Sunitha, Anovel bottom-spacer ground-plane (BSGP) FinFET for improved logic and analog/RF performance,AEU- International Journal of Electronics and Communications, **127** 153459 (2020).

[23] N. Chowdhury, G. Iannaccone, G. Fiori, D. A. Antoniadis and T. Palacios, GaN Nanowire n-MOSFET With 5 nm Channel Length for Applications in Digital Electronics. IEEE Electron Device Letters. **38**, 859-862(2017). doi: 10.1109/LED.2017.2703953.

[24] E. Yu, K. Heo and S. Cho, Characterization and Optimization of Inverted-T FinFET Under Nanoscale Dimensions. IEEE Transactions on Electron Devices. **65**, 3521-3527 (2018).doi: 10.1109/TED.2018.2846478.

Figures

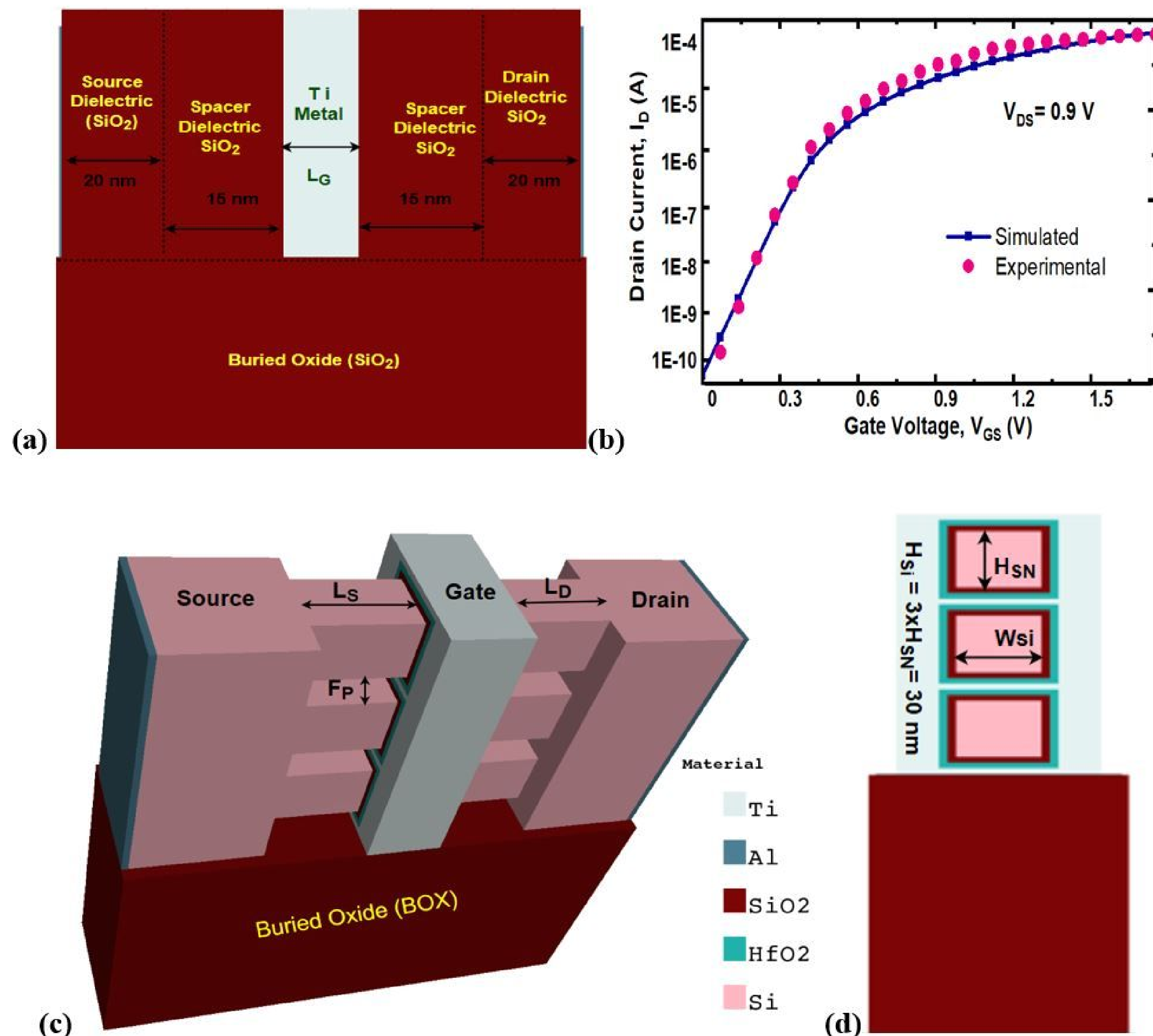


Figure 1

(a)The 3D schematic view of n-channel SOI nano Sheet with isolation oxide and Spacer dielectric (b) Calibration with experimental data [16] (c) 3D View of SOI FinFET without spacer dielectric and outer isolation oxide (d) 2D cross sectional view of n-channel SOI FinFET.

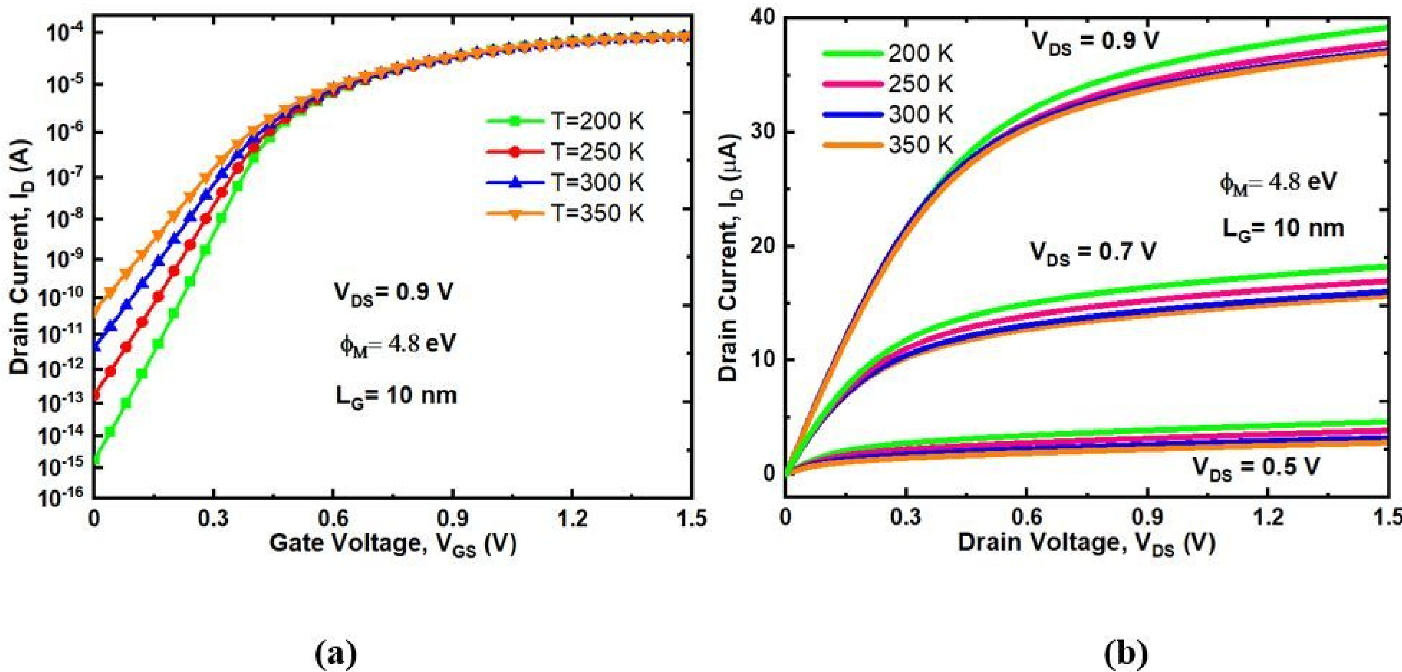


Figure 2

(a) Transfer (ID-VGS) (b) Output characteristics of nano-sheet FET with variation of temperature.

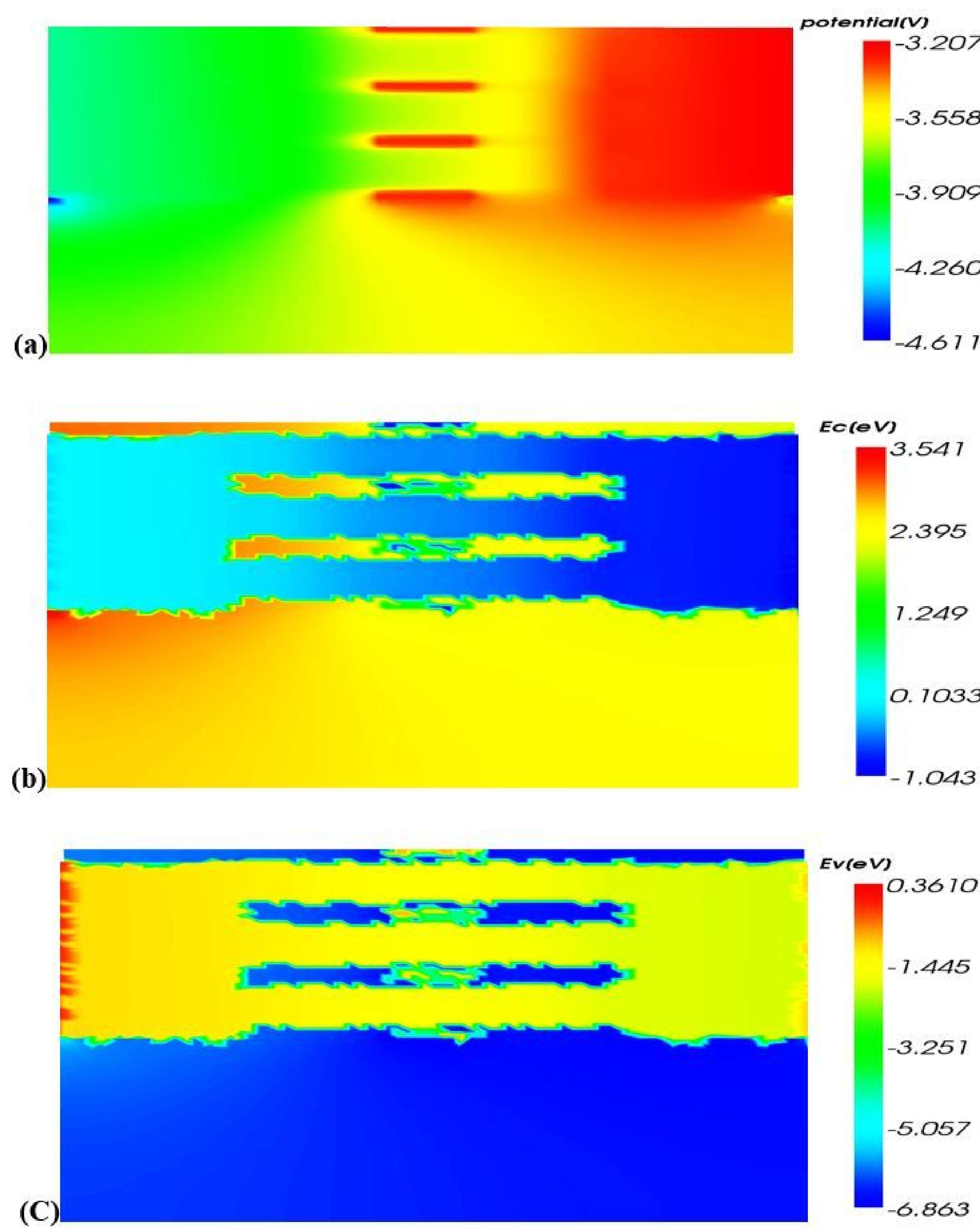


Figure 3

The (a) Potential distribution (b) Conduction band energy (C) Valence band energy of nano-sheet FET at 300 K with VDS= 0.9 V and VGS = 1.5 V i.e., ON state.

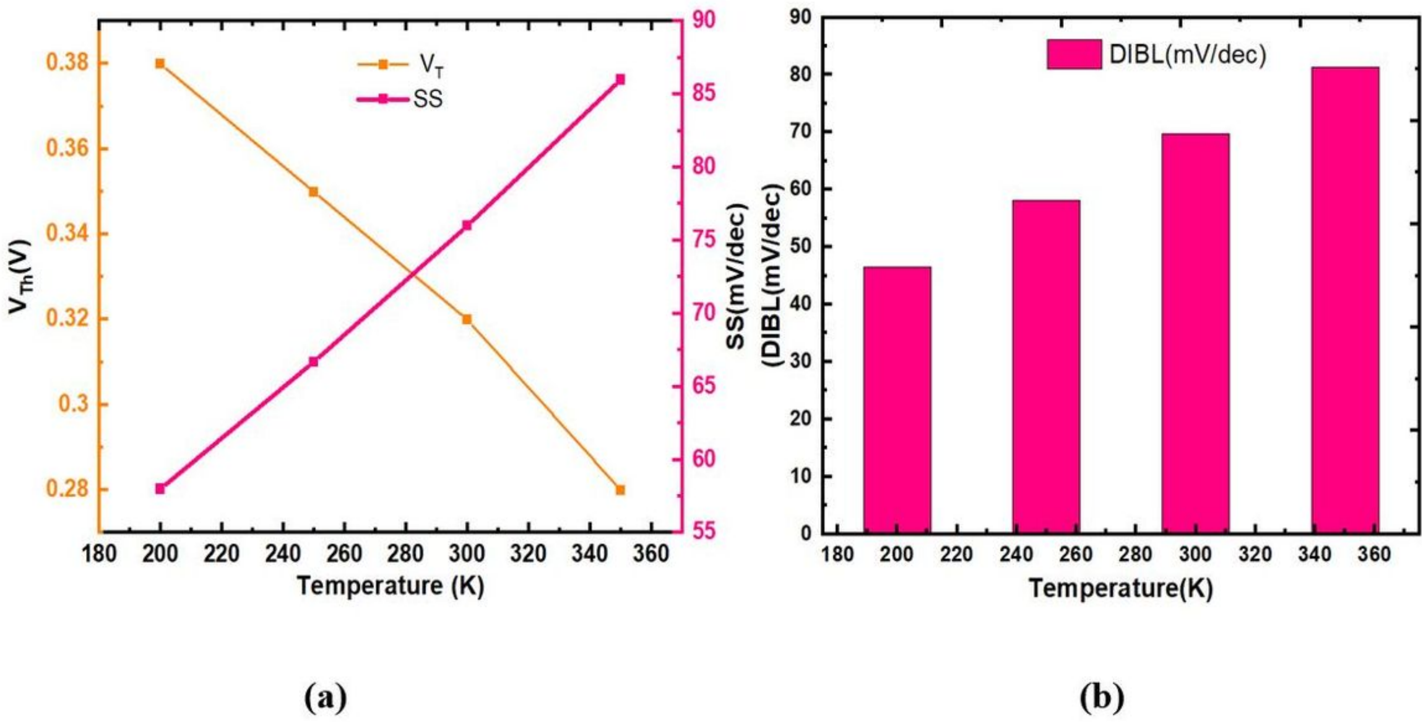


Figure 4

The nano-sheet FET subthreshold characteristics (a) Threshold voltage (Vth) and subthreshold swing (SS) (b) Drain induced barrier lowering (DIBL) with variation of temperature.

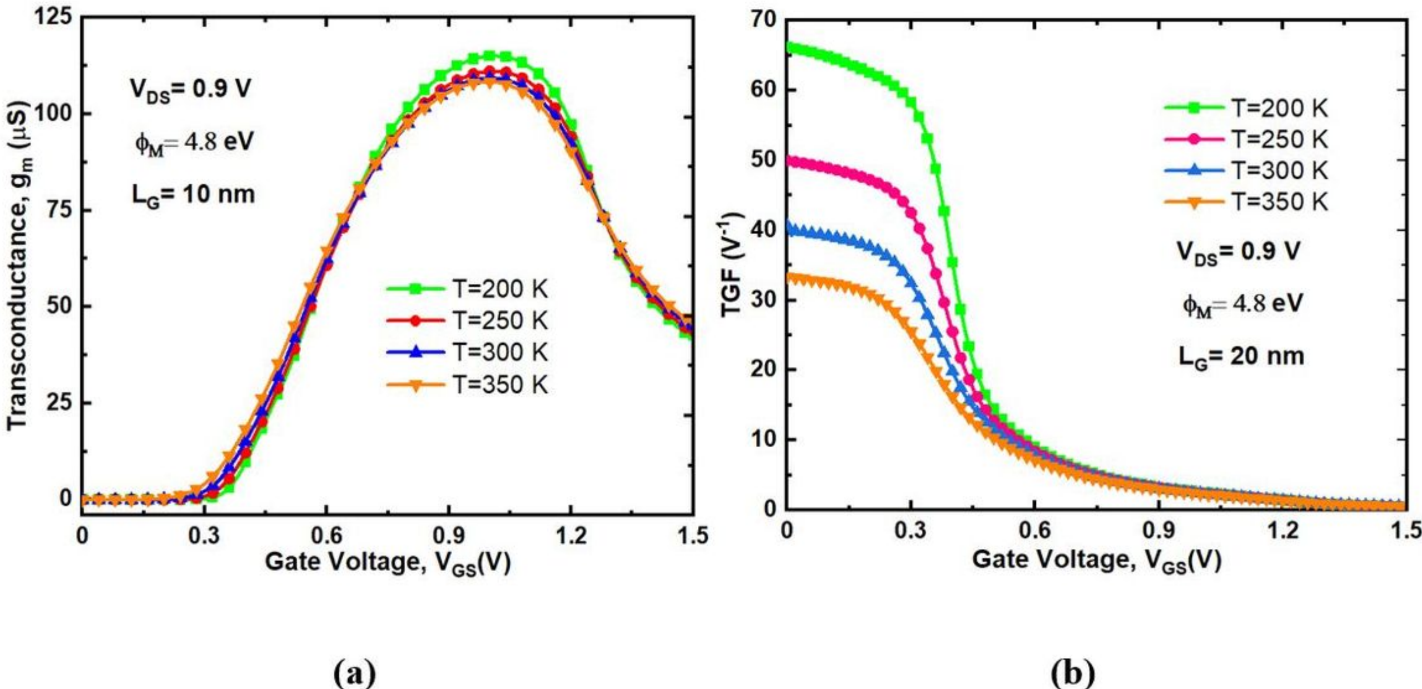


Figure 5

The analog characteristics of nano-sheet FET(a) Transconductance (gm) (b) Transconductance generation Factor (TGF) with variation of temperature.

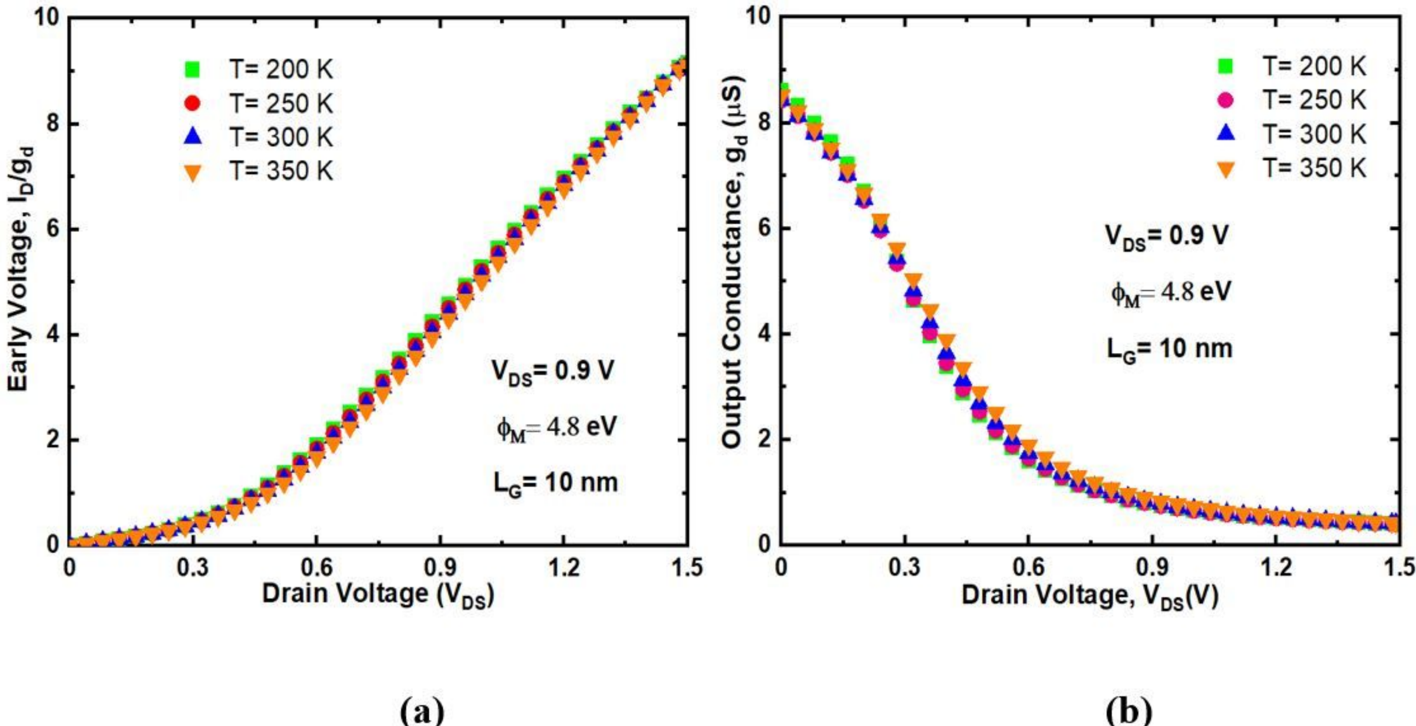


Figure 6

The output characteristics of nano-sheet FET (a) Early voltage (VEA) (b) Output conductance (gd) with variation of temperature.

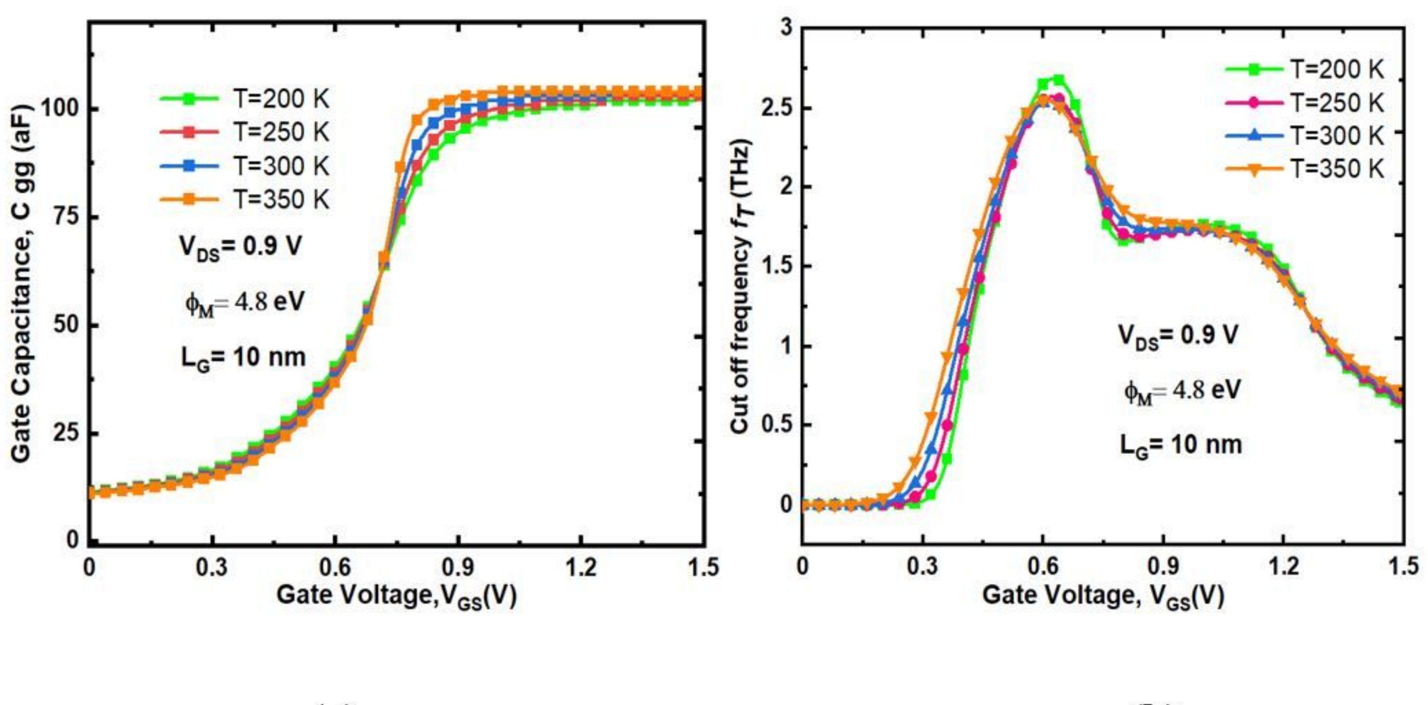


Figure 7

The nano-sheet FET characteristics (a) Gate capacitance (Cgs) (b) Cut-off frequency (ft) with variation of temperature.

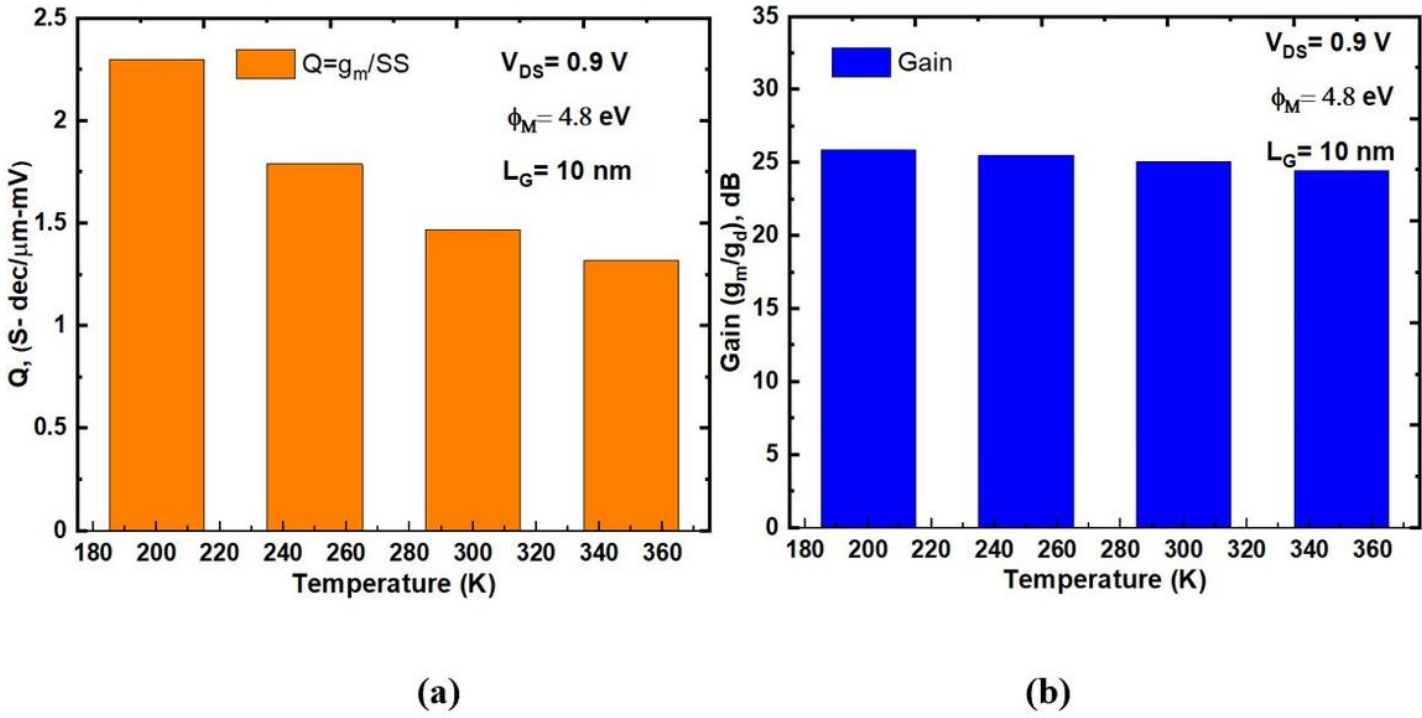


Figure 8

The nano-sheet FET characteristics (a)The ON-OFF performance characteristics (Q) (b) Gain (AV) with variation of temperature.

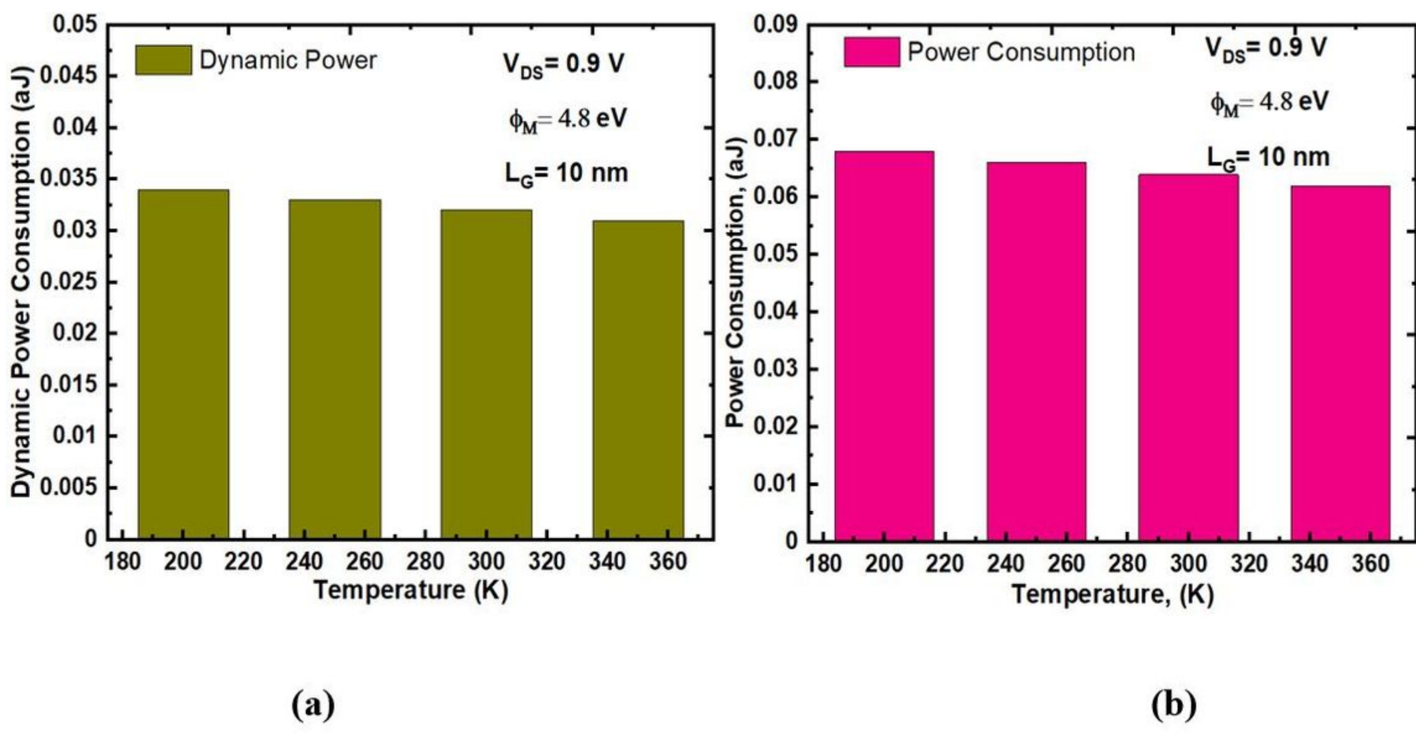


Figure 9

The nano-sheet FET characteristics (a)The dynamic power characteristics (DP) (b) Power consumption (PC) with variation of temperature.

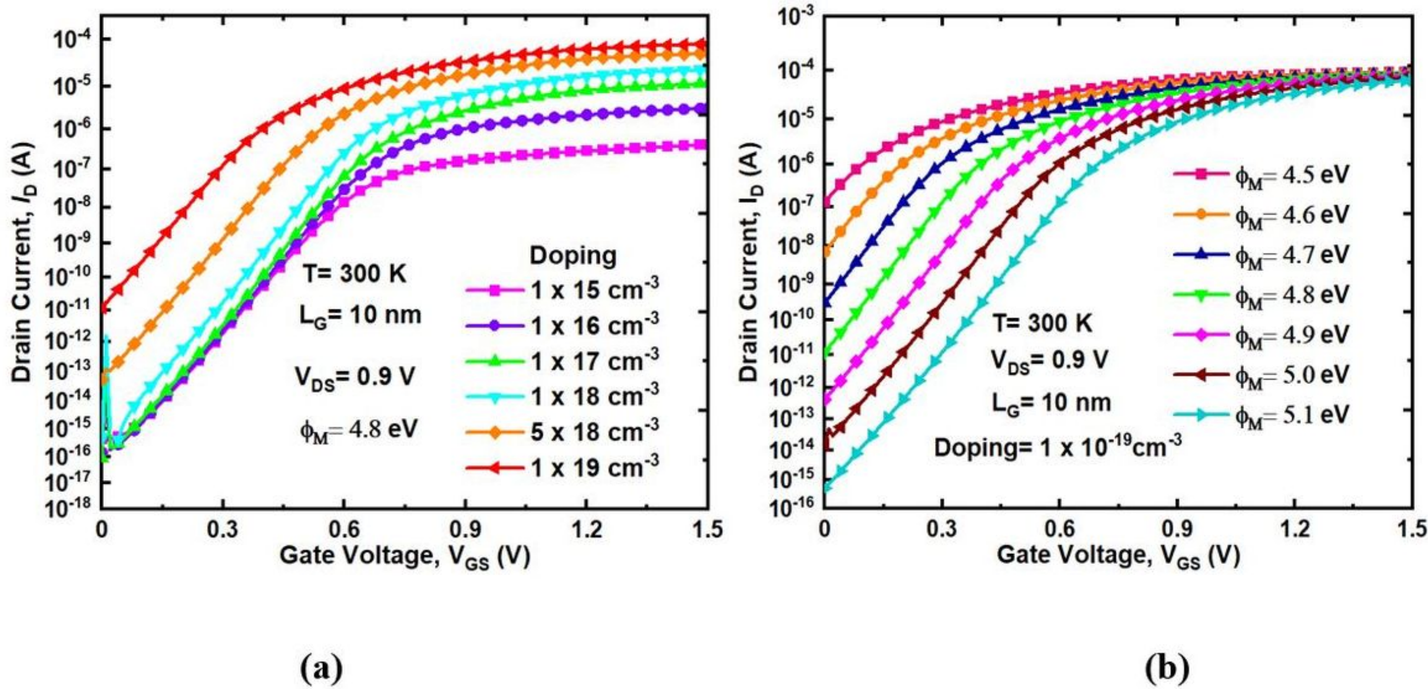


Figure 10

The nano-Sheet FET characteristics (a)The Doping Characteristics (b) Work Function (WF) variation with variation of temperature.

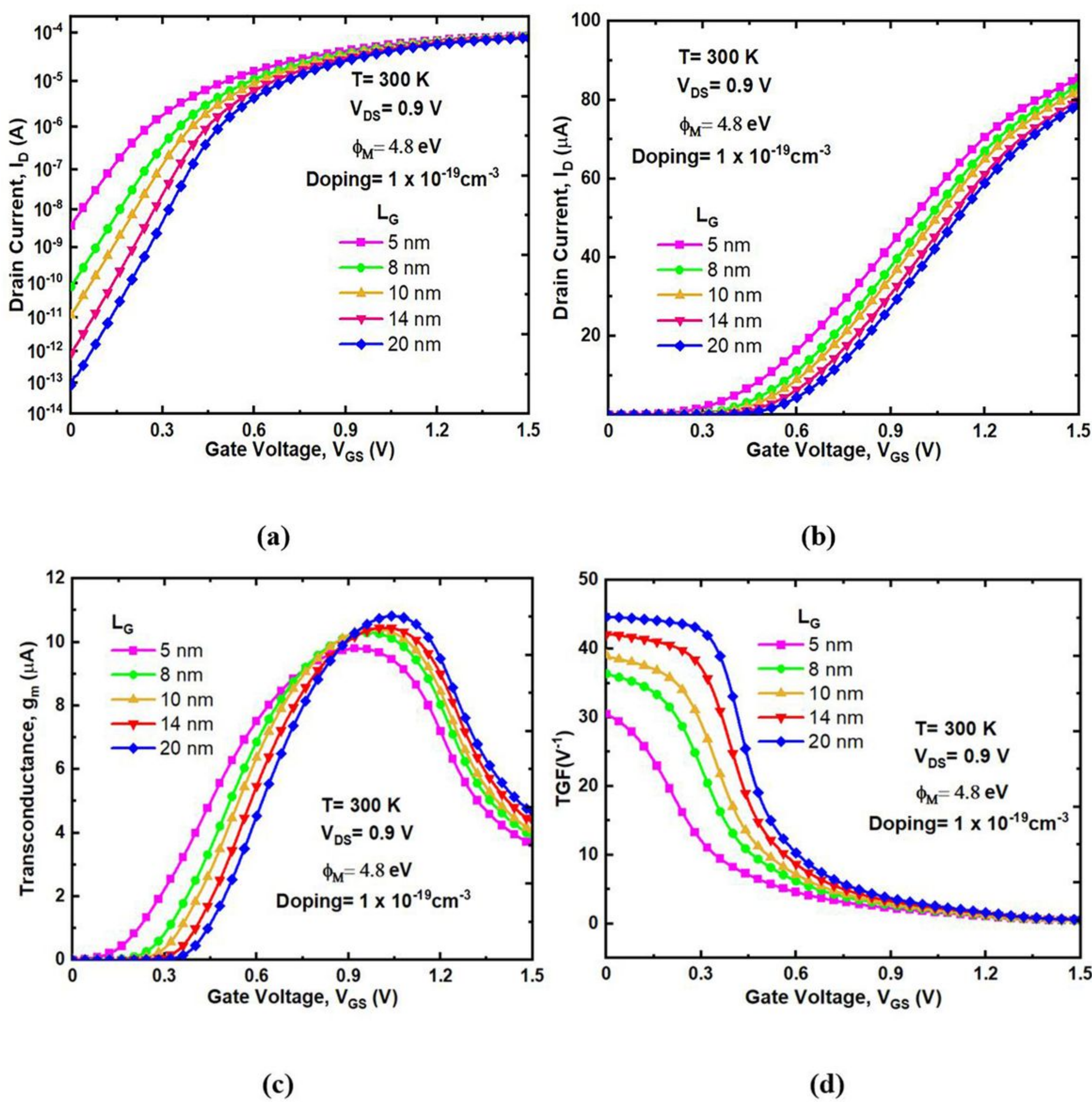


Figure 11

The nano-sheet FET characteristics (a) Gate length (LG) scaling in log scale (b) (b) Gate length (LG) scaling in linear scale (c) Transconductance variation (gm) (d) Transconductance generation factor (TGF) variation with gate length (LG).

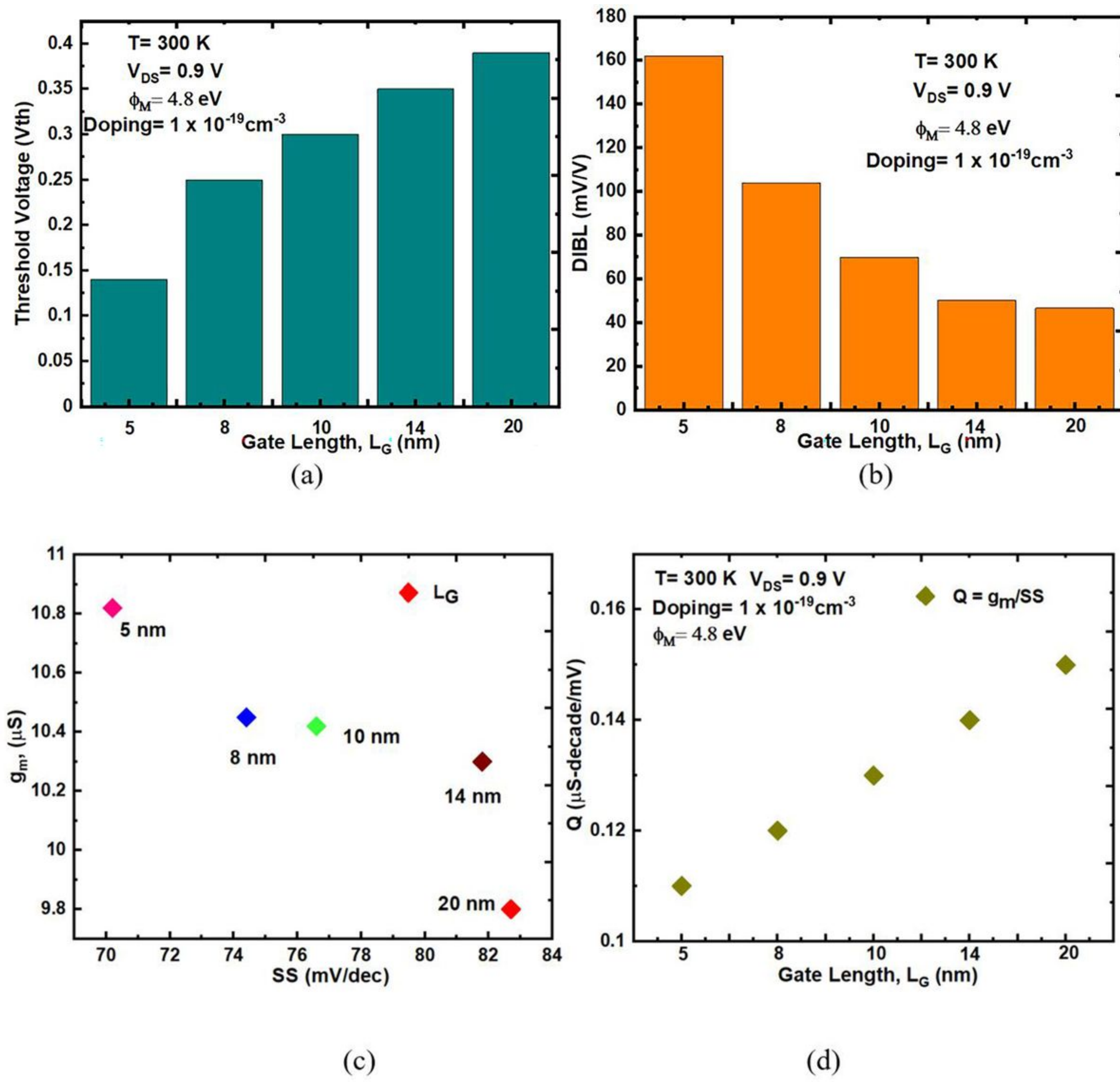


Figure 12

The nano-sheet FET characteristics (a) Threshold voltage (Vth) roll-off (b) DIBL (c) gm and SS and (d) ON-OFF performance metric (Q).