2012

Design, Characterization And Analysis Of Electrostatic Discharge (esd) Protection Solutions In Emerging And Modern Technologies

Wen Liu
University of Central Florida

DESIGN, CHARACTERIZATION AND ANALYSIS OF ELECTROSTATIC DISCHARGE (ESD) PROTECTION SOLUTIONS IN EMERGING AND MODERN TECHNOLOGIES

by

WEN LIU
B.S. SUN YAT-SEN University, 2008
M.S. University of Central Florida, 2010

A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
in the Department of Electrical Engineering and Computer Science
in the College of Engineering and Computer Science
at the University of Central Florida
Orlando, Florida

Fall Term
2012

Major Professor: Juin J. Liou

ABSTRACT

Electrostatic Discharge (ESD) is a significant hazard to electronic components and systems. Based on a specific processing technology, a given circuit application requires a customized ESD consideration that includes the devices' operating voltage, leakage current, breakdown constraints, and footprint. As new technology nodes mature every 3-5 years, design of effective ESD protection solutions has become more and more challenging due to the narrowed design window, elevated electric field and current density, as well as new failure mechanisms that are not well understood. The endeavor of this research is to develop novel, effective and robust ESD protection solutions for both emerging technologies and modern complementary metal–oxide–semiconductor (CMOS) technologies.

The Si nanowire field-effect transistors are projected by the International Technology Roadmap for Semiconductors as promising next-generation CMOS devices due to their superior DC and RF performances, as well as ease of fabrication in existing Silicon processing. Aiming at proposing ESD protection solutions for nanowire based circuits, the dimension parameters, fabrication process, and layout dependency of such devices under Human Body Mode (HBM) ESD stresses are studied experimentally in company with failure analysis revealing the failure mechanism induced by ESD. The findings, including design methodologies, failure mechanism, and technology comparisons should provide practical knowhow of the development of ESD protection schemes for the nanowire based integrated circuits.

Organic thin-film transistors (OTFTs) are the basic elements for the emerging flexible, printable, large-area, and low-cost organic electronic circuits. Although there are plentiful studies focusing on the DC stress induced reliability degradation, the operation mechanism of OTFTs

subject to ESD is not yet available in the literature and are urgently needed before the organic technology can be pushed into consumer market. In this work, the ESD operation mechanism of OTFT depending on gate biasing condition and dimension parameters are investigated by extensive characterization and thorough evaluation. The device degradation evolution and failure mechanism under ESD are also investigated by specially designed experiments.

In addition to the exploration of ESD protection solutions in emerging technologies, efforts have also been placed in the design and analysis of a major ESD protection device, diode-triggered-silicon-controlled-rectifier (DTSCR), in modern CMOS technology (90nm bulk). On the one hand, a new type DTSCR having bi-directional conduction capability, optimized design window, high HBM robustness and low parasitic capacitance are developed utilizing the combination of a bi-directional silicon-controlled-rectifier and bi-directional diode strings. On the other hand, the HBM and Charged Device Mode (CDM) ESD robustness of DTSCRs using four typical layout topologies are compared and analyzed in terms of trigger voltage, holding voltage, failure current density, turn-on time, and overshoot voltage. The advantages and drawbacks of each layout are summarized and those offering the best overall performance are suggested at the end.

To my parents LIU Jianqiang and WANG Xiangju

ACKNOWLEDGMENTS

It would be extremely difficult for me to accomplish this work without the help and support of a number of people. First of all, I owe sincere gratitude to my advisor, Dr. Juin J. Liou. His timely advice and patient help are the indispensable sources for my research. His diligence and earnestness in science and engineering always inspire me to become a better learner.

I want to thank my dissertation committee members, Dr. John Shen, Dr. Kalpathy B. Sundaram, Dr. Jiann S. Yuan and Dr. Quanfang Chen, for their valuable reviews, comments and suggestions on improving my research.

I would like to thank all the collaboration partners, Dr. Navab Singh, Dr. Y. Jiang, and Dr. G. Q. Lo (Institute of Microelectronics, Singapore); Dr. Takao Someya, Dr. Tsuyoshi Sekitani, Dr. Kazunori Kuribara, and Kenjiro Fukuda (University of Tokyo, Japan); Dr. H. C. Lin and Dr. Wei-Chen Chen (National Chiao Tung University, Taiwan); Dr. Huei Wang and Han-Chih Yeh (National Taiwan University, Taiwan); Dr. J. Chung and Dr. Y. H. Jeong (Pohang University of Science and Technology, Korea), for not only providing me with abundant samples and measurements support, but also numerous insightful discussions and suggestions for in-depth research.

I am also grateful to IBM System and Technology Group, and Singapore Institute of Manufactory Technology for offering me the invaluable internship opportunities, from which I gained the experience of applying research concepts to real-world industrial trouble-shooting. Special thanks to Dr. Fernando Guarin (IBM) and all the colleagues in IBM and SIMTech for tremendous guidance and helpful tutorials whenever I have a problem.

I am fortunate to work within a research group of talented students. I appreciate the kind help from Dr. Zhiwei Liu (UESTC), Dr. You Li (IBM), David Ellis, Dr. Slavica Malobabic (Maxim), Blerina Aliaj (Maxim). I also want to thank Dr. Xiang Liu (RFMD), Qiang Cui (ADI), Brian Chang (Lockheed Martin), Zhixin Wang (UCF), Sirui Luo (UCF), Yunfeng Xi (UCF), I have enjoyed every moment that we have worked together. And sincere gratitude goes to my friends, Dr. Jian Lv (Volterra), Carolyn Loftin, Laura Messia, and Sayilila Nulu (IBM).

I would like to express my gratitude to the financial, academic and technical support from University of Central Florida and its staff.

I am heartily thankful to my advisors in SUN YAT-SEN University for encouraging me pursuing Ph.D. education oversea. An incomplete list includes Prof. YU Shijie, Prof. ZHENG Shouseng, Prof. CHEN Ming, and Prof. QI Xinmei.

Last but not least, I am deeply indebted to my parents, LIU Jianqiang and Wang Xiangju, and my husband LI You. Their love, understanding, and support motivated me to accomplish this work.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS

BDS	Bi-Directional Diode String
BDTSCR	Bi-Directional Diode Triggered Silicon Controlled Rectifier
BigMOS	Big MOSFET
BJT	Bipolar Junction Transistor
BSCR	Bi-Directional Silicon Controlled Rectifier
CBM	Charge Board Model
CDE	Cable Discharge Event
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide-Semiconductor
CVD	Chemical Vapor Deposition
DTSCR	Diode Triggered Silicon Controlled Rectifier
DUT	Device Under Test
ESD	Electrostatic Discharge
FOM	Figure of Merits
GAA	Gate-All-Around
GGNMOS	Gate-Grounded N-type MOSFET
HBM	Human Body Model
HMM	Human Metal Model
IC	Integrated Circuits
IEC	International Electrotechnical Commission

MM	Machine Model
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NWFET	Nanowire Field-Effect Transistor
NWTFT	Nanowire Thin-Film Transistor
OTFT	Organic Thin-Film Transistor
RF	Radio Frequency
SAM	Self-Assembled Monolayer
SCR	Silicon Controlled Rectifier
SCS	Semiconductor Characterization System
SEM	Scanning Electron Microscope
SOI	Silicon-on-Insulator
STI	Shallow Trench Isolation
TEM	Transmission Electron Microscope
TLP	Transmission Line Pulsing
VFTLP	Very Fast Transmission Line Pulsing

CHAPTER 1 INTRODUCTION

1.1 ESD and failure mode

Electrostatic Discharge (ESD) is the transient transportation of accumulated charges between two objects with different potentials. It is associated with the generation and transfer of huge current within pico-second to a few hundreds nano-second time domain. The prerequisites of ESD event include accumulation of charges, two items with different potentials, and touching or close proximity of the two items. In our daily life, ESD is the essential mechanism for electric shock and sparkles when touching a metal object after walking across a carpet or taking off sweater in dry winter. Unlike the mild discomfort human body suffering from ESD, modern integrated circuits (IC) sustain a great loss in various forms of soft and catastrophic damages resulting from ESD stresses through the entire life cycle, from front-end-of-line and back-end-of-line fabrication, wire bonding, packaging and shipping, to user end applications, during which the prerequisites of ESD could be met easily if the protection solution against ESD is insufficient or absent. Over the years, ESD failure percentages as total failure modes ranging from 10% to 90% were reported by different research groups [1-4].

The failure mechanisms of ICs subject to ESD events can be essentially classified into two categories: high voltage induced oxide and junction breakdown, and high current evoked material deterioration. The former is electric field dominant failure that becomes more and more significant in advance technologies, because supply voltage does not shrink as much as physical dimensions. The latter is primarily thermally driven as localized high current arouses overheating of materials and ultimate property change or burn-out. For the sake of discovering the root cause

of failures and trouble shooting, failure analysis is performed by electrical characterization based qualification testing and simulation, as well as microscopy based visual inspection using transmission electron microscope (TEM), scanning electron microscope (SEM), and optical or emission microscopes [5]. Typically, soft failure can be diagnosed by rise of leakage current or shift of electrical characteristics, and hard failure is revealed by malfunction due to open or short of circuits. By making use of various microscopes, certain types of ESD induced damages can be observed visually. Figure 1.1 shows the top layer interconnect burn-out (a) [6], metal contact rupture (b) [6], crystal structure change and fusing of FinFET (c) [7], and junction melting (d) [8] caused by ESD stresses.

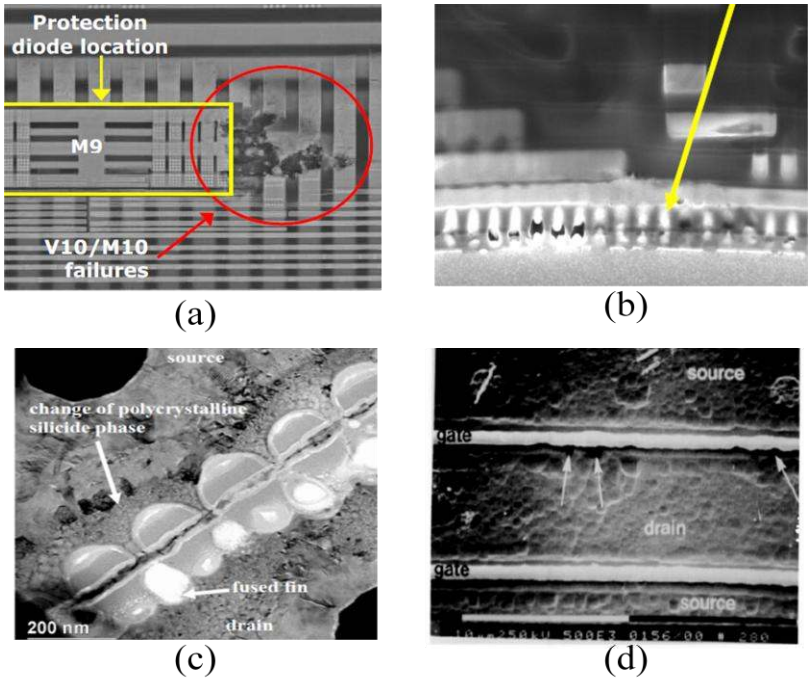


Figure 1.1: Various failures caused by ESD events [6-8].

1.2 ESD models

The characterization and analysis of IC chips under ESD stress necessitate the reproduction of real-world ESD events, thereby different models were introduced and developed. Such models include Human Body Model (HBM), Machine Model (MM), Charged Device Model (CDM), system level IEC (International Electrotechnical Commission) test, Charge Board Model (CBM), Human Metal Model (HMM), Cable Discharge Events (CDE) [9], etc., where human body, machine, IC chip, circuit board, cable, or an entire system are modeled by certain capacitance for charge accumulation, as well as resistance and inductance along the discharging path.

HBM and MM represent a charged human body or machine discharging to a grounded unpowered device under test (DUT). HBM is the most commonly used and well understood model and MM was considered the worst case HBM with lower discharging impedance. Typically, components passing 1 kV HBM are expected to have MM performance around 1/20 ~ 1/30kV. Recent improvement of static controlled manufacturing environment has made HBM and MM less critical. For instance, component level ESD requirements for HBM / MM have been reduced from 2kV (HBM) / 200V (MM) to 1kV (HBM) / 30V(MM) [10].

The basic system level test IEC 61000-4-2 replicates a charged person discharging to a system in a user end environment when the system is unpowered or operating with power applied. HMM is an alternative standard to address individual device using IEC 61000-4-2 basic. The motivation of system level ESD testing is to ensure that the finished products can survival ESD events that occur during normal day-to-day use such that ordinary users do not need to conduct ESD prevention procedures. Comparing to HBM, the peak current of IEC is about 6

times of that of HBM, and its rise time is less than 1/10 of that of HBM. Therefore, products designed with high HBM robustness may not survive under system level ESD stresses.

CDM and CBM simulate charged device or printed circuit board discharging through their own resistance and inductance to an object with ground potential. The CBM discharges higher energy than CDM due to high board capacitance and faster rise time [11]. CDM is becoming primary ESD hazard due to advanced IC development trends, such as larger IC package feature sizes and pin counts, smaller and thinner device active region and interconnect, and higher speed or mixed signal sensitive pins [12]. The resulting larger capacitance, higher resistance, and more complicated discharging path restrict the design of robust CDM protections. Up to 99.9% ESD damages may stem from CDM modes failure in light of a recent survey [13].

The ESD models share the same simplified equivalent circuits using different parameters for capacitor, resistor and inductor. As shown in Figure 1.2, circuit (b) can be used for CDM, CBM and CDE whereas circuit (a) works for the rest models. The corresponding values for R, C and L are listed in Table 1.1, in company with the major parameters for the typical discharge current waveform. Such information comes from the joint efforts of ESD Association, JEDEC, U.S. military agencies and governmental units, IEC, and European standards development bodies [14].

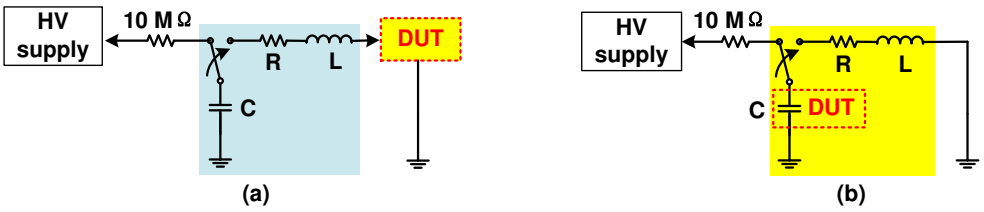


Figure 1.2: Equivalent circuit of ESD models.

Table 1.1: Parameters of major ESD models

ESD Model	Rise time (ns)	Decay time (ns)	Peak Current (A/kV)	R (Ω)	C (pF)	L (μH)
HBM	2~10	100~170	0.67	1500	100	7.5
MM	6~7.5	66~90	0.16	<10	200	~0.75
CDM	<0.4	0.4~2	11.5	10	<10	0+
IEC 61000-4-2	0.7~1	30	3.75	330	150	-

1.3 ESD component assessment and TLP technology

For the purpose of diminishing the generation of ESD induced failures and degradations during manufacturing, shipping and user-end applications, ESD tests based on the aforementioned models are performed as a part of product qualification. HBM and CDM are the two models required for ESD component robustness assessments [10, 12].

The early version of ESD HBM testers only supply pass or fail information that serve as a part of products quality specs. The destructive nature of this test demands a large quantity of test structures. Failure mechanisms are hidden in the 'black box' until failure analysis tools dig into the damaged components. For ESD protection designers and researchers, merely knowing the failure threshold is not enough to diagnose underlying mechanisms and perform troubleshooting. Recently, HBM testers capturing voltage and current waveforms of DUT are available from major manufacturers to provide more details of the HBM ESD performances.

Alternatively, transmission line pulsing (TLP) technology offers an insightful view of devices and circuits' quasi-static behaviors under ESD stress as a function of current severity in time domain. First introduced by T. Maloney and N. Khurana in 1985[15], the TLP technology has became an indispensable ESD analysis tool since mid 90s with the development of commercial and in-house-built TLP systems. Research endeavors have been spread among system development and standardization [16, 17], correlation between HBM and TLP [18, 19], and definition of failure criterion [20], etc. Instead of interpreting the fundamentals of transmission line theory, which can be found in plenty of literatures [21, 22], this section focuses two inquiries: how to use TLP for ESD protection design, and why it is reasonable.

The TLP system circuit topology and waveforms are illustrated in Figure 1.3. The system includes the transmission line part to generate rectangular pulses with pulse width of 100ns to 200ns and rise time of 0.2ns to 10ns, and DC voltage supply to test leakage current for failure identification. The current and voltage waveforms under single ESD pulse can be captured and measured for DUT I-V curve plotting. In TLP systems, like Barth 4002, the default measurement window, also called the quasi-static region, is 70%-90% of the pulse width [23], where current and voltage across DUT become stable and averaged values are used to plot one point in I-V curve. Sufficient points can be collected to fill out the curve by successively increasing amplitude of the pulses with proper steps. DC voltage biasing or sweep is applied to the same DUT after each pulse to identify soft or hard failure. Typical indications of failure are significant change (a few orders) of leakage current, or user defined current criterion for certain applications, say leakage of 1μA is taken as a fixed failure criterion. For some devices, the I-V curve reveals failures by saturated current at high voltage due to self-heating effect, or sudden huge drop of

current due to the damage of metal wires or vias, as well as abrupt voltage drop due to internal short. Major ESD characteristics, including trigger voltage V_{t1}, holding voltage V_h, failure current I_{t2}, failure voltage V_{t2}, on resistance R_{on}, and leakage current $I_{leakage}$ can be obtained by direct reading or simple extraction from the I-V and I-$I_{leakage}$ curves.

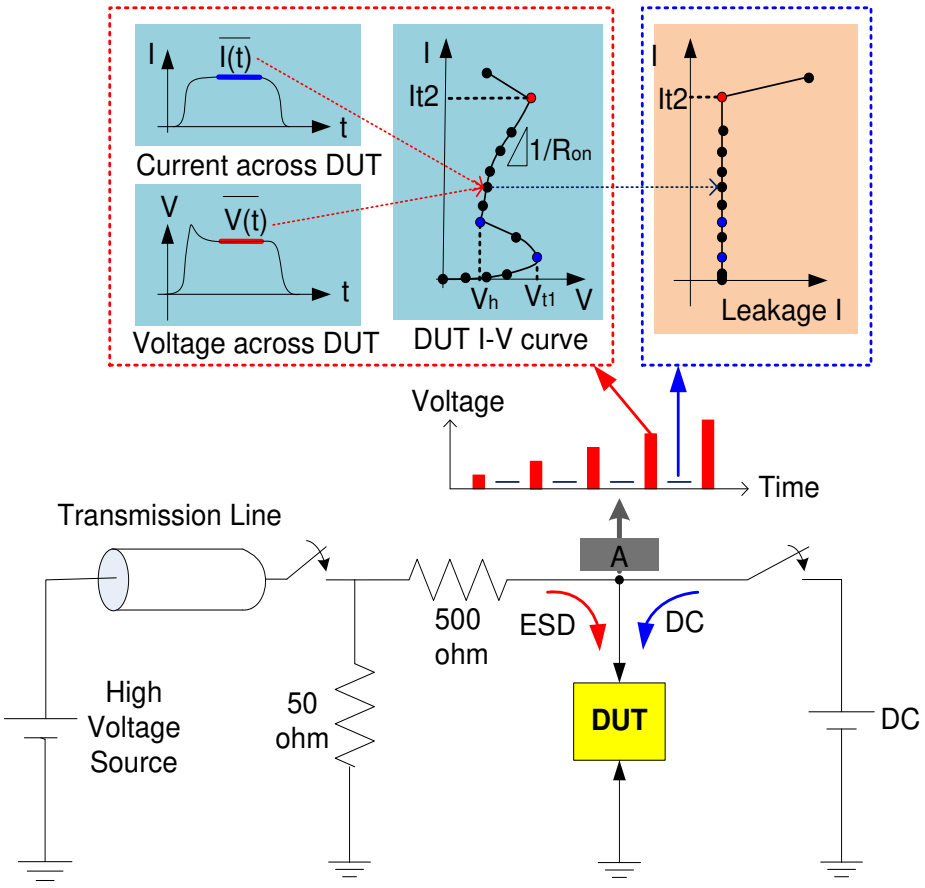


Figure 1.3: TLP system circuit topology and waveforms.

The advantages of using TLP for HBM/MM characterization and analysis are obvious:

1) The rectangular pulse makes the measurement along pulse width more accurate than other pulse shapes [24];

2) Self heating effect, which damages the DUT in DC test easily, can be avoided to a great extent attributing to the short duration of the pulse, such that ESD stress can reach a much higher level and important characteristics like snapback, soft failure, and breakdown can be captured;
3) The correlations between TLP and HBM have been established solidly given that the failure criterion and current paths are properly defined [18]. The approximate HBM robustness of DUT can be simply achieved by multiply the TLP failure current I_{t2} with 1500Ω, which is the typical resistance of a human body [19, 20].

In respect that TLP is only valid to simulation HBM and MM ESD events, very fast TLP (VFTLP) system has been applied to study CDM event [25]. VFTLP is capable of generating rectangular pulses with 1ns to10ns pulse width and rise time of 0.1ns to 0.4ns. The system setup and application of VFTLP is close to that of TLP. It must be noted that the VFTLP I-V curve and waveforms are adaptable to characterize parameters including V_{t1}, V_h, R_{on}, and transient performance like turn on time and voltage overshoot. But it is not adequate for failure threshold prediction due to the dissimilar ESD current paths and directions under VFTLP and CDM [25, 26].

1.4 ESD protection concept, zapping mode and design window

The ideal whole-chip ESD protection concept assumes that if there is an ESD stress targeting at any two pins of a circuit, a low resistive ESD protection device or circuit bypasses the stress and prevent the core circuits from damage. On the other hand, such ESD protection blocks must keep off with low parasitic effects, like leakage current, capacitance and resistance, during IC normal operation so that the function and power consumption of the whole chip will

not be affected. As shown in Figure 1.4, ESD protection blocks are incorporated between I/O pad and VDD, I/O and VSS, as well as VDD and VSS. Take input pad for example, a comprehensive ESD protection should be able to bypass stress under four ESD zapping modes:

(1) PD mode: positive ESD stress zapping at input pin with VDD grounded. The current paths are illustrated by blue solid line and blue dotted line in Figure 1.4. The latter requires I/O ESD protection II operates bi-directionally.

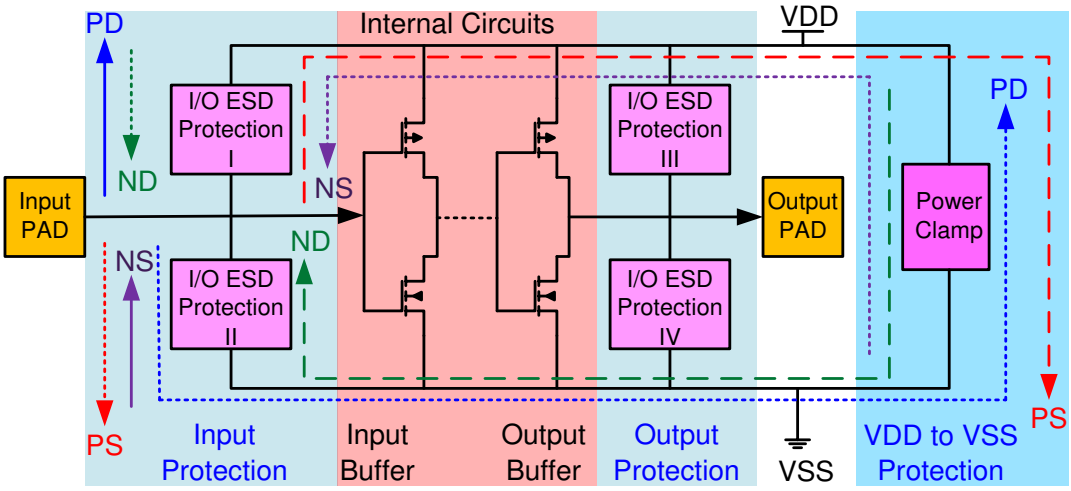


Figure 1.4: Whole chip ESD protection and zapping modes.

(2) PS mode: positive ESD stress at input and VSS is grounded. The primary current path consists of I/O ESD protection I, VDD bus, and power clamp, as marked by red dash line in Figure 1.4. This mode is usually considered to be the most vulnerable path due to high voltage drop and voltage-overshoot-induced gate oxide damage at input buffer. The current path

indicated in red dotted line has lower resistance if ESD protection II is bi-directionally conductive.

(3) ND mode: negative ESD stressing at input with VSS grounded. The primary current path is denoted by green dash line whereas the alternative current path (green dotted line) establishes when I/O ESD Protection I is bi-directional.

(4) NS mode: negative ESD zapping at input with VSS grounded, shown by purple solid line and dotted line representing the primary and alternative current paths, respectively.

The building elements of the I/O ESD protection and power clamp can be a single device or a circuit that have a different operation mechanism comparing to core circuit. The ESD protection block keeps in off-status under normal circuit operation and switches on in the presence of ESD stresses to provide a low impedance shunt path. Therefore, ESD device or circuits should be capable of detecting ESD events, which has much higher voltage and current and shorter duration than typical core circuits biasing signal.

As shown in Figure 1.5, the design window of ESD protection devices is defined by IC operation voltage V_{DD} and transient oxide breakdown voltage BV_{ox}. A 10% safety margin is usually considered to make ESD protection designs more reliable.

The snap-back type devices, like silicon-control-rectifier (SCR), should have a trigger voltage (V_{t1}) smaller than BVox but larger than V_{DD}, such that they turn on at ESD pulses having voltage higher than V_{DD} without damage the gate oxide, and keeps in OFF state when there is no ESD stresses but normal operation biasing. The holding voltage V_h has to be higher than V_{DD} to avoid latch-up issue, otherwise the ESD protection devices will stay on after ESD stress and

short the core circuit. Alternatively, there are some devices using high holding current I_h as a latch-up intervention solution.

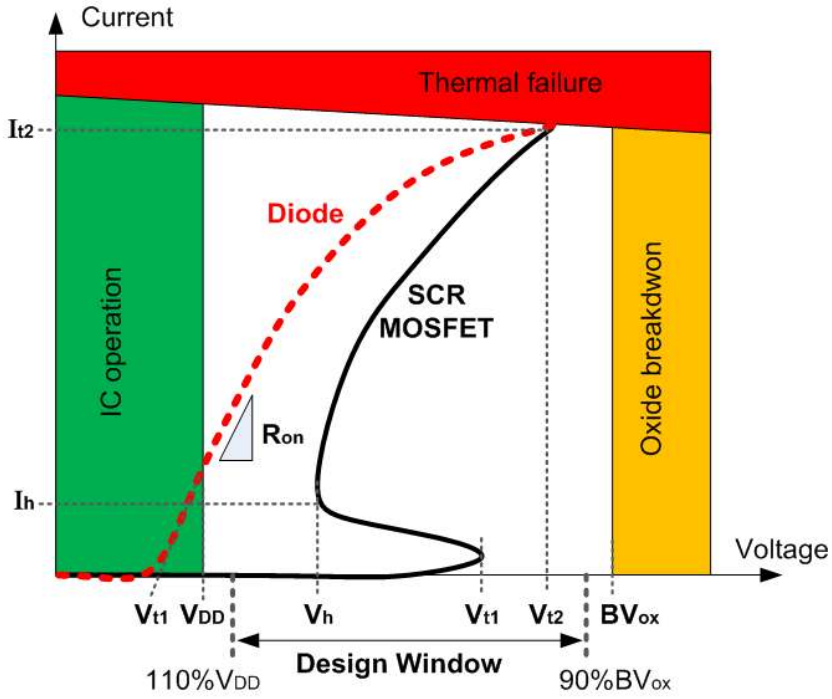


Figure 1.5: ESD design window and TLP I-V curves of basic ESD devices.

The non-snapback device, like diode, has the flexibility to cater for supply signal by stacking and biasing. For I/O protection, the pull-up and pull-down diodes are reverse biased under regular operation biasing condition and get turned on once ESD at I/O pin reaches |±0.6|~|±1|V. For power clamp, a few diodes are connected in series to achieve a V_{t1} higher than V_{DD}. The diode strings are also applied as trigger circuit for SCR to reduce V_{t1}.

The major figure of merits (FOM) of ESD protection devices and circuit include V_{t1}, V_h, and I_h, I_{t2}, V_{t2}, R_{on}, $I_{leakage}$, voltage overshoot and turn on time. Designers should take all this

parameters into consideration to guarantee protection efficiency and minimize the interference introduced by ESD protection solutions to core circuit. It becomes more and more difficult to realize this goal due to technology scaling and thereof smaller design windows [27, 28].

1.5 Basic ESD protection devices and circuits

1.5.1 Diode

Diode is the one of the most widely used ESD protection devices thanks to the structure simplicity, high current under forward biasing and low leakage current under reverse biasing condition. Figure 1.6 illustrates the cross-section schematics of diode consisting of different junctions: (a) P+ and N-well, (b) P-substrate and N+, (c) polysilicon diode realized on shallow trench isolation (STI) layer, (d) poly-bound diode, and (e) isolated P-well and N+. The performance comparison of such diodes in terms of ESD robustness, on resistance, turn-on speed, capacitance, and layout optimization were investigated in a few literatures [29-32], which provides importance information and guideline for diode-based ESD protection design.

A circuit with whole chip ESD protection using local diodes for I/O protection and diode strings for power clamp is shown in Figure 1.7. In order to achieve high ESD robustness but low parasitic effect and small area, multi-figure configuration is usually adopted for local diode. Because the capacitance is proportional to junction area and the current is defined by perimeter, multi-finger layout of diode satisfies the needs by generating longer perimeter within smaller total area [33].

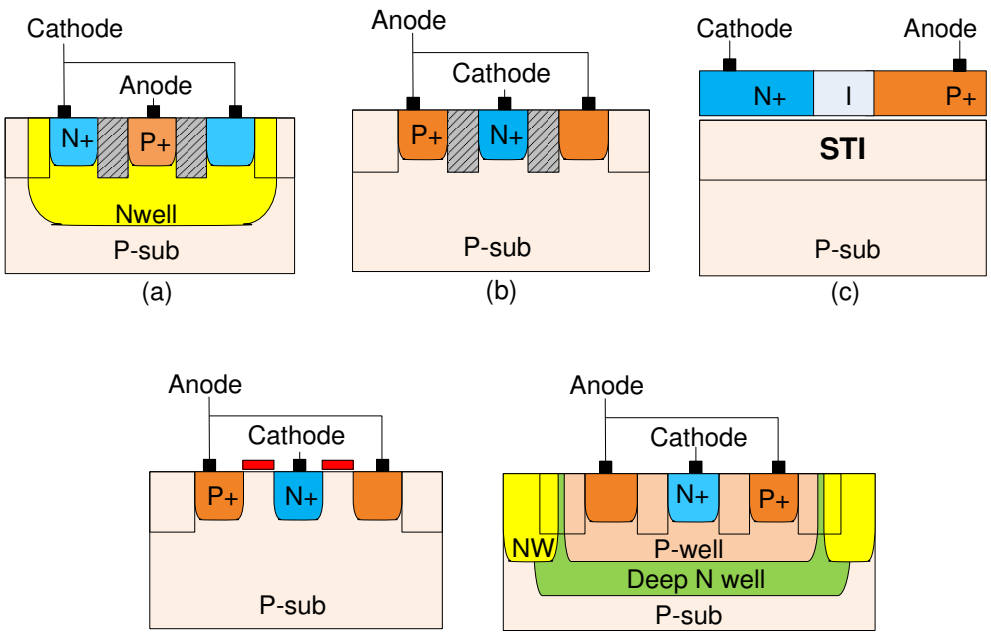


Figure 1.6: Cross-section schematics of diodes made up with various junctions.

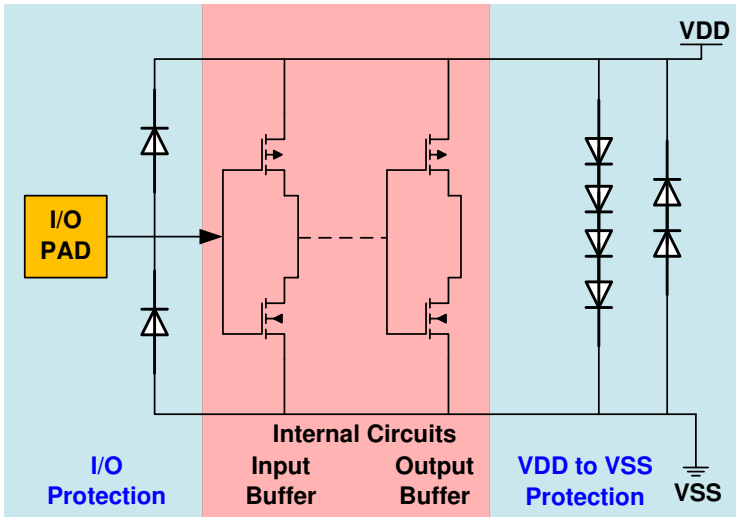


Figure 1.7: Whole chip ESD protection utilizing diodes and diode strings.

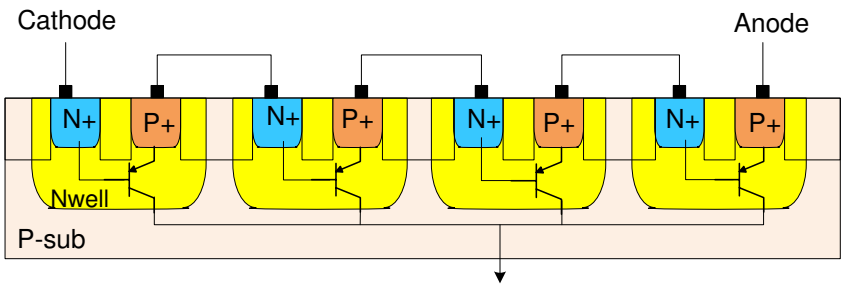


Figure 1.8: Four diode string with Darlington effect.

In some cases, local ESD protection requires more than one diode connecting in series, known as diode string, to suppress leakage current. For power clamp, diode string is used to obtain a V_{t1} higher than V_{DD}. The turn on voltage of diode string is supposed to be the product of the number of diodes and V_{t1} of a single diode. However, the conduction of parasitic bipolar junction transistors (BJT) resulting from substrate acting as collector, also called the Darlington effect, as shown in Figure 1.8, reduces forward voltage due to BJT current gain β. The turn on voltage V_{t1} of a m-stage diode string can be expressed by the following equation [34]:

$$V_{t1} = mV_1 - \frac{\ln(10)nkT}{q}\log(\beta + 1)\left(\frac{m(m-1)}{2}\right) \quad (1.1)$$

where V_1 is the turn-on voltage of one base-emitter junction and n is a process dependent constant. Aiming at preventing latch-up, the number of diodes in a string should be defined base on equation (1.1) so that trigger voltage of the string is larger than 110% V_{DD}, taking design margin into consideration.

The drawbacks of diode-based protection include high voltage drop due to severe self-heating effect, high capacitance under forward biasing with short depletion region, high on-resistance of diode string, and leakage induced power dissipation in reverse bias condition.

Despite all these issues, diode is an important ESD protection device and trigger assisting component, especially for the I/O protection of radio frequency (RF) circuits.

1.5.2 MOSFET

The appeal of using metal-oxide-semiconductor field-effect transistor (MOSFET) for ESD protection lies in the fact that it is complementary metal-oxide-semiconductor (CMOS) process compatible and clamps ESD stress with proper trigger voltage and holding voltages. Figure 1.9 presents a cross-section schematic of gate-grounded N-type MOSFET (GGNMOS) with isolated P-well in technologies including deep N-well process. One application example of this device is illustrated in Figure 1.10, where the GGNMOS clamp voltage across the gate of internal circuit, primary ESD clamp bypass the most current, and resistor R limit the ESD current passing through GGNMOS. In some other cases, GGNMOS with large dimension can be used independently as an ESD protection device.

The operation of parasitic BJT dominates the working mechanism of MOSFET under ESD. In Figure 1.9, N+(Drain)/Pwell(body) junction gets reverse biased when positive ESD zaps at anode with source and substrate grounded. Avalanche breakdown takes place as the stress level goes higher and holes and electrons are generated by impact ionization. The body current I_{body} is formed by holes drifting from anode toward body and source, whereas the electrons get extracted by drain and add up to the total drain current. As I_{body} increases, the potential at body reaches the level to forward bias the base-emitter junction of parasitic BJT. The condition for triggering GGNMOS is given by formula (1.2) [35]:

$$M(\beta - 1) \geq 1 \tag{1.2}$$

where β is the current gain of BJT and M is the avalanche multiplication factor. After triggering, electrons are swept from emitter (source) to collector (drain) giving rise to even higher drain current. As a result, a positive feedback is built to sustain the on-status of BJT and less drain voltage is demanded. The negative resistance during snapback characteristic of GGNMOS stems from such mechanism, during which conductivity modulation of the body takes place. The post-snapback phase requires higher voltage to maintain the BJT action due to the reduced body resistance after conductivity modulation. The operation of parasitic BJT is called self-biasing in some literatures.

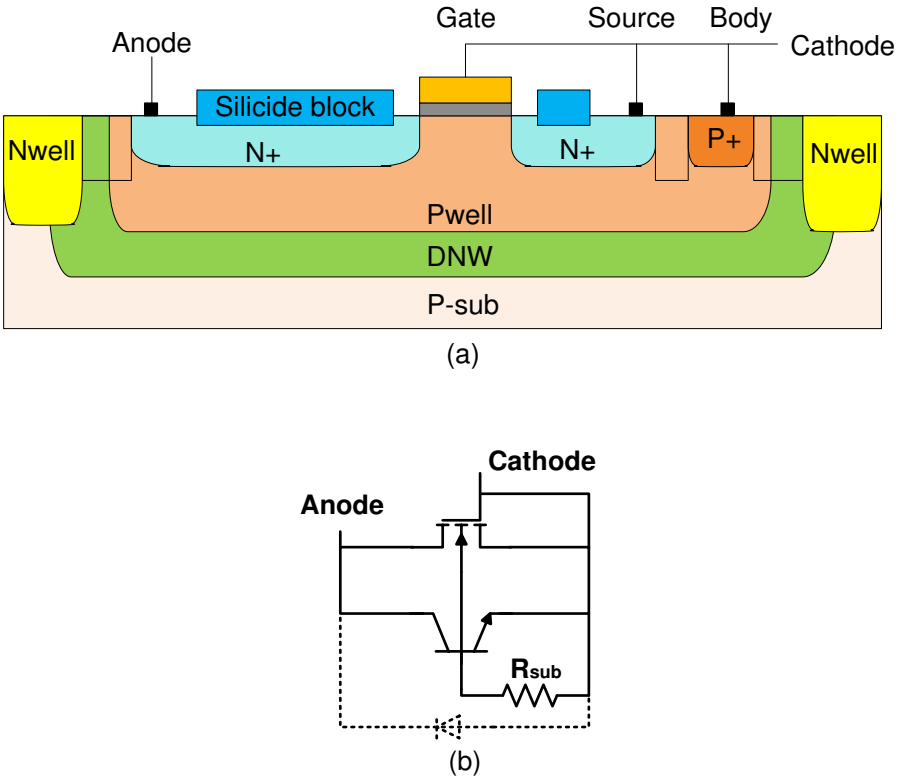


Figure 1.9: GGNMOS cross-section and simplified equivalent circuit.

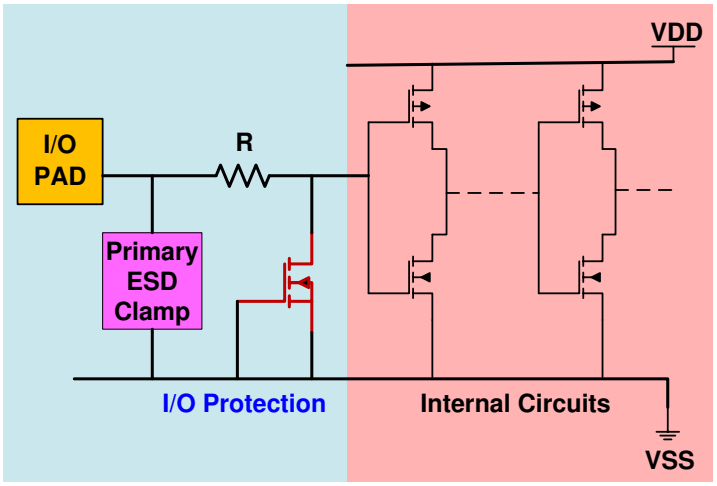


Figure 1.10: Two stage ESD protection using GGNMOS.

The major design challenges of GGNMOS in modern technologies originate from multi-finger layout and silicidation process. The former improves area efficiency and ESD robustness at the risk of non-uniform turn-on of fingers. The latter became an indispensable process in deep-sub-micron CMOS process to reduce resistance and delay, yet weakens ESD performance owing to surface crowded current, and violates turn-on uniformity condition ($V_{t2} > V_{t1}$) for multi-finger devices. Many literatures aiming at solving these issues have been published with valid solutions. For example, silicide block mask is added to process to prevent drain, source and gate region from silicidation, although the cost of fabrication is increased by additional process [36, 37]. Alternatively, cost-effective ballast resistance achieved by N well [38], segmentation [39], back-end poly resistor [40, 41] has been proposed.

1.5.3 SCR

Given the same layout width, SCR offers supreme ESD robustness and least capacitance comparing to diode and GGNMOS. The cross-section schematic and equivalent circuit are illustrated in Figure 1.11. The lateral PNP and NPN BJTs are formed by P+/N-well/P-sub and N-well/P-sub/N+. During positive ESD stress, the N-well and P-sub junction gets reverse biased and initiates avalanche breakdown. The generated current renders voltage drop that turns on either PNP (Q1) or NPN (Q1) transistor. In general NPN turns on first due to higher gain and pulls down the potential at collector, which is also the base of PNP, as a result, PNP turns on and injects current to the base of NPN. The PNP and NPN transistors form positive feedback so that high voltage biasing is no longer necessary to maintain the on-status[1]. The trigger voltage of SCR is determined by the avalanche breakdown voltage of N-well and P-sub, which is a relatively high voltage due to low doping concentration.

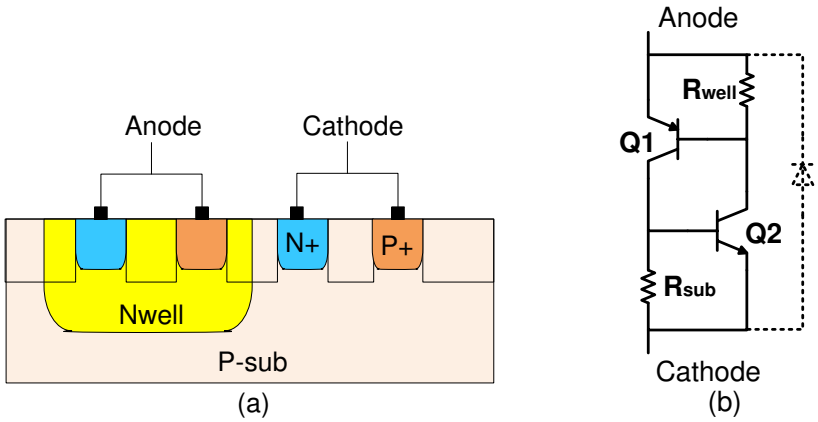


Figure 1.11: SCR cross-section and simplified equivalent circuit.

SCR can be used for both power clamp and local ESD protection. However, the high trigger voltage and low holding voltage render SCR defective for certain I/O and power bus

protections. Take 90nm CMOS technology for example, the transient (100ns) oxide breakdown voltage is around 10V, whereas the trigger voltage of SCR is around 14V. In such scenario, the gate oxide at input buffer gets impaired before SCR fully turns on. On the other hand, latch-up of core circuit may occur if V_{DD} or signal at input is higher than the holding voltage. Therefore, research endeavors have been found on reducing the trigger voltage and increase the holding voltage or current [42, 43].

The design of low-trigger-voltage SCR is based on changing the doping-dependent avalanche breakdown. After embedding the N+ or P+ regions between N-well and P-sub [44], the trigger voltage of SCR tones down to the breakdown voltage of N+/P-sub or P+/N-well. Alternatively, ESD devices with lower trigger voltages, such as diode string and MOSFET, are also incorporated into SCR and dominants the trigger voltage of the entire structure [45-47]. These designs are based on the essential condition to turn on SCR -- the injection of base current and turn-on of emitter-base junction.

As to enhancing holding voltage and current, BJT gain and resistance play an important role. Layout dimensions, such as anode-to-cathode distance, base widths of the parasitic BJTs are increased to boost holding voltage. Other special designs for such purpose include segmentation layout, external shunt resistance, stacking of SCRs, and insertion of holding diodes in diode-triggered SCR [43, 45, 48, 49].

Besides tuning design window, turn on speed is another substantial design consideration for SCR. Although SCR offers low capacitance feature that is favorable for high frequency application, the relatively long turn-on time and high overshoot voltage make it susceptible to CDM ESD stress. For example, it takes more than 1ns to turn on a SCR whereas the pulse width

of CDM ESD is only 0.4-2ns. Chances are SCR fails to switch on and bypass current during CDM event and the induced high voltage overshoot destroys the gate oxide of core circuit. Solutions to improve SCR CDM performance based on research of turn-on time dependency on layout parameters, trigger path, and current density were reported in a few literatures [50, 51].

1.5.4 RC clamp

Different from GGNMOS and SCR that needs special models accounting for breakdown and snapback mechanisms, RC clamp with big MOSFET (BigMOS) has been used extensively in industry thanks to its compatibility to circuit-level simulation and ease of design cycle. A simplified circuit of power-rail RC clamp is illustrated in Figure 1.12 [52]. The clamp use transient dV/dt of ESD stress as trigger detection, and RC delay to maintain on-status of BigMOS during ESD event. A robust RC clamp demands large capacitor and resistor to retain a RC constant of several hundred nanoseconds that covers entire duration of an ESD event, as well as a BigMOS to shunt large amount of ESD current operating in normal condition rather than avalanche breakdown mode. Such requirements lead to large silicon area occupation and possible mis-triggering of BigMOS under fast-on V_{DD}. As a result, design of effective RC clamp with reduced capacitor size and latchup immunity becomes a major challenge. Incorporating various feedback circuits into the basic RC clamp has been demonstrated in previous studies to improve the RC clamp ESD performance [53-55].

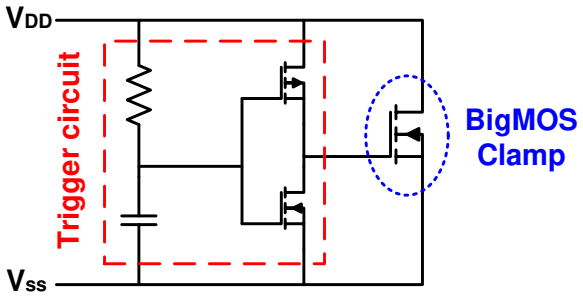


Figure 1.12: Basic RC clamp.

1.6 Dissertation outline

Different technologies and circuit applications require customized ESD consideration at the early stage of design and development. The goal of this research is to develop novel, effective and robust ESD protection solutions for emerging technologies (Silicon/Poly-Si nanowire and Organic thin film) and modern CMOS technologies (sub-90nm). The organization of the dissertation is summarized as following:

Chapter 1 presents the background information including ESD event description, ESD models, failure modes, as well as major ESD protection devices and concept. Chapter 2 covers a comprehensive study of Sub-10nm-diameter gate-all-around silicon nanowire field-effect transistors for ESD protection application. Characterization, simulation, failure analysis, and technology comparison are conducted to assess ESD performance and extract design methodology. Chapter 3 investigates the primary ESD parameters' dependency on nanowire dimension and number, plasma treatment and layout of N-type double-gated poly-Si nanowire thin-film transistors. Chapter 4 studies the mechanism of low-voltage pentacene-based organic thin-film transistors subject to HBM ESD events as a function of gate biasing conditions and key design parameters. Chapter 5 reports the design of bi-directional diode-triggered SCR in 90nm

CMOS technologies. These devices offer optimized design window, small parasitic capacitance, and high ESD robustness. Chapter 6 explores and compares the ESD performances of diode-triggered SCR using four different layout configurations designed in a 90nm CMOS technology. Chapter 7 covers the summary of the dissertation and outlook for future research.

CHAPTER 2 GATE-ALL-AROUND NANOWIRE FIELD-EFFECT TRANSISTORS FOR ESD PROTECTION APPLICATIONS

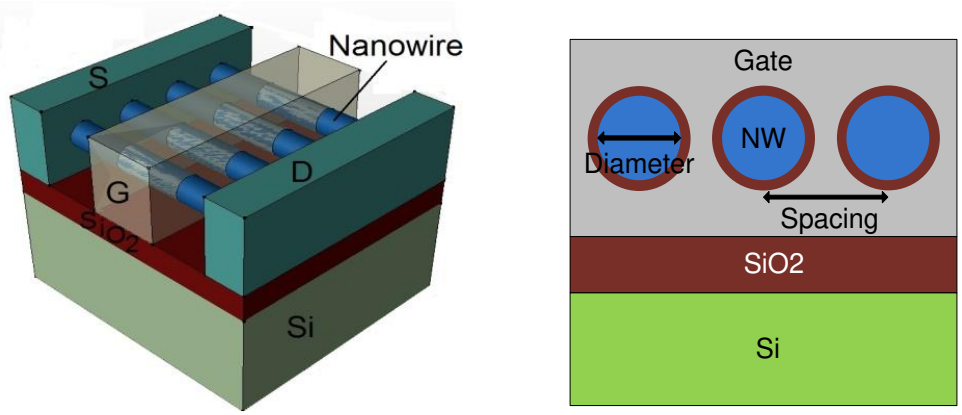
2.1 Introduction

The Si nanowire field-effect transistor (NWFET) has been regarded as a promising alternative CMOS technology in the beyond Moore Era due to its superior electrostatic channel controllability, high on/off current ratio, better noise performance, and ease of fabrication in the existing silicon process [56-59]. Nevertheless, the sub-10nm dimension, silicon-on-insulator (SOI) structure, and silicided diffusion of NWFETs also lead to localized high current density and high electric field, suggesting that it might be fairly susceptible to ESD stress. Moreover, a large number of nanowires may need to be fabricated in parallel to achieve a satisfactory on-current level, and unevenly distributed currents among these nanowires may further degrade ESD tolerance. Previous research efforts were mostly focused on the processing, performance optimization, modeling and reliability analysis of NWFET [60-63]. The operation and robustness of these devices subject to ESD events are still not well understood.

In this work, for the first time, the ESD performances of N-type and P-type NWFETs are investigated experimentally using TLP test system, and their ESD robustness is compared with those of other advanced devices including sub-90nm bulk/SOI MOSFETs and FinFETs. The ESD figures of merits (FOM), including the failure current (I_{t2}), leakage current ($I_{leakage}$), trigger voltage (V_{t1}), and on-state resistance (R_{on}) are characterized as a function of major design parameters, including gate length, nanowire diameter, and nanowire counts.

2.2 Device structure and process

The silicon nanowire transistors can be fabricated by either bottom-up or top-down processes [60]. The former has nanowire grew from nanoparticle catalysts by chemical synthesis, including chemical vapor deposition, vapor–liquid–solid, oxide-growth and solution-phase-based approaches. Such method allows better scalability of nanowires but has difficulties to precisely control chemical composition, physical dimension and nanowire-to-nanowire spacing. On the other hand, the top-down process makes use of CMOS compatible lithographic patterning and etching methods to synthesis nanowires down to sub-10nm-diameter by proper control of electron-beam currents, dry or wet etching process, system noise, etc. Such method enables precise control of nanowire dimension and pitch but limit the minimum diameter of nanowire.



(a) (b)

Figure 2.1: (a) 3D schematic and (b) cross-section of a multi-channel NWFET.

The NWFETs under study were fabricated by top-down process at the Institute of Microelectronics, Singapore. The process starts from nanowires patterning and etching from SOI

wafers and further trimmed by thermal oxidation. Poly-Si gate is then deposited and trimmed before drain/source implantation and activation. Both gate and drain/source extension region went through salicidation process to optimize threshold voltage and reduce contact resistance. More detailed process information can be found in [56, 64].

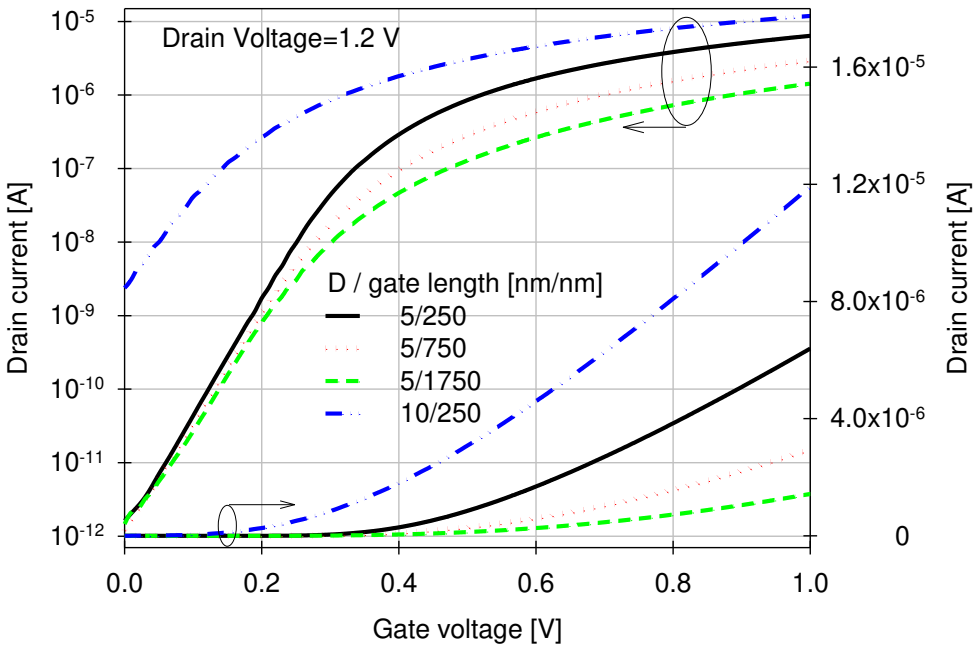


Figure 2.2: Drain current versus gate voltage of N-type NWFETs.

The off-scale three-Dimensional (3D) and two-Dimensional (2D) schematics of the NWFET are shown in Figure 2.1. The circular (sometimes elliptical) shape NWs are surrounded by 5nm of SiO_2 and NiSi fully silicide metal gate. Accordingly, such an device is called gate-all-around (GAA) Si NWFET. The number of parallel naowires within one transistor ranges from 1 to 1000 to obtain different on-currents. The spacing of adjacent nanowires is fixed at 400nm. Figure 2.2 shows the DC transfer characteristics (drain voltage = 1.2V) of the single-nanowire

NWFETs having NW diameters (D) of 5nm and 10nm, and gate length of 250nm, 750nm and 1750nm, in both logarithmic scale (left Y-axis) and linear scale (right Y-axis). The devices offer saturation current at micron ampere and up to 6 orders on/off current ratio. Higher on current can be achieved by shorter gate and larger nanowire diameter, which also increases off-current due to reduced gate control capability and short channel effects.

2.3 ESD performance characterization and simulation

In an effort to determine the parameter dependency, we characterized the aforementioned GAA Si NWFET using the Barth 4002 TLP tester that generates pulses with 100 ns pulse width and 10 ns rise time. The TLP I-V characteristics of N-type and P-type NWFETs, having various gate lengths, 1000 nanowires in parallel with diameters of 10 nm and 5 nm, operating in bipolar and diode modes are shown in Figure 2.3. The stressing setups for the bipolar and diode modes are illustrated in Figure 2.4.

Unlike conventional MOSFET operating at bipolar mode, the absence of snapback behavior of NWFETs stems from the floating feature of the imbedded nanowires, which serve as base of the parasitic BJT. The dominant trigger mechanism of NWFET is avalanche breakdown in nanowire-drain junction and turn-on of parasitic BJT formed by drain-nanowire-source. Owing to the floating body effect, the augmented body potential facilitates the forward biasing of nanowire-source junction and thereof reduces trigger voltage. The absence of snapback is one of the favorable features of SOI structures that benefits turn-on uniformity of multiple channels. As for the operation in diode mode, the NWFETs trigger around 0.6V and allow highest I_{t2} at gate length of 750nm.

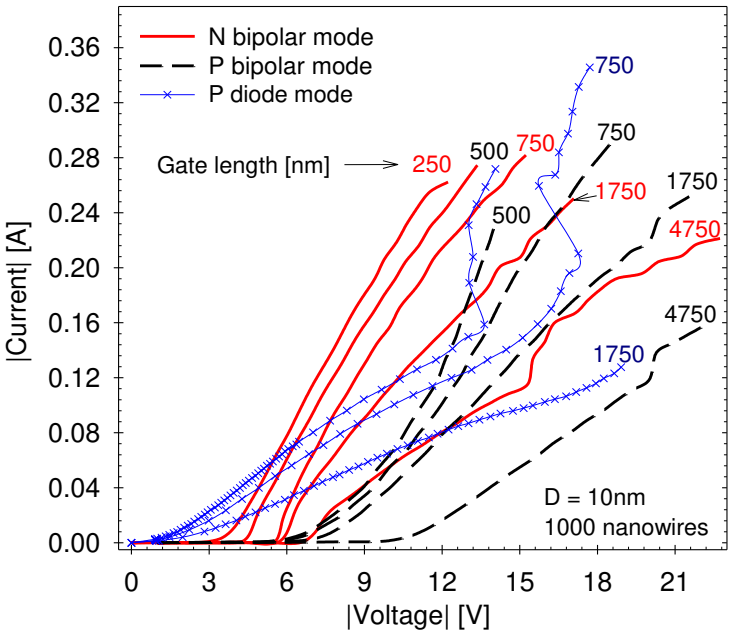


Figure 2.3: TLP I-V curves for the bipolar and diode modes, N- and P-type NWFETs.

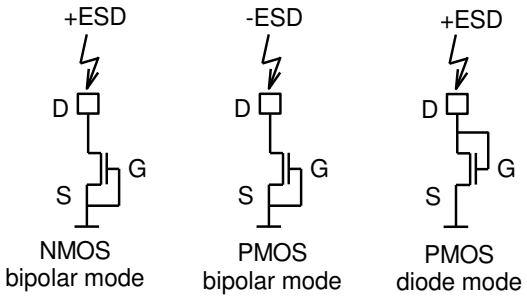


Figure 2.4: TLP stressing setups for bipolar mode and diode mode NWFETs.

The major ESD parameters are further extracted from the TLP I-V curves to investigate dimension (nanowire diameter and gate length), and doping (N-type or P-type) dependency. As shown in Figure 2.5, V_{t1} increases with increasing gate length, and N-type devices have a lower

trigger voltage than P-type ones. The trigger mechanism is determined by the turn-on of parasitic BJT with condition [35]:

$$\beta \times (M - 1) \geq 1 \tag{2.1}$$

where β is the common emitter current gain and M is the multiplication factor. Gate length determines the base width of parasitic BJT, which reduces β as its value increases. Lower carrier mobility of P-type NWFETs and longer channel length result in lower β, which in turn requires larger avalanche multiplication factor M to turn on the BJT. Thus a higher drain voltage is needed for triggering.

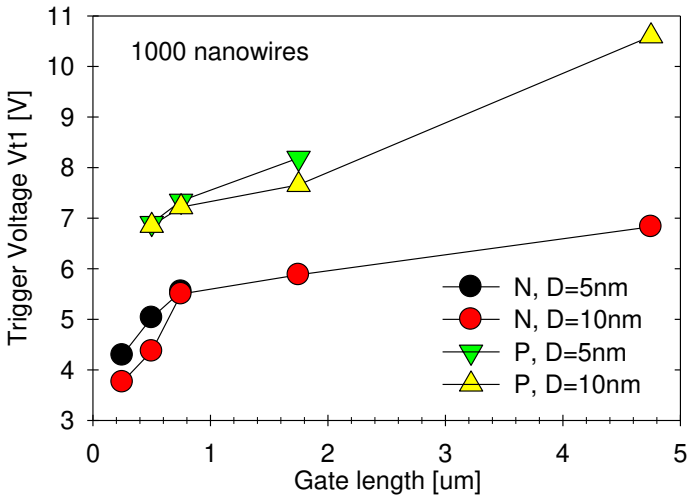


Figure 2.5: Trigger voltage V_{t1} vs. gate length of N- and P-type NWFETs.

In Figure 2.6, I_{t2} increases with expanding gate length initially but drops when the gate length exceeds 750nm, a trend similar to that of the FinFETs [65]. As summarized in Table 2.1, longer gate has both positive and negative impacts over I_{t2} and the best tradeoff is achieved at medium gate length holding the balance of heat dissipation and power consumption. As expected,

the smaller diameter (D) gives rise to a lower I_{t2} because narrow nanowire is apt to be impaired by localized heating generated from the product of ESD current and channel resistance.

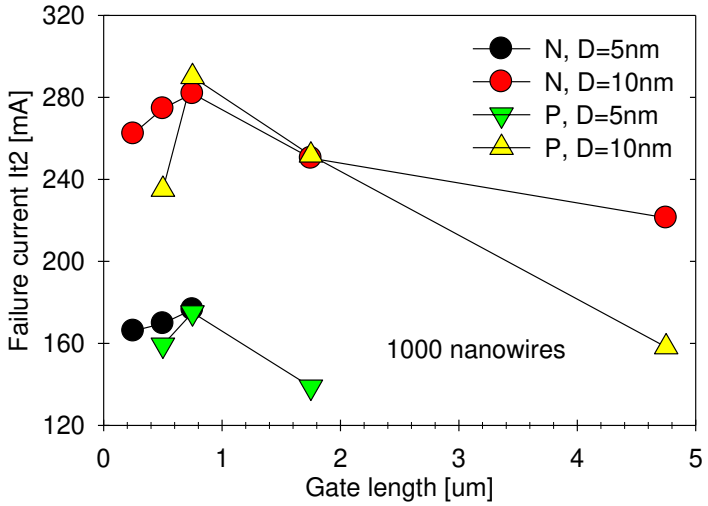


Figure 2.6: Failure current I_{t2} vs. gate length of N- and P-type NWFETs.

Table 2.1: Impacts of gate length over failure current I_{t2}

Larger gate length improves I_{t2}	Larger gate length weakens I_{t2}
Harder for drain-to-source filamentation [66].	Higher voltage drop and more energy consumption [27, 65, 67].
Larger ballistic resistance and better current distribution [67].	More dimension fluctuations of the nanowire cross-section [65];.
Larger volume covered by the gate improves heat dissipation [27, 65]	More defects[68].

The on-resistance R_{on} and leakage current $I_{leakage}$ (measured at 1V for N-type and -1V for P-type devices) of the same devices are compared in Figure 2.7 and Figure 2.8. Narrower nanowire (D = 5 nm) and longer gate lead to higher R_{on} but lower $I_{leakage}$, because the resistance of a nanowire is proportional to its length and inversely proportional to its cross-section area. For devices having the same gate length and nanowire diameter, N-type NWFETs have a lower $I_{leakage}$ than its P-type counterpart. The P-type devices with a diameter of 10 nm are unsuitable for ESD protection applications due to high $I_{leakage}$.

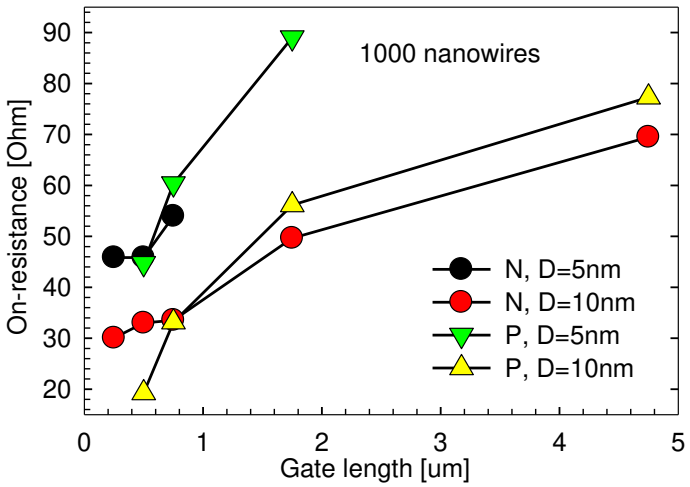


Figure 2.7: On-resistance vs. gate length of N- and P-type NWFETs.

Desirable devices for ESD protection application should have high I_{t2}, small R_{on} and low $I_{leakage}$, which can be represented by the following FOM:

$$FOM = \frac{I_{t2}}{R_{on} \times I_{leakage}} \tag{2.2}$$

Inserting measurement data into the above equation, we can plot the FOM against gate length. As indicated in Figure 2.9, the n-type, medium gate length, narrow (D=5nm) NWFET has the highest FOM, followed by P-type narrow and n-type wide (D=10nm) devices.

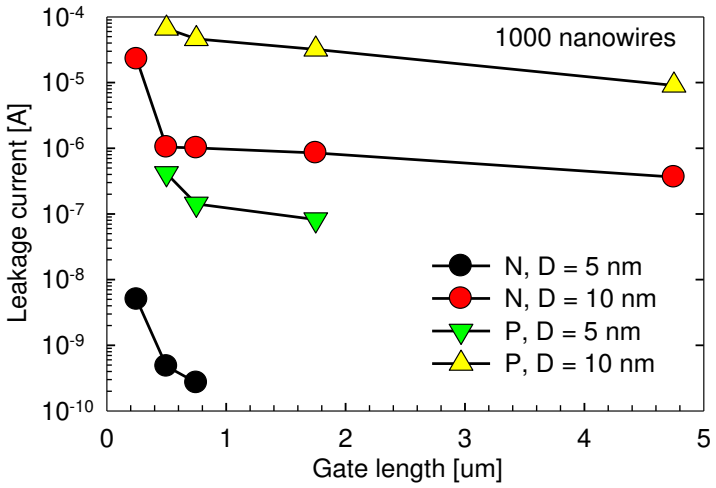


Figure 2.8: Leakage current vs. gate length for N- and P-type NWFETs.

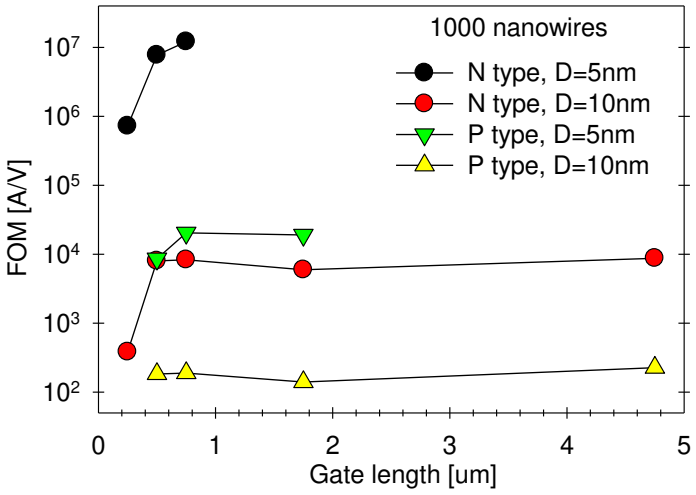
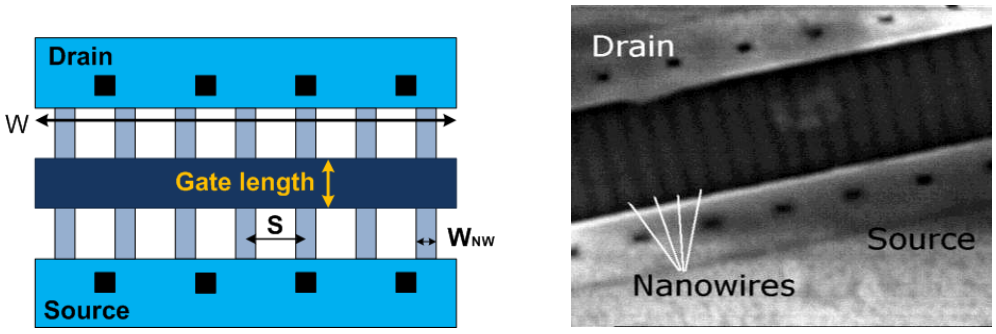


Figure 2.9: FOM vs. gate length of N- and P-type NWFETs.



(a) (b)

Figure 2.10: (a) Simplified layout of multi-channel NWFET and (b) SEM image.

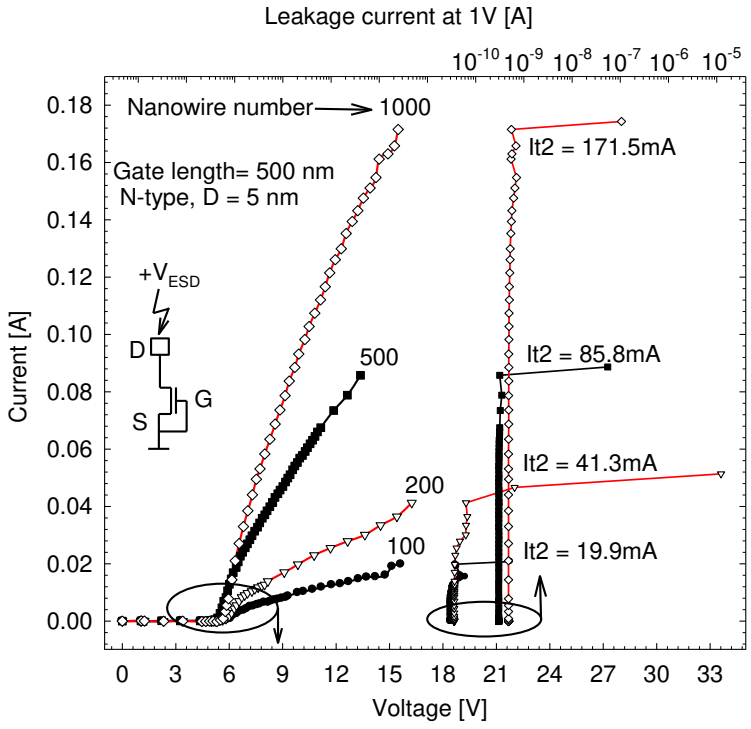


Figure 2.11: TLP curves and leakage currents (measured at 1V) for the bipolar-mode N-type NWFETs with different nanowire numbers.

Multi-channel NWFETs were fabricated to realized high on-state current. Their simplified layout view and SEM photo are shown in Figure 2.10 (a) and (b). In order to study the

ESD performance scalability with the number of nanowires, N-type devices with a 5nm diameter and 500nm gate length (Lg), 100, 500 and 1000 nanowires were characterized in Figure 2.11, where the curves on the right hand side (top abscissa) are the leakage currents measured after each corresponding I-V points plotted on the left hand side (bottom abscissa). The major ESD parameter and FOM calculated by Equation 2.2 as a function of nanowire numbers are illustrated in Figure 2.12. The results suggest that I_{t2} of these devices scales almost linearly with the number of nanowires, at the cost of boosting leakage current as the nanowire number goes higher. The linearity relationship of NW number (N) and It2 can be fitted by Equation 2.3:

$$I_{t2} = 0.166 \times N + 4.9 \quad (2.3)$$

Overall, adding nanowire numbers is an alternative solution to raise FOM of the NWFETs.

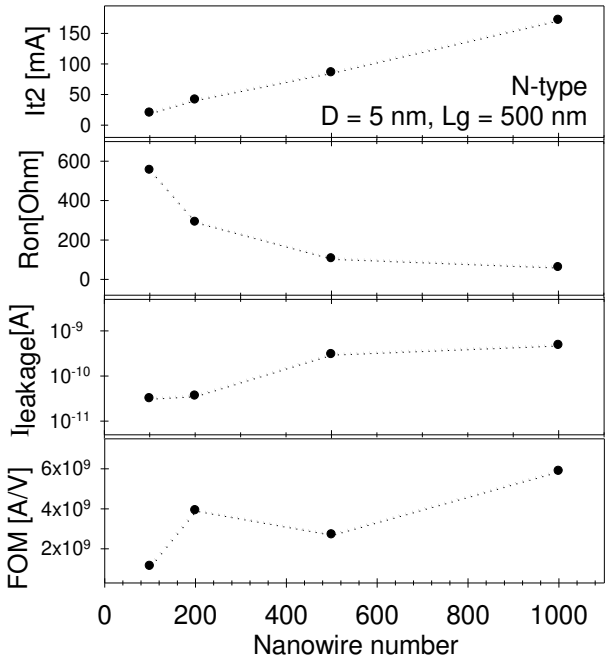


Figure 2.12: ESD performance dependency on nanowire numbers.

To further understand the electric field, carrier density and temperature distributions of the NWFET subject to ESD, 3-dimentianal simulations are carried out using Synopsys TCAD Sentaurus Device Simulation tools [69]. A few solutions are adapted to reduce calculation time and improve accuracy, including simplified 3-D structure (Figure 2.13(a)), incorporation of hydrodynamic model, and application of Noffset3D mesh generation tool with curved surface adaption (Figure 2.13 (b)). TLP equivalent voltage pulses having 10ns rise time and 100ns pulse width are applied to the bipolar mode N-type NWFET with gate length of 250nm, nanowire diameter of 5nm and oxide thickness of 5nm. From Figures 2.14 to 2.17, the cross-sectional distributions of NWFET subject to 14V ESD pulse captured at t=5ns and t=80ns are presented. Noted that Figures 2.14 were obtained by cutting the NWFET at Z=0 and the rest figures come from cutting the device at X=0. The X-Y-Z coordinate is marked in Figure 2.13(a). The simulation results are summarized as follows:

1) In Figure 2.14, the center of nanowire has the highest electron density, proving that quantum effect induced volume inversion existed at bipolar mode [70]. Such phenomenon is favorable for ESD robustness as interface charge trapping could be suppressed due to low electron density at surface.

2) Figure 2.15 suggests that highest electric field exist at the drain side oxide-Silicon interface, making this region most vulnerable to ESD.

3) The profiles shown in Figure 2.16 indicate that drain-nanowire-junction, source-nanowire-junction and near-surface area of nanowire are the major regions for impact ionization and carrier multiplications.

4) In Figure 2.17, peak temperature can be found near drain-nanowire-junction. The heat sink consisting of nanowire, gate oxide and gate implies that heat dissipation of NWFET could benefit from the surrounding-cylinder gate structure and better thermal performance is expected from such gate-all-around devices comparing to planar MOSFET and multi-gate FinFET.

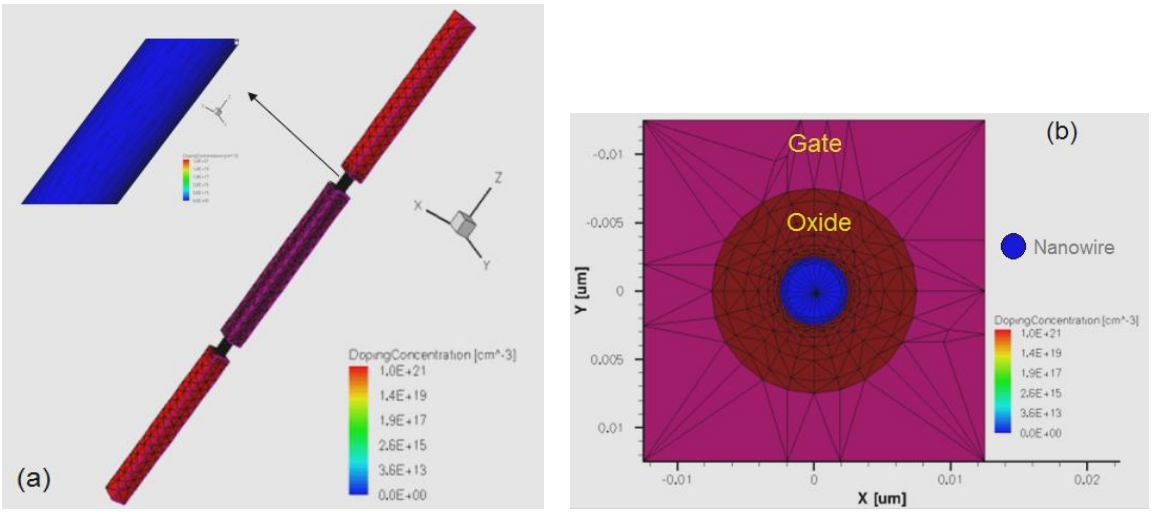


Figure 2.13: (a) Simplified 3D and (b) cross-section (cut at Z=0) of the NWFET with mesh.

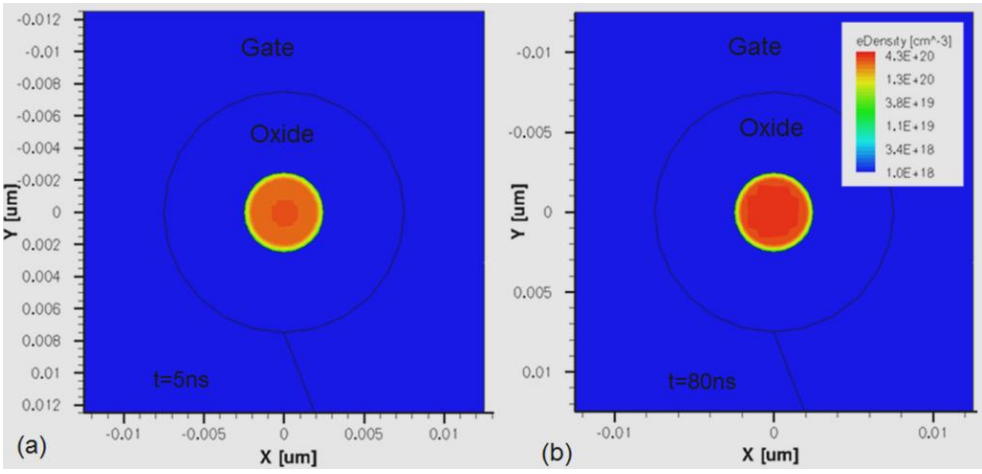


Figure 2.14: Electron density distribution of NWFET at 5ns and 80ns.

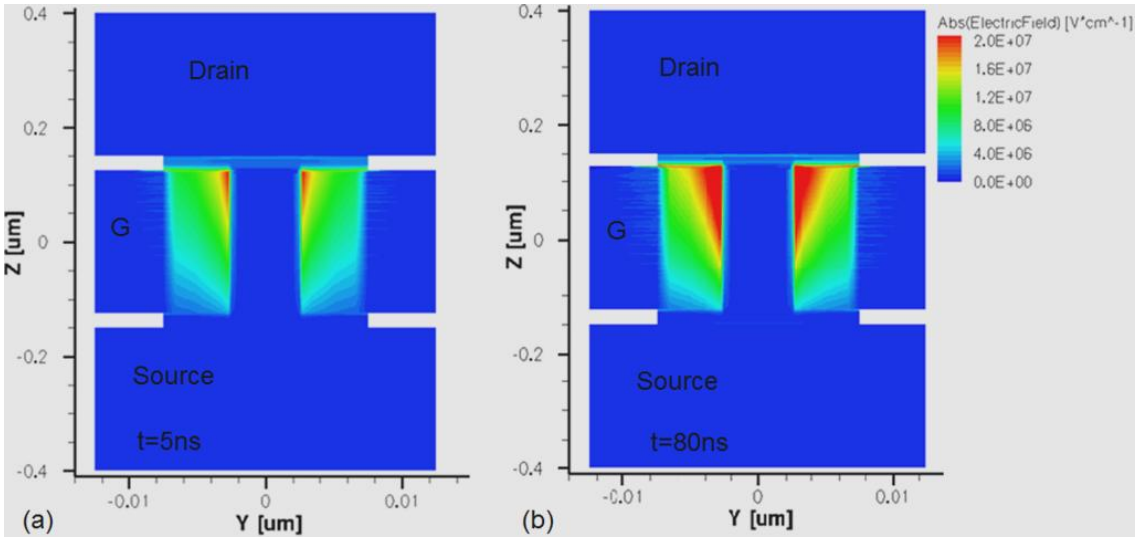


Figure 2.15: Electric field profile of NWFET at 5ns and 80ns.

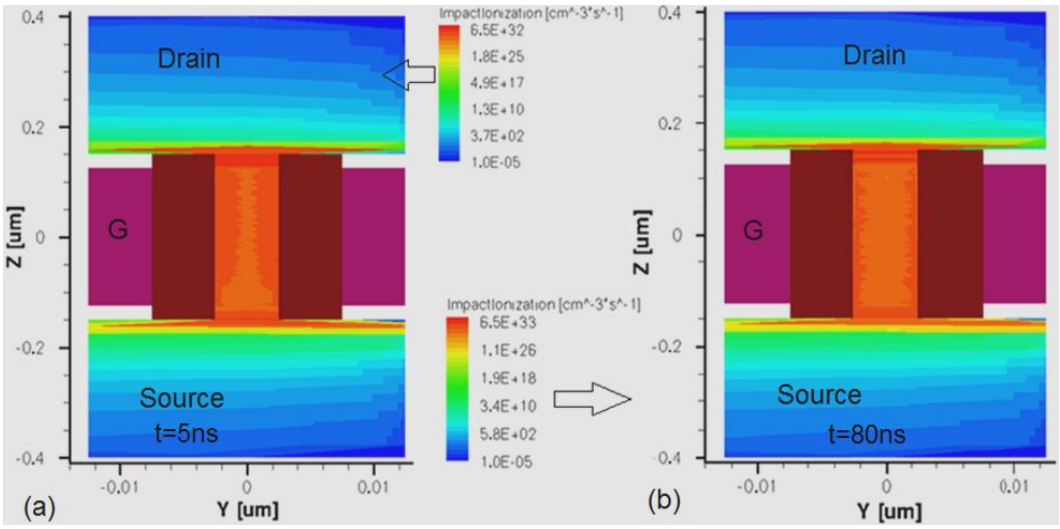


Figure 2.16: Impact ionization profile of NWFET at 5ns and 80ns.

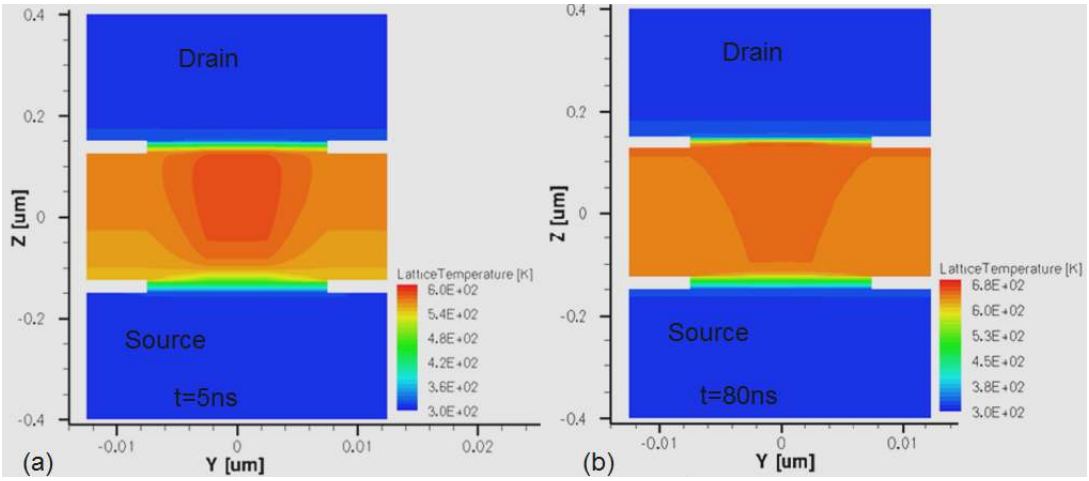


Figure 2.17: Lattice temperature distribution of NWFET at 5ns and 80ns.

2.4 ESD design window

Summarizing the measurement data, the transient safe operation area and ESD design window of NWFET is defined in Figure 2.18. The DC operation voltage of NWFET is below 1.5V. The DC gate oxide breakdown voltage for CMOS technology can be approximated by the equation (2.4) [71]:

$$V_{bd} = t_{ox} \times 1V/\text{nm} \tag{2.4}$$

Given that the oxide thickness of NWFET is 5nm, the gate oxide breakdown voltage is about 5V. Under 100nm ESD-like pulse, the NWFETs with 5nm gate oxide should have a transient gate oxide breakdown voltage of 10V-12V [1, 27, 72].

The bipolar mode NWFET triggers above 3.6V without snapback whereas the diode mode NWFET turns on at 0.6~1V and several devices need to be connected in series to achieve higher trigger voltage. Further improvements are desired to enhance the failure current and reduce on-resistance.

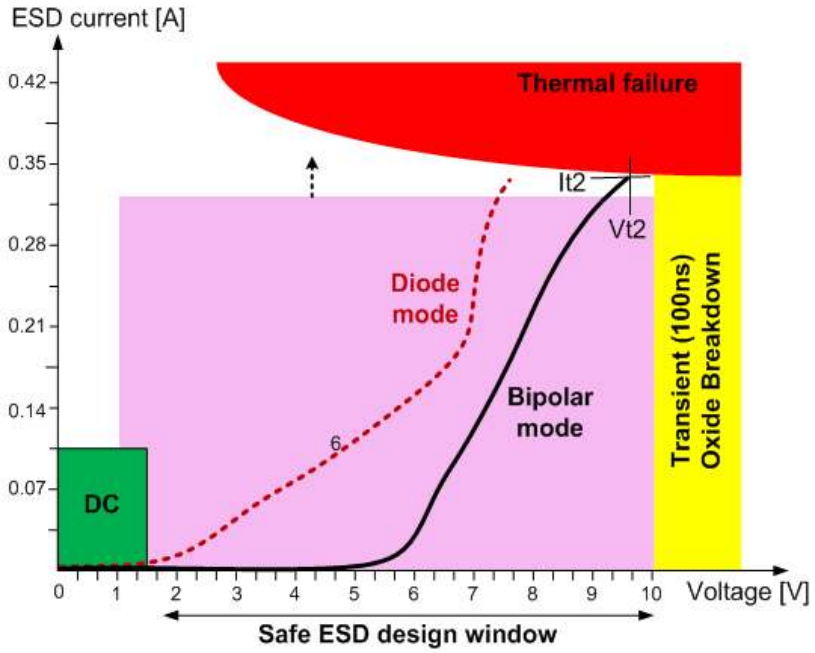


Figure 2.18: ESD design window of NWFETs.

2.5 ESD performance comparison in Nanowire, FinFET and modern CMOS technologies

We now compare the ESD performances of the NWFETs with those of the devices fabricated using other modern technology nodes, such as FinFET, 32nm, 45nm and 65nm SOI/bulk CMOS technologies [36, 37, 65, 67, 73-77], and the results are given in Table 2.2. To obtain a consistent assessment, the devices considered have similar gate lengths. Moreover, because of the different device widths and structures, failure current densities J_{t2}, J_{t2}' and J_{t2}'' are normalized by the effective silicon width, total layout width, and layout area respectively. For NWFET and FinFET:

$$J_{t2} = \frac{I_{t2}}{D \times N} \tag{2.5}$$

$$J'_{t2} = \frac{I_{t2}}{D \times N + (N-1) \times S} \tag{2.6}$$

For planar MOSFET:

$$J_{t2} = J'_{t2} = \frac{I_{t2}}{W} \tag{2.7}$$

where N is the number of nanowires or fins, S is the space between adjacent nanowires or fins, and W is the width of planar MOSFET.

According to Table 2.2, the NWFETs possess higher J_{t2} than all the other devices due to the miniature size and circular cross-section of conduction channels. However, J_{t2}' and J_{t2}'' of the NWFETs are smaller than the planar MOSFETs. This can be ascribed to the relatively large nanowire spacing (400 nm), which gives rise to a larger NWFET layout width and area. In addition to reducing the nanowire spacing, multi-finger-multi-channel layout, as shown in Figure 2.19 (only 10 channels shown here, can be more), is capable of reducing more than 21% of effective layout area and facilitating a uniform turn-on of multiple channels, for the NWFET with 100 nanowires, 750nm gate length and 5nm diameter. Such layout topology benefits overall ESD performance and a case study will be discussed in section 3.5.

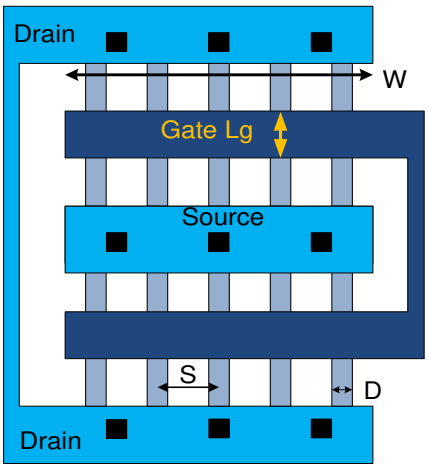


Figure 2.19: Multi-finger-multi-channel layout of NWFET.

Table 2.2: Comparison of failure current densities in various technologies

Technology node	Gate length (nm)	D or W (μm)	J_{t2} (mA/μm)	J_{t2}' (mA/μm)	J_{t2}'' (mA/μm^2)
NW FET	750	0.01	29	0.73	0.24
	250	0.005	33.2	0.42	0.17
	250	0.01	26.2	0.66	0.26
32 nm bulk MOSFET	150 [73]	NA	7~10		2.9~5.4
45 nm bulk MOSFET	260 [74]	240	7.2~11.8		3.7
	240 [75]	240	6.5~11		2.7~4.9 [73, 75]
45 nm SOI MOSFET	40 [37]	468	1.88~4.91		1.4~1.76
65 nm bulk MOSFET	260 [36]	100~400	4~11.8		1.27~3.76
	270 [76]	20	8~15		2.36~3.75
SOI FinFET	250 [65]	0.03	7.5	1.2	0.054~0.108 [77]
	250 [67]	0.02	11.5	1.15	0.938
Bulk FinFET	250 [67]	0.02	6.5~26	0.65~2.61	0.056~0.224

The ESD performances of the NWFET and SOI FinFET, on the other hand, are quite comparable to each other, although NWFETs have smaller channel and larger nanowire spacing. The nanowire cross-section is circular for NWFETs, whereas the channels (fins) in FinFET are

rectangular. Higher electric field and current density exist in the corner areas of the rectangular fins, making the SOI FinFET more susceptible to ESD stress.

2.6 Failure analysis

Although NWFET presents superior current density per effective silicon width comparing to FinFETs and planar MOSFETs, the extremely scaled nanowire size, gate-all-around structure, and multiple channels in parallel make such devices quite sensitive to ESD [78, 79]. Among all the NWFETs characterized, the one with 1000 nanowires, 10nm diameter, and 750nm gate length is the most robust with an I_{t2} of 0.29A (see Figure 2. 6) under bipolar mode, corresponding to an HBM tolerance of 435V (calculated by 0.29A × 1500Ω), a figure lower than typical HBM standard of 500V~2000V for consumer ICs [10]. A thorough understanding of ESD-induced failures in NWFETs is essential at this point to realize effective ESD protection solutions needed for the commercialization of future nanowire-based integrated circuits. In this section, the pre- and post-stress current-voltage characteristics of the NWFETs subject to HBM ESD will be studied, and the mechanisms underlying NWFET ESD failure will be analyzed based on electrical measurements, SEM and TEM observations.

P-type NWFETs fabricated at the Institute of Microelectronics, Singapore, were considered in this study [56]. The devices consist of 1000 nanowires in parallel, each with a diameter of 5nm and gate length of 250nm. The circular (sometimes elliptical) shape nanowires are surrounded by a 5nm SiO2 and NiSi fully silicided metal gate without gate pre-doping. As illustrated in Figure 2.20, the devices were stressed with HBM equivalent pulses generated by the Barth 4002 TLP tester with the gate of NWFET floating. Keithley 4200 semiconductor

characterization system (SCS) was also used for measuring pre- and post-stress DC current-voltage (I-V) characteristics. The gate-floating configuration is considered because it has been used frequently for effective ESD protection applications [80, 81]. Several identical NWFETs were characterized. While some variations on the measured data were observed, all the DUTs suggest consistent reliability trend.

Figure 2.21 shows the pulsed I-V curve and DC leakage current (the curve on the left) of a p-type NWFET obtained from TLP testing. The four testing conditions undertaken, with increasing stress level, are indicated by the N1, N2, N3, and N4 points. N1 is the pre-stress condition, N2 and N3 are the post-stress conditions when the device is still functional, and N4 is the post-stress condition where the pulsed I-V curve ends and device is completely damaged. The device failure is evidenced by the over 5 orders increase of the leakage current after N3 shown in Figure 2.21. For easier description of the experimental procedure, the current causing the device to fail at N4 is defined as I_{t2}.

The complete experimental procedure, as shown in Figure 2.20, is as follows: 1) at N1, the fresh device was first measured using Keithley 4200-SCS to obtain the pre-stress DC I-V curves; 2) TLP stresses were then applied to the device and gradually increased until the pulsed current reached about 1/3 of I_{t2} (i.e., N2); 3) post-stress DC I-V measurements at N2; 4) apply TLP pulses till the pulsed current reached around 2/3 of I_{t2} (i.e., N3); 5) post-stress DC I-V measurements at N3; 6) TLP pulsing again until hard failure occurred (i.e., N4); and 7) post-damage I-V measurements at N4.

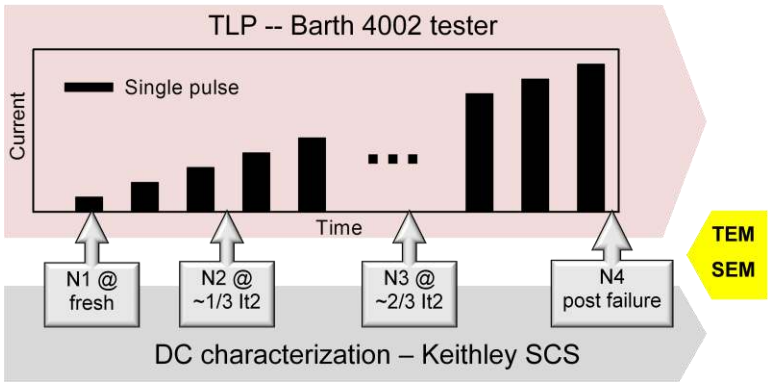


Figure 2.20: Experiment procedure.

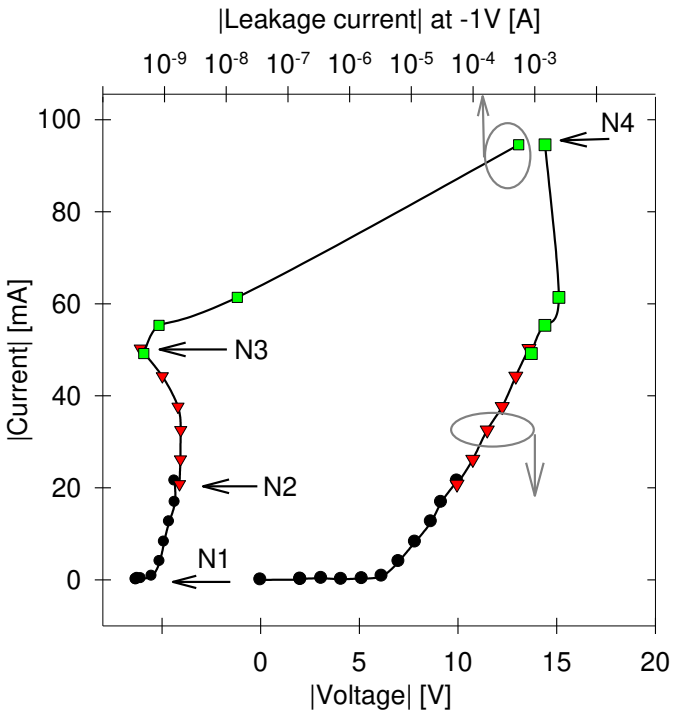


Figure 2.21: TLP I-V (bottom x-axis) curve and leakage current (top x-axis) of a P-type NWFET.

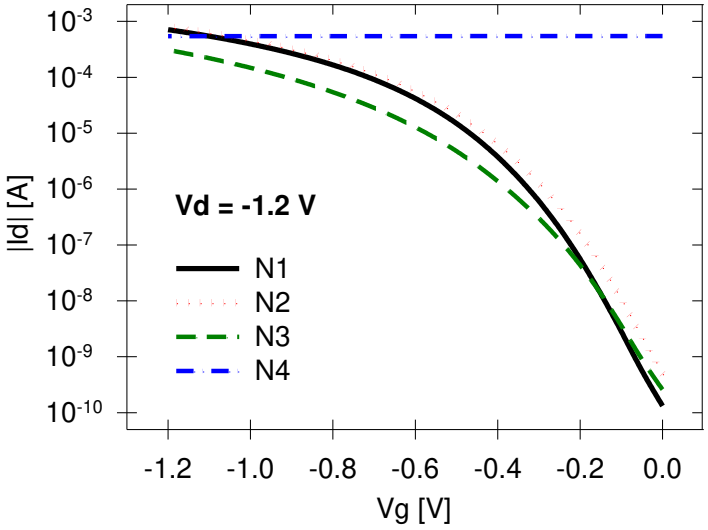


Figure 2.22: Drain current Id vs. gate voltage Vg at N1, N2, N3 and N4.

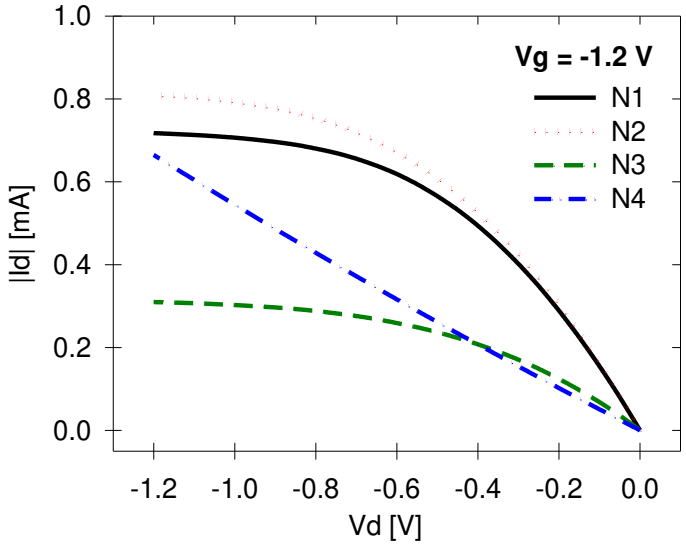


Figure 2.23: Drain current Id vs. drain voltage Vd at N1, N2, N3 and N4.

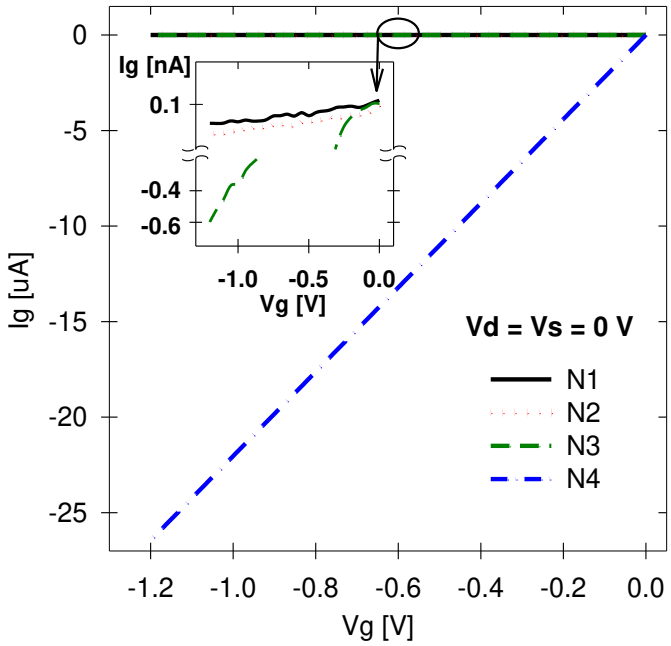


Figure 2.24: Gate current Ig vs. gate voltage Vg at N1, N2, N3 and N4 status, and partial enlarged view (the insert).

According to Figure 2.22 and Figure 2.23, the saturation current at N2, $I_{dsat(N2)}$ can be up to 11% higher than $I_{dsat(N1)}$ at N1, while the gate at N2 still exerts effective control on the channel conduction. The relatively weak ESD stress induces avalanche breakdown that leads to electron trapping in the oxide-silicon interface and drop of threshold voltage |Vth|[82]. Therefore, under the same bias conditions, drain current is increased after the device is stressed modestly. The difference in the post-stress Ig-Vg curves at N1 and N2 (Figure 2.24) stems from the charge trapping / de-trapping in association with the gate oxide defect accumulation and trap-assisted tunneling [83].

At N3, $I_{dsat(N3)}$ is 43% of $I_{dsat(N1)}$ (see Figure 2.22 and Figure 2.23), after the device is subject to the relatively severe stresses. Minor gate oxide degradation is revealed from the Ig-Vg characteristics in the insert of Figure 2.24. This observation, together with the increased threshold voltage |Vth| and reduced transconductance Gm, suggest the occurrence of partial nanowire damage and mild gate oxide degradation [84-86].

At the N4 point where the catastrophic failure takes place, the device behaves like a resistor, having linear Ig vs. Vg and linear Id vs. Vd characteristics shown in Figure 2.24 and Figure 2.23. This implies that current inside NWFET is conducted through the impaired drain-nanowire-source junction and gate oxide.

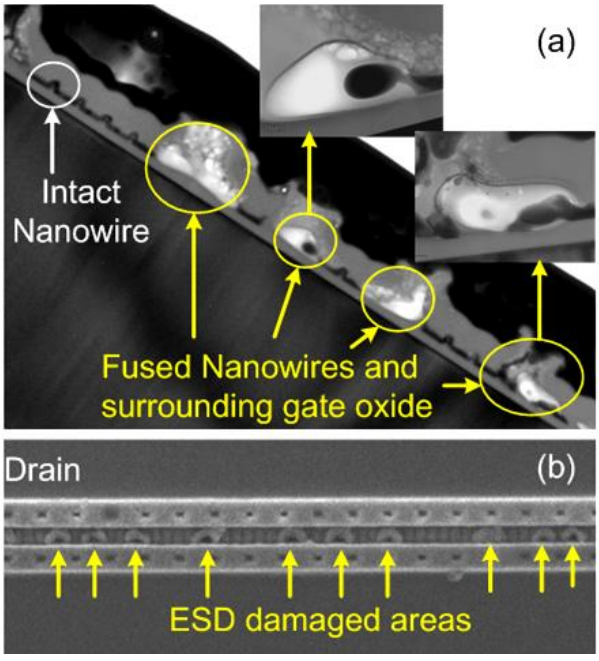


Figure 2.25: (a) TEM cross-section image and (b) SEM surface image at N4.

SEM and TEM were used to analyze the destructive failure at N4. Figure 2.25 (a) and (b) illustrate the TEM cross-section image and SEM surface image of the damaged device, indicating the fusing of a large percentage of nanowires as well as the surrounding gate oxide is the main mechanism underlying the ESD-induced failure of the NWFET. The severity of the fusing varies considerably among the damaged areas (see circled areas in Figure 2.25(a) and arrow pointing regions in Figure 2.25(b)). This is due to the non-uniform distribution of ESD current among the multiple nanowires. It is worth mentioning that no physical defects could be observed at the N2 and N3 status.

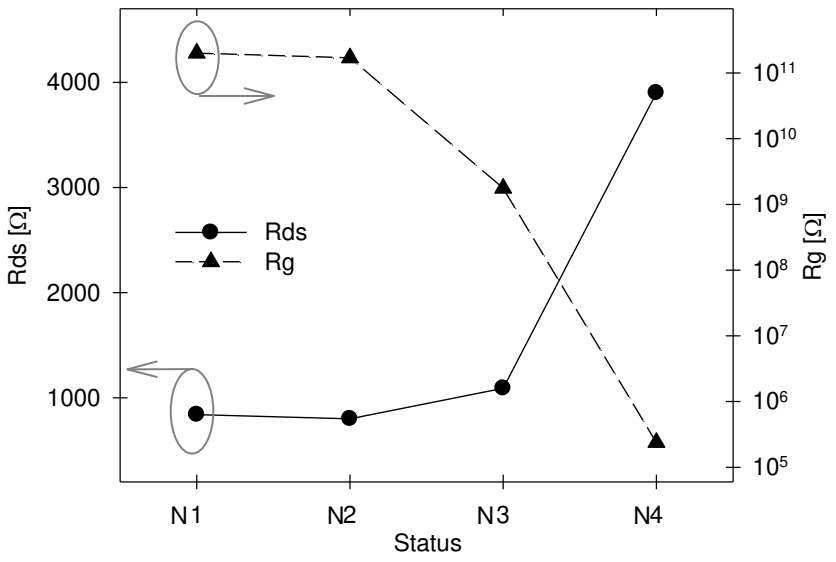


Figure 2.26: Gate resistance Rg and drain-source resistance Rds at N1, N2, N3 and N4.

Calculating the slopes of the Ig-Vg curve and the linear region of Id-Vd curve yields the gate resistance Rg and drain-source resistance Rds, and the resulting Rds and Rg values at N1, N2, N3 and N4 are plotted in Figure 2.26. Soft and hard failures take place after N2 status, when

the ESD stress becomes relatively severe. These data are useful in modeling the NWFET's electrical performance under different ESD stress conditions.

2.7 Conclusion

This chapter provides useful insight into the design and implementation of ESD protection solutions for the emerging nanowire-based technology. Aiming to understand the ESD robustness of gate-all-around Si NWFETs, the layout parameter dependency is investigated experimentally and FOM is proposed. It is found that adjusting the gate length, nanowire diameter, and nanowire number is an efficient and simple way to design NWFET with optimal ESD performance to meet the ESD design constrains and targets.

Comparing to FinFETs and planar MOSFET, NWFET offers highest failure current density normalized by effective silicon width, thanks to the circular cross-section and miniature diameter of the nanowire channels. Nevertheless, the ESD robustness of NWFET is still below typical HBM standards when 1000 nanowires are connected in parallel. Multi-finger-multi-channel layout topology is an effective solution to improve area efficiency and ESD robustness without changing fabrication process.

By experimentally investigating the reliability and failure mechanisms of NWFETs subject to HBM ESD event, it is discovered that nondestructive nanowire burn-out and mild gate oxide degradation occurs under a modest ESD stress, and destructive fusing of nanowires and surrounding gate oxides gives rise to catastrophic failure under severe ESD stresses.

CHAPTER 3 ESD ROBUSTNESS OF POLY-SI NANOWIRE THIN-FILM TRANSISTORS

3.1 Device structure and process

In this chapter, the poly-Si nanowire thin-film transistor (NWTFT) fabricated by National Chiao-Tung University, Taiwan, is studied [87]. Such a process bears the advantages of simple fabrication flow, reliable contact, low cost, and precise alignment of nanowires [88]. The major fabrication steps are illustrated in Figure 3.1. N+ poly-Si gate is sandwiched between Nitride layers (Figure 3.1(a)), which act as etchant barrier to preserve the rectangular shape of nanowires in later steps. The gate was then etched laterally (Figure 3.1(b)) for Si channels self-alignment. Following chemical vapor deposition (CVD) of gate dielectric layer, a-Si layer was deposited and annealed to form poly-Si, after which dopant implantation was applied (Figure 3.1(c)). Poly-Si nanowire and drain/source electrodes are formed afterward by anisotropic reactive plasma etching (Figure 3.1(d)). The structured was completed after top gate deposition and patterning (Figure 3.1(e)). More fabrication details can be found in references [87, 89].

Figure 3.2 presents simplified layout top-view and cross-section views along the nanowire channels, which is illustrated as NW in Figure 3.2(a) with an effective channel length of L. The DC transfer characteristics in logarithm and linear scales of three n-type devices with the following makeup are shown in Figure 3.3: nanowire width of 18nm and height of 60nm, channel lengths of 0.4μm, 1.0μm, and 2.0 μm, n+ polysilicon gate with 10^{21} cm^{-3} doping, gate SiO_2 oxide thickness of 20nm, and S/D doping density of $5x10^{20}$ cm^{-3}.

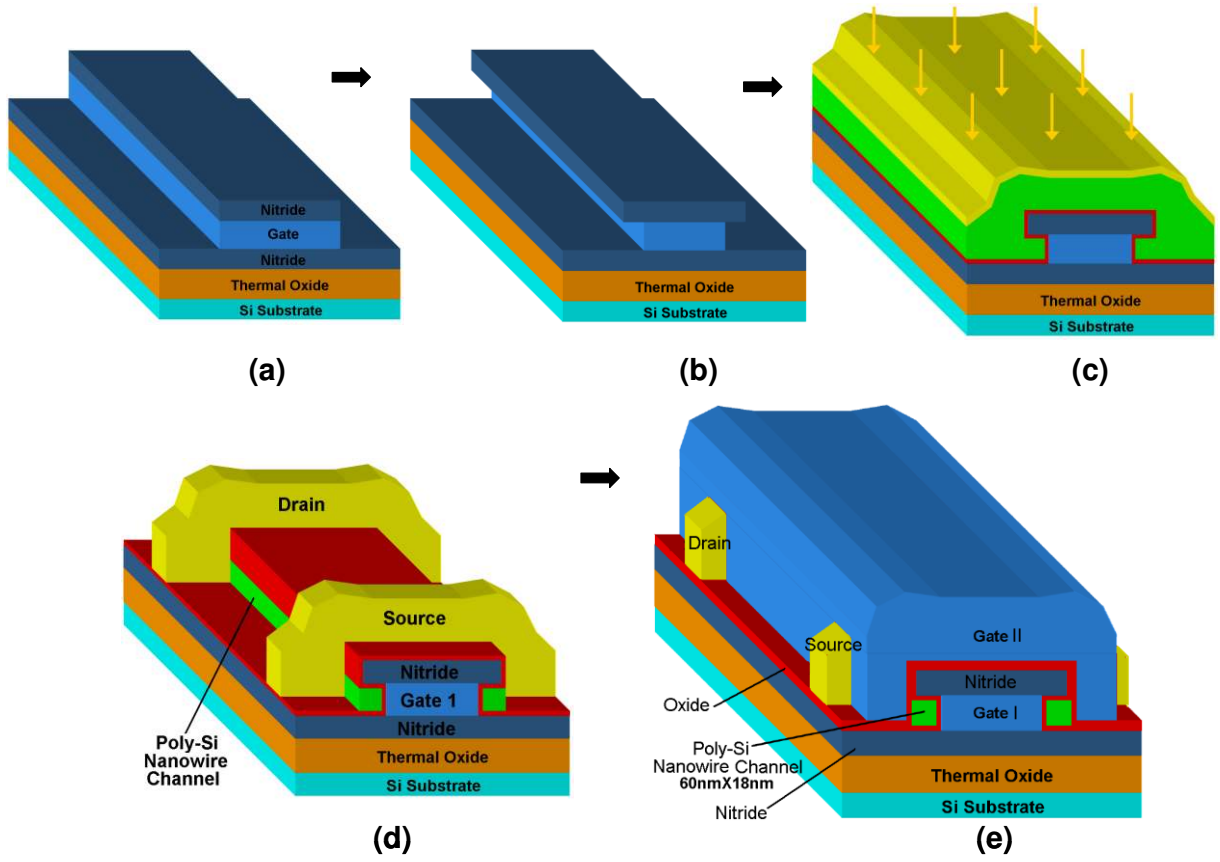


Figure 3.1: Major process flow of the poly-Si NWTFT.

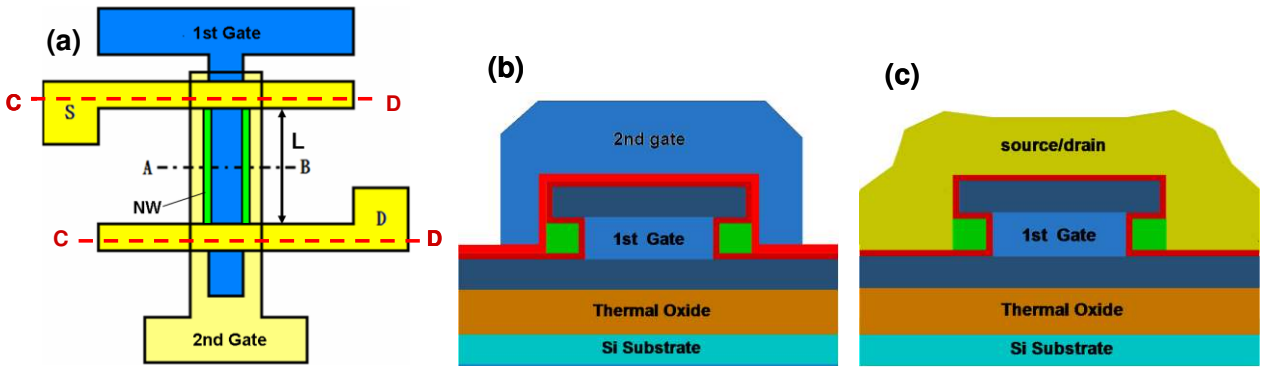


Figure 3.2: (a) Layout top view and cross-section views along black dashed line A-B (b) and red dashed line C-D (c).

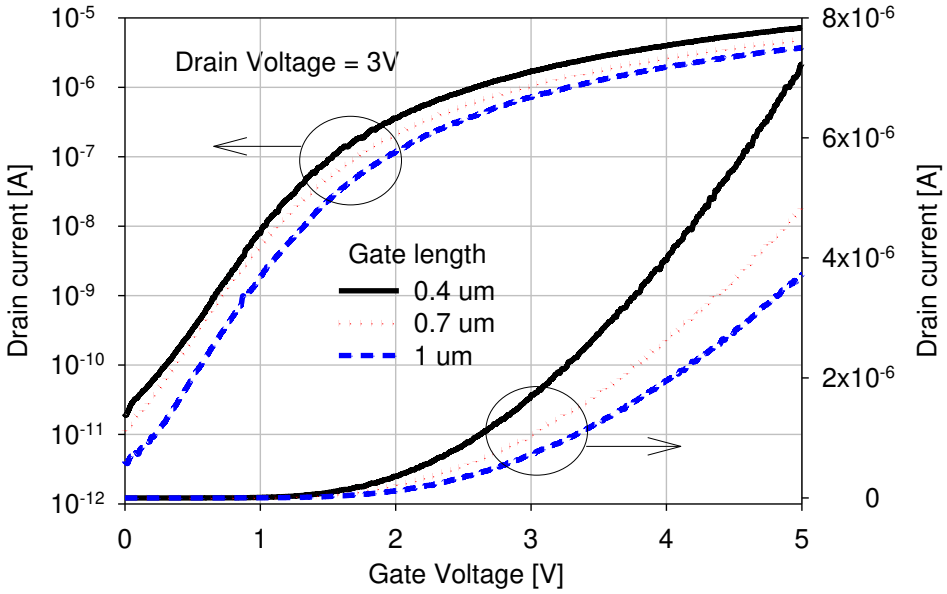


Figure 3.3: Drain current vs. gate voltage of N-type NWTFTs.

3.2 ESD performance characterization and evaluation

N-type NWTFTs having various channel numbers (1, 9, 25, 50, 100), channel lengths (0.4µm, 0.7µm, 1µm, 4µm), nanowire widths (43nm and 18nm), and a spacing of 500 nm were characterized under both bipolar mode (gate grounded) and diode mode (gate-drain connected). The Barth 4002 TLP tester generating pulses having 100ns pulse width and 10ns rise time was used. The TLP measurement results shown in Figure 3.4 (a-d) are summarized as follows:

(1) In bipolar mode (Figure 3.4 (a-b)), NWTFTs turn on in the voltage range of 10 to 15V without snapback. This is due to the fact that the base terminal of the parasitic BJT imbedded in the NWTFT is floating.

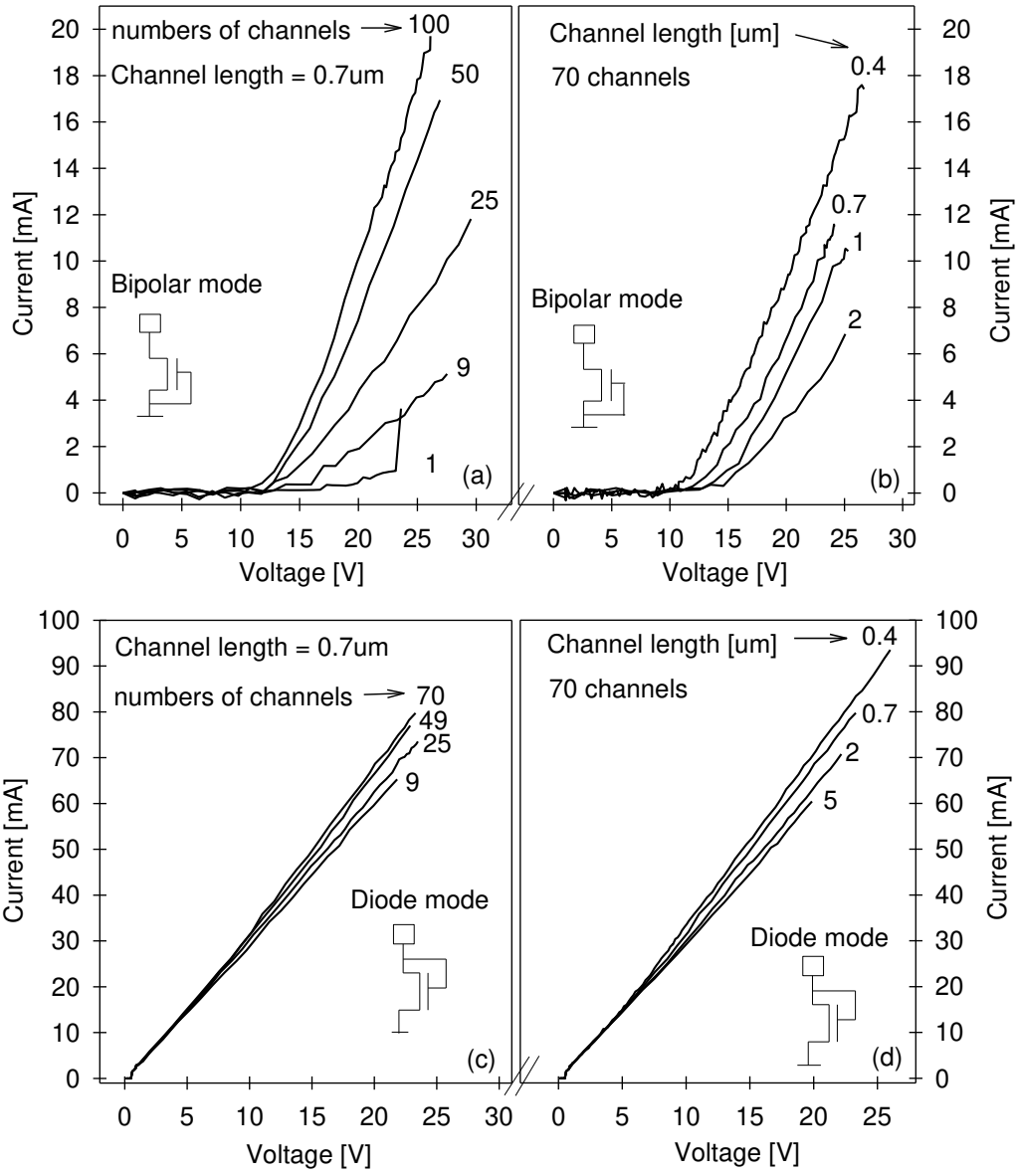


Figure 3.4: TLP I-V characteristics of N-type NWTFTs in bipolar mode (a and b) and diode mode (c and d).

(2) Figure 3.4(b) suggests that shorter channels devices have lower trigger voltage. This can be attributed to the larger size and smaller number of grains inside the shorter nanowires. Shorter channel also means narrower base width and larger β to facilitate the trigger

mechanism. Fewer grains lead to a larger voltage drop in each depletion region and consequently a higher electric field under the same drain voltage, which allows for the impact ionization to be activated at lower voltage. In addition to trigger voltage, shorter channel length results in a higher I_{t2} (the currents where the I-V curves end) and smaller R_{on}. The mechanism underline such trends will be explained in the next section.

(3) In bipolar mode (Figure 3.4(a)), I_{t2} and R_{on} increase and decrease with increasing channel number, but they do not scale linearly with the number of channels. Such phenomenon indicates non-uniform switch of multiple channels.

(4) When the gate is connected to the drain (diode mode in Figure 3. 4 (c-d)), the NWTFT triggers at around 0.6 V and exhibits a linear I-V behavior after triggering. Its failure current is about four times higher than that of the bipolar mode NWTFT thanks to the lower voltage drop and gate-modulated channel conduction.

3.3 Dimension dependency

To further examine the ESD robustness dependency on nanowire dimensions, N-type NWTFTs having wide and narrow nanowires (W=43nm and W=18nm) were measured and compared in terms of I_{t2} and failure current density J_{t2} as a function of channel length, as shown in Figure 3.5, where J_{t2} is calculated by the following equation:

$$J_{t2} = \frac{I_{t2}}{nanowire\ width \times number\ of\ nanowires} \tag{3.1}$$

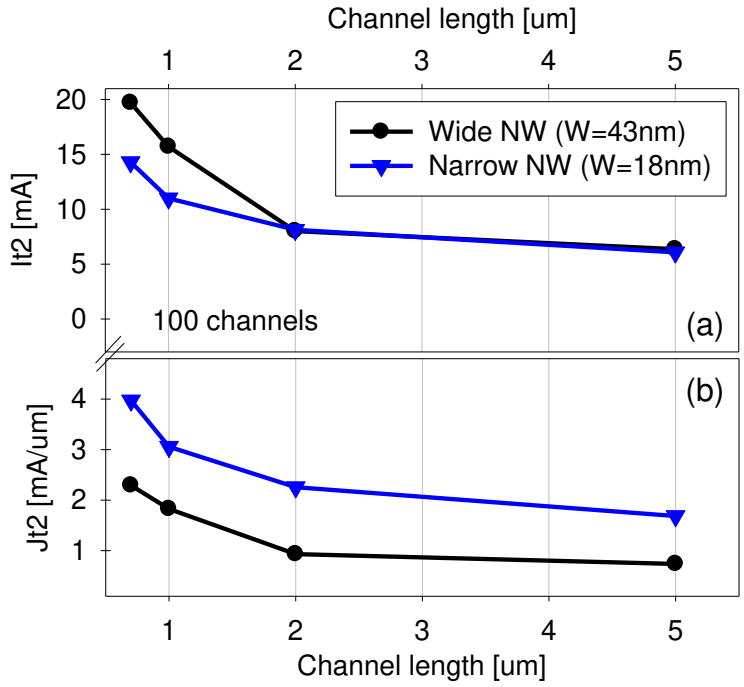


Figure 3.5: Comparisons of (a) I_{t2}, and (b) J_{t2} of the bipolar mode NWTFTs having different channel lengths and nanowire widths.

According to Figure 3.5, shorter channel length leads to higher I_{t2} and J_{t2}. Thanks to the reduced numbers of grains within the shorter nanowires, current conduction takes place deeper in the junction at lowered source barrier potential [90], thus giving rise to a higher I_{t2}. Also, given the same amount of Joule heat that could damage the nanowires, NWTFTs having shorter channel and smaller voltage drop incline to carrier higher currents. In Figure 3.5(b), NWTFT with narrower nanowires exhibits a higher J_{t2} due to the presence of the relatively high resistivity in those narrow channels, a mechanism similar to that of planar GGNMOS imbedded with ballast resistors [41], in which the increased voltage drop across the spreading resistance minimizes the likelihood of filamentation.

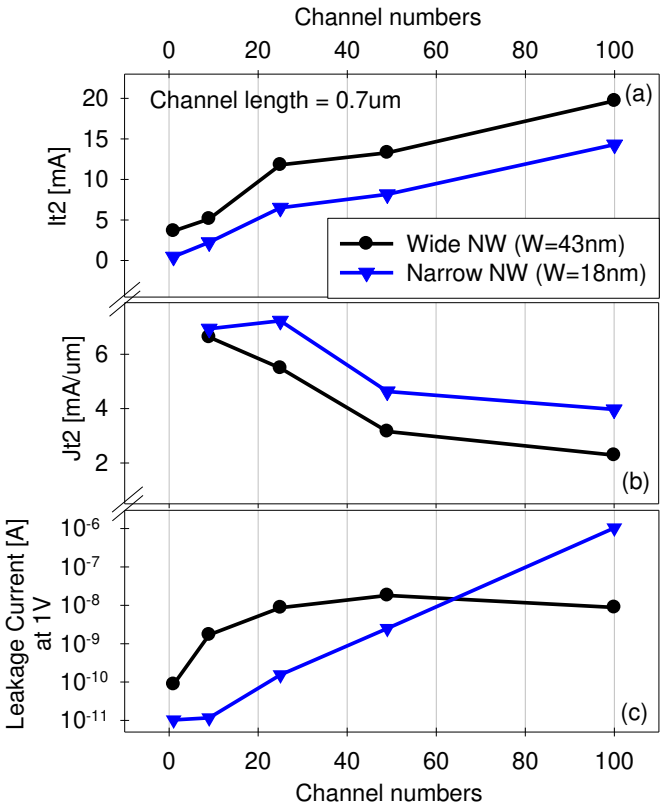


Figure 3.6: Comparisons of (a) I_{t2}, and (b) J_{t2}, and (c) leakage current of N-type NWTFTs having various channel numbers.

The channel number dependency is illustrated in Figure 3.6. Larger number of channel increases the overall I_{t2} but to a lesser extent decreases J_{t2}, a trend confirming that I_{t2} does not scale linearly with the channel numbers. Devices having narrow nanowires present higher J_{t2} shown in Figure 3.6(b), further proving that higher percentage of nanowires are conducting current in narrow nanowire devices than that of wide ones. However, as shown in Figure 3.6(c), the narrow nanowire device with 100 channels has a high leakage current that is too high for ESD protection application.

3.4 Plasma treatment impact

3 hours NH3 plasma treatment at 300℃ was applied to all the devices in the purpose of improving DC performance [91]. However, the results shown in Figure 3.7 suggest that ESD robustness of N-type NWTFT does not benefit from plasma treatment, except for the reduced leakage current.

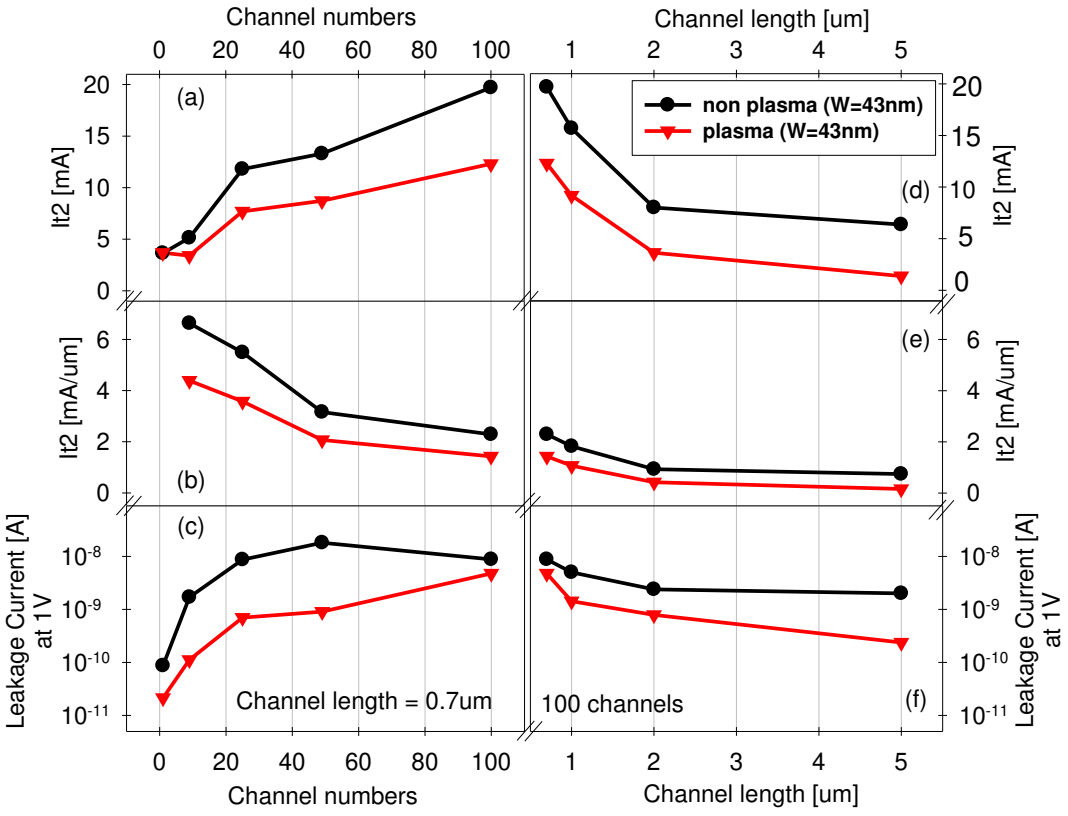


Figure 3.7: Comparisons of (a, d) I_{t2}, (b, e) J_{t2}, and (c, f) leakage current (measured at 1V) of N-type NWTFTs with and without plasma treatment.

Plasma treatment is typically used to passivate the inherent inter-intra grain boundary defects located in the poly-Si to reduce performance fluctuation, DC leakage current and threshold voltage[92]. Nevertheless, it is believed that the nanowires become more fragile after

the plasma treatment, because the hot-carrier endurance and thermal stability degrades after passivation [92]. As the driving forces of ESD performance are avalanche breakdown and impact ionization, the plasma induced degradation reduces the ESD robustness of NWTFTs.

3.5 Layout optimization

Non-uniform current distribution among multiple channels is suggested by the J_{t2} and channel number relationship shown in Figure 3.6(b). This undesirable effect can be minimized by implementing multi-finger drain/source layout topology. Figure 3.8(a-c) present devices having three different drain and source layouts but the same total channel number of 50, and their TLP measurement results are compared in Table 3.1. In the direction from (a) to (c) in Figure 3.8, while the drain and source finger number is increased from 5, 7 to 10, the channel number for each drain and source pair is decreased from 10, 7, to 5. Noted that the black lines denote nanowire channels and the effective layout area is calculated by X×Y.

It is evident that the layout in Figure 3.8(c) yields the highest I_{t2}, lowest leakage current, and smallest effective layout area, followed by the layout in Figure 3.8(b), and the layout in Figure 3.8(a) renders the worst ESD performance. The layout topology shown in Figure 3.8(c) has least number of channels in parallel for each pair of drain and source. Therefore, unevenly distribution of current is less possible to occur for such a layout. Moreover, the higher I_{t2} in Figure 3.8(c) can be ascribed to the longer and less nanowires in parallel that offers better heat dissipation than other options.

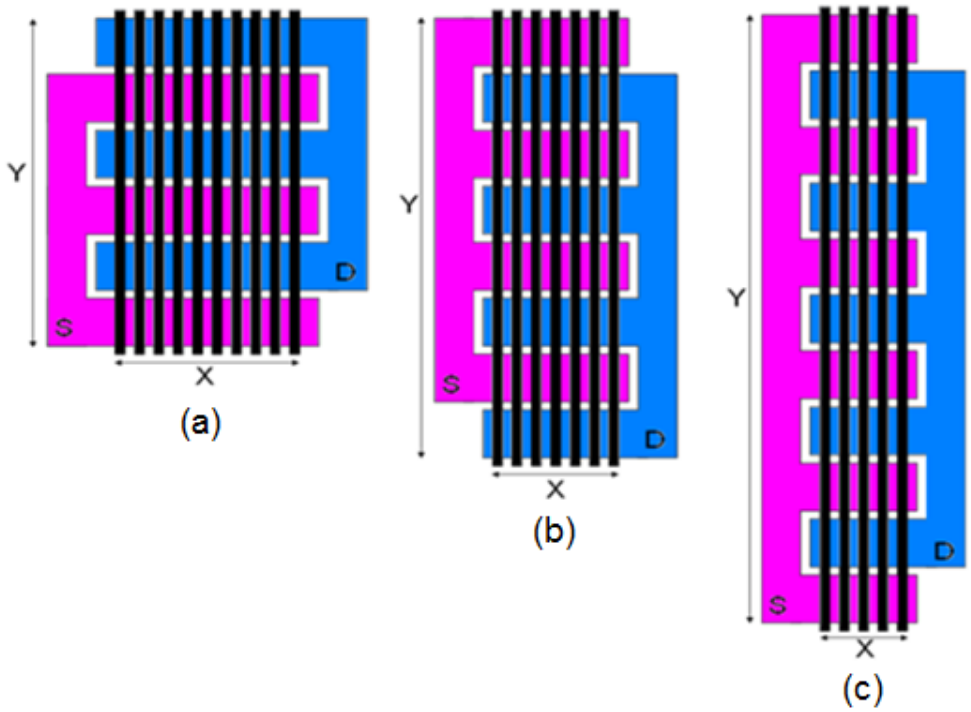


Figure 3.8: Layout topologies of N-type NWTFTs having total channel numbers of 50 but different numbers of drain/source fingers and nanowires in parellel.

Table 3.1: Performances of NWTFTs having the different layouts shown in Figure 3.8(a-c)

Layout topology	Fig. 3(a)	Fig. 3(b)	Fig. 3(c)
Channel number	50	49	50
Drain/source fingers	5	7	10
Number of nanowires in parallel	10	7	5
Failure current I_{t2} (A)	12.5	13.3	16.9
Effective layout area (X×Y) (μm^2)	653	606	589
Leakage current (at 1 V) (nA)	3.84	1.81	0.71

Different from conventional planar MOSFET, the nanowire devices allow further freedom of layout design for performance optimization and silicon property reduction. In addition to raising the total channel number, increasing the drain/source finger numbers with reduced numbers of nanowires between each pair of drain/source is an effective approach to enhance the ESD robustness of multi-channel NWTFTs.

3.6 ESD performances comparison of Poly-Si NWTFT and Si NWFET

We now compare the ESD performances of the poly-Si NWTFT with those of the Si NWFET studied in Chapter 2 and the results are given in Table 3.2. To obtain a consistent assessment, the devices considered have similar make-ups. Because of the different device sizes and geometries, failure current densities J_{t2}, J_{t2}' and J_{t2}'' normalized by the effective channel width, effective silicon area and total width were also examined (see Table 3. 2) and the expressions are listed below:

$$J_{t2} = \frac{I_{t2}}{nanowire\ width \times number\ of\ nanowires} \tag{3.2}$$

$$J'_{t2} = \frac{I_{t2}}{nanowire\ cross\text{-}section\ area \times number\ of\ nanowires} \tag{3.3}$$

$$J''_{t2} = \frac{I_{t2}}{total\ layout\ width} \tag{3.4}$$

The Si NWFET possesses higher I_{t2} and failure current densities than poly-Si NWTFT, owing in part to the circular nanowire cross-section. Higher electric field and current density exist in the corner regions of the rectangular nanowires within poly-Si NWTFT, making such a

device more susceptible to ESD stress. The different trigger voltages found in poly-Si NWTFT and Si NWFET result from the distinct nanowire materials (polysilicon vs. silicon) and nanowire geometries (cuboid vs. cylinder).

Table 3.2: ESD performances of N-type Si NWFET and poly-Si NWTFT having similar gate length and channel numbers

Devices	Si NWFET		Poly-Si NWTFT
NW Dimension (nm)	D= 5	D= 10	W=18
Gate length (nm)	750		700
Channel numbers	100		
I_{t2} (mA)	25.2	37.8	14.3
J_{t2} (mA/μm)	50.4	37.8	7.9
J_{t2}' (A/μm^2)	3.21	1.20	0.13
J_{t2}" (mA/μm)	0.634	0.951	0.73
Trigger Voltage (V)	6.2	5.28	12.9
$I_{leakage}$ (at 1V) (nA)	0.014	2.19	1040
Layout size (μm^2)	121.8		1209
R_{on} (Ω)	689.4	377.6	720.2

3.7 Conclusion

This chapter presents experiment data pertinent to the ESD robustness of a promising nanowire device called the poly-Si NWTFT. The TLP measurement results reveal that these devices are in general suitable for serving as ESD protection elements. The study further suggested that a higher ESD robustness can be obtained by decreasing the channel length and increasing the number of channels. For NWTFTs having a fixed number of channels, improved ESD robustness and smaller area consumption can be achieved by using a multi-finger-multi-channel layout. Plasma treatment commonly used to enhance the electrical performance of poly-Si based devices does not seem to improve the NWTFT's ESD current handling capability. Nonetheless, since the NWTFT-based integrated circuits operating at relatively low operating voltages (i.e., around 1~4 V), the high trigger voltage and low robustness of the gate-grounded NWTFT may impose a great difficulty in implementing ESD protection for future low-power nanowire based integrated circuits. More research work is definitely needed to address these issues, and the diode-mode NWTFT having a trigger voltage of about 0.6V appears to be more attractive for ESD protection applications.

CHAPTER 4 ORGANIC THIN-FILM TRANSISTORS UNDER ESD

4.1 Introduction

Organic thin-film transistors (OTFT) are the building blocks for the emerging large-area, printable, low-cost, and flexible electronics circuits, such as flexible displays, e-papers, sensors, actuators and radio-frequency identification tags [93-96]. Different from conventional ICs, organic circuits are fabricated on flexible substrate by solution based printing and wiring at room temperature, thus simplifies the fabrication process and reduces costs to a great extent. The low power applications of OTFTs plead in favor of a low operation voltage of sub-3V, which attracted a lot of research attention during the past a few years. Among the various solutions, gate oxide made of AlOx and self-assembled alkyl-phosphonic acid monolayer has been proved to be applicable for both low-voltage OTFTs and large scale organic circuits [97].

In terms of reliability study, the DC stress induced degradation and hysteresis behavior of OTFT were investigated thoroughly [98-100], but research on OTFT's performance under ESD is not yet available in the literature and it deserves more attention before the organic technology can be pushed to consumer market. The objective of this chapter is seeking answers for the first time on the following questions: (1) what is the ESD robustness of the OTFT; and (2) how do the relevant parameters, such as the channel width, channel length and gate biasing, affect the OTFT's ESD performance? To this end, OTFTs fabricated at University of Tokyo will be stressed with HBM equivalent pulses generated from TLP tester. These pulses have a 100 ns pulse width, a 10 ns rise time, and a large range of pulse amplitudes. Degradation and failure conditions will be identified by leakage current measured by grounding the source terminal and

applying either a DC bias or a DC voltage sweep to the drain terminal after ESD stresses. All the measurements were conducted under shielded and dark conditions at room temperature.

4.2 Device structure and DC performance

The cross-section schematic and microscope photo of the p-type OTFT considered in this study are shown in Figure 4.1 (a) and (b). Aluminum oxide layer and n-octadecyl phosphonic acid self-assembled monolayer (SAM) are employed as the gate dielectric to accommodate low-voltage operations in the range of 1.5V ~ 2V. The pentacene layer served as p-type conduction channel, and undoped Au and Al layer are evaporated to form drain/source, and gate electrodes, respectively. Detailed fabrication process can be found in [97].

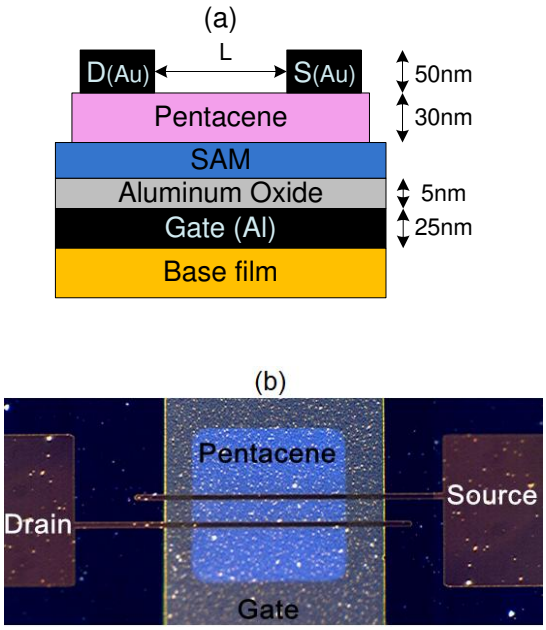


Figure 4.1: (a) Cross-section schematic and (b) top-view microscopy photo of the OTFT.

Comparing to conventional inorganic field effect transistors, the OTFTs operate mostly under accumulation and transportation of majority charge carriers activated by the electric field applied to gate and drain terminals. The DC transfer characteristic (in both linear and logarithmic scales) of the p-type OTFT having a channel width of 500µm and a length of 15µm are illustrated in Figure 4.2. The drain current saturates at micron-ampere and possesses on/off ratio of approximately 5 orders.

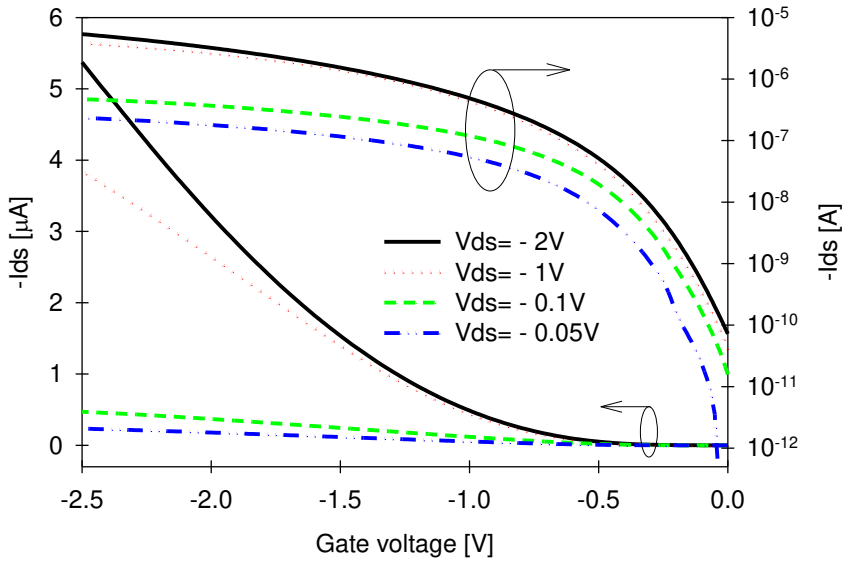


Figure 4.2: Transfer characteristics of OTFT with W/L = 500µm/15µm.

4.3 ESD performance characterization and evaluation

Let us focus on the gate-grounded configuration first, as it is frequently used to investigate the ESD tolerance of MOSFETs [75, 101, 102]. Shown in Figure 4.3 are the current-voltage characteristics of the Si p-type TFT [102] with W/L = 500um/20um and OTFT with W/L = 500um/35um under gate-grounded configuration measured by the 100ns-pulse-width TLP

tester. The voltage at which the current starts to increase sharply is the trigger voltage V_{t1}, and the current at the point where the I-V curve ends is the failure current I_{t2}.

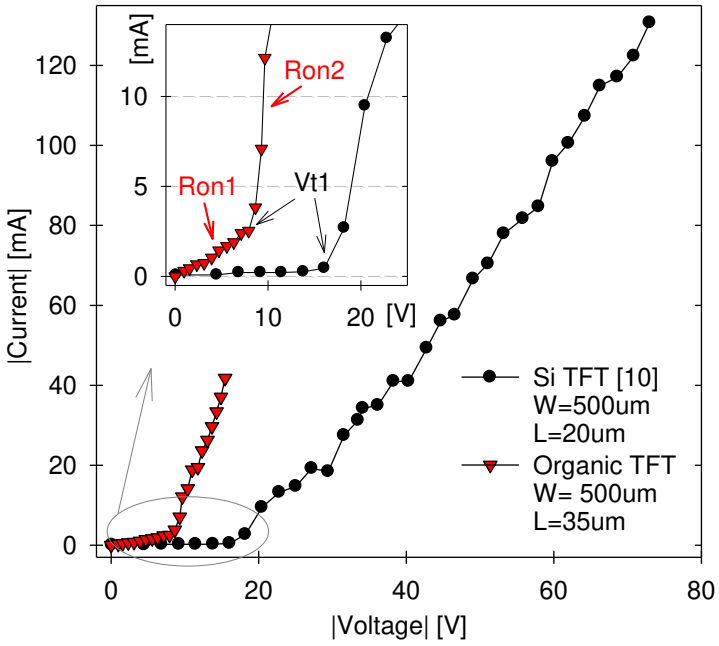


Figure 4.3: Current-voltage curves of OTFT and Si p-TFT [102] measured by TLP tester.

The Si p-TFT exhibits two notable operations: off-state (phase-I) having an extremely large resistance and on-state (phase-II) with a much smaller resistance. On the other hand, the OTFT behaves somewhat differently presenting less distinguishable first and second phases (see insert in Figure 4.3), with phase-I and phase-II resistances of R_{on1}=3126.5Ω and R_{on2}=179.4Ω, respectively. The dissimilarity results from the different drain-channel-source structures: Au/pentacene/Au in the OTFT and p+/poly Si/p+ in the Si TFT. As such, mechanisms including breakdown of organic-metal Schottky junction, electrons injection from drain, and conductivity

modulation of channel govern the transition of the two phases and produce a smaller V_{t1} of OTFT. The OTFT's relatively low R_{on1} is possibly caused by thermionic emission from metallic drain to organic channel and carrier diffusion through depletion region of the leaky Au-pentacene contacts at the drain/source electrodes [103]. The TLP results also indicate that the OTFT is more susceptible to ESD than the Si counterpart, with less robustness (i.e., lower I_{t2}) but quite similar dimension.

4.4 Gate biasing effects

Figure 4.4 (a) and (b) show the TLP pulsed I-V curves and post-stress DC leakage current $I_{leakage}$ of an OTFT having W/L =500μm/70μm in various gate biasing conditions. The major ESD parameters, V_{t1}, I_{t2}, and on-resistances of two phases (R_{on1} and R_{on2}), were extracted from Figure 4.4 (a) and plotted as a function of gate voltage Vg in Figure 4.4 (c), (d) and (e). The charge transport in cross-section view are also demonstrated in Figure 4.5 to assist the illustration of the conduction mechanisms in negative, positive and zero gate biasing conditions.

Figure 4.4 (b) indicates that leakage current increases as gate biasing approaching DC operation voltage (-2V). This can be attributed to the fact that more holes are accumulated when gate is more negative biased and subsequently the channel becomes more conductive during DC leakage current measurement. Besides, the trapped charges at pentacene-oxide interface also enlarge leakage current. The smallest leakage current at Vg=2V suggests that pentacene is quite depleted under positive bias leaving very small amount of accumulated holes for transport.

In Figure 4.4(c), the lowest trigger voltage is obtained when a zero voltage is applied to the gate. Under such a bias condition the least transverse electric field is needed to overcome the perpendicular field, fewest free-carriers are accumulated at the bottom of pentacene, and consequently the metal-organic Schottky junction can be triggered at a smallest drain voltage.

In terms of failure current shown in Figure 4.4 (d), the gate-grounded OTFT renders the highest I_{t2}, thanks again to the lack of perpendicular electric field. Since the carriers are more evenly distributing in the channel, the depletion region got expanded and the effective lateral electric filed is reduced.

By calculating the reciprocal of the slope of the TLP I-V curves, on-resistances at phase-I and phase-II are rendered and illustrated in Figure 4.4(e). Prior to phase-II, highest R_{on1} exists at negative gate biasing and lowest R_{on1} occurs at positive gate biasing. Holes accumulate at the bottom of the channel during negative gate voltage and transient voltage induced carriers have to pass through a longer resistive depletion region. The slightly reduced R_{on1} at positive gate voltage comparing to that at Vg=0V indicates that only modicum holes can be accumulated at positive gate voltage. In phase-II, lowest resistance can be obtained at Vg=0V, followed by Vg=-2V. The zero Vg bias is expected to render best conductivity modulation within the channel, whereas the negative Vg facilitates the accumulation of hole and in turn enhance conductivity of the channel.

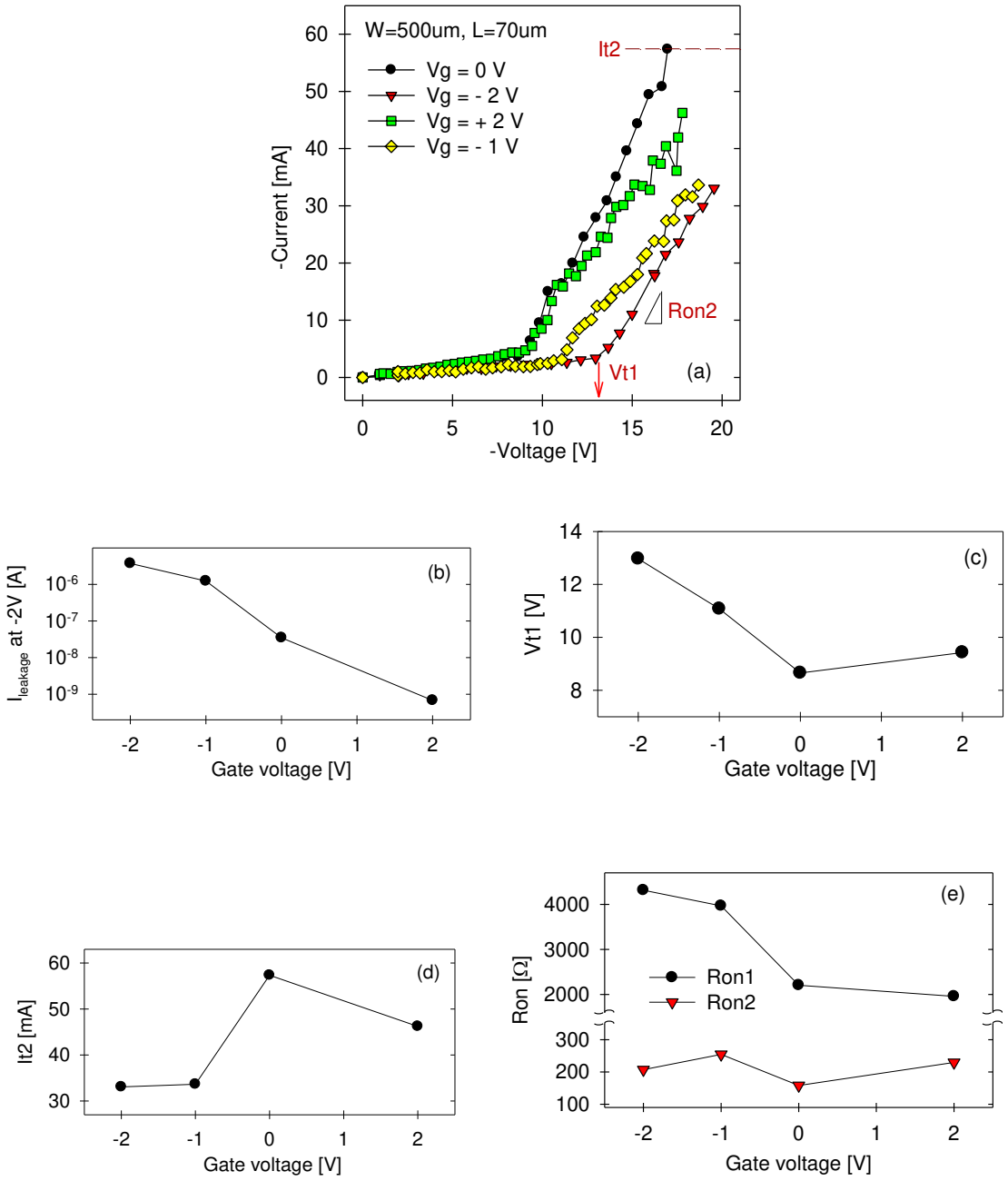


Figure 4.4: (a) Pulsed I-V characteristics of OTFT; (b) post-stress DC leakage current at -2V; (c) V_{t1}; (d) I_{t2}, and (e) on-resistance of phase-I and phase-II (R_{on1} and R_{on2}) under different gate voltages.

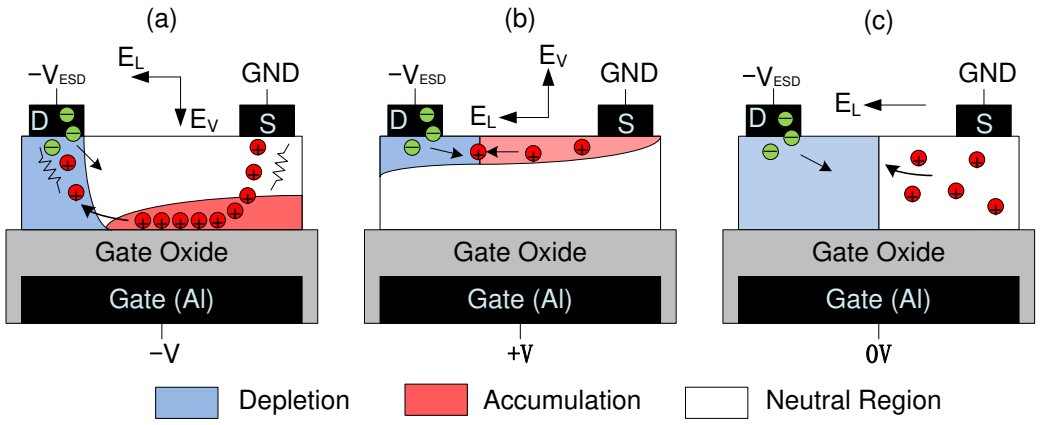


Figure 4.5: Schematic showing the charge transport under different gate voltages.

Comparing the cases of Vg=0V and Vg=-2V, the former yields better ESD performances of a lower V_{t1}, smaller R_{on}, lower $I_{leakage}$, and higher I_{t2} than the latter. These improvements stem from the absence of hole accumulation at the bottom of pentacene layer, reduction of free-carrier trapping at the channel-oxide interface, and minimal vertical electric field when Vg=0V [93, 104] .

Table 4.1 compares the OTFT's pulsed current I_{pulse} and DC current I_{dc} measured under the pulsed (pulse width of 100ns and rise time of 10ns) and DC drain voltages having magnitude of -2V, but various gate voltages. The results indicate an augmented I_{pulse}/I_{dc} ratio as the gate voltage increasing from negative to positive values. Moreover, I_{pulse} does not show obvious change under various gate voltages due to low level charge injection at -2V whereas I_{dc} has a strong dependency on V_g and is the dominate factor of I_{pulse}/I_{dc} ratio. The mechanism of I_{dc} follows the same principal as the leakage current dependency of gate voltage. The large values of I_{pulse}/I_{dc} imply that OTFT is still suitable for constructing self-protection solutions, and those

biased at positive and zero gate voltages provide highest ESD robustness under the same ESD stress condition.

Table 4.1: Drain currents of OTFT under pulsed and DC drain voltage of -2V with various DC gate biasing

Vg (V)	0	+2	-1	-2
I_{pulse} (mA)	-1.43	-1.70	-1.00	-1.43
I_{dc} (μA)	-4.24×10^{-2}	-7.67×10^{-4}	-1.38	-3.19
I_{pulse}/I_{dc}	33582	2213432	728	447

4.5 Dimension dependency

The width and length of the pantecene channel are the major design parameters and their effects on ESD performances are investigated in this section. As shown in Figure 4.6, I_{t2} increases and R_{on2} decreases with the increasing channel width. This is expected, as the larger width gives rise to a higher energy dissipation tolerance and larger conductivity. Nonetheless, the highest I_{t2} of about 0.468A, approximately equivalent to an HBM passing voltage of 700V, obtained from the OTFT with the largest width of 4cm is still too low compared to the industry standard of 2 kV in place for the Si technology. Channel length is another design parameter. OTFTs with a gate voltage of -2V, a width of 500um, and 10 different channel lengths ranging from 35 to 120 um were measured. As shown in Figure 4.7, I_{t2} and DC leakage current reduce slightly as the channel length increases. The same evolution is also found in the gate-grounded OTFTs. The reduced defects in a shorter channel may give rise to a minor improvement in I_{t2}. A

shorter channel responds faster to the injected charges under the ESD stress, thus minimizing the likelihood of localized over-heating near the drain electrode [104].

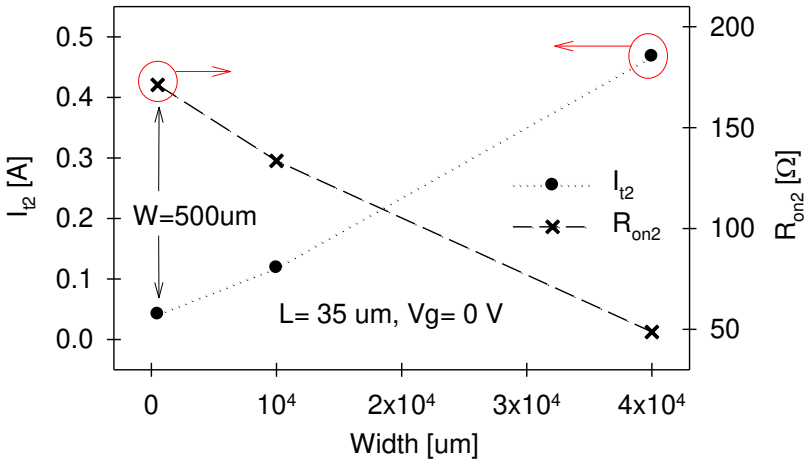


Figure 4.6: I_{t2} and R_{on2} as a function of channel width.

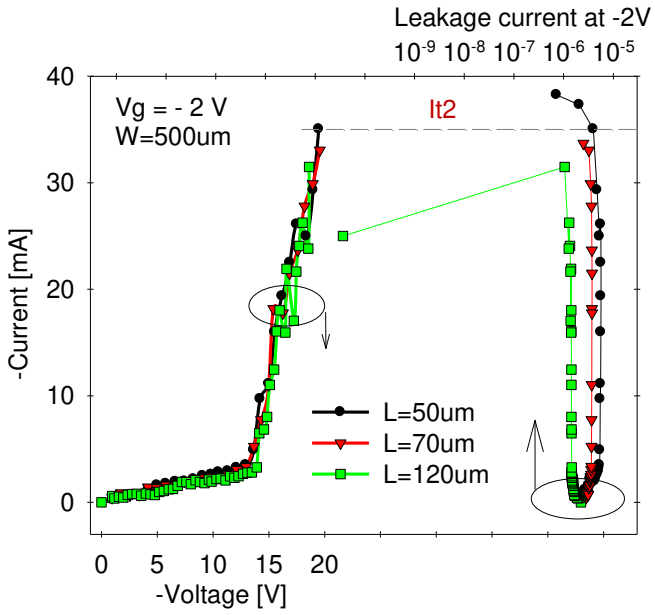


Figure 4.7: Pulsed I-V curves and DC leakage current of OTFTs having various channel lengths.

4.6 ESD induced DC performance degradation and hard failure

To understand the DC performance degradation due to ESD, TLP pulsing and post-stress DC sweep tests were conducted. The measurement procedure as a function of time is demonstrated in Figure 4.8. The OTFT (W/L=500µm/90µm) was kept in the dark at room temperature, and the gate was biased at -2V five minutes prior to the drain-source pulsing. There was a 10-min interval between the two sequential pulsing stresses. This is required to minimize the previous drain bias effect while stabilize the gate stress impact [98]. Following each pulsing stress, a DC sweep (from 0V to -2V) was carried out to measure the post-stress I-V. As shown in Figure 4.9, the post-stress I-V curves did not change notably for pulsing voltages up to -10V. Beyond that, the I-V degradation becomes visible, and the device was eventually destroyed at a pulsing voltage of -14V. It was found that the catastrophic damage took place on the drain electrode, leading to an open connection and zero current conduction. Such an ESD-induced damage is indicated in the OTFT microscopy photo given in Figure 4.10.

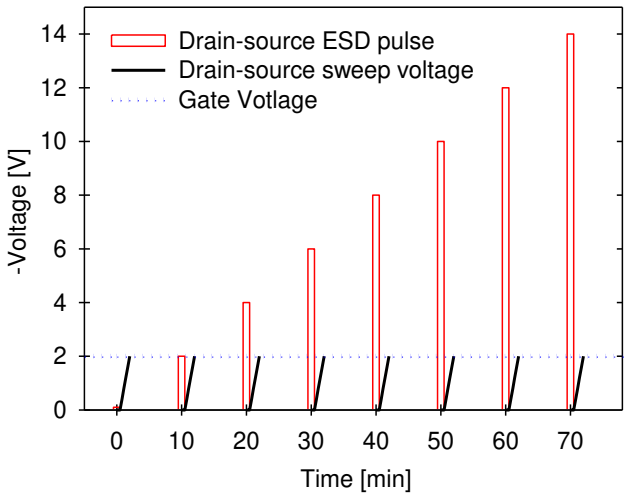


Figure 4.8: measurement procedure as a function of time.

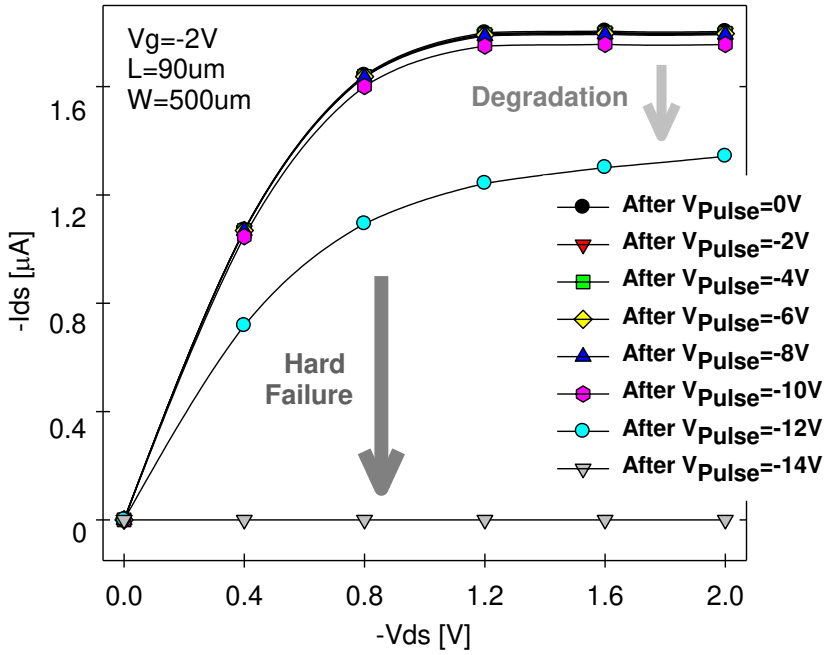


Figure 4.9: Post-stress output characteristics of an OTFT.

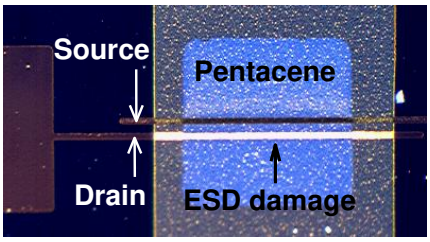


Figure 4.10: Microscope photo of an OTFT with ESD-induced damage on the drain electrode.

4.7 Conclusion

The robustness and behavior of low-voltage pentacene-based OTFTs under ESD events are characterized and analyzed in this chapter. Unlike the conventional Si-based transistors, the OTFTs possess two-phase resistor-like characteristics when subjecting to HBM ESD stresses. The OTFT's ESD performances depend strongly on the gate bias condition, stress level, and

channel width, but are rather insensitive to the channel length. In addition, the OTFT failed at a relatively low stress level with the damage being the metal burn-out on the drain contacts. This chapter renders important insights into the development of effective ESD protection solutions for the emerging organic technology.

CHAPTER 5 DESIGN OF BI-DIRECTIONAL DIODE TRIGGERED SILICON CONTROLLED RECTIFIERS FOR LOW VOLTAGE ESD PROTECTION

5.1 Introduction

The design of bi-directional silicon-controlled-rectifiers (BSCRs) for ESD protection can be dated back to 1999[105]. These devices are capable of conducting both positive and negative ESD currents (PS and NS modes) and are particularly useful for protecting I/O pins that have a varying operating voltage in the positive and negative domains [105-109]. One of the design challenges of BSCRs is to meet the requirement of a small ESD design window for the protection of modern integrated circuits. For instance, ideal trigger voltages of ESD protection devices at input should be lower than 10V and 6V, in 180nm and 90nm CMOS technologies, respectively [27], yet typical BSCRs have a trigger voltage in the range of 14V~16V. An ESD stress with 12V magnitude would damage the gate of input buffer since BSCR fails to turn on at such voltage level. To mitigate the trigger voltage, BSCRs with MOSFET assisted trigger [108] and additional implantation regions [106, 107] have been proposed in the literatures. On the other hand, diode-triggered-SCR (DTSCR) is used extensively for ESD protections [45, 110]. The trigger voltage of the DTSCR can be adjusted by the number of diodes used, hence yielding a relatively small trigger voltage. But the DTSCR has so far been limited to one-directional ESD applications.

In this work, for the first time, we report a bi-directional diode triggered SCR (BDTSCR) for low-voltage ESD protection that offers a narrow voltage window, small parasitic capacitance, good area efficiency, and high ESD robustness in both PS and NS modes.

5.2 Design and layout

The equivalent circuit of the proposed BDTSCR is shown in Figure 5.1(a). The BSCR is composed of three bipolar junction transistors Q1, Q2, and Q3. The diode string consisting of D1, D3 and D5 (three shown here, the number can vary) triggers the BSCR at a relatively small voltage in PS mode. Similarly, the other diode string consisting of D2, D4, and D6 turns on the device in NS mode. These two diode strings will collectively be called the bi-directional diode string (BDS). The current conduction paths for the PS and NS modes are also shown in Figure 5.1.

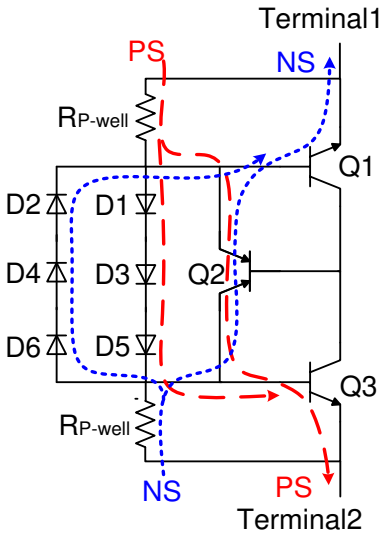


Figure 5.1: Equivalent circuit of BDTSCR with current conduction paths in PS (red dash lines) and NS (blue dotted lines) modes.

Several BDTSCRs were fabricated in a 90nm bulk CMOS technology having P-well, N-well and deep N-well regions. As illustrated in Figure 5.2, the BDS is located in the middle and connected to the P-wells on Terminal1 and Terminal2 of BSCR. The layout of BDS is elaborated

as follows: one pair of anti-parallel diodes is constructed inside each P-well, 4 diodes in the adjacent P-wells are connected in parallel to increase total diode width, and these building blocks are linked in series to form the BDS, whose equivalent circuit is shown in Figure 5.3. The regions forming Q1, Q2 and Q3 shown in Figure 5.1 are listed in Table 5.1. The total width of the BDTSCR is not only determined by the width of BSCR, but also the total number of diodes calculated by n×m marked in Figure 5.3. The key dimensions determining the ESD performance of BDTSCR are D1, D2, D3, and D4 shown in Figure 5.2 and will be discussed in details in the next section.

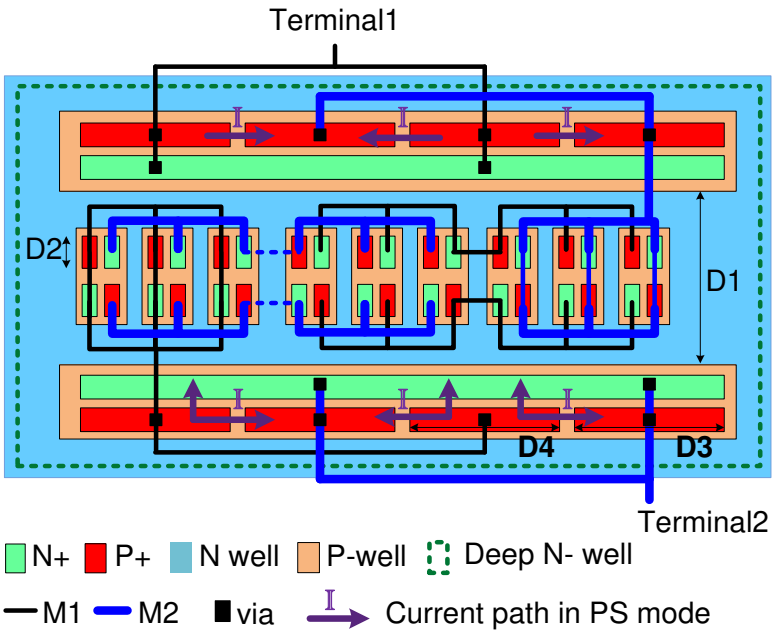


Figure 5.2: Layout topology of BDTSCR having BDS incorporated in the middle of BSCR.

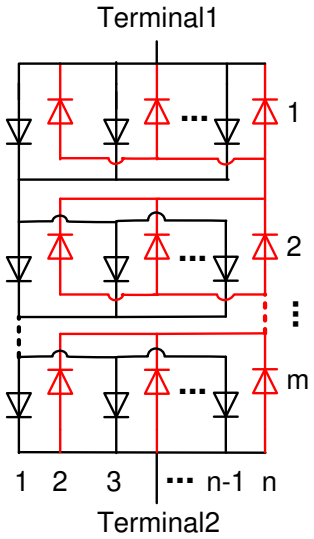


Figure 5.3: Equivalent circuit of the bi-directional diode string (BDS).

Table 5.1: Regions in Figure 5.2 and Figure 5.6 forming Q1, Q2 and Q3 shown in Figure 5.1

BJT	Emitter	Base	Collector
Q1	N+ in upper P-well	upper P-well	N-well
Q2	Upper or lower P-well	N-well	Lower or upper P-well
Q3	N+ in lower P-well	lower P-well	N-well

5.3 Results and discussion

A TLP test system generating pulses with 100ns pulse width, 10ns rise time and continuously increasing amplitude was used to characterize the BDTSCR, standalone BSCR and BDS under the PS and NS modes. Table 5.2 lists the major layout parameters of these devices. As shown in Figure 5.4, the standalone BSCR turns on at ±14V, whereas the BDTSCR triggers at ±4.9V. The partial enlargement of the I-V curves is inserted in Figure 5.4. The much lower failure current I_{t2} of DBS comparing to that of BDTSCR stems from the small diode width of

4μm, indicating that BDS is mainly responsible for triggering of BDTSCR, rather than carrying ESD currents after the BSCR is switched on.

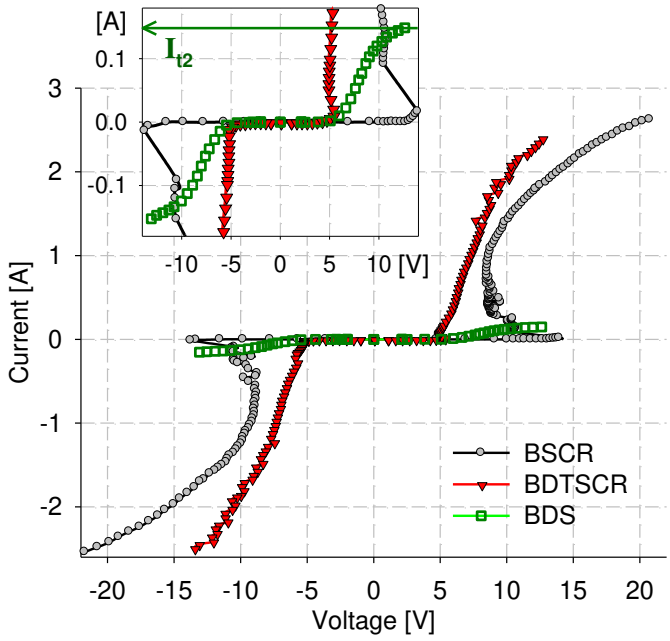


Figure 5.4: TLP I-V curves of BDTSCR, standalone BSCR and standalone BDS.

The trigger voltage $V_{t1,}$ holding voltage V_h, and failure current density J_{t2} of BDTSCRs having different D1 and D2 dimensions are shown in Figure 5.5. The higher J_{t2} and smaller V_{t1} stem mainly from the larger D2, which improves the robustness of diode string and allows higher current to be injected into the base of Q1 and Q3, although the cost of increasing D2 is a larger D1 that leads to higher on-resistance.

Table 5.2: Key design parameters

Devices	BDTSCR	BDS	BSCR
Total Width	68 µm	/	68 µm
Total Diode width in one direction ((n/2)×D2)	4 µm	4 µm	/
Base width of BJT Q2 (D1)	5.46 µm	/	5.46 µm
D3, D4	6.34 µm	/	6.34 µm
Diode number in each string (m)	5	5	0
Number of strings (n)	8	8	0

* D1, D2, D3, D4, m, and n are marked in Figure 5.3 and Figure 5.2.

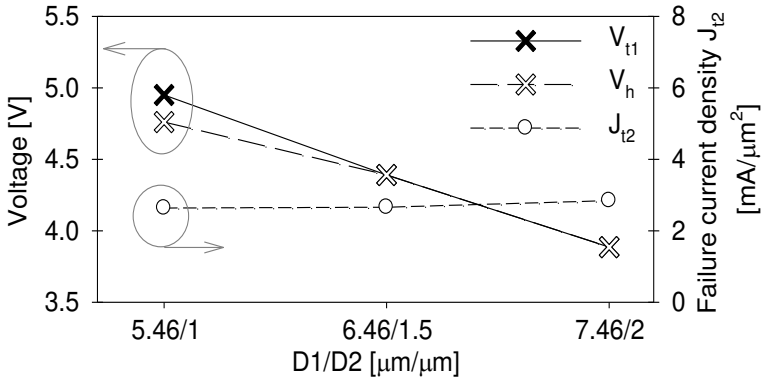


Figure 5.5: V_{t1}, V_h, and J_{t2} of BDTSCRs with different D1 and D2 dimensions.

The D3/D4 ratio (i.e., Terminal1 and Terminal2 segmentations) also impacts the ESD performances of BDTSCR. In addition to the segmentation shown in Figure 5.2 (i.e., with the P+ region segmented), there is an alternative way to segment the N+ implantation regions connected to Terminal1 and Terminal2 as demonstrated in Figure 5.6. Figure 5.7 shows the measured I_{t2}

and R_{on} of BDTSCRs having different D3/D4 ratios and different segmentations. The results suggested that one should use the segmentation in Figure 5.6 and a relatively large D3/D4 value to achieve optimal ESD performances. This is mainly due to the fact that an improved current distribution along the width can be achieved by the layout given in Figure 5.6. Moreover, the enlarged D3/D4 ratio in layouts of Figure 5.2 and Figure 5.6 does not have the same impact over ESD performances because higher ratio in Figure 5.6 increase the emitter width of Q1 and Q3 whereas in Figure 5.2 it only reduces P-well tie area that leads to higher localized current density.

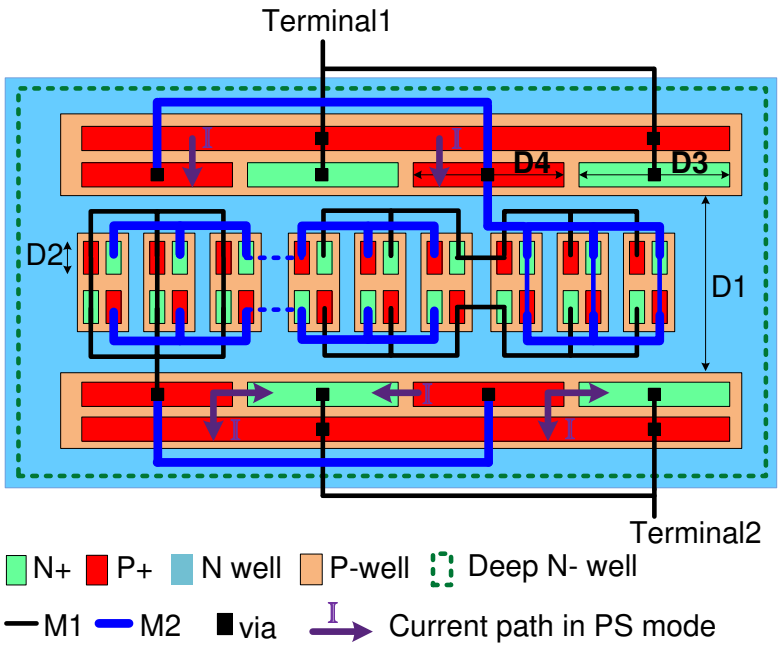


Figure 5.6: Layout topology of BDTSCR with N+ regions segmented.

The parasitic capacitances of the BDTSCR, BSCR and BDS plotted in Figure 5.8 were extracted from S-parameters using standard de-embedding [111]. The comparable capacitances of BDTSCR and BSCR imply that the inclusion of BDS in BSCR does not adversely impact the BDTSCR's suitability for RF ESD protection applications.

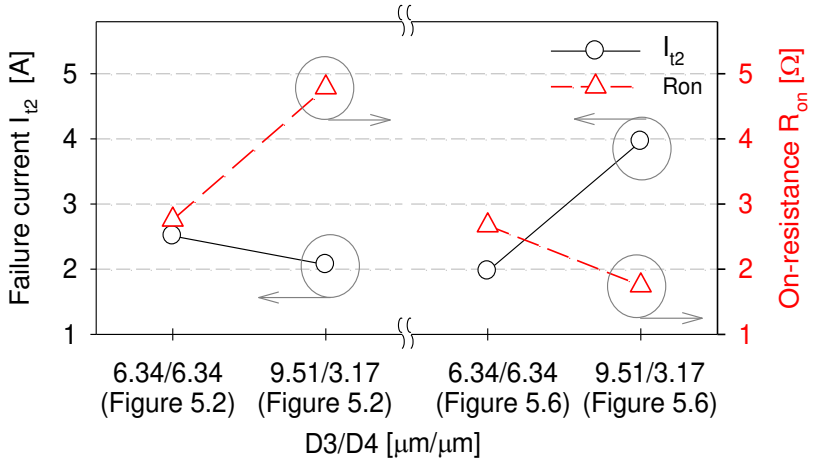


Figure 5.7: I_{t2} and R_{on} of BDTSCRs having layouts shown in Figure 5. 2 and Figure 5.6 with different D3/D4 ratios.

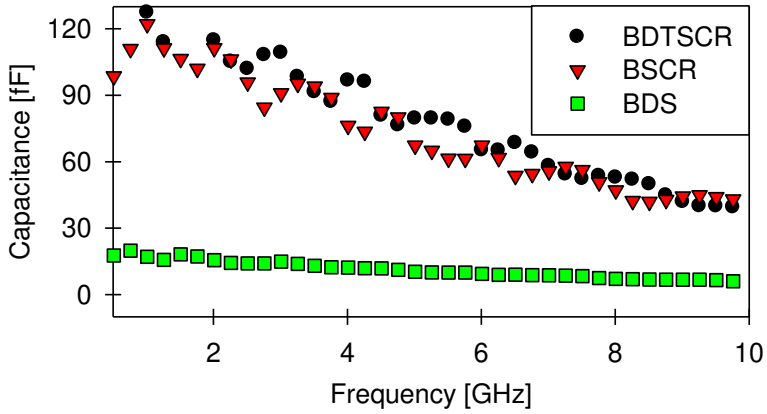


Figure 5.8: Extracted parasitic capacitance of BDTSCR, BSCR and BDS.

The number of diodes used in the BDTSCR is another design consideration to balance the tradeoff between leakage current and trigger voltage [110]. For the BDTSCRs proposed using 4 to 6 diodes, trigger voltages below ±5.5V and leakage currents in nano-ampere range at DC voltage up to ±2V can be obtained.

The HBM robustness, trigger and holding voltages, as well as capacitance of the new BDTSCR and existent BSCRs are summarized in Table 5.3. The comparison clearly demonstrates that BDTSCR is an attractive device for building an effective ESD protection solution that demands bi-directional conduction, narrow design window, small capacitance, and high protection capability.

Table 5.3: ESD performances of BDTSCR and previously reported BSCRs

Device	Ref [108]	Ref [107]	Ref [106]	This work *
Technology	0.18um CMOS	0.6um BiCMOS	0.5um/5V CMOS	90nm CMOS
HBM (mA/μm)	58.2	75	26	58.3
Vt1 (V)	3.8~6.2	10~15	10-14	3.4~5.5
Vh (V)	2.99	3~7.5	> 5	3.2~5.3
Capacitance (fF/μm^2)	~0.14	NA	NA	< 0.095

* BDTSCR with N+ region segmented, D3/D4=3, and D1/D2 between 5.46μm/1μm and 7.46μm/2μm, m=5 and n=8.

5.4 Conclusion

A new ESD protection device, called the BDTSCR, consisting of a bi-directional SCR and diode strings was developed in this study. The effect of layout parameters on the failure

current, on-resistance, trigger voltage and holding voltage were investigated. Data measured from a TLP test system show that the BDTSCR can offer an attractive bi-directional, low-voltage ESD protection with a design window of ±3.4 to ±5.5V, HBM robustness of 58.3mA/μm, and parasitic capacitance below 0.095fF/μm^2. Such a device should be a decent candidate for RF I/O ESD protection and its application can be expanded to power clamp as well.

CHAPTER 6 LAYOUT DEPENDENCY OF DIODE-TRIGGERED SILICON CONTROLLED RECTIFIER FOR HBM AND CDM ESD PROTECTIONS

6.1 Introduction

Diode triggered silicon controlled rectifier (DTSCR) is highly attractive for low voltage CMOS ESD protection applications for its excellent protection efficiency and tunable design window [42, 45, 112]. In such a structure, a diode string is incorporated into the SCR to inject current into the base of parasitic BJT at a relatively low voltage. As a result, a trigger voltage which is much lower than that of a conventional SCR can be obtained. The number and placement of diodes play an important role on the trigger voltage, holding voltage and leakage current of the DTSCR.

There are four typical layout configurations for the DTSCR, as show in Figure 6.1 for the case of four external diodes. They include the diode string connected to the anode and base of the NPN transistor (DTSCR1), to the base of PNP transistor and cathode (DTSCR2 and DTSCR3), and to the base of the PNP transistor and base of the NPN transistor (DTSCR4). To minimize the likelihood of snapback induced latchup in some high V_{DD} applications, one of the diodes (D1) can be inserted between the anode and emitter of the PNP transistor, as in the cases of DTSCR 3 and DTSCR4, or between the emitter of NPN transistor and cathode to increase the holding voltage of DTSCR. Previous works have studied the ESD performance of DTSCRs constructed using one or two of these layouts [50, 110, 113], but a comprehensive comparison of the four different layout configurations is not available.

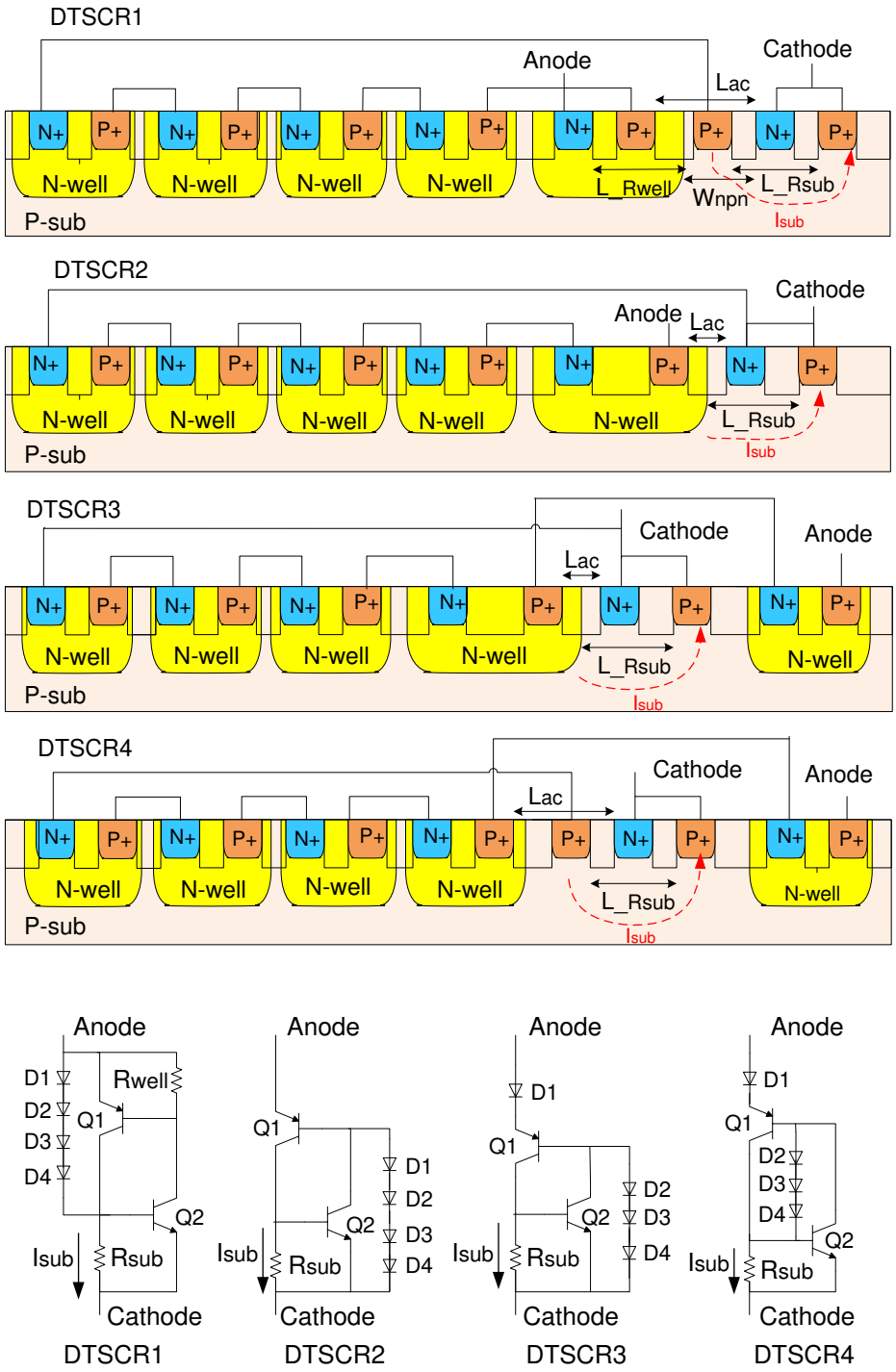


Figure 6.1: Cross-section schematics and equivalent circuits of DTSCRs constructed using 4 typical layout configurations.

In this work, DTSCRs with the four different layouts were fabricated in a 90nm CMOS technology. Their performances subject to HBM and CDM ESD events are characterized using the TLP tester and VFTLP tester. Critical ESD parameters, such as trigger and holding voltages, failure current density, turn on time and voltage overshoot, were extracted from the TLP I-V curves and VFTLP voltage waveforms. Besides the layout dimensions (see Figure 6.1) listed in Table 6.1, same effective width of 50μm and total external diode quantity of four are used for all the DTSCRs

Table 6.1: Layout dimensions of the four DTSCRs

Device	DTSCR1	DTSCR2	DTSCR3	DTSCR4
Total length L_{total} (μm)	25.2	23.2	23.5	25.52
Total width W_{total} (μm)	50.78	50.78	50.78	50.78
PNP base width W_{pnp} (μm)	0.4	0.4	0.4	0.4
NPN base width W_{npn} (μm)	3.1	1.1	1.1	3.1
Anode to Cathode distance (Lac) (μm)	3.5	1.5	1.5	3.5
L_R_{sub} (μm)	3	3.1	3.1	3
L_R_{well} (μm)	2.4	/	/	/

6.2 HBM performance analysis

The DTSCRs and 4-diode-string were first stressed using TLP pulses with a 100ns width and 10ns rise time. Figure 6.2(a) shows the pulsed I-V (bottom x-axis) curves and post-stress leakage current (top x-axis) measured at 1.5V. The I-V curves of the same devices at low current

level are further presented in Figure 6.2(b) to obtain a clear observation of the trigger voltage and holding voltage, which are defined by the voltage when more than 1mA of current is carried and the lowest voltage after triggering, respectively.

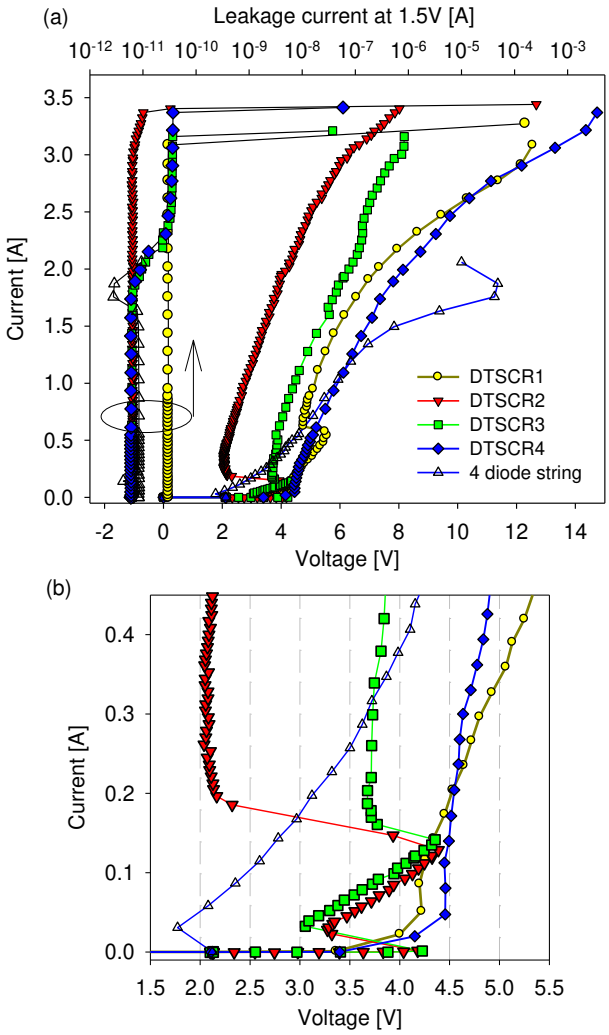


Figure 6.2: TLP I-V curves and leakage currents, and (b) TLP I-V curves at low current level of the DTSCRs and 4-diode-string.

Although all the DTSCRs studied have the same amount of external diodes, the effective numbers of diodes contributing to the triggering of SCR are different. The emitter and base junctions of Q1 in DTSCR2, DTSCR 3 and DTSCR 4 can be counted as another diode that give rise to the trigger voltages and reduce leakage currents under DC biasing. As the trigger mechanism of DTSCR is initialized by forward biasing the base-emitter junction of NPN transistor (Q2 in Figure 6.1), I_{sub}*R_{sub} plays an important role in determining trigger voltage. The four DTSCRs have comparable R_{sub} due to the similar dimension of L_R_{sub}. On the other hand, I_{sub} in DTSCR1 and DTSCR 4 mainly stems from the current injection of diode string whereas I_{sub} in DTSCR2 and DTSCR3 it is dominated by the lateral PNP (Q1 in Figure 6.1) operation and avalanche breakdown of N-well and P-sub. Therefore, the lower trigger voltage of DTSCR1 and DTSCR4 can be attributed to the higher I_{sub} injected by diode string.

The holding voltage of DTSCR depends on current gain of BJT, total resistance and number of holding diodes. Lower holding voltage is demanded to sustain the turn on of BJTs when the gain is higher, which can be achieved by reducing the base width of BJT. Total on-resistance is proportional to the anode to cathode distance L_{ac}. The highest holding voltage shown by DTSCR4 stems from the combined effects of long L_{ac}, wide base width W_{npn}, and the existence of holding diode D1. Owing to the resistance of N-well (R_{well} in Figure 6.1), as well as long L_{ac} and W_{npn}, DTSCR1 has the second largest holding voltage even though the holding diode is absent. The weak or near-absence feature of snapback in DTSCR1 and DTSCR4 mainly arise from the long anode to cathode distance, which is augmented for P+ implantation providing P-sub tie to collect injection current from diode string. As for DTSCR3 and DTSCR2, it can be seen from Figure 6.2(b) that moving one diode from the diode string to the anode, making it as a

holding diode, can increase the holding voltage by ~1V without changing the trigger voltage and on resistance. The unchanged resistance indicates that another current path is generated in DTSCR3 by P+/N-well (D1 in Figure 6.1) and P-sub. This mechanism is further supported by the increased leakage current at 2A for DTSCR3 and DRSCR4, in which the trigger diode D1 is placed on the right hand side and a parasitic BJT is formed. The double snapback feature of DTSCR2 and 3 indicates the sequential turn-on of PNP and NPN transistors.

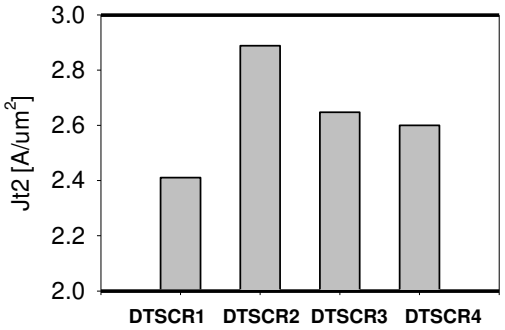


Figure 6.3: Failure current density per layout area of the DTSCRs.

Failure current I_{t2} is defined as the point where the leakage current increases abruptly in Figure 6.2(a). The devices are capable of providing a maximum HBM protecting voltage V_{HBM} = 0.1kV/μm, defined by the product of I_{t2} and a typical human body resistance of 1500Ω normalized by the effective device width:

$$V_{HBM} = \frac{(I_{t2} \times 1.5)\ kV}{50\ \mu m} \tag{6.1}$$

The failure current density J_{t2} is calculated by the following equation and plotted in Figure 6.3:

$$J_{t2} = \frac{I_{t2}}{L_{total} \times W_{total}} \tag{6.2}$$

where L_{total} and W_{total} are the total layout length and width listed in Table 6.1. Because of a longer anode to cathode distance, DTSCR1 and DTSCR4 have smaller failure current densities. On the other hand, DTSCR2 and DTSCR3 can clamp the voltage to a lower level and thus offer a higher protection capability.

6.3 Transient performance investigation

The devices were further characterized using VFTLP system having a pulse width of 5ns and rise time of 0.1ns. The bandwidth of the oscilloscope used in the VFTLP system is 6GHz.VFTLP has been regarded as a valid tool to study transient performance of ESD devices in previous literatures [28, 30, 112]. The parasitic effects of the system are minimized by RF probes and strict system calibrations so that the rising edge of DTSCRs is not affected by the tester parasitic artifacts [114]. Figure 6.4(a) shows the voltage waveform without overshoot of an open calibration at VPTLP pulsing voltage of 9V.

During each VFTLP stress, voltage and current vs. time waveforms were captured. The quasi-static current and voltage of the DUT were obtained by averaging the values between the 25% and 75% time window. The averaged voltage V_{ave} was further used as reference voltage level for the turn on time t_{on}, which is defined as the time from 10% V_{ave} (before voltage overshoot (V_{peak})) to the time of 110% V_{ave} (after V_{peak}), as shown in Figure 6.4 (b) [30]. V_{ave} can also be obtained by linear regression [50], but such a method makes it difficult to determine t_{on} in certain cases and will be discussed in details later on.

The turn on times of DTSCRs and diode strings of 3 and 4 diodes at the current I_{DUT} of 1A, 1.5A, 2A, 3A, and 4A were calculated using the aforementioned method and plotted in

Figure 6.5. The diode strings have the same dimensions as those used for DTSCRs. The overshoot voltages V_{peak} of these devices at different current levels are plotted in Figure 6.6.

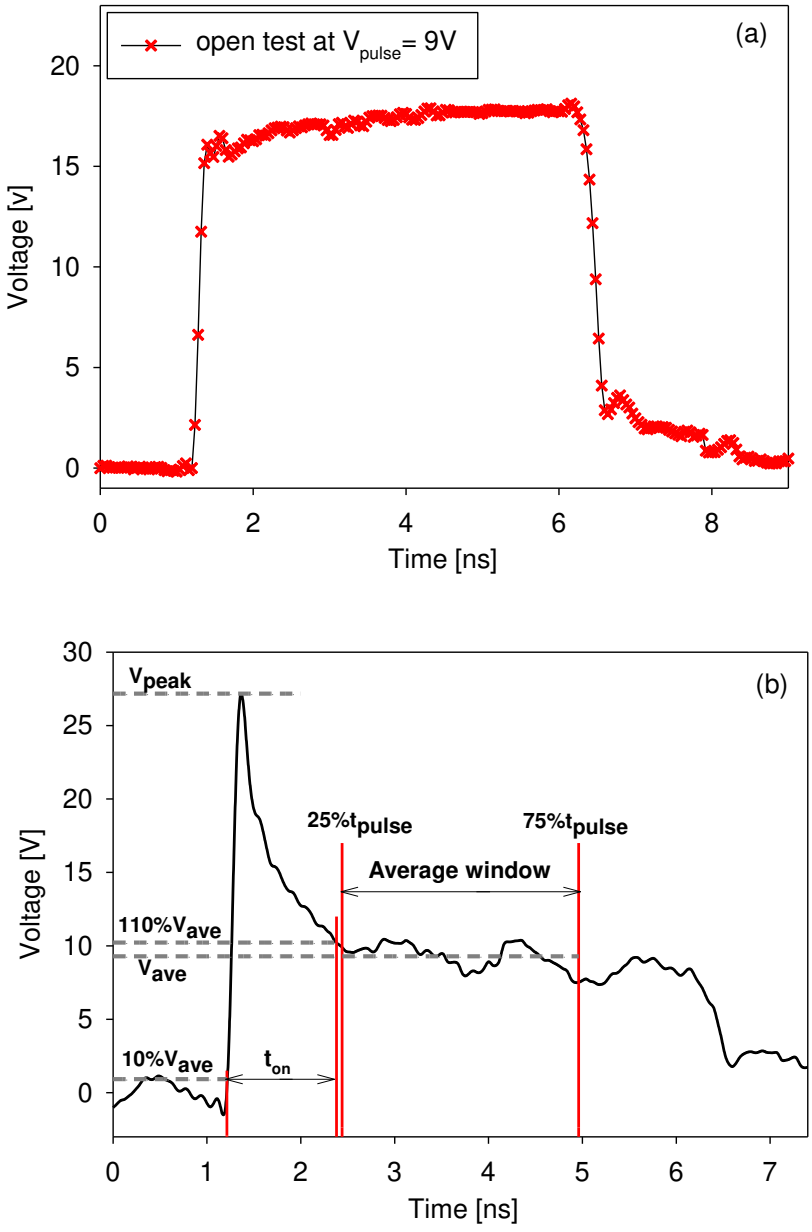


Figure 6.4: Voltage vs. time waveform of (a) open test, and (b) DUT with the definitions for the average window and turn on time t_{on} indicated.

The turn on time of DTSCRs is the combination of the turn on time of diode string, the PNP base transit time τ_{B_PNP}, the NPN base transit time τ_{B_NPN}, and the time to charge the capacitance of base-emitter junction [50]. The base transit times for the NPN and PNP BJTs are defined by [115]:

$$\tau_{B\_NPN} = \frac{W_{NPN}^2}{2D_N} \tag{6.3}$$

$$\tau_{B\_PNP} = \frac{W_{PNP}^2}{2D_P} \tag{6.4}$$

where D_N and D_P are the diffusion coefficients for electrons and holes, and W_{NPN} and W_{PNP} are the base widths of NPN and PNP BJTs. The time to charge a capacitance to the turn on voltage V_{be} of a BJT's emitter-base junction can be expressed as:

$$V_{be} = C \cdot \int_0^t i(t)dt \tag{6.5}$$

where C is the capacitance of the base-emitter junction and i(t) is the dynamic junction current.

The results given in Figure 6.5 and Figure 6.6 can be summarized and explained below:

(1) Turn on time of diode strings does not have strong dependency on the number of diodes. Although the overshoot voltage of 4-diode-string is higher than that of 3-diode-string, the times of reaching V_{peak} are identical for both strings at different stress level, as shown in Figure 6.7. This suggests that diodes connected in series turn on simultaneously rather than one by one [51].

(2) The turn on time decreases as I_{DUT} increases, a trend consistent with equation (6.5). This is because less time is required to charge a capacitance to V_{be} at a higher current level.

(3) DTSCR2 and DTSCR3 turn on faster than DTSCR1 and DTSCR4 due to the smaller base width of NPN BJT, suggested by equations (3) and (4). The similar t_{on} of DTSCR2, DTSCR3 and diode strings indicates that the turn on mechanism in DTSCR2 and DTSCR3 is dominated

by the diode strings. On the other hand, for DTSCR1 and DTSCR4, the base transit time plays a major role on the total t_{on}. DTSCR2 has lower V_{peak} and sligher lower t_{on} than DTSCR3 thanks to the higher voltage available at the base of PNP that helps NPN switch on faster.

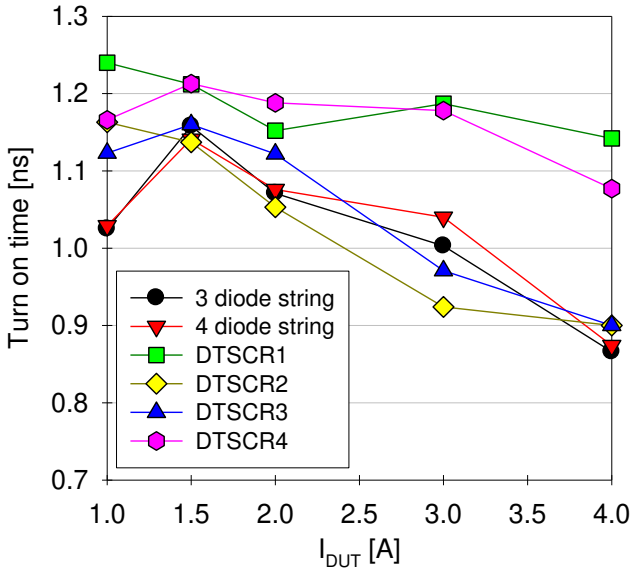


Figure 6.5: Turn on time as a function of quasi-static current I_{DUT} for diode strings and DTSCRs.

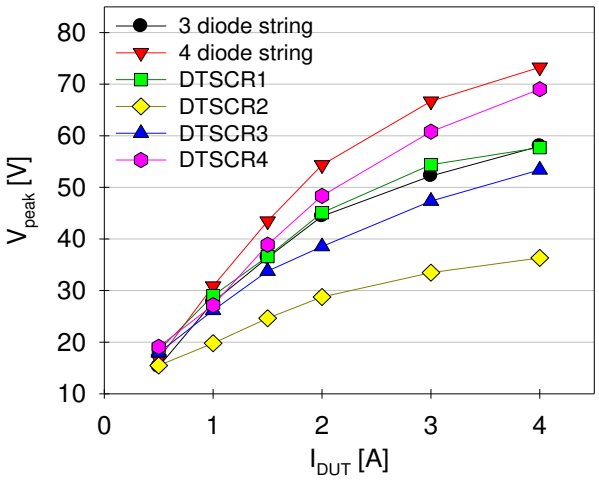


Figure 6.6: V_{peak} as a function of I_{DUT} for diode strings and DTSCRs.

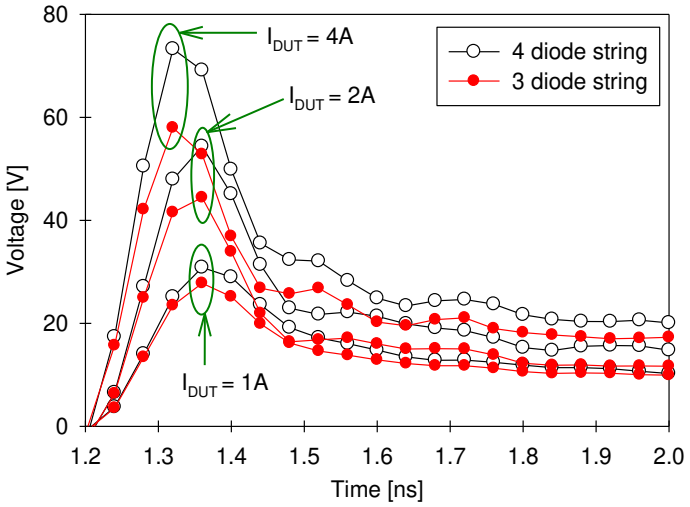


Figure 6.7: Voltage vs. time waveforms of 3 and 4 diode strings at I_{DUT} of 1A, 2A and 4A.

(4) All the DTSCRs are capable of clamping the overshoot voltage to a level lower than that of the 4-diode-string, suggesting that SCRs and parasitic BJTs start to carry current before the DTSCRs fully turned on, as the voltage overshoot takes place during the turn on process [28].

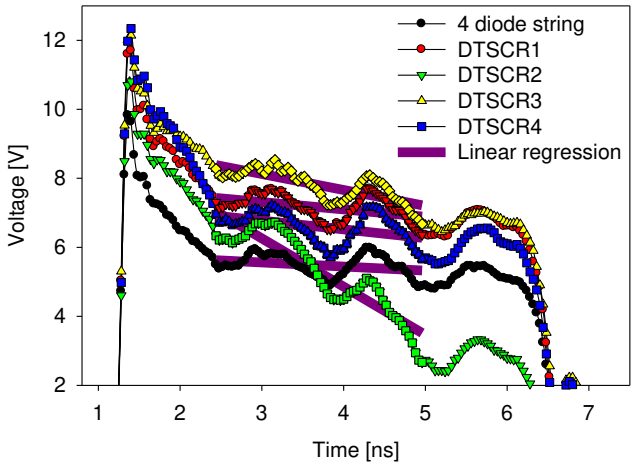


Figure 6.8: Voltage waveforms of DTSCRs and 4-diode-string subject to a relatively low stress of V_{pulse}=10V.

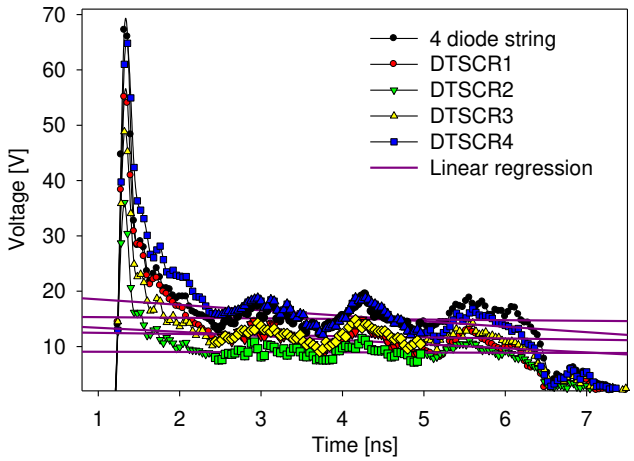


Figure 6.9: Voltage waveforms of DTSCRs and 4-diode-string subject to a relatively large stress of V_{pulse}=100V.

It has been found in Figure 6.8 that at a relatively low level ESD stress of V_{pulse}=10V, corresponding to an I_{DUT} of about 0.25A, the DTSCRs turn on slower than the 4-diode-string. This can be attributed to the fact that it takes a longer time to charge the emitter-base capacitance when the stress is relatively weak. In Figure 6.8, the voltage waveforms within the averaging window are not stable, making the linear regression extraction method questionable. Fairly stable voltage waveforms can be obtained at a higher stress of V_{pulse}=100V, as shown in Figure 6.9.

6.4 Conclusion

The ESD performances of DTSCRs with four different layouts were investigated and compared in this work. For HBM protection, DTSCR3 is the strongest candidate that offers the most favorable trigger and holding voltages, low on-resistance and excellent failure current density. DTSCR2 possess an even higher failure current density, but the low holding voltage makes it susceptible to latchup for protecting circuits with a supply voltage V_{DD} higher than

1.85V, taking 10% design margin into consideration (V_h = 2.04V = 110% × V_{DD}). For CDM protection, DTSCR2 is the best candidate owing to its shortest turn on time and smallest overshoot voltage. However, it takes around 1ns to switch on the DTSCRs but less than 1ns for CDM event to reach its peak current. The efficiency of using DTSCRs for CDM protection is limited by the relatively slow turn-on speed.

CHAPTER 7 SUMMARY AND OUTLOOK

This work has investigated for the first time the ESD performances of two types of Si nanowire transistors (GAA Si NWFET and poly-Si NWTFT) and organic thin-film transistor (OTFT). The results suggest that these devices are applicable for ESD protection in corresponding technologies and optimization can be achieved based on the dependency study of design parameters, process, layout topology and biasing conditions.

The silicon NWFETs present several favorable features comparing to conventional planar MOSFET and FinFET: (1) the floating body enables no-snapback I-V characteristic at the gate-grounded configuration; (2) the mulfi-finger (drain and source) and multi-nanowire layout topology introduces an alternative option to improve area efficiency; (3) the ESD performances of gate-all-round nanowire FETs are superior to that of FinFETs in terms of the failure current density and trigger voltage thanks to the cylinder shape of the nanowire channel.

However, of all the nanowire FETs studied, the most robust device exhibited a meager HBM ESD tolerance of 435 V, a level lower than that of a typical 90-nm bulk MOSFET and 2 kV industry standard for commercial products. Although a few solutions can be adapted to improve ESD robustness, such as multi-finger-multi-channel layout, proper gate lengths and increment of total number of channels, significant research efforts are still needed in the next several years before mass manufacture of nanowire-based products. Further research should cover process-level improvement based on failure analysis and simulation, characterization and evaluation of ESD performance of NWFETs fabricated by optimized process, compact modeling

of nanowire based ESD protection devices, and design of whole chip ESD protection in nanowire-based circuits.

The OTFT exhibits novel I-V characteristics under ESD stress comparing to the in-organic counterparts due to the accumulation mode operation and metal-semiconductor junctions. The two-phase resistor-like pulsed I-V curve requires additional leakage consideration for the design of ESD protection solution. The measurement results demonstrate that gate bias, pulse width and channel width are the major design parameters to realized performance optimization. The failure mechanism implies the necessity to improve the drain contact for ESD robustness enhancement. As an OTFT having width of 4cm only offers 700V HBM robustness, future research should be focused on how to improve the area efficiency of such devices.

Diverting attention from the future to the present, this work also seeks efficient ESD protect solutions for modern technologies. Based on the widely used ESD protection device, DTSCR, the design of new devices and layout impact analysis were presented.

The new ESD protection device BDTSCR combines bi-directional SCR and bi-directional diode strings together to achieve an optimized design window of ±3.4-±5.5V, decent HBM robustness of 58.3mA/μm, and record low parasitic capacitance below 0.095fF/μm^2. The segmentation design along the width makes device simulation inadaptable at this moment. Development of fast 3D device-level simulation in the future will facilitate the design optimization of such devices.

There are various methods to layout DTSCR but the best topology for ESD protect was not summarized previously. The four typical layouts of DTSCRs were designed in 90nm bulk

CMOS technology and investigated in terms of HBM and CDM ESD performance. The findings allow circuit designers to obtain a deeper insight in regard to DTSCR applications.

LIST OF REFERENCES

[1] O. Semenov, H. Sarbishaei, and M. Sachdev, *ESD protection device and circuit design for advanced CMOS technologies*: Springer Verlag, 2008.

[2] R. Wagner, C. Hawkins, and J. Soden, "Extent and cost of EOS/ESD damage in an IC manufacturing process," in *Proc. EOS/ESD Symposium*, 1993, pp. 49-49.

[3] W. D. T. Green, "A review of EOS/ESD field failures in military equipment," in *Proc. EOS/ESD Symposium*, 1988, pp. pp 7-13.

[4] C. Russ, "ESD Protection Devices for CMOS Technologies: Processing Impact, Modeling, and Testing Issues," PhD, Technical University Munich, 1999.

[5] B. Euzent, T. Maloney, and I. Donner, "Reducing Field Failure Rate with Improved EOS/ESD Design," in *Proc. EOS/ESD Symposium*, 1991, pp. 59-64.

[6] W. R. Anderson, D. Eppes, and S. Beebe, "Metal and silicon burnout failures from CDM ESD testing," in *Proc. EOS/ESD Symposium*, 2009, pp. 1-8.

[7] H. Gossner, C. Russ, F. Siegelin, J. Schneider, K. Schruefer, T. Schulz, C. Duvvury, C. R. Cleavelin, and W. Xiong, "Unique ESD failure mechanism in a MuGFET technology," in *International Electron Devices Meeting (IEDM)*, 2006, pp. 1-4.

[8] C. Duvvury and A. Amerasekera, "State-of-the-art issues for technology and circuit design of ESD protection in CMOS ICs," *Semiconductor Science and Technology,* vol. 11, p. 833, 1996.

[9] K. Chatty, P. Cottrell, R. Gauthier, M. Muhammad, F. Stellari, A. Weger, P. Song, and M. McManus, "Model-based guidelines to suppress cable discharge event (CDE) induced latchup in CMOS ICs," in *Proc. Int. Reliability Physics Symposium (IRPS)*, 2004, pp. 130-134.

[10] "White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements," *Industry Council on ESD Target Levels, www.esdtargets.blogspot.com,* 2010.

[11] A. Olney, B. Gifford, J. Guravage, and A. Righter, "Real-world printed circuit board ESD failures," *Microelectronics and reliability,* vol. 45, pp. 287-295, 2005.

[12] "White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements," *Industry Council on ESD Target Levels, www.esdtargets.blogspot.com,* 2010.

[13] R. J. Peirce, "ESD-Coping With ESD-The Most Common Causes of ESD Damage," *Evaluation Engineering,* vol. 41, pp. 56-59, 2002.

[14] *Compliance Engineering List*: Electrostatic Discharge Association, http://www.esda.org/IndustryDocuments.html.

[15] T. Maloney and N. Khurana, "Transmission line pulsing techniques for circuit modeling of ESD phenomena," in *Proc. EOS/ESD Symposium*, 1985, pp. 49-54.

[16] B. Keppens, V. De Heyn, M. Natarajan Iyer, and G. Groeseneken, "Contributions to standardization of transmission line pulse testing methodology," in *Proc. EOS/ESD Symposium*, 2001, pp. 456-462.

[17] S. H. Voldman, R. Ashton, J. Barth, D. Bennett, J. Bernier, M. Chaine, J. Daughton, E. Grund, M. Farris, and H. Gieser, "Standardization of the transmission line pulse (TLP) methodology for electrostatic discharge (ESD)," in *Proc. EOS/ESD Symposium*, 2003, pp. 1-10.

[18] G. Notermans, P. De Jong, and F. Kuper, "Pitfalls when correlating TLP, HBM and MM testing," in *Proc. EOS/ESD Symposium*, 1998, pp. 170-176.

[19] J. Barth and J. Richner, "Correlation considerations: Real HBM to TLP and HBM testers," *Microelectronics Reliability,* vol. 42, pp. 909-917, 2002.

[20] J. E. Barth, K. Verhaege, L. G. Henry, and J. Richner, "TLP calibration, correlation, standards, and new techniques," *Electronics Packaging Manufacturing, IEEE Transactions on,* vol. 24, pp. 99-108, 2001.

[21] S. Joshi and E. Rosenbaum, "Transmission line pulsed waveform shaping with microwave filters," in *Proc. EOS/ESD Symposium*, 2003, pp. 1-8.

[22] T. J. Maloney, "Evaluating TLP transients and HBM waveforms," in *Proc. EOS/ESD Symposium*, 2009, pp. 1-9.

[23] I. Barth Electronics, "Barth Model 4002 TLP Pulse Curve Tracer User's Manual," vol. Version 9.

[24] I. Barth Electronics, "Barth 4002 Preliminary Application note #3."

[25] H. Gieser and M. Haunschild, "Very fast transmission line pulsing of integrated structures and the charged device model," *Components, Packaging, and Manufacturing Technology, Part C, IEEE Transactions on,* vol. 21, pp. 278-285, 1998.

[26] D. Linten, P. Roussel, M. Scholz, S. Thijs, A. Griffoni, M. Sawada, T. Hasebe, and G. Groeseneken, "Calibration of very fast TLP transients," in *Proc. EOS/ESD Symposium*, 2009, pp. 1-6.

[27] C. Russ, "ESD issues in advanced CMOS bulk and FinFET technologies: Processing, protection devices and circuit strategies," *Microelectronics Reliability,* vol. 48, pp. 1403-1411, 2008.

[28] R. Gauthier, M. Abou-Khalil, K. Chatty, S. Mitra, and J. Li, "Investigation of voltage overshoots in diode triggered silicon controlled rectifiers (DTSCRs) under very fast transmission line pulsing (VFTLP)," in *Proc. EOS/ESD Symposium*, 2009, pp. 1-10.

[29] S. Hyvonen and E. Rosenbaum, "Diode-based tuned ESD protection for 5.25-GHz CMOS LNAs," in *Proc. EOS/ESD Symposium*, 2005, pp. 1-9.

[30] Y. Li and J. J. Liou, "Evaluation of Transient Behavior of Polysilicon-Bound Diode for Fast ESD Applications," *Electron Devices, IEEE Transactions on,* vol. 57, pp. 2736-2743, 2010.

[31] Y. Li, J. J. Liou, and J. Vinson, "Investigation of diode geometry and metal line pattern for robust ESD protection applications," *Microelectronics Reliability,* vol. 48, pp. 1660-1663, 2008.

[32] Y. Li, J. J. Liou, J. E. Vinson, and L. Zhang, "Investigation of LOCOS-and polysilicon-bound diodes for robust electrostatic discharge (ESD) applications," *Electron Devices, IEEE Transactions on,* vol. 57, pp. 814-819, 2010.

[33] P. Leroux, M. Steyaert, V. Vassilev, and G. Groeseneken, "A 1.3 dB NF CMOS LNA for GPS with 3kV HBM ESD–protection," in *Proceedings of the 28th European Solid-State Circuits Conference*, 2002, pp. 335-338.

[34] T. J. Maloney and S. Dabral, "Novel clamp circuits for IC power supply protection," *Components, Packaging, and Manufacturing Technology, Part C, IEEE Transactions on,* vol. 19, pp. 150-161, 1996.

[35] A. Amerasekera and J. Verwey, "ESD in integrated circuits," *Quality and reliability engineering international,* vol. 8, pp. 259-272, 1992.

[36] J. Li, D. Alvarez, K. Chatty, M. J. Abou-Khalil, R. Gauthier, C. Russ, C. Seguin, and R. Halbach, "Analysis of Failure Mechanism on Gate-Silicided and Gate-Non-Silicided, Drain/Source Silicide-blocked ESD NMOSFETs in a 65nm Bulk CMOS Technology," in *International Symposium on the Physical and Failure Analysis of Integrated Circuits*, 2006, pp. 276-280.

[37] S. Mitra, R. Gauthier, J. Li, M. Abou-Khalil, C. S. Putnam, R. Halbach, and C. Seguin, "ESD protection using grounded gate, gate non-silicided (GG-GNS) ESD NFETs in 45nm SOI technology," in *Proc. EOS/ESD Symposium*, 2008, pp. 312-316.

[38] M. D. Ker, W. Y. Chen, W. T. Shieh, and I. J. Wei, "New ballasting layout schemes to improve ESD robustness of I/O buffers in fully silicided CMOS process," *Electron Devices, IEEE Transactions on,* vol. 56, pp. 3149-3159, 2009.

[39] B. Keppens, M. P. J. Mergens, J. Armer, P. C. Jozwiak, G. Taylor, R. Mohn, C. S. Trinh, C. C. Russ, K. G. Verhaege, and F. De Ranter, "Active-area-segmentation (AAS) technique for compact, ESD robust, fully silicided NMOS design," in *Proc. EOS/ESD Symposium*, 2003, pp. 1-9.

[40] K. G. Verhaege and C. C. Russ, "Wafer cost reduction through design of high performance fully silicided ESD devices," in *Proc. EOS/ESD Symposium*, 2000, pp. 18-28.

[41] M. Okushima, T. Shinzawa, and Y. Morishita, "Layout technique to alleviate soft failure for short pitch multi finger ESD protection devices," in *Proc. EOS/ESD Symposium*, 2007, pp. 1A. 5-1-1A. 5-10.

[42] M. D. Ker and K. C. Hsu, "Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits," *Device and Materials Reliability, IEEE Transactions on,* vol. 5, pp. 235-249, 2005.

[43] M. P. J. Mergens, C. C. Russ, K. G. Verhaege, J. Armer, P. C. Jozwiak, and R. Mohn, "High holding current SCRs (HHI-SCR) for ESD protection and latch-up immune IC operation," *Microelectronics Reliability,* vol. 43, pp. 993-1000, 2003.

[44] C. Duvvury and R. Rountree, "A synthesis of ESD input protection scheme," *Journal of electrostatics,* vol. 29, pp. 1-19, 1992.

[45] M. P. J. Mergens, C. C. Russ, K. G. Verhaege, J. Armer, P. C. Jozwiak, R. Mohn, B. Keppens, and C. S. Trinh, "Diode-triggered SCR (DTSCR) for RF-ESD protection of BiCMOS SiGe HBTs and CMOS ultra-thin gate oxides," in *IEEE International Electron Devices Meeting*, 2003, pp. 21.3. 1-21.3. 4.

[46] S. H. Chen and M. D. Ker, "Optimization on MOS-triggered SCR structures for on-chip ESD protection," *Electron Devices, IEEE Transactions on,* vol. 56, pp. 1466-1472, 2009.

[47] C. C. Russ, M. P. J. Mergens, K. G. Verhaege, J. Armer, P. C. Jozwiak, G. Kolluri, and L. R. Avery, "GGSCRs: GGNMOS triggered silicon controlled rectifiers for ESD protection in deep sub-micron CMOS processes," presented at the Proc. EOS/ESD Symposium, 2001.

[48] Z. Liu, J. J. Liou, S. Dong, and Y. Han, "Silicon-Controlled Rectifier Stacking Structure for High-Voltage ESD Protection Applications," *Electron Device Letters, IEEE,* vol. 31, pp. 845-847, 2010.

[49] Z. Liu, J. J. Liou, and J. Vinson, "Novel silicon-controlled rectifier (SCR) for high-voltage electrostatic discharge (ESD) applications," *Electron Device Letters, IEEE,* vol. 29, pp. 753-755, 2008.

[50] J. Di Sarro, K. Chatty, R. Gauthier, and E. Rosenbaum, "Study of design factors affecting turn-on time of silicon controlled rectifiers (SCRS) in 90 and 65nm bulk CMOS technologies," in *Proc. Int. Reliability Physics Symposium (IRPS)*, 2006, pp. 163-168.

[51] G. Wybo, S. Verleye, B. Van Camp, and O. Marichal, "Characterizing the transient device behavior of SCRs by means of VFTLP waveform analysis," in *Proc. EOS/ESD Symposium*, 2007, pp. 6A. 5-1-6A. 5-10.

[52] C. T. Yeh and M. D. Ker, "Capacitor-less design of power-rail ESD clamp circuit with adjustable holding voltage for on-chip ESD protection," *Solid-State Circuits, IEEE Journal of,* vol. 45, pp. 2476-2486, 2010.

[53] M. Stockinger, J. W. Miller, M. G. Khazhinsky, C. A. Torres, J. C. Weldon, B. D. Preble, M. J. Bayer, M. Akers, and V. G. Kamat, "Boosted and distributed rail clamp networks for ESD protection in advanced CMOS technologies," in *Proc. EOS/ESD Symposium*, 2003, pp. 1-10.

[54] J. Li, R. Gauthier, and E. Rosenbaum, "A compact, timed-shutoff, MOSFET-based power clamp for on-chip ESD protection," in *Proc. EOS/ESD Symposium*, 2004, pp. 1-7.

[55] J. C. Smith and G. Boselli, "A MOSFET power supply clamp with feedback enhanced triggering for ESD protection in advanced CMOS technologies," *Microelectronics and reliability,* vol. 45, pp. 201-210, 2005.

[56] Y. Jiang, T. Liow, N. Singh, L. Tan, G. Lo, D. Chan, and D. Kwong, "Nanowire FETs for low power CMOS applications featuring novel gate-all-around single metal FUSI gates with dual Φm and VT tune-ability," in *International Electron Devices Meeting (IEDM)*, 2008, pp. 1-4.

[57] K. H. Yeo, S. D. Suk, M. Li, Y. Yeoh, K. H. Cho, K. H. Hong, S. K. Yun, M. S. Lee, N. Cho, and K. Lee, "Gate-all-around (GAA) twin silicon nanowire MOSFET (TSNWFET) with 15 nm length gate and 4 nm radius nanowires," in *International Electron Devices Meeting (IEDM)*, 2006, pp. 1-4.

[58] K. Moselund, P. Dobrosz, S. Olsen, V. Pott, L. De Michielis, D. Tsamados, D. Bouvet, A. O'Neill, and A. Ionescu, "Bended Gate-All-Around Nanowire MOSFET: a device with enhanced carrier mobility due to oxidation-induced tensile stress," in *International Electron Devices Meeting (IEDM)*, 2007, pp. 191-194.

[59] S. D. Suk, K. H. Yeo, K. H. Cho, M. Li, Y. Y. Yeoh, S. Y. Lee, S. M. Kim, E. J. Yoon, M. S. Kim, and C. W. Oh, "High-performance twin silicon nanowire MOSFET

(TSNWFET) on bulk Si wafer," *Nanotechnology, IEEE Transactions on,* vol. 7, pp. 181-184, 2008.

[60] P. Bandaru and P. Pichanusakorn, "An outline of the synthesis and properties of silicon nanowires," *Semiconductor Science and Technology,* vol. 25, p. 024003, 2010.

[61] K. Iniewski, *Nanoelectronics: Nanowires, Molecular Electronics, and Nanodevices*: McGraw-Hill Professional, 2010.

[62] R. Wang, J. Zhuge, R. Huang, D. W. Kim, D. Park, and Y. Wang, "Investigation on Self-Heating Effect in Gate-All-Around Silicon Nanowire MOSFETs From Top-Down Approach," *Electron Device Letters, IEEE,* vol. 30, pp. 559-561, 2009.

[63] B. C. Paul, R. Tu, S. Fujita, M. Okajima, T. H. Lee, and Y. Nishi, "An analytical compact circuit model for nanowire FET," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 1637-1644, 2007.

[64] N. Singh, A. Agarwal, L. Bera, T. Liow, R. Yang, S. Rustagi, C. Tung, R. Kumar, G. Lo, and N. Balasubramanian, "High-performance fully depleted silicon nanowire (diameter$\leqslant$ 5 nm) gate-all-around CMOS devices," *Electron Device Letters, IEEE,* vol. 27, pp. 383-386, 2006.

[65] D. Trémouilles, S. Thijs, C. Russ, J. Schneider, C. Duvvury, N. Collaert, D. Linten, M. Scholz, M. Jurczak, and H. Gossner, "Understanding the optimization of sub-45nm FinFET devices for ESD applications," in *Proc. EOS/ESD Symposium*, 2007, pp. 7A. 5-1-7A. 5-8.

[66] K. Bock, C. Russ, G. Badenes, G. Groeseneken, and L. Deferm, "Influence of well profile and gate length on the ESD performance of a fully silicided 0.25 μm CMOS technology," *Components, Packaging, and Manufacturing Technology, Part C, IEEE Transactions on,* vol. 21, pp. 286-294, 1998.

[67] A. Griffoni, S. Thijs, C. Russ, D. Trémouilles, D. Linten, M. Scholz, N. Collaert, L. Witters, G. Meneghesso, and G. Groeseneken, "Next generation bulk FinFET devices and their benefits for ESD robustness," in *Proc. EOS/ESD Symposium*, 2009, pp. 1-10.

[68] J. E. Vinson and J. J. Liou, "Electrostatic discharge in semiconductor devices: an overview," *Proceedings of the IEEE,* vol. 86, pp. 399-420, 1998.

[69] "TCAD Sentaurus Device User's Manual," *Synopsys, Mountain View, CA*.

[70] G. Curatola and S. Nuttinck, "The role of volume inversion on the intrinsic RF performance of double-gate FinFETs," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 141-150, 2007.

[71] P. Leroux and M. Steyaert, *LNA-ESD co-design for fully integrated CMOS wireless receivers* vol. 843: Kluwer Academic Pub, 2006.

[72] H. Gossner, "ESD protection for the deep sub micron regime-a challenge for design methodology," in *Proceedings of the International Conference on VLSI Design*, 2004, pp. 809-818.

[73] J. Li, K. Chatty, R. Gauthier, R. Mishra, and C. Russ, "Technology scaling of advanced bulk CMOS on-chip ESD protection down to the 32nm node," in *Proc. EOS/ESD Symposium*, 2009, pp. 1-7.

[74] K. Chatty, D. Alvarez, M. Abou-Khalil, C. Russ, J. Li, and R. Gauthier, "Investigation of ESD performance of silicide-blocked stacked NMOSFETs in a 45nm bulk CMOS technology," in *Proc. EOS/ESD Symposium*, 2008, pp. 304-312.

[75] D. Alvarez, K. Chatty, C. Russ, M. J. Abou-Khalil, J. Li, R. Gauthier, K. Esmark, R. Halbach, and C. Seguin, "Design optimization of gate-silicided ESD NMOSFETs in a 45nm bulk CMOS technology," *Microelectronics Reliability,* vol. 49, pp. 1417-1423, 2009.

[76] K. Chatty, D. Alvarez, R. Gauthier, C. Russ, M. Abou-Khalil, and B. Kwon, "Process and design optimization of a protection scheme based on NMOSFETs with ESD implant in 65nm and 45nm CMOS technologies," in *Proc. EOS/ESD Symposium*, 2007, pp. 7A. 2-1-7A. 2-10.

[77] C. Russ, H. Gossner, T. Schulz, N. Chaudhary, W. Xiong, A. Marshall, C. Duvvury, K. Schrufer, and C. Rinn Cleavelin, "ESD evaluation of the emerging MUGFET technology," *Device and Materials Reliability, IEEE Transactions on,* vol. 7, pp. 152-161, 2007.

[78] W. Liu, J. Liou, Y. Jiang, N. Singh, G. Lo, J. Chung, and Y. Jeong, "Investigation of Sub-10-nm Diameter, Gate-All-Around Nanowire Field-Effect Transistors for Electrostatic Discharge Applications," *Nanotechnology, IEEE Transactions on,* vol. 9, pp. 352-354, 2010.

[79] S. Voldman, "Nano electrostatic discharge," *Nanotechnology Magazine, IEEE,* vol. 3, pp. 12-15, 2009.

[80] H. M. Chou, J. W. Lee, and Y. Li, "A floating gate design for electrostatic discharge protection circuits," *Integration, the VLSI Journal,* vol. 40, pp. 161-166, 2007.

[81] H. H. Chang and M. D. Ker, "Improved output ESD protection by dynamic gate floating design," *Electron Devices, IEEE Transactions on,* vol. 45, pp. 2076-2078, 1998.

[82] E. Y. Wu, R. P. Vollertsen, J. Sune, and G. La Rosa, *Reliability wearout mechanisms in advanced CMOS technologies* vol. 12: Wiley-IEEE Press, 2009.

[83] L. Zhang, R. Wang, J. Zhuge, R. Huang, D. W. Kim, D. Park, and Y. Wang, "Impacts of non-negligible electron trapping/detrapping on the NBTI characteristics in silicon nanowire transistors with tin metal gates," in *International Electron Devices Meeting (IEDM)*, 2008, pp. 1-4.

[84] T. Pompl, H. Wurzer, M. Kerber, R. Wilkins, and I. Eisele, "Influence of soft breakdown on NMOSFET device characteristics," in *Proc. Int. Reliability Physics Symposium (IRPS)*, 1999, pp. 82-87.

[85] A. Ille, W. Stadler, T. Pompl, H. Gossner, T. Brodbeck, K. Esmark, P. Riess, D. Alvarez, K. Chatty, and R. Gauthier, "Reliability aspects of gate oxide under ESD pulse stress," *Microelectronics Reliability,* vol. 49, pp. 1407-1416, 2009.

[86] Y. B. Park and D. K. Schroder, "Degradation of thin tunnel gate oxide under constant Fowler-Nordheim current stress for a flash EEPROM," *Electron Devices, IEEE Transactions on,* vol. 45, pp. 1361-1368, 1998.

[87] H. C. Lin, M. H. Lee, C. J. Su, T. Y. Huang, C. Lee, and Y. S. Yang, "A simple and low-cost method to fabricate TFTs with poly-Si nanowire channel," *Electron Device Letters, IEEE,* vol. 26, pp. 643-645, 2005.

[88] C. J. Su, H. C. Lin, H. H. Tsai, T. Y. Huang, and W. X. Ni, "Fabrication and characterization of poly-Si nanowire devices with performance enhancement techniques," in *International Symposium on VLSI Technology, Systems and Applications*, 2007, pp. 1-2.

[89] H. C. Lin, W. C. Chen, C. D. Lin, and T. Y. Huang, "Performance enhancement in double-gated poly-Si nanowire transistors with reduced nanowire channel thickness," *Electron Device Letters, IEEE,* vol. 30, pp. 644-646, 2009.

[90] A. Amerasekera and C. Duvvury, "The impact of technology scaling on ESD robustness and protection circuit design," *Components, Packaging, and Manufacturing Technology, Part A, IEEE Transactions on,* vol. 18, pp. 314-320, 1995.

[91] H. H. Hsu, H. C. Lin, L. Chan, and T. Y. Huang, "Threshold-Voltage Fluctuation of Double-Gated Poly-Si Nanowire Field-Effect Transistor," *Electron Device Letters, IEEE,* vol. 30, pp. 243-245, 2009.

[92] F. S. Wang, M. J. Tsai, and H. C. Cheng, "The effects of NH3 plasma passivation on polysilicon thin-film transistors," *Electron Device Letters, IEEE,* vol. 16, pp. 503-505, 1995.

[93] Z. Bao and J. J. Locklin, *Organic field-effect transistors* vol. 128: CRC, 2007.

[94] T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai, and T. Someya, "Organic nonvolatile memory transistors for flexible sensor arrays," *Science,* vol. 326, p. 1516, 2009.

[95] I. Kymissis, *Organic Field Effect Transistors: Theory, Fabrication and Characterization*: Springer Verlag, 2009.

[96] T. Sekitani, M. Takamiya, Y. Noguchi, S. Nakano, Y. Kato, T. Sakurai, and T. Someya, "A large-area wireless power-transmission sheet using printed organic transistors and plastic MEMS switches," *Nature materials,* vol. 6, pp. 413-417, 2007.

[97] K. Fukuda, T. Hamamoto, T. Yokota, T. Sekitani, U. Zschieschang, H. Klauk, and T. Someya, "Effects of the alkyl chain length in phosphonic acid self-assembled monolayer gate dielectrics on the performance and stability of low-voltage organic thin-film transistors," *Applied Physics Letters,* vol. 95, pp. 203301-203301-3, 2009.

[98] C. Ucurum, H. Siemund, and H. Göbel, "Impact of electrical measurement parameters on the hysteresis behavior of pentacene-based organic thin-film transistors," *Organic Electronics,* vol. 11, pp. 1523-1528, 2010.

[99] C. L. Fan, T. H. Yang, and C. Y. Chiang, "Performance degradation of pentacene-based organic thin-film transistors under positive drain bias stress in the atmosphere," *Electron Device Letters, IEEE,* vol. 31, pp. 887-889, 2010.

[100] T. Sekitani, S. Iba, Y. Kato, Y. Noguchi, T. Someya, and T. Sakurai, "Suppression of DC bias stress-induced degradation of organic field-effect transistors using postannealing effects," *Applied Physics Letters,* vol. 87, pp. 073505-073505-3, 2005.

[101] J. Li, R. Gauthier, K. Chatty, D. Kontos, M. Muhammad, M. Woo, C. Putnam, C. Russ, D. Alvarez, and J. Schneider, "PMOSFET-based ESD protection in 65nm bulk CMOS technology for improved external latchup robustness," in *Proc. EOS/ESD Symposium*, 2005, pp. 1-8.

[102] M. D. Ker, J. Y. Chuang, C. K. Deng, C. H. Li, and C. H. Kuo, "Investigation on ESD Robustness of P-type TFTs under Different Layout Structures in LTPS Process for On-Panel ESD Protection Design," in *Proc. Int. Electrostatic Discharge Workshop*, 2007.

[103] C. R. Newman, R. J. Chesterfield, M. J. Panzer, and C. D. Frisbie, "High mobility top-gated pentacene thin-film transistors," *Journal of applied physics,* vol. 98, p. 084506, 2005.

[104] T. Miyadera, T. Minari, K. Tsukagoshi, H. Ito, and Y. Aoyagi, "Frequency response analysis of pentacene thin-film transistors with low impedance contact by interface molecular doping," *Applied Physics Letters,* vol. 91, p. 013512, 2007.

[105] A. Wang and C. Tsay, "A low-triggering circuitry for dual-direction ESD protection," 1999, pp. 139-142.

[106] V. Vashchenko, V. Kuznetsov, and P. Hopper, "Implementation of dual-direction SCR devices in analog CMOS process," in *Proc. EOS/ESD Symposium*, 2007, pp. 1B. 5-1-1B. 5-5.

[107] Z. Liu, J. Vinson, L. Lou, and J. J. Liou, "An improved bidirectional SCR structure for low-triggering ESD protection applications," *Electron Device Letters, IEEE,* vol. 29, pp. 360-362, 2008.

[108] X. Wang, J. Liu, S. Fan, L. Lin, H. Tang, A. Wang, H. Chen, L. Yang, and B. Zhao, "Cross-Coupling Low-Triggering Dual-Polarity CLTdSCR ESD Protection in CMOS," *Electron Device Letters, IEEE,* vol. 31, pp. 1143-1145, 2010.

[109] A. Z. H. Wang and C. H. Tsay, "On a dual-polarity on-chip electrostatic discharge protection structure," *Electron Devices, IEEE Transactions on,* vol. 48, pp. 978-984, 2001.

[110] S. L. Jang, M. S. Gau, and J. K. Lin, "Novel diode-chain triggering SCR circuits for ESD protection," *Solid-State Electronics,* vol. 44, pp. 1297-1303, 2000.

[111] M. D. Ker and C. Y. Lin, "Low-capacitance SCR with waffle layout structure for on-chip ESD protection in RF ICs," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 56, pp. 1286-1294, 2008.

[112] C. Chu, A. Gallerano, J. Watt, T. Hoang, T. Tran, D. Chan, W. Wong, J. Barth, and M. Johnson, "Using VFTLP data to design for CDM robustness," in *Proc. EOS/ESD Symposium*, 2009, pp. 1-6.

[113] K. Esmark, H. Gossner, S. Bychikhin, D. Pogany, C. Russ, G. Langguth, and E. Gornik, "Transient behavior of SCRs during ESD pulses," in *Proc. Int. Reliability Physics Symposium (IRPS)*, 2008, pp. 247-253.

[114] I. Barth Electronics, "Barth Model 4012 VFTLP+ Pulse Curve Tracer User's Manual."

[115] S. M. Sze, *Semiconductor devices: physics and technology*: John Wiley & Sons, 2008.