Design Considerations and Performance Evaluations of Synchronous Rectification in Flyback Converters

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***Abstract*— Design tradeoffs and performance comparisons of various implementations of the flyback converter with a synchronous rectifier (SR) are presented. Specifically, the merits and limitations of the constant-frequency (CF) continuous-conduction mode (CCM), CF discontinuous-conduction mode (DCM), variable-frequency (VF) DCM, and zero-voltage-switched (ZVS) DCM flyback converters with SR's are discussed. The theoretical efficiency improvements of the discussed synchronous rectification approaches relative to Schottky diode implementations are derived. Finally, theoretical results are verified on an experimental universal-input off-line 15-V/36-W flyback prototype.**

***Index Terms*— Efficiency, flyback converter, synchronous rectification.**

I. Introduction

GENERALLY, in low-output-voltage power supplies, the conduction loss of the diode rectifier (DR) due to its forward voltage drop is the dominant loss component. In power supplies with the output voltage not too many times higher than the rectifier forward voltage drop, the DR loss accounts for more than 50% of the total power loss. The rectification loss can be reduced by replacing the DR with a synchronous rectifier (SR), i.e., with a low-on-resistance MOSFET [1], [2]. Synchronous rectification is most often applied to the buck and buck-derived isolated topologies, which are suitable for step-down low-output-voltage applications [2]. Generally, in the isolated buck-derived topologies, such as the forward, bridge-type, and push–pull converters, synchronous rectification can be implemented by a direct replacement of the DR's with low-voltage MOSFET's [3], [4]. Namely, in these self-driven SR implementations, the secondary voltage of the transformer is used to directly drive the SR's, thus reducing the circuit complexity and cost without sacrificing the efficiency.

A number of applications of the SR in the flyback converter have also been reported [5]–[7]. However, in all of these applications, the main purpose of the SR was to provide the postregulation of the output voltage and not to maximize the conversion efficiency. Specifically, in [5]–[7], the SR is used as a voltage-controlled resistor in a control loop which adjusts the SR's resistance so that the output voltage is maintained within the regulation range. Generally, the regulation range of these postregulation approaches is limited to the forward voltage drop of the SR body diode, i.e., ~0.7 V. Moreover, since the voltage drop across the SR is not minimized because of the resistance modulation, the conversion efficiency of these postregulators is reduced, compared to that of the converter with the "true" SR.

The objective of this paper is to evaluate the theoretical and practical limits of the efficiency improvements for various implementations of the flyback converter with the SR with respect to the corresponding converter with the DR. Specifically, the design considerations and performance evaluations of the constant-frequency (CF) continuous-conduction mode (CCM), CF discontinuous-conduction mode (DCM), variable-frequency (VF) DCM, and zero-voltage-switched (ZVS) DCM flyback converters with the SR are discussed.

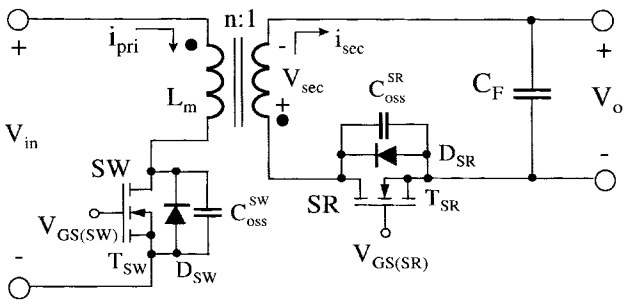

Fig. 1. Flyback converter with SR.

II. Synchronous Rectifier Implementations

A flyback converter with the SR is shown in Fig. 1. For proper operation of the converter, conduction periods of primary switch SW and secondary-side switch SR must not overlap. To avoid the simultaneous conduction of the SW and the SR, a delay between the turn-off instant of switch SW and the turn-on instant of the SR as well as between the turn-on instant of the SW and turn-off instant of the SR must be introduced in the gate-drive waveforms of the switches. With properly designed gate drives, the operation of the circuit shown in Fig. 1 is identical to that with a conventional DR. Namely, during the time switch SW is turned on, energy is stored in the transformer magnetizing inductance and transferred to the output after SW is turned off.

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Generally, the circuit sown in Fig. 1 can work in CCM or DCM either with a constant or variable switching frequency pulse-width-modulation (PWM) control. Design considerations and SR loss estimates for various modes of operation and different control approaches are given next.

A. Constant-Frequency CCM

The key waveforms of the flyback converter with the SR operating in CCM are given in Fig. 2. As can be seen from Fig. 2, during delay times $T_D^{\rm on}$ and $T_D^{\rm off}$, secondary current $i_{\rm sec}$ flows through the body diode of the SR (shaded $i_{\rm sec}$ region in Fig. 2). The conduction of body diode $D_{\rm SR}$ not only increases the conduction loss, but also introduces a reverse recovery loss when primary switch SW is turned on. The total conduction loss of the SR is given by the sum of the channel-resistance loss (unshaded $i_{\rm sec}$ region in Fig. 2) and body-diode loss (shaded $i_{\rm sec}$ region in Fig. 2). Assuming that the conduction time through the channel of the SR is much longer than the conduction time through the body diode of the SR, i.e., assuming that the SR conducts through the channel for the entire off period, the rms value of the trapezoidal secondary current which flows through the channel can be derived as

$$I_{\rm sec}^2 = \frac{I_o^2}{1-D} + \frac{(\Delta I_{\rm sec})^2}{12}(1-D) \tag{1}$$

where $R_{\rm DS(on)}$ is the SR on resistance, $D = T_{\rm on}/T_s$ is the duty ratio of the primary switch, I_o is the output current, $\Delta I_{\rm sec} = Vo(1-D)Ts/(L_m/n^2)$ is the secondary peak-to-peak ripple current, L_m is the primary-side magnetizing inductance of the transformer, T_s is the switching period, and n is the turns ratio of the transformer, respectively. Using (1), the total conduction loss of the SR can be calculated as

$$P_{\rm cond}^{\rm SR} = R_{\rm DS(on)}\left[\frac{I_o^2}{1-D} + \frac{\Delta I_{\rm sec}^2(1-D)}{12}\right] + V_D\left(I_{\rm sec}^{\rm on}T_D^{\rm on} + I_{\rm sec}^{\rm off}T_D^{\rm off}\right)f_s \tag{2}$$

where the second term represents the loss incurred by the conduction of the body diode of the SR. In (2), V_D is the forward voltage drop of the SR's body diode and $I_{\rm sec}^{\rm on}$ and $I_{\rm sec}^{\rm off}$ are the SR's body diode currents during dead times $T_D^{\rm on}$ and $T_D^{\rm off}$, respectively. Because dead times $T_D^{\rm on}$ and $T_D^{\rm off}$ are short compared with off-time $T_{\rm off}$, currents $I_{\rm sec}^{\rm on}$ and $I_{\rm sec}^{\rm off}$ can be considered constant during the SR's body diode conduction. Since in the CCM $I_{\rm sec}^{\rm on} = I_o/(1-D) + \Delta I_{\rm sec}/2$ and $I_{\rm sec}^{\rm off} = I_o/(1-D) - \Delta I_{\rm sec}/2$, the total conduction loss of the SR can be expressed as

$$P_{\rm cond}^{\rm SR} = R_{\rm DS(on)}\left[\frac{I_o^2}{1-D} + \frac{\Delta I_{\rm sec}^2(1-D)}{12}\right] + \frac{V_D I_o\left(T_D^{\rm on} + T_D^{\rm off}\right)f_s}{1-D}. \tag{3}$$

The total reverse recovery loss of the body diode of the SR is [8]

$$P_{\rm RR}^{\rm SR} = Q_{\rm RR}\left(V_o + \frac{V_{\rm in}}{n}\right)f_s \tag{4}$$

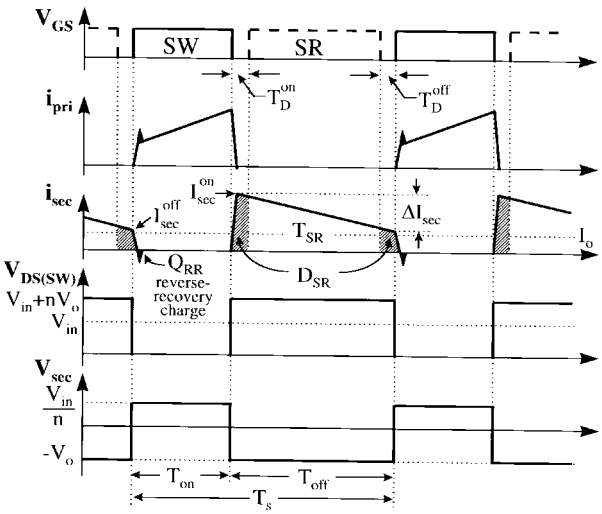


Fig. 2. Key waveforms of CF CCM flyback converter with SR. Body diode of SR conducts in shaded area (▨).

where $Q_{\rm RR}$ is the recovered charge of the SR body diode and $V_o + V_{\rm in}/n$ is the steady-state reverse voltage across the SR.

In addition to $P_{\rm cond}^{\rm SR}$ and $P_{\rm RR}^{\rm SR}$ losses, the CF CCM converter in Fig. 1 exhibits a loss each time the SR is turned off (i.e., each time the SW is turned on) because of a parasitic resonance between $C_{\rm oss}^{\rm SR}$ and the leakage inductance of the transformer (see Fig. 9). Since the parasitic resonance must be damped by a snubber to limit the maximum voltage across the SR, the resonance dies out completely before SR is turned on again. As a result, the power loss due to this parasitic resonance can be calculated from

$$P_{\rm off}^{\rm SR} = \frac{1}{2}C_{\rm oss}^{\rm SR}\left(V_o + \frac{V_{\rm in}}{n}\right)^2 f_s. \tag{5}$$

Finally, for proper operation of the circuit, the SR must be turned off before primary switch SW is turned on (delay time $T_D^{\rm off}$ in Fig. 2). Therefore, the flyback converter with the SR cannot be self-driven from the secondary winding of the transformer. In fact, the circuit shown in Fig. 1 requires an external control circuit to turn off the SR.

B. Constant-Frequency DCM

The key waveforms of the CF flyback converter with the SR operating in DCM are shown in Fig. 3. In DCM, the energy stored in the magnetizing inductance of the transformer during the on time of switch SW is completely discharged during the subsequent off time. As can be seen from Fig. 3, secondary current $i_{\rm sec}$ reaches zero before primary switch SW is turned on. To prevent the discharging of the output filter capacitor through a conducting SR, the SR channel conduction (transistor $T_{\rm SR}$) must be terminated at the moment $i_{\rm sec}$ reaches zero, or a short while after. Therefore, the DCM flyback converter with the SR requires a zero-current crossing detector in the control circuit.

After the SR is turned off, the magnetizing inductance of the transformer L_m and capacitance $C_{\rm eq} = C_{\rm oss}^{\rm SW} + C_{\rm oss}^{\rm SR}/n^2$ starts resonating, as shown in Fig. 3. For a converter with a regulated output, the duration of resonant interval $T_{\rm DCM}$ in

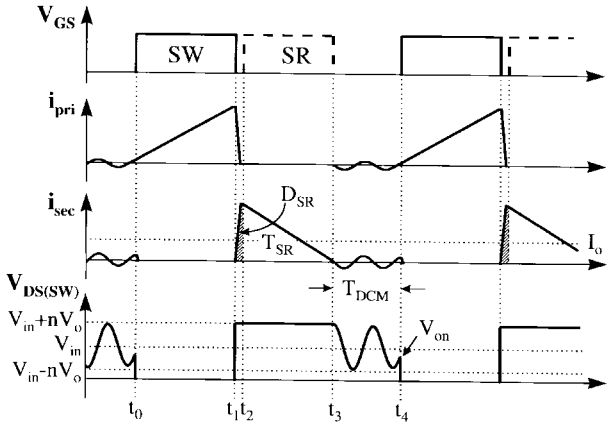


Fig. 3. Key waveforms of CF DCM flyback converter with SR. Body diode of SR conducts in shaded area (▨).

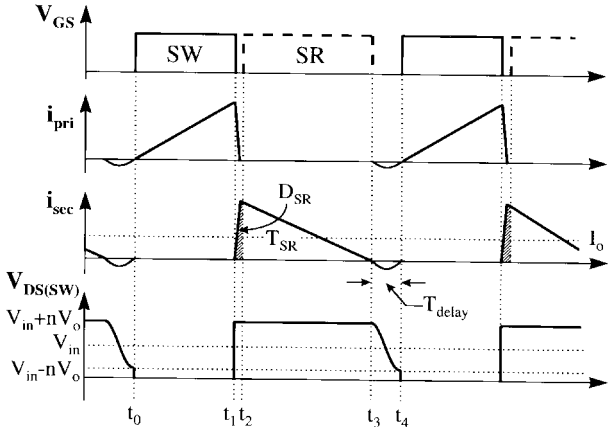


Fig. 4. Key waveforms of VF DCM flyback converter with SR. Body diode of SR conducts in shaded area (▨).

Fig. 3 changes significantly with the input voltage and less dramatically with the output current. As a result, the voltage across the primary switch at the moment of its turn on can range anywhere between $V_{\rm in}+nV_o$ and $V_{\rm in}-nV_o$, producing the capacitive turn-on loss of

$$P_{\rm cap(SW)}=\frac{1}{2}C_{\rm oss}^{\rm SW}V_{\rm on}^2 f_s \tag{6}$$

where $V_{\rm in}-nV_o \le V_{\rm on} \le V_{\rm in}+nV_o$. Since $P_{\rm cap(SW)}$ is maximum at the peaks of the $V_{\rm DS(SW)}$ oscillation and minimum at its valleys, the efficiency of the converter shows strong fluctuations with the input voltage. In addition, because typical SR's have a much larger output capacitance $C_{\rm oss}^{\rm SR}$ than the Schottky rectifiers, the characteristic impedance $Z_m=\sqrt{L_m/C_{\rm eq}}$ of the resonant tank consisting of L_m and $C_{\rm eq}$ is much lower for the converter with an SR compared to that with a Schottky diode. As a result, the resonant-tank current of the converter with an SR is much higher than that of the converter with a Schottky, causing a larger conduction loss. For certain line and load conditions, this power loss can completely offset the power-loss savings obtained by the SR, making the efficiency of the converter with the SR lower than that of the converter with the DR.

Finally, it should be noted that in the DCM flyback converter reverse-rectifier loss $P_{\rm RR}^{\rm SR}$ is eliminated because the rectifier current becomes zero before primary switch SW is turned on.

C. Variable-Frequency DCM

Capacitive switching loss $P_{\rm cap(SW)}$ can be minimized, and parasitic oscillation caused by the interaction of L_m and $C_{\rm eq}$ can be eliminated if the primary switch SW is turned on at the moment $V_{\rm DS(SW)}$ reaches its minimum voltage $V_{\rm in}-nV_o$ the first time after the SR is turned off, as shown in Fig. 4. This can be accomplished by sensing the zero-current crossing of $i_{\rm sec}$ and turning on SW after a constant delay $T_{\rm dealy}$, which is equal to one half of the parasitic-resonance period, i.e.,

$$T_{\rm delay}=\pi\sqrt{L_m C_{\rm eq}}. \tag{7}$$

With this VF control, the efficiency fluctuations with the input voltage are eliminated. It should be noted that with the VF control, the switching frequency is minimum at low line and full load, and it increases as the line increases and/or load decreases.

The conversion efficiency at low line of the VF DCM converter can be always made higher than the efficiency of the corresponding CF counterpart. In addition, the high-line efficiency of the VF DCM converter can also be higher than that of the CF DCM implementation if the power-loss savings due to elimination of the parasitic oscillations and the minimization of the turn-on voltage $V_{\rm on}$ are lower than the increased switching losses and magnetic losses due to the increased switching frequency.

D. Variable-Frequency ZVS DCM

As can be seen from Fig. 4, if the amplitude of the oscillation after the turn off of the SR is larger than the input voltage, i.e., if

$$V_{\rm in}<nV_o \tag{8}$$

primary-switch voltage $V_{\rm DS(SW)}$ will fall to zero before the switch is turned on at the moment $t_4=t_3+T_{\rm delay}$. Therefore, for $V_{\rm in}<nV_o$, the VF flyback converter can achieve ZVS, i.e., the capacitive turn-on loss of the primary switch can be eliminated. While the ZVS condition in (8) may be met for certain designs at low input-voltages, generally it is not met at higher input voltages. As a result, at higher input voltages, the VF flyback converter with gate-drive timing given in Fig. 4 operates with partial ZVS.

However, the complete ZVS of the primary switch in the VF flyback converter with the SR can be achieved in the entire input-voltage range if the turn-off instant of the SR after the secondary current zero crossing is delayed enough to allow a negative secondary current to build up, as shown in Fig. 5. To achieve ZVS in the entire input-voltage range, the energy stored in magnetizing inductance L_m by the negative secondary current $I_{\rm ZVS}$ must be large enough to discharge primary switch capacitance $C_{\rm oss}^{\rm SW}$ from voltage $V_{\rm in}+nV_o$ down to zero, i.e.,

$$I_{\rm ZVS}\ge\frac{n\sqrt{V_{\rm in(max)}^2-(nV_o)^2}}{Z_m}. \tag{9}$$

TABLE I
POWER LOSS COMPARISONS OF FLYBACK CONVERTERS WITH DR AND SR

		CF CCM	CF DCM	VF DCM	VF ZVS DCM
P_{con}	DR	$V_F I_o$	$V_F I_o$	$V_F I_o$	not possible to implement
	SR	$R_{DS(on)}\left[\frac{I_o^2}{1-D}+\frac{\Delta I_{sec}^2(1-D)}{12}\right]$ $+V_D I_o(T_D^{on}+T_D^{off})f_s/(1-D)$	$R_{DS(on)}\frac{4I_o^2}{3(1-D)}$	$R_{DS(on)}\frac{4I_o^2}{3(1-D)}$	$R_{DS(on)}\frac{4I_o^2}{3(1-D)}$ $+\frac{I_{ZVS}[2I_o+I_{ZVS}(1-D)]}{3}$
$P_{sw}=$ $P_{off}+P_{RR}$	DR†	$\left[\frac{C_T}{2}(V_o+\frac{V_{in}}{n})^2+Q_{RR}^{DR}(V_o+\frac{V_{in}}{n})\right]f_s$	0	0	not possible to implement
	SR	$\left[\frac{C_{oss}^{SR}}{2}(V_o+\frac{V_{in}}{n})^2+Q_{RR}^{SR}(V_o+\frac{V_{in}}{n})\right]f_s$	0	0	0
$P_{cap(SW)}$	DR	$\frac{C_{oss}^{SW}}{2}(V_{in}+nV_o)^2 f_s$	$\frac{C_{oss}^{SW}}{2}V_{on}^2 f_s$	$\frac{C_{oss}^{SW}}{2}(V_{in}-nV_o)^2 f_s$	not possible to implement
	SR	$\frac{C_{oss}^{SW}}{2}(V_{in}+nV_o)^2 f_s$	$\frac{C_{oss}^{SW}}{2}V_{on}^2 f_s$	$\frac{C_{oss}^{SW}}{2}(V_{in}-nV_o)^2 f_s$	0

† Note that for Schottky rectifiers, $Q_{RR}\approx 0$.

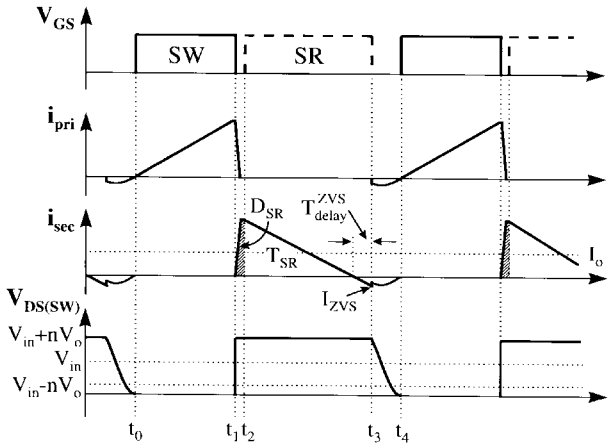


Fig. 5. Key waveforms of VF ZVS DCM operation.

Therefore, to build up the necessary $I_{\rm ZVS}$, the turn off of the SR should be delayed after the zero crossing of $i_{\rm sec}$ for

$$T_{\rm delay}^{\rm ZVS}=\frac{L_m\cdot I_{\rm ZVS}}{n^2\cdot V_o} \tag{10}$$

as shown in Fig. 5.

Finally, it should be noted that in the VF ZVS DCM flyback converter with the SR, the capacitive turn-on switching loss of the primary switch is traded off for the conduction loss. Namely, according to Fig. 5, due to the negative secondary current, the rms value of the secondary current is slightly increased. Therefore, the VF ZVS converter in Fig. 5 might not necessarily achieve higher efficiency compared to the VF converter with partial ZVS (Fig. 4).

III. SR EFFICIENCY IMPROVEMENT ESTIMATES

Generally, in a flyback converter, the substitution of the DR with an SR affects the conduction and switching losses of the rectifier. In addition, the employment of an SR allows for the implementation of VF flyback converter with complete ZVS, i.e., without any primary-switch capacitive turn-on switching loss $P_{\rm cap(SW)}$. Table I summarizes theoretical rectifier conduction loss $P_{\rm cond}$, rectifier switching losses, $P_{\rm sw}=P_{\rm off}+P_{\rm RR}$, and the primary switching loss $P_{\rm cap(SW)}$ of the flyback converter with the DR and the SR.

The efficiency of a converter with the DR can be expressed as

$$\eta_{\rm DR}=\frac{P_o}{P_o+P_{\rm cond}^{\rm DR}+P_{\rm sw}^{\rm DR}+P_{\rm cap(SW)}^{\rm DR}+P_{\rm other}} \tag{11}$$

where P_o is the output power and $P_{\rm other}$ is the loss other than the conduction and switching losses of the rectifier and the capacitive turn-on switching loss of the primary switch. Specifically, $P_{\rm other}$ includes the transformer, input [electromagnetic interference (EMI)] filter, output filter, and control circuit losses, i.e., the losses which are virtually the same for both the SR and rectifier diode implementations of the converter.

Similarly, the efficiency of the flyback converter with the SR can be written as

$$\eta_{\rm SR}=\frac{P_o}{P_o+P_{\rm cond}^{\rm SR}+P_{\rm sw}^{\rm SR}+P_{\rm cap(SW)}^{\rm SR}+P_{\rm other}}. \tag{12}$$

By eliminating $P_{\rm other}$ from (11) and (12), the efficiency difference between the SR and the DR implementations can

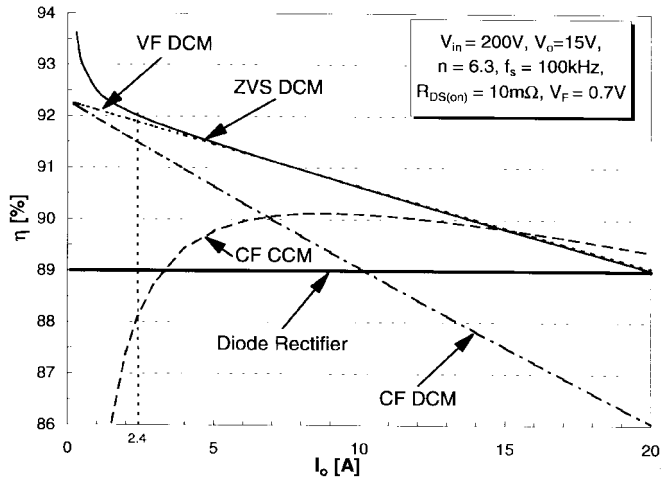


Fig. 6. Theoretical efficiency estimates.

be calculated as

$$\Delta\eta = \eta_{\rm SR} - \eta_{\rm DR} = \frac{\Delta P_{\rm REC}\eta_{\rm DR}^2}{P_o - \Delta P_{\rm REC}\eta_{\rm DR}} \tag{13}$$

where

$$\Delta P_{\rm REC} = \left(P_{\rm cond}^{\rm DR} - P_{\rm cond}^{\rm SR}\right) + \left(P_{\rm sw}^{\rm DR} - P_{\rm sw}^{\rm SR}\right) + \left(P_{\rm cap(SW)}^{\rm DR} - P_{\rm cap(SW)}^{\rm SR}\right). \tag{14}$$

Using the power loss expressions from Table I and knowing the device characteristics and the circuit parameters, the efficiency improvement of the flyback converter with the SR can be calculated. As an example, Fig. 6 presents the calculated efficiencies for the discussed four implementations of the converter with the SR as functions of the load current. In Fig. 6, it is assumed that the DR versions of the converter have conversion efficiencies of 89%, which correspond to the efficiencies of the experimental circuit discussed in the next section.

As can be seen from Fig. 6, the efficiency of the ZVS DCM implementation (solid line) is highest at low-power levels (i.e., for $I_o \leq$ 5–6 A) because the switching turn-on loss of the primary switch contributes significantly to the total loss in the other implementations. For the same range of the output power, the CF CCM implementation exhibits the lowest efficiency due to the dominant effect of the turn-on switching loss of the primary switch and the turn-off switching loss of the SR. For example, at $I_o = 2.4$ A (which corresponds to the full-load current of the experimental converter presented in the next section), the efficiency of the ZVS DCM implementation with the SR is approximately 3% higher than the efficiency of the corresponding circuit with the Schottky rectifier. However, at $I_o = 2.4$ A, the efficiency of the CCM implementation with the SR at $I_o = 2.4$ A is 1% lower than the efficiency of the same circuit with the Schottky rectifier.

At higher power levels, the conduction losses of the primary switch and the SR start dominating the total loss. As a result, the CF CCM implementation exhibits the highest efficiency at $I_o > 15$ A due to its smallest primary and secondary rms currents. On the other hand, the efficiency of the CF DCM implementation monolithically decreases as the load current (output power) increases. In fact, as can be seen from Fig. 6, for $I_o > 10$ A the efficiency of the CF DCM implementation is lower than that of the Schottky implementation. Also, as the load current, and therefore the conduction losses, become larger, the efficiencies of the VF DCM and ZVS DCM implementations converge because the power savings brought about by soft switching in ZVS DCM implementation are less significant.

Finally, as the output current continues to increase, so that the voltage drop across the SR $R_{\rm DS(on)}i_{\rm RMS}$ approaches that of the Schottky rectifier V_F, the efficiencies of the CF CCM, VF DCM, and ZVS DCM implementations approach that of the Schottky-rectifier implementation. As can be seen from Fig. 6, at $I_o = 20$ A, the efficiencies of the VF DCM and ZVS DCM implementations fall to the level of the Schottky implementation efficiency. The CF CCM implementation efficiency drops to that of the Schottky-rectifier implementation at $I_o > 20$ A due to lower $i_{\rm sec}^{\rm RMS}$. The only way to achieve efficiency improvements at higher load currents, i.e., when $R_{\rm DS(on)}i_{\rm RMS} \approx V_F$, is to resort to paralleling of SR's in order to reduce the effective $R_{\rm DS(on)}$.

IV. Evaluation Results

The discussed SR implementations were experimentally evaluated on a 15-V/2.4-A flyback converter designed to operate in the 100–370-Vdc input-voltage range. The diode-version power stages were implemented with Motorola MTP6N60 ($V_{\rm RRM} = 600$ V, $R_{\rm DS(on)} = 1.2\ \Omega @ T_j = 25$°C, and $C_{\rm oss}^{\rm SW} = 350$ pF @ $V_{\rm DS} = 25$ V) MOSFET's for the primary switches and two IR 10CQT150 ($V_{\rm RRM} = 150$ V, $V_F = 0.73$ V @ 5 $A_{\rm PK}$, $T_j = 125$°C, and $C_T = 200$ pF @ $V_R = 5$ V) Schottky diodes in parallel for the secondary rectifiers. In implementations of the power stages with SR's, the Schottky diodes were replaced with IXYS IXFK100N10 ($V_{\rm RRM} = 100$ V, $R_{\rm DS(on)} = 11$ mΩ @ $T_j = 25$°C, $C_{\rm oss}^{\rm SR} = 3300$ pF @ $V_{\rm DS} = 25$ V, and $V_{\rm BD} = 1.1$ V) MOSFET's. The turns ratio of the transformer for the CCM implementation was $n = 64:10$ ($L_m = 637\ \mu$H), and the converter was operated in CCM at full load over the entire input line range with switching frequency $f_s = 100$ kHz [9]. The transformer used for all other implementations (CF DCM, VF DCM, and ZVS DCM) had a turns ratio of $n = 38:6$ ($L_m = 229\ \mu$H).

Fig. 7 shows the control and drive circuit for the variable frequency DCM flyback converter implementations with the SR. As can be seen from Fig. 7, the converter has a detector which senses zero crossings of secondary current $i_{\rm sec}$. The delay time between the zero crossing of secondary current $i_{\rm sec}$ and the turn off of the SR is set by the R-C time constant of the $T_{\rm delay}^{\rm ZVS}$ circuit which is connected to the output of the zero-crossing detector comparator. Resistors R_3 and R_4 are used to set the hysteresis of the zero-crossing detector. The VF control of the converter is achieved by employing the UC 3852 IC controller. Also, an R-C delay circuit is used on the primary side to set a proper delay between the turn off of the SR and the turn on of the primary switch. The UC3852 functional description, operation, and implementation in VF ZCS applications are thoroughly explained in [10].

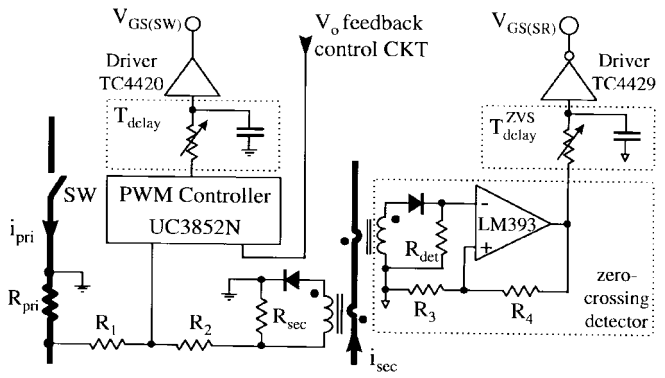


Fig. 7. Control and drive circuit for VF DCM flyback converter with SR. The thick lines belong to the power stage.

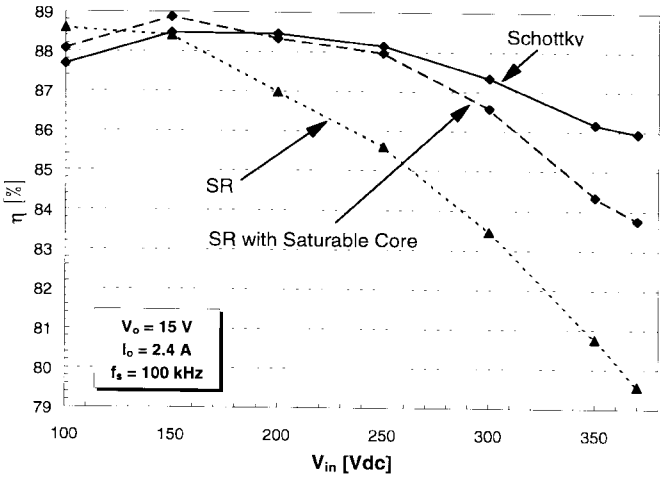


Fig. 8. Measured efficiencies of CF CCM implementation with SR and Schottkies rectifier at full power.

A. Constant-Frequency CCM

Fig. 8 shows the measured efficiencies of the CF CCM experimental converters with the Schottky diode and the SR. Because the SR body diode conducts current during delay times, $T_D^{\rm on}$ and $T_D^{\rm off}$ in Fig. 2, the rectifier turn-off loss becomes significant at high frequencies. In fact, in the experimental 100-kHz converter, the excessive rectifier turn-off loss in the SR converter exceeds the conduction loss savings. As predicted in Section III, the efficiency of the SR implementation is lower than that of the Schottky implementation, especially at high line, where the reverse recovery loss given by (4) is highest.

Fig. 9(a) shows the SR turn-off waveforms which are initiated by the primary switch SW turn on. The fast-rising voltage $V_{\rm DS(SR)}$ causes large superimposed capacitor charging and body reverse recovery currents. To suppress these currents, a saturable core was connected in series with the SR to slow down the rate of $V_{\rm DS(SR)}$ rise, as shown in Fig. 9(b). As can be seen from Fig. 9(b), with the saturable-core snubber, not only the reverse current amplitude was reduced significantly, but also the rectifier voltage stress was decreased. As a result, the conversion efficiency was improved, as can be seen in Fig. 8. However, this approach cannot completely eliminate the body diode reverse recovery problem. In fact, output capacitance of the SR $C_{\rm oss}^{\rm SR}$ is significantly higher than the junction capacitance of the two paralleled Schottky diodes $C_T (C_{\rm oss}^{\rm SR} = 3300$ pF versus $2C_T = 800$ pF), causing a higher capacitor charging loss according to (5). Therefore, at 36-W power level the CCM converter with the Schottky rectifier exhibits higher efficiency than that with the SR.

B. Constant-Frequency DCM

Fig. 10 shows an oscillogram with the key waveform of the CF DCM converter with the SR. During the resonant interval $T_{\rm DCM}$, $L_m - C_{\rm eq}$ resonance can be clearly seen in both $I_{\rm (SR)}$ and $V_{\rm DS(SW)}$ waveforms. The measurement points of the efficiency plot shown in Fig. 11 were collected at the valleys, $V_{\rm in} - nV_o$, and the peaks, $V_{\rm in} + nV_o$, of $V_{\rm DS(SW)}$. As can be seen from Fig. 11, the resonant peak points correspond to the lowest efficiencies, and the resonant valley points corresponds to the highest efficiencies. The SR and DR implementations have peaks and valleys at different time instants within a switching period because the resonant period in the SR converter is longer due to a higher $C_{\rm oss}$ value. Therefore, at certain input voltages, the SR efficiency is lower than that of Schottky and the efficiency improvement is not constant throughout the input range.

C. Variable-Frequency DCM and ZVS DCM

Figs. 12 and 13 show the measured waveforms of the VF DCM and ZVS DCM converters with the SR. As can be seen from Fig. 12, primary switch SW in the VF DCM implementation is turned on at a voltage lower than $V_{\rm in}$. To achieve the switch turn on with minimum voltage $V_{\rm DS(SW)}$, the delay time between the zero-crossing instant of $i_{\rm sec}$ and the turn on of the primary switch SW must be properly designed. Taking the nonlinear effect of the MOSFET output capacitance into consideration, i.e., recognizing that the output capacitance of the MOSFET is inversely proportional to the square root of the drain-to-source voltage [11], the equivalent capacitance of the resonant tank $L_m - C_{\rm eq}$ is

$$C_{\rm eq} = \frac{C_{\rm oss}^{\rm SR}}{n^2} \cdot \sqrt{\frac{25}{V_{\rm DS}^{\rm SR}}} + C_{\rm oss}^{\rm SW} \cdot \sqrt{\frac{25}{V_{\rm DS}^{\rm SW}}} \tag{15}$$

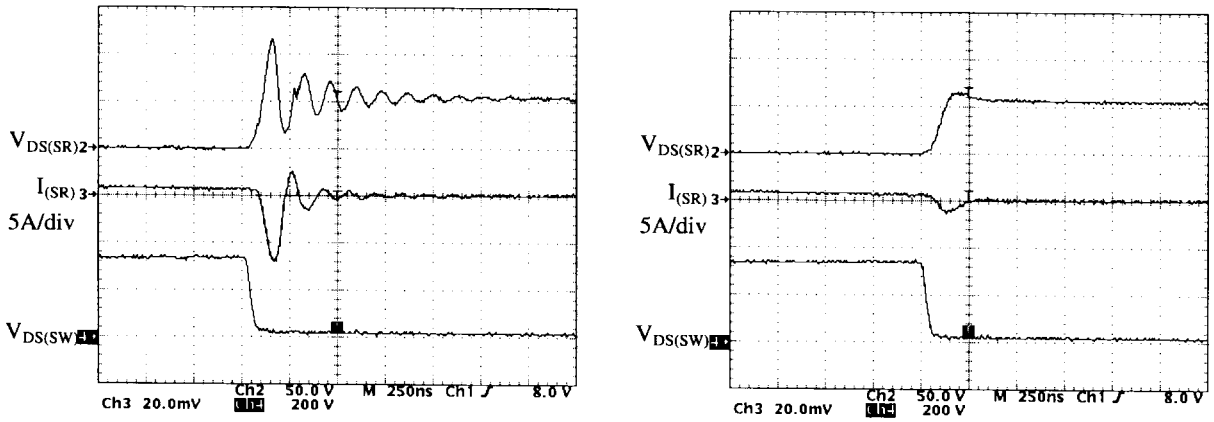
where $C_{\rm oss}^{\rm SR}$ and $C_{\rm oss}^{\rm SW}$ are the values of the output capacitances of the SR and the primary-switch MOSFET's at $V_{\rm DS}^{\rm SR} = V_{\rm DS}^{\rm SR} = 25$ V, respectively. Since for the experimental converter, $C_{\rm oss}^{\rm SR} = 3300$ pF and $C_{\rm oss}^{\rm SW} = 350$ pF, and since at the maximum input voltage $V_{\rm in} = 370$ V, $V_{\rm DS}^{\rm SR} = V_{\rm in}/n + V_o = 370/(38:6) + 15 = 73$ V and $V_{\rm DS}^{\rm SW} = V_{\rm in} + nV_o = 370 + (38:6)15 = 465$ V, and the value of $C_{\rm eq}$ in the experimental converter is

$$C_{\rm eq} = \frac{3300 \cdot 10^{-12}}{(38:6)^2} \cdot \sqrt{\frac{25}{73}} + 350 \cdot 10^{-12} \cdot \sqrt{\frac{25}{465}} \approx 106 \text{ pF}. \tag{16}$$

Therefore, according to (7), the turn-on delay of VF DCM converter with the SR was adjusted to

$$T_{\rm delay} = \pi \sqrt{229 \cdot 10^{-6} \cdot 106 \cdot 10^{-12}} = 0.5\ \mu\text{s} \tag{17}$$

as shown in Fig. 12.



(a) (b)

Fig. 9. SR turn-off waveforms of CF CCM converter with SR: (a) without saturable core and (b) with saturable core.

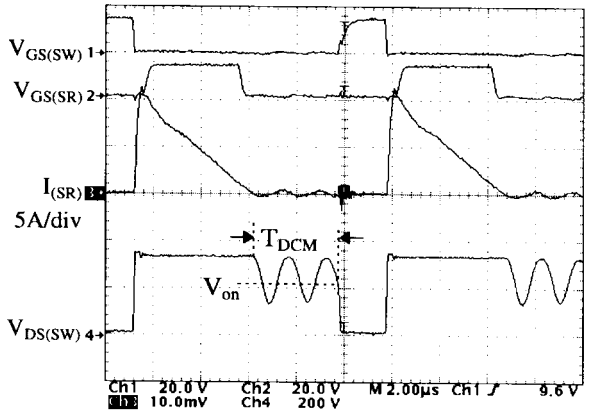


Fig. 10. Measured waveforms of CF DCM converter with SR at $V_{\rm in} = 250$ Vdc, $V_o = 15$ V, and $I_o = 2.4$ A.

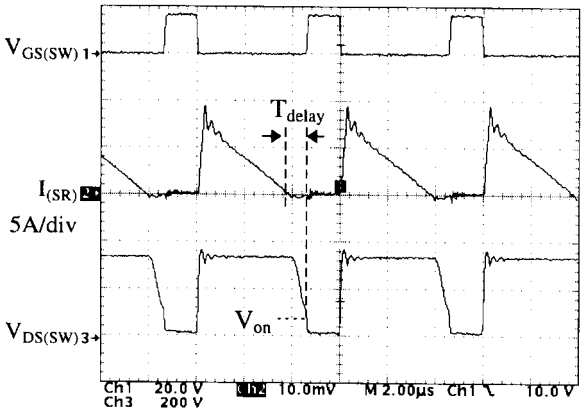


Fig. 12. Measured waveforms of VF DCM implementation with SR at $V_{\rm in} = 250$ Vdc, $V_o = 15$ V, and $I_o = 2.4$ A.

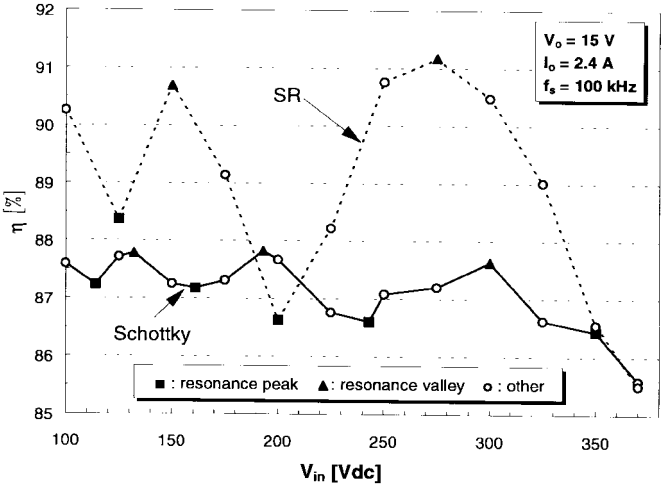


Fig. 11. Measured efficiency of CF DCM implementation with SR and Schottky at full power.

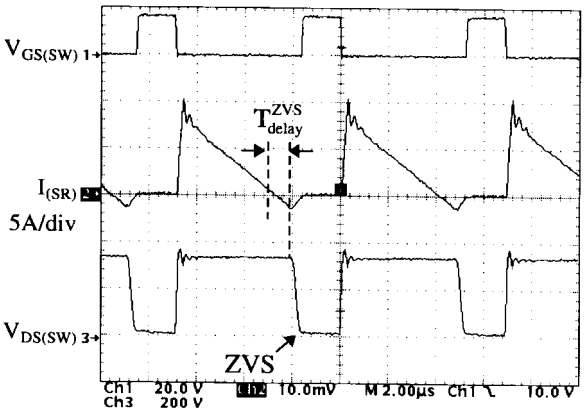


Fig. 13. Measured waveforms of ZVS DCM implementation at $V_{\rm in} = 250$ Vdc, $V_o = 15$ V, and $I_o = 2.4$ A.

It should be noted that $T_{\rm delay}$ changes with the input voltage since $C_{\rm eq}$ is a function of input voltage $V_{\rm in}$. However, the dependence of $C_{\rm eq}$ on $V_{\rm in}$ is relatively weak. Namely, in the experimental converter, the change $T_{\rm delay}$ in the entire input-voltage range from 100 to 370 V is less than 20%. Therefore, a simple low-cost drive circuit with a constant delay can be used in the implementations of the VF converters in Figs. 12 and 13 without significantly affecting their performance.

By eliminating the parasitic resonance during the $T_{\rm DCM}$ interval, the efficiency of the VF DCM implementation with the Schottky rectifier is 1% higher than the efficiency of the corresponding CF DCM implementation, as can be seen comparing measurements given in Figs. 11 and 14. Furthermore,

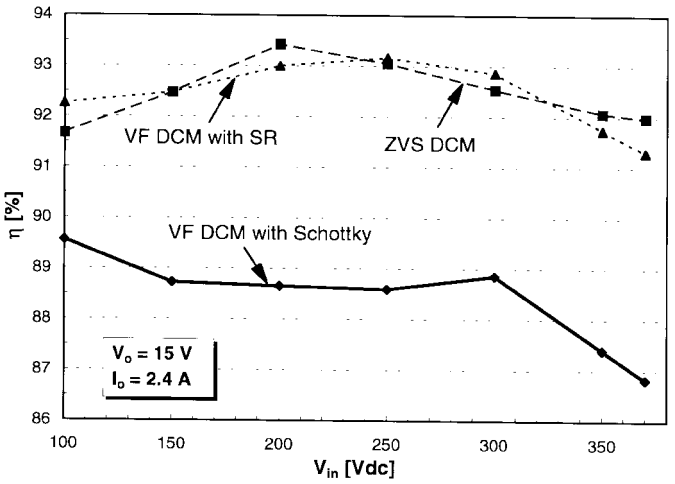


Fig. 14. Measured efficiencies of VF DCM implementations with SR and Schottky and ZVS DCM implementation at full power.

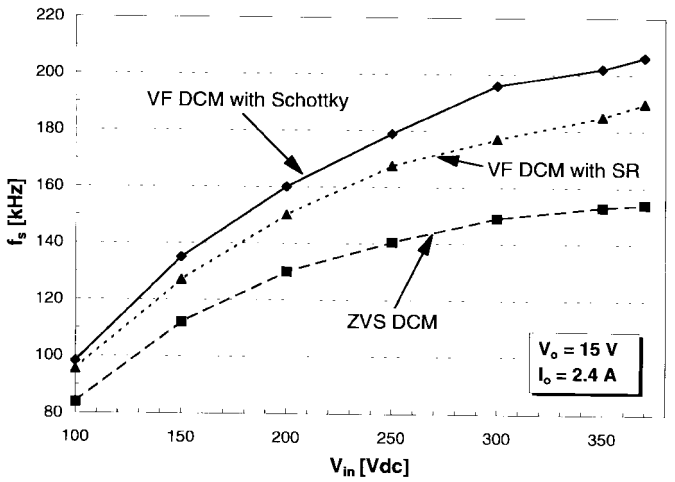


Fig. 15. Switching frequency comparison of VF DCM implementations with SR and Schottky and ZVS DCM implementation.

the efficiency comparisons in Fig. 14 shows that VF DCM implementation with the SR has a relatively constant 2.5%–4% efficiency improvement over VF DCM implementation with the Schottky, as has been predicted. However, in the VF DCM implementation, only partial ZVS can be achieved, since in this design, input voltage ($V_{\text{in}} = 100$–370 V) is larger than the reflected output voltage ($nV_o = 95$ V), i.e., $V_{\text{in}} > nV_o$.

Soft switching can be obtained for the entire input line range if secondary current i_{sec} is allowed to flow in the negative direction to the level I_{ZVS} given in (9), i.e.,

$$I_{\text{ZVS}} = \frac{(38:6)\cdot\sqrt{370^2-[(38:6)\cdot 15]^2}}{\sqrt{\frac{229\ \mu}{106\ p}}} = 1.5\text{ A}. \quad (18)$$

The required delay time for the secondary current to reach I_{ZVS} is

$$T_{\text{delay}}^{\text{ZVS}} = \frac{229\ \mu\cdot 1.5}{(38:6)^2\,15} = 0.6\ \mu\text{s} \quad (19)$$

as shown in Fig. 13.

The obtained efficiency of the ZVS DCM converter is very close to that of the VF DCM converter with the SR due to the increased conduction loss in the ZVS DCM converter. The switching frequencies of the three VF implementations are shown in Fig. 15. Because of the larger SR output capacitance and additional delay $T_{\text{delay}}^{\text{ZVS}}$ required to obtain I_{ZVS}, VF DCM converter with the Schottky has the highest switching frequency, while ZVS DCM implementation has the lowest switching frequency. Also, the switching frequency range in ZVS DCM implementation is the smallest due to the longest delay time.

V. Summary

It was shown that the VF DCM flyback converter implementation is most suitable for synchronous rectification. Moreover, this implementation can be easily designed to work with complete or partial ZVS of the primary switch by properly adjusting the delay time between the zero crossing of the secondary current and the turn-off instant of the SR. In off-line applications, the VF DCM flyback converter with a SR shows a typical efficiency improvement in the 2%–4% range compared to the corresponding circuit with a DR. While the 2%–4% efficiency improvement and the added circuit complexity may not justify the employment of the SR in low-cost low-performance (low-end) power supplies, the SR approach is a prudent choice in applications where it is required to achieve high-power densities with limited cooling as, for example, in ac/dc adapters for portable equipment. Generally, in high-power-density applications, the power density and reliability of a converter are in a large extent limited by the power dissipated within the converter's enclosure. Therefore, a 2%–4% efficiency improvement in an already 85% efficient converter, which translates into approximately 15%–40% reduction in the power loss, has a significant impact on the converter's size as well as thermal and reliability performance.

References

[1] M. W. Smith and K. Owyang, "Improving the efficiency of low output voltage switch-mode converters with synchronous rectification," in *Proc. POWERCON 7*, 1980, p. H-4.

[2] "MOSFET's move in on low voltage rectification," *MOSPOWER Applications Handbook*, Siliconix, Santa Clara, CA, 1984.

[3] J. A. Cobos, J. Sebastian, J. Uceda, E. de la Cruz, and J. M. Gras, "Study of the applicability of self-driven synchronous rectification to resonant topologies," in *IEEE Power Electron. Specialists' Conf. Rec.*, 1992, pp. 933–940.

[4] M. M. Jovanović, M. T. Zhang, and F. C. Lee, "Evaluation of synchronous-rectification efficiency improvement limits in forward converters," *IEEE Trans. Ind. Electron.*, vol. 42, no. 4, pp. 387–395, 1995.

[5] D. J. Harper, D. R. Hyde, G. M. Fry, and J. A. Houldsworth, "Controlled synchronous rectifier," in *High Freq. Power Conversion Conf. Proc.*, 1988, pp. 165–172.

[6] F. M. Barlage, "Synchronous rectification and regulation in multiple cross regulated outputs," in *High Freq. Power Conversion Conf. Proc.*, 1994, pp. 185–193.

[7] S. Ollero, E. De la Cruz, L. Alvarez, and C. Garcia, "New post-regulation and protection methods for multiple output power converters with synchronous rectification," in *Proc. IEEE Int. Telecommun. Energy Conf.*, 1996, pp. 462–469.

[8] Y. Khersonsky, M. Robinson, and D. Gutierrez, "New fast recovery diode technology cuts circuit losses, improves reliability," *Power Conversion Intelligent Motion*, vol. 18, pp. 16–25, May 1992.

[9] L. Huber and M. M. Jovanović, "Evaluation of flyback topologies for notebook ac/dc adapter/charger applications," in *High Freq. Power Conversion Conf. Proc.*, 1995, pp. 284–294.
[10] B. Andreycak, "Power factor correction using the UC3852 controlled on-time zero-current switching techniques," *Unitrode Product & Applications Handbook 1995–1996*, Application Note U-132, pp. 10-269–10-283.
[11] J. G. Kassakian, M. F. Schelcht, and G. C. Verghese, *Principle of Power Electronics*. Reading, MA: Addison-Wesley, 1991.

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