Design Considerations for Direct-Conversion Receivers

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***Abstract*— This paper describes the issues and tradeoffs in the design and monolithic implementation of direct-conversion receivers and proposes circuit techniques that can alleviate the drawbacks of this architecture. Following a brief study of heterodyne and image-reject topologies, the direct-conversion architecture is introduced and effects such as dc offset, I/Q mismatch, even-order distortion, flicker noise, and oscillator leakage are analyzed. Related design techniques for amplification and mixing, quadrature phase calibration, and baseband processing are also described.**

***Index Terms*— Analog circuits, RF circuits, receivers, wireless transceivers.**

I. Introduction

THE RECENT SURGE in applications of radio-frequency (RF) transceivers has been accompanied with aggressive design goals: low cost, low power dissipation, and small form factor. Together with the usual bandwidth and sensitivity limitations, these goals call for circuit and architecture breakthroughs. Moreover, as integrated circuit (IC) technologies embrace more parts of RF systems, transceiver architectures that once seemed impractical may return as plausible solutions.

Direct conversion (called herein "dicon" for brevity) was invented many decades ago, has been tried many times, and has failed almost every time. Nevertheless, this architecture has recently become the topic of active research again [1]–[5], perhaps to a much greater extent than before. Several reasons account for this renaissance: 1) dicon, in principle, lends itself to monolithic integration much more easily than do heterodyne receivers; 2) dicon suffers much less from mismatch-induced effects than do image-reject architectures; 3) dicon's past failures arose primarily from effects that could not be removed in *discrete* implementations, but may be controlled and suppressed in integrated circuits. In other words, dicon is one of few reception techniques whose drawbacks can be remedied through the use of only more transistors.

The goal of this paper is to describe the issues and tradeoffs in the design of direct-conversion receivers (DCR's) and propose possible circuit techniques that can relax the limitations of this architecture. In Section II, we briefly study the limitations of heterodyne and image-reject architectures and in Section III the dicon topology. In Section IV, we analyze design issues such as dc offset, I/Q mismatch, even-order distortion, flicker noise, and oscillator leakage. Finally, in Section V we present circuit techniques for RF amplification and mixing, quadrature phase calibration, and baseband processing.

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II. Heterodyne and Image-Reject Receivers

In order to appreciate the advantages of DCR's, let us briefly review the difficulties in heterodyne and image-reject architectures.

Fig. 1 shows a simple heterodyne receiver. The RF signal is applied to a low-noise amplifier (LNA) and subsequently an image-reject filter. The result is mixed with the output of a local oscillator (LO), thus producing the intermediate-frequency (IF) signal. The IF filter suppresses out-of-channel interferers, performing channel selection.

The principal issue in heterodyning is the tradeoff between image rejection and adjacent channel suppression. As illustrated in Fig. 1, for given filter quality factors (Qs) and losses, if the IF is high, the image is greatly attenuated whereas nearby interferers remain at significant levels. Conversely, if the IF is low, the image corrupts the downconverted signal but the interferers are suppressed. For this reason, both the image-reject filter and the IF filter require highly selective transfer functions that are impractical in today's IC technologies. The solution has been to employ external, bulky filters such as surface acoustic wave (SAW) devices. Furthermore, most systems utilize two IF's so as to achieve an acceptable compromise between the two rejections.

Another important drawback of heterodyne receivers is that the LNA must drive a 50-Ω load because the image-reject filter is placed off-chip. This adds another dimension to the tradeoffs among noise, linearity, gain, and power dissipation of the amplifier.

The tradeoff depicted in Fig. 1 can be alleviated through the use of image-reject architectures. Two examples based on the Hartley [6] and Weaver [7] topologies are shown in Fig. 2. It can be shown that the spectra at points A and B contain the desired signal with the same polarity and the image with opposite polarity [8]. Thus, in the ideal case the summed output is free from the image.

The primary issue in the architectures of Fig. 2 is imperfect image rejection resulting from gain and phase mismatches between the upper and lower signal paths. With one page of algebra, it can be proved [8] that the image rejection ratio, IRR, is given by

$$\mathrm{IRR} = \frac{1 - a(1+\epsilon)\cos\theta + (1+\epsilon)^2}{1 + a(1+\epsilon)\cos\theta + (1+\epsilon)^2} \tag{1}$$

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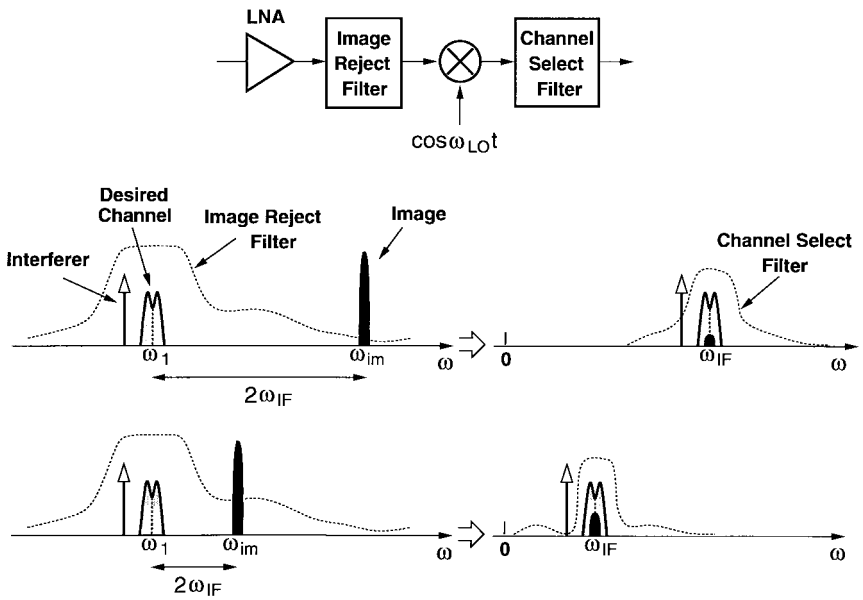

Fig. 1. Simple heterodyne receiver.

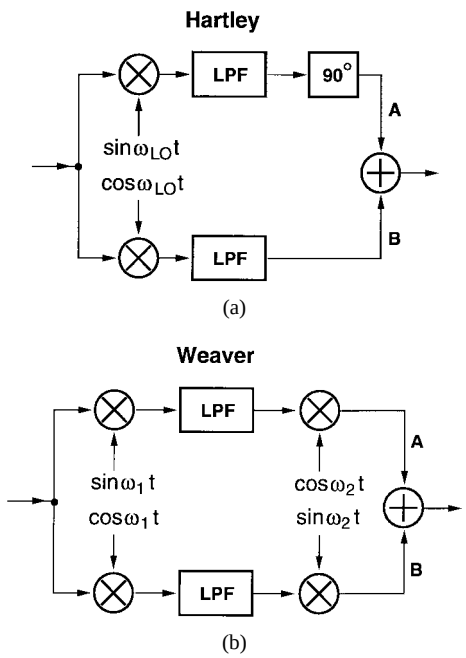

Fig. 2. Hartley and Weaver image-reject architectures.

where ϵ denotes the relative voltage gain mismatch and θ the phase imbalance. For small ϵ and θ, (1) reduces to

$$\mathrm{IRR} = \frac{\epsilon^2 + \theta^2}{4} \tag{2}$$

where θ is in radians. For example, if $\epsilon = 5\%$ and $\theta = 5°$, then $\mathrm{IRR} \approx 26$ dB. If the circuit is to achieve 60 dB of image suppression, then θ must remain below 0.1°, a value difficult to attain in typical IC technologies. In practice, these architectures exhibit an IRR of 30–40 dB [9].

III. Direct-Conversion Architecture

Direct conversion, also called zero-IF or homodyne conversion, is the natural approach to downconverting a signal from RF to baseband. A DCR translates the band of interest directly to zero frequency and employs low-pass filtering to suppress nearby interferers, as shown in Fig. 3. The quadrature I and Q channels are necessary in typical phase- and frequency-modulated signals because the two sidebands of the RF spectrum contain different information and result in irreversible corruption if they overlap each other without being separated into two phases.

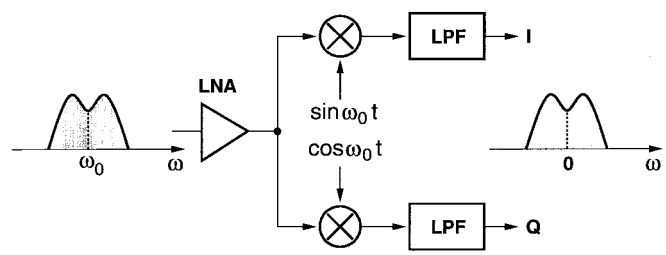

Fig. 3. Direct-conversion architecture.

Direct conversion has several advantages over heterodyning. First, the problem of image is circumvented because the IF is zero. Second, the LNA need not drive a 50-Ω load because no image rejection filter is required. Third, the IF SAW filter and subsequent stages are replaced with low-pass filters (LPF's) and baseband amplifiers that are amenable to monolithic integration.

If the dicon architecture is so simple, why has it not become popular in RF systems? Direct translation of the spectrum to zero frequency entails a number of issues that do not exist or are not as serious in a heterodyne receiver.

IV. Design Issues

A. DC Offsets

Since in a dicon architecture the downconverted band extends to zero frequency, extraneous offset voltages can corrupt the signal and, more importantly, saturate the following stages.

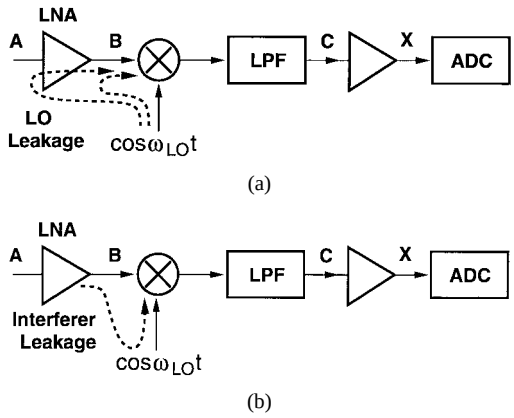

Fig. 4. Self-mixing of (a) LO. (b) Interferers.

To understand the origin and impact of offsets, consider the receiver shown in Fig. 4, where the LPF is followed by an amplifier and an analog-to-digital converter (ADC). Let us make two observations.

First, the isolation between the LO port and the inputs of the mixer and the LNA is not perfect, i.e., a finite amount of feedthrough exists from the LO port to points A and B [Fig. 4(a)]. Called "LO leakage," this effect arises from capacitive and substrate coupling and, if the LO signal is provided externally, bond wire coupling. The leakage signal appearing at the inputs of the LNA and the mixer is now *mixed* with the LO signal, thus producing a dc component at point C. This phenomenon is called "self-mixing." A similar effect occurs if a large interferer leaks from the LNA or mixer input to the LO port and is multiplied by itself [Fig. 4(b)].

Second, the total gain from the antenna to point X is typically around 100 dB so as to amplify the microvolt input signal to a level that can be digitized by a low cost, low power ADC. Of this gain, typically 25 to 30 dB is contributed by the LNA/mixer combination.

With the above observations, we can obtain a rough estimate of the offset resulting from self-mixing to appreciate the problem. Suppose in Fig. 4(a) the LO signal has a peak-to-peak swing of 0.63 V ($\approx$0 dBm in a 50-Ω system) and experiences an attenuation of 60 dB as it couples to point A. If the gain of the LNA/mixer is 30 dB, then the offset produced at the output of the mixer is on the order of 10 mV. We also note that the desired signal level at this point can be as low as approximately 30 $\mu\mathrm{V}_{\mathrm{rms}}$. Thus, if directly amplified by the remaining gain of 70 dB, the offset voltage saturates the following circuits, thereby prohibiting the amplification of the desired signal.

The problem of offset is exacerbated if self-mixing varies with time. This occurs when the LO signal leaks to the antenna and is radiated and subsequently reflected from moving objects back to the receiver. For example, when a car moves at a high speed, the reflections may change rapidly.

From the above discussion, we infer that DCR's require some means of offset removal or cancellation.

AC Coupling: A possible approach to removing the offset is to employ ac coupling, i.e., high-pass filtering, in the downconverted signal path. However, since the spectrum of random binary (or M-ary) data exhibits a peak at dc, such signals may be corrupted if filtered with a high corner frequency. Simulations indicate that, in the absence of noise and frequency offset, the corner frequency of the high-pass filter (HPF) must be less than 0.1% of the data rate for the signal degradation to be negligible. Thus, in IS-54, for example, a data rate of 48.6 kb/s mandates a corner frequency less than 50 Hz. Such a low value yields a slow response to variations in the offset and requires prohibitively large capacitors and resistors.

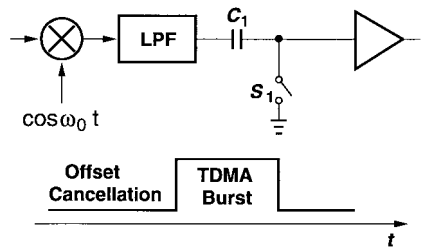

Fig. 5. Offset cancellation in a TDMA system.

A low corner frequency in the HPF may also lead to temporary loss of data in the presence of wrong initial conditions. If no data is received for a relatively long time, the output dc voltage of the HPF droops to zero. Now if data is applied, the time constant of the filter causes the first several bits to be greatly offset with respect to the detector threshold, thereby introducing errors.

A possible solution to the above problems is to minimize the signal energy near dc by choosing "dc-free" modulation schemes. A simple example is the type of binary frequency shift keying (BFSK) used in pager applications [5].

Offset Cancellation: In wireless standards that incorporate time-division multiple access (TDMA), each mobile station periodically enters an idle mode so as to allow other users to communicate with the base station. The offset in the receive path can be stored on a capacitor during this mode and subtracted from the signal during actual reception. Fig. 5 shows a simple example, where capacitor C_1 stores the offset between consecutive TDMA bursts while introducing a virtually zero corner frequency during the reception of data. For typical TDMA frame rates, offset cancellation is performed frequently enough to compensate variations due to moving objects.

The major issue in the circuit of Fig. 5 is the thermal noise of S_1 (kT/C noise). For example, if a 1-$\mu\mathrm{V}_{\mathrm{rms}}$ signal received at the antenna experiences a gain of 30 dB before offset cancellation, then C_1 must be at least 200 pF so that kT/C remains 15 dB below the signal level. If the signal path is differential, then two capacitors, each equal to 400 pF, are required so that the overall kT/C noise is still 15 dB below the signal. Thus, with I and Q channels, the total capacitance reaches 1.6 nF. Note that since C_1 is a floating capacitor, it cannot be easily implemented with MOS transistors. Nonpolar structures providing so much capacitance typically occupy a very large area.

A general difficulty with offset cancellation in a receiver is that interferers may be stored along with offsets. This occurs because reflections of the LO signal from nearby objects must be included in offset cancellation and hence

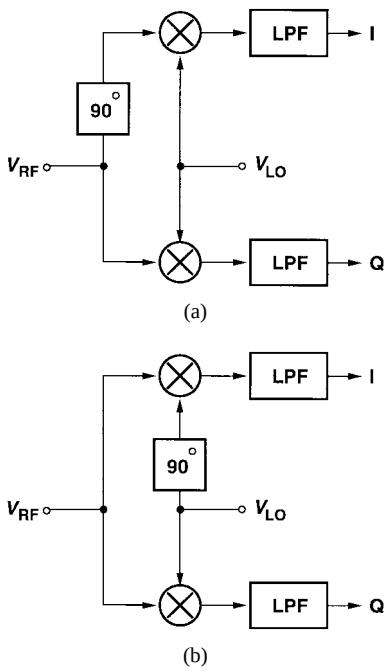

Fig. 6. Quadrature generation in (a) RF path. (b) LO path.

the antenna cannot be disconnected (or "shorted") during this period. While the timing of the actual signal (the TDMA burst) is well-defined, interferers can appear any time. A possible approach to alleviating this issue is to sample the offset (and the interferer) several times and average the results.

Other methods of dealing with offsets are described in [10] and [11].

B. I/Q Mismatch

As shown in Fig. 3, for most phase and frequency modulation schemes, a DCR must incorporate quadrature downconversion. This requires shifting either the RF signal or the LO output by 90° (Fig. 6). Since shifting the RF signal generally entails severe noise-power-gain tradeoffs, it is desirable to use the topology in Fig. 6(b). In either case, the errors in the nominally 90° phase shift and mismatches between the amplitudes of the I and Q signals corrupt the downconverted signal constellation, thereby raising the bit error rate. Note that all sections of the circuit in the I and Q paths contribute gain and phase error.

To gain more insight into the effect of I/Q imbalance, suppose the received signal $x_{\text{in}}(t) = a\cos\omega_C t + b\sin\omega_C t$, where a and b are either -1 or $+1$. Now let us assume that the I and Q phases of the LO signal are equal to

$$x_{\text{LO},I}(t) = 2\cos\omega_C t$$
$$x_{\text{LO},Q}(t) = 2(1+\epsilon)\sin(\omega_C t + \theta)$$

where the factor 2 is included to simplify the results and ϵ and θ represent gain and phase errors, respectively. Multiplying $x_{\text{in}}(t)$ by the two LO phases and low-pass filtering the result, we obtain the following baseband signals:

$$x_{BB,I}(t) = a \tag{3}$$
$$x_{BB,Q}(t) = (1+\epsilon)b\cos\theta - (1+\epsilon)a\sin\theta. \tag{4}$$

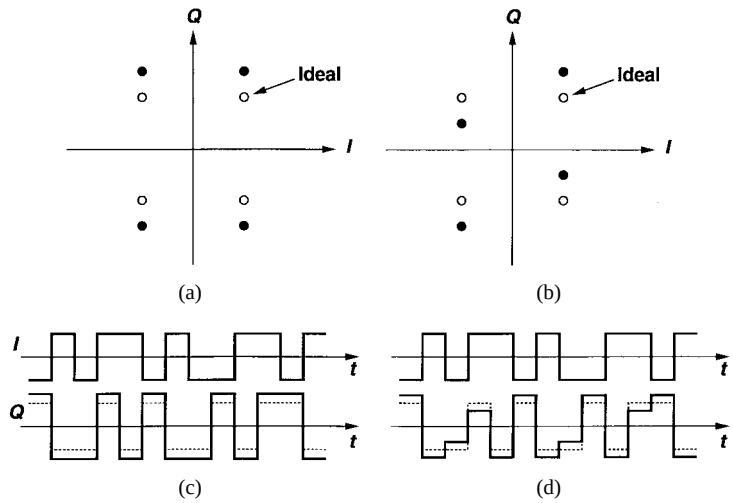

Fig. 7. Effect of I/Q mismatch. Constellation (a) with gain error.; (b) with phase error. Time-domain waveforms (c) with gain error; (d) with phase error.

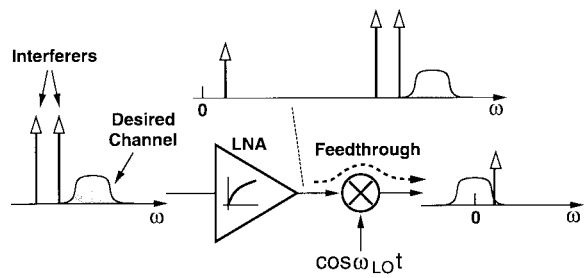

Fig. 8. Effect of even-order distortion on interferers.

Fig. 7(a) and (b) shows the resulting signal constellation with finite ϵ or θ. This effect can be better seen by examining the downconverted signals in the time domain [Fig. 7(c) and (d)]. Gain error simply appears as a nonunity scale factor in the amplitude. Phase imbalance, on the other hand, corrupts one channel with a fraction of the data pulses in the other channel, in essence degrading the signal-to-noise ratio if the I and Q data streams are uncorrelated.

The problem of I/Q mismatch has been a major obstacle in discrete designs, but it tends to decrease with higher levels of integration. The key point, however, is that I/Q mismatch is much less troublesome in DCR's than in image-reject architectures. A 5° phase imbalance degrades the SNR by roughly 1 dB in the former while yielding an image rejection of only 27 dB in the latter.

C. Even-Order Distortion

Typical RF receivers are susceptible to only odd-order intermodulation effects. In direct conversion, on the other hand, even-order distortion also becomes problematic. Suppose, as illustrated in Fig. 8, two strong interferers close to the channel of interest experience a nonlinearity such as $y(t) = \alpha_1 x(t) + \alpha_2 x^2(t)$ in the LNA. If $x(t) = A_1\cos\omega_1 t + A_2\cos\omega_2 t$, then $y(t)$ contains a term: $\alpha_2 A_1 A_2 \cos(\omega_1 - \omega_2)t$, indicating that two high-frequency interferers generate a low-frequency beat in the presence of even-order distortion.

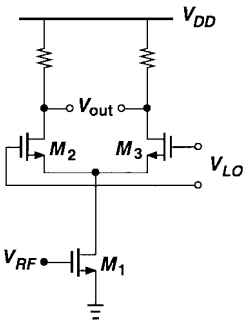

Fig. 9. Single-balanced mixer.

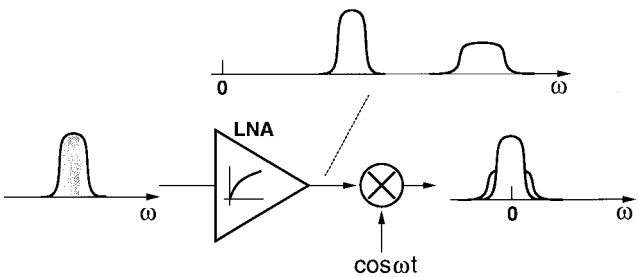

Fig. 10. Downconversion of signal harmonics.

Upon multiplication by $\cos\omega_{\rm LO}t$ in an *ideal* mixer, such a term is translated to high frequencies and hence becomes unimportant. In reality, however, mixers exhibit a finite direct feedthrough from the RF input to the IF output. For example, in the single-balanced mixer of Fig. 9, mismatches between M_2 and M_3 and the deviation of the LO duty cycle from 50% create asymmetry in the circuit, thereby producing an output signal such as $v_{\rm RF}(t)(a + A\cos\omega_{\rm LO}t)$. Thus, a fraction of $v_{\rm RF}(t)$—on the order of 1% in IC technologies—appears at the output with no frequency translation.

The even-order distortion phenomenon can be studied from another point of view. Suppose in addition to phase or frequency modulation, the received signal exhibits some amplitude modulation (AM) as well. This could arise from filtering in the transmitter or disturbance and fading during propagation. If $x_{\rm in}(t) = (A + \epsilon\cos\omega_m t)(a\cos\omega_C t + b\sin\omega_C t)$, where $\epsilon\cos\omega_m t$ represents a low-frequency amplitude-modulating signal, then second-order distortion yields a term such as $(a^2 + b^2)A\epsilon\cos\omega_m t$. Since this term is a baseband signal, it is often said that even-order distortion demodulates AM components. As mentioned above, this signal passes through the mixer with finite attenuation, thereby corrupting the downconverted signal of interest.

Another manifestation of second-order nonlinearity is the second harmonic of the desired RF signal, which is downconverted to the baseband if mixed with the second harmonic of the LO output (Fig. 10). This effect arises for higher harmonics as well, but it is negligible in differential mixers because the magnitude of the harmonics of both the RF signal and the LO is inversely proportional to the frequency.

In our illustration here, we have assumed that only the LNA exhibits even-order distortion. In practice, the mixer RF port may also suffer from the same effect, requiring special attention in the design because the signals applied to the mixer are already amplified by the LNA and can create significant distortion.

Second-order nonlinearity can be characterized using the "second intercept point," IP_2. In a manner similar to the definition of the third intercept point (IP_3), two equal-amplitude interferers are applied at the input and their low-frequency beat signal is observed at the output. Plotting the beat signal power versus the input power and extrapolating the results yield the IP_2.

Can we use differential LNA's and mixers to suppress even-order distortion? Two issues must be considered here. First, the antenna and the duplexer filter are usually single-ended because they must operate with single-ended power amplifiers in the transmit path. Thus, a means of converting the received signal to differential form is necessary. The difficulty is that such means, e.g., transformers, typically exhibit several decibels of loss at high frequencies, thus directly raising the overall noise figure. Second, if the LNA is designed as a differential circuit, it requires higher power dissipation than the single-ended counterpart to achieve a comparable noise figure.

A simple differential pair may seem a feasible solution for converting the single-ended RF signal to differential form. However, such a configuration fails to fully suppress even-order distortion because high-frequency signals experience different delays (and gains) from one input to the two outputs.

D. Flicker Noise

With a typical gain of roughly 30 dB in the LNA/mixer combination, the downconverted signal usually falls in the range of tens of microvolts. The input noise of the following stages, e.g., amplifiers and filters, is therefore still critical. In particular, since the downconverted spectrum is located around zero frequency, the $1/f$ noise of devices has a profound effect on the signal, a severe problem in MOS implementations.

To gain a better feeling about the effect of $1/f$ noise, let us estimate the input-referred noise voltage of a single MOS transistor in common-source configuration with and without this type of noise. In typical submicron MOS technologies, minimum-channel MOSFET's with a width of a few hundred microns and bias current of a few hundred microamperes exhibit a $1/f$ noise corner frequency in the vicinity of 1 MHz. Thus, we can write

$$\frac{K}{WLC_{\rm ox}} \cdot \frac{1}{f}\bigg|_{f\approx 1\,\rm MHz} \approx 4kT\frac{2}{3g_m}. \tag{5}$$

We calculate the total flicker noise power in a bandwidth from 10 Hz to 200 kHz:

$$P_{n1} = \int_{10\,\rm Hz}^{200\,\rm kHz} \frac{K}{WLC_{\rm ox}}\frac{df}{f} \tag{6}$$

$$= \frac{K}{WLC_{\rm ox}}\ln(2\times 10^4) \tag{7}$$

$$= 4kT\frac{2}{3g_m}(1\,\rm MHz)\ln(2\times 10^4). \tag{8}$$

With only thermal noise, we have

$$P_{n2} = \int_{10\,\mathrm{Hz}}^{200\,\mathrm{kHz}} 4kT\frac{2}{3g_m}\,df \tag{9}$$

$$\approx 4kT\frac{2}{3g_m}(2\times 10^5). \tag{10}$$

Thus, the relative increase in the noise power is $P_{n1}/P_{n2} = 49.5 = 16.9$ dB.

The effect of flicker noise can be reduced by a combination of techniques. As the stages following the mixer operate at relatively low frequencies, they can incorporate very large devices (several thousand microns wide) to minimize the magnitude of the flicker noise. Moreover, periodic offset cancellation also suppresses low-frequency noise components through correlated double sampling.

E. LO Leakage

In addition to introducing dc offsets, leakage of the LO signal to the antenna and radiation therefrom creates interference in the band of *other* receivers [12]. Each wireless standard and the regulations of the Federal Communications Commission (FCC) impose upper bounds on the amount of *in-band* LO radiation, typically between −50 and −80 dBm. The issue is less severe in heterodyne and image-reject mixers because their LO frequency usually falls out of the reception band.

The problem of LO leakage becomes less serious as more sections of RF transceivers are fabricated on the same chip. With differential local oscillators, the net coupling to the antenna can approach acceptably low levels.

V. Design Techniques

A. LNA/Mixer Design

As explained in Section IV-C, it is difficult to eliminate even-order distortion by incorporating differential circuits in the RF signal path. A more practical alternative is to suppress the resulting low-frequency components *after* the signal experiences nonlinearity. As an example, consider the mixer shown in Fig. 11 [13], where capacitive degeneration and ac coupling substantially reduce the gain at low frequencies. The impedance of C_1 is negligible at RF to avoid noise differentiation [13] but relatively large at baseband frequencies. Note that the circuit following C_2 is differential and hence much less susceptible to even-order distortion.

The possibility of implementing highly-linear passive mixers in CMOS [14] makes these configurations an attractive alternative to active mixers. In DCR's, however, it is important that the gain of the LNA/mixer be sufficient to overcome the flicker noise of the baseband stages. Since passive mixers exhibit substantial loss and hence would require a prohibitively large gain in the LNA, active mixers are more suitable to DCR's.

A 3-V LNA/mixer circuit designed for dicon reception is shown in Fig. 12. The LNA consists of a cascode stage, Q_1 and Q_2, and the mixer is a single-balanced topology comprising Q_3–Q_5. In order to linearize the circuit without increasing the noise, capacitor C_2 feeds the voltage at the emitter of Q_3 back to the base of Q_1. It can be shown that the small-signal collector current of Q_3 is roughly equal to $V_{\mathrm{RF}}C_1 s$, indicating relatively high linearity in the voltage-to-current conversion required for the mixer. Note that capacitive degeneration of Q_3 heavily attenuates low-frequency beat components created by even-order distortion.

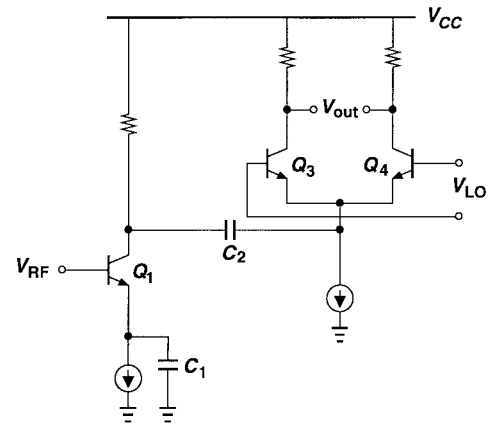

Fig. 11. Mixer with capacitive degeneration.

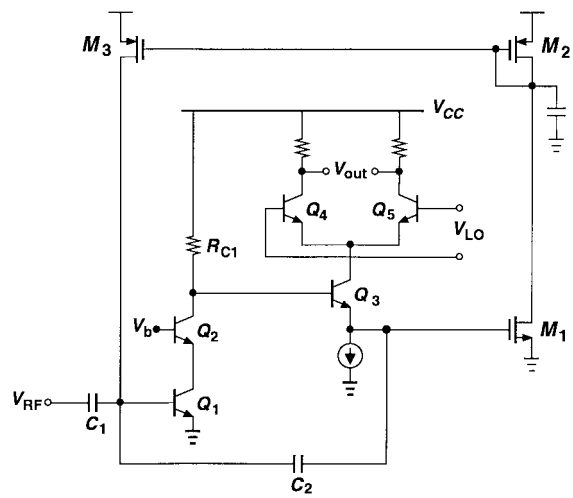

Fig. 12. LNA/mixer circuit with capacitive feedback.

The MOS bias network in Fig. 12 adjusts the base current of Q_1 such that the voltage at the emitter of Q_3 is equal to V_{GS1} ($\approx V_{THN}$ at low current levels). Since M_3 carries a small current and can have a V_{DS} of approximately 2 V, its transconductance and hence noise current are quite small.

B. I/Q Calibration

As I/Q mismatches vary negligibly with time, analog or digital calibration techniques can be employed to reduce their effect. An example where the phase imbalance is corrected is shown in Fig. 13. The circuit operates as follows. In the calibration mode, the main LNA, A_1, is disabled and amplifier A_2 injects onto node X a sinusoidal tone with a frequency slightly different from ω_{LO}. The downconverted quadrature signals are low-pass filtered and subsequently mixed so as to yield a dc voltage proportional to their phase difference. This voltage then adjusts the phase shift of delay lines Δ_1 and Δ_2

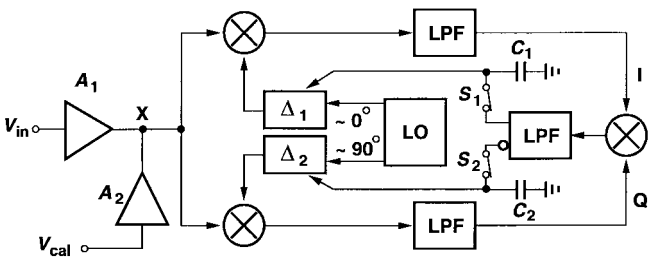

Fig. 13. Calibration of I/Q phase mismatch.

such that the phase difference between the I and Q signals approaches 90°. At the end of calibration, S_1 and S_2 turn off, C_1 and C_2 store the proper voltage, A_2 is disabled, and A_1 is enabled.

In order to minimize the phase noise of Δ_1 and Δ_2, the LO must provide nominally quadrature phases so that the delay lines perform only a small adjustment. Various approaches to quadrature generation are described in [5] and [15].

C. RF/Baseband Interface

After the signal is downconverted to the baseband, it must be filtered, amplified, and digitized, but not necessarily in that order. Consider the interface between the mixer and the first baseband stage [Fig. 14(a)]. We make three observations. First, at this point the signals are still quite small (in the range of tens of microvolts) and the interferers quite large (e.g., 60 dB above the signal level). Thus, both the noise and the nonlinearity of A_1 are critical. Second, to avoid lowering the voltage gain of the mixer, A_1 must exhibit a relatively high input impedance. Third, resistive feedback techniques such as that of Fig. 14(b) suffer from severe tradeoffs among noise, input resistance, and power dissipation. Moreover, high-input impedance amplifiers such as that shown in Fig. 14(c) exhibit substantial noise because of the contributions of the two amplifiers.

With the above in mind, let us consider the three permutations depicted in Fig. 15. In Fig. 15(a), a low-pass filter suppresses out-of-channel interferers, allowing A_1 to be a nonlinear, high-gain amplifier and the ADC to have a moderate dynamic range (roughly 4 to 8 b depending on the gain control in the RF domain and the type of modulation). However, the low-pass filter becomes problematic. Fig. 16(a) shows a representative input stage of a continuous-time LPF, indicating a tradeoff between the input impedance and the noise. In the switched-capacitor counterpart of Fig. 16(b), the kT/C noise mandates the use of very large capacitors.

The second permutation, shown in Fig. 15(b), relaxes the LPF noise requirements while demanding a higher performance in the amplifier. A typical one-stage differential amplifier may be utilized here to provide a gain of 20 dB before channel filtering. Furthermore, another amplifier may be interposed between the LPF and the ADC to overcome the noise of the latter.

The third permutation, Fig. 15(c), suggests the possibility of channel filtering in the digital domain. In this case, the ADC must both achieve a high linearity so as to digitize the signal with minimal intermodulation of interferers and exhibit a thermal and quantization noise floor well below the signal level, which is in the range of a few hundred microvolts.

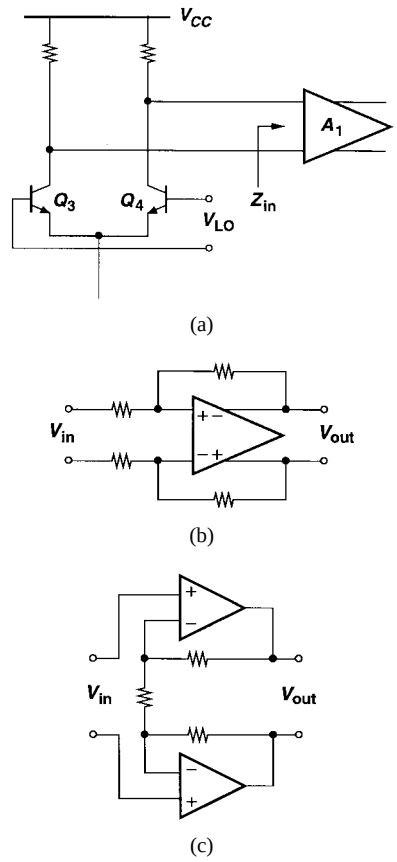

Fig. 14. (a) Interface between mixer and baseband. (b) Baseband amplifier with shunt feedback. (c) Baseband amplifier with series feedback.

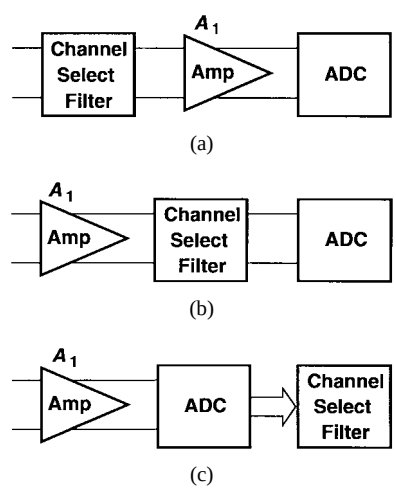

Fig. 15. Three permutations of filtering, amplification, and A/D conversion in baseband processing.

In order to achieve a noise floor of a few tens of microvolts, oversampled $\Sigma\Delta$ converters can be used. Since noise shaping in effect divides the kT/C and op amp noise by the oversampling ratio, these converters are particularly well-suited to the approach depicted in Fig. 15(c). For a signal bandwidth of 200 kHz, a second- or third-order modulator with an oversampling ratio of 64 appears practical in today's CMOS technologies.

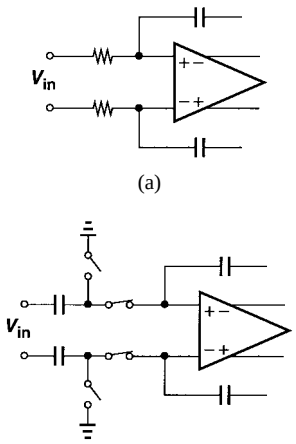

Fig. 16. Representative input stages of (a) continuous-time and (b) switched-capacitor low-pass filters.

In the three permutations studied above, no offset cancellation is included. If the ADC noise floor is low enough so that only one gain stage appears after the mixer, then the offset voltage remains relatively small (on the order of 50 mV) and need not be removed in the analog domain. In view of the difficulties described in Section IV-A, this greatly simplifies the design.

VI. Conclusion

Direct conversion exhibits potential for compact, low power implementation of RF receivers. While dicon systems entail a number of design issues that are less problematic in other architectures, greater circuit sophistication can alleviate such drawbacks.

Direct conversion is presently limited to a few applications [4], e.g., pager receivers [16], [17], but new circuit and algorithmic techniques along with higher levels of integration can make it an accepatable choice for various RF systems.

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