Design Considerations for Stacked Class-E-like mmWave High-Speed Power DACs in CMOS

Anandaroop Chakrabarti and Harish Krishnaswamy
Department of Electrical Engineering, Columbia University, New York, NY-10027

***Abstract*—This work describes design considerations for realizing high power mmWave DACs with high efficiency under modulation based on switching-PA DAC cells. A stacked Class-E-like SOI CMOS power amplifier is turned ON/OFF by means of digital circuitry to sustain high-speed 1-bit ASK (OOK) modulation, while high average efficiency is achieved by means of supply-switching. Factors affecting modulation speed, dynamic power dissipation, impact of digital path delays and supply/ground bounce are discussed and design guidelines are provided. A fully-integrated 47GHz prototype has been fabricated in IBM's 45nm SOI CMOS technology. Measurement results yield a saturated output power of 18.2 dBm with a peak PAE of 15.3% under static (continuous-wave) operation, and high-speed OOK modulation (upto 1Gbps and beyond) is demonstrated with high average efficiency.**

I. Introduction

There has been significant progress of late towards the implementation of high-power, high-efficiency mmWave power amplifiers in scaled CMOS through techniques such as switch-mode operation and series stacking of devices [1], [4] as well as power combining [2], [3]. Recently, a 0.5W PA was demonstrated in the Q-band using a single-step, 8-way, low-loss lumped quarter-wave power combiner and stacked Class-E-like PA unit cells [3]. Achieving high-efficiency not only at P_{sat} but also under backoff remains a significant challenge, and is crucial for complex modulation schemes with high peak-to-average power ratio (PAPR). Recently, high-power high-efficiency mmWave Digital-to-Analog-Converter (DAC) cells have been proposed [4] which either operate in saturated output power mode or turn off to maximize average efficiency. Several such mmWave power DAC unit cells can be combined in a large-scale, on-chip/free-space power-combining architecture (Fig. 1(a)) to realize a power DAC with multi-bit resolution and high efficiency under backoff. Depending on the nature of the combiner (isolating versus non-isolating), load modulation effects may be observed which can be exploited for benefit to linearize the DAC [3].

This work describes design considerations for the realization of mmWave power DAC cells. Factors affecting modulation speed, dynamic power dissipation, impact of digital path delays and supply/ground bounce are discussed in detail. The PA unit cell is augmented with digital circuitry at strategic locations in order to facilitate high-speed 1-bit ASK (OOK) modulation. Furthermore, a supply switch is used to eliminate power consumption when the PA is turned off. A 47GHz prototype demonstrating the concept has been fabricated in IBM's 45nm SOI CMOS technology.

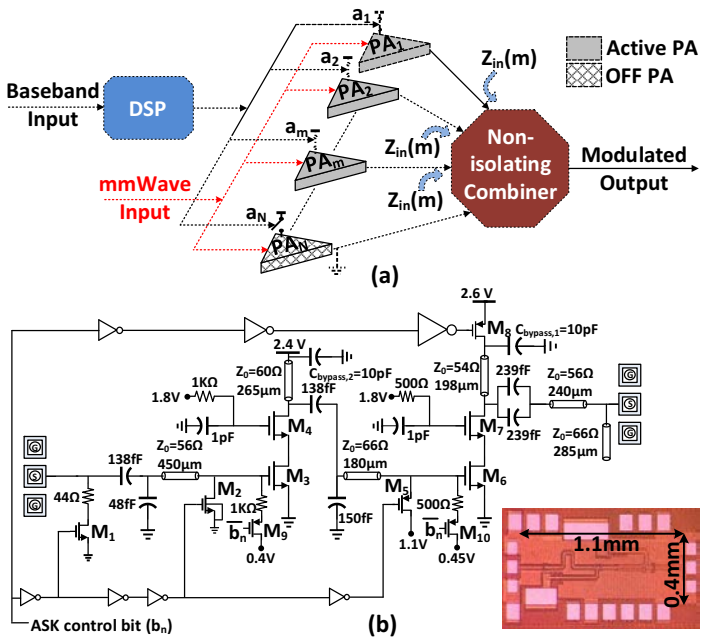

Fig. 1. (a) mmWave power-combined DAC employing multiple 1-bit supply-switched DAC cells, (b) Schematic and chip microphotograph of the implemented 1-bit mmWave 47GHz Class-E-like SOI CMOS power DAC.

II. mmWave 1-bit Power DAC Architecture

Fig. 1(b) depicts the architecture of the proposed 1-bit mmWave CMOS power DAC. It consists of a driver stage followed by the main amplifier, both of which are Class-E-like PAs with 2 devices stacked. Device stacking allows for an increased output voltage swing, thus increasing the output power that can be delivered to a fixed load impedance [1], [4]. Both stages are designed using the Class-E-like mmWave design principles described in [1]. Modulation capability is incorporated into the PA by means of the following digitally controlled switches: (a) pMOS supply-switch M_8 for the main PA (b) input-match switch M_1 for the driver (c) gate-bias switches M_2 and M_5 and (d) bias-control switches M_9 and M_{10} for the driver and main PAs respectively. When the PA is ON, M_8 is turned ON, allowing the PA to draw its dc current. Simultaneously, M_2 and M_5 are turned OFF while M_9 and M_{10} are turned ON, so that the driver and the main PA receive their nominal operating gate biases. M_1 is turned OFF as well, since the input impedance of the driver is matched to 50Ω. When the PA is turned OFF, M_8 is turned OFF ensuring that there is no wasteful dc current drawn by the main PA. A different strategy is adopted for de-activating the driver

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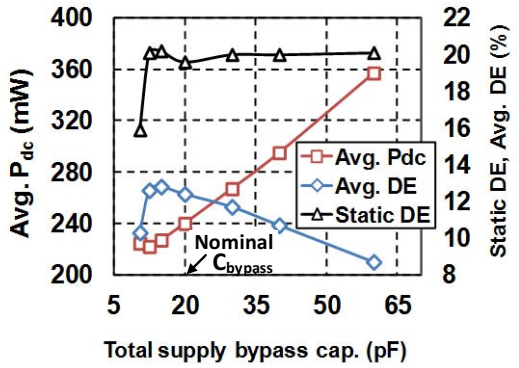

Fig. 2. Average DC power consumption and average drain efficiency (DE) of the supply-switched DAC cell as a function of total supply bypass capacitance in the main PA ($C_{bypass,1}$) for a 500MHz clock input with 50% duty-cycle.

PA. M_2 shorts the gate of the driver's input device (M_3) to ground ensuring that an OFF driver draws no dc current. The combination of these two techniques helps conserve power. M_1 is also turned ON, which, in conjunction with the series 44Ω resistor preserves input-match for the OFF driver. The DAC cell is envisioned to be used in a large-scale power-combining architecture (Fig. 1(a)) which requires that an OFF PA present a short-circuit impedance to the combiner in order to facilitate load modulation under back-off, resulting in a linear output amplitude with number of PAs ON [3]. This is accomplished by means of gate-bias switch M_5 for the main PA, which applies a high gate bias to M_6 when the PA is in the OFF state. The switches M_9 and M_{10} are turned OFF as well. A single control bit b_n is used for all the switches, with appropriate logic inversion. As shown in Fig. 1(c), the control bit is fed to two separate inverter chains: one driving the supply switch and the other the input-match and gate-bias switches. Two separate inverter chains are required to support the different supply voltage levels required to turn ON/OFF the switches. The inverters in each path (in particular, the chain driving M_8) are sized up progressively to drive their respective load capacitances.

In 45nm SOI technology, the DC $V_{DS,max}$ is 1.2V, and the peak RF swing across any two device junctions must be kept below $2 \times V_{DS,max}$ for the 40nm floating-body (FB) devices for long term reliable operation. A thick-oxide pMOS device is used as the supply switch with a DC $V_{DS,max}$ of 2.4V. Therefore, at most two FB devices can be stacked in the main PA to prevent breakdown of the pMOS supply switch in both ON and OFF states. To increase output power, the main PA is designed for an optimal load of 25Ω, which is transformed to 50Ω using transmission lines.

III. Design Considerations and Trade-offs

A. Modulation Speed:

The modulation speed of the DAC is essentially limited by the bias-path RC time constants associated with nodes whose bias voltages are changed during turn ON/OFF. In particular, bias resistors connected to the gates of M_3 and M_6 present an important trade-off: a large bias resistor will have less

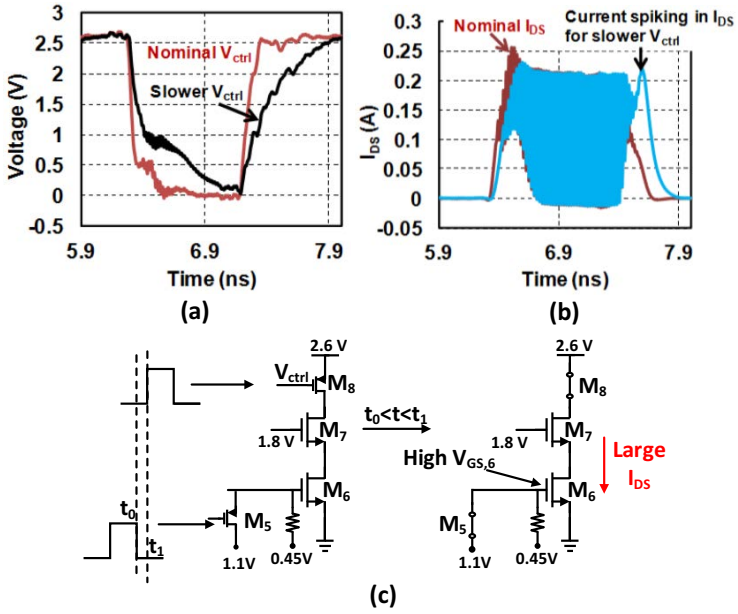

Fig. 3. (a) Slow rise time of the supply-switch control (V_{ctrl}) in the presence of extra digital path interconnect, (b) the resulting spike in drain current I_{DS} of the main PA in the DAC cell, and (c) circuit illustration of the mechanism.

impact on mmWave static performance but will slow down the rise/fall time of the PA when it is turned ON/OFF. Based on the total capacitance at the gate nodes, bias resistors of 1KΩ for the driver and 500Ω for the main PA were found to be optimal for supporting Gbps modulation. Large off-chip decoupling capacitors at the input and output nodes would severely restrict the modulation speed as well. Consequently, series decoupling capacitors were incorporated into the input and output impedance transformation networks.

B. Dynamic Power Dissipation:

The charging and discharging of circuit nodes under modulation is also associated with capacitive discharge loss, given by $P_{loss,cap} = k f_0 C (\Delta V)^2$, where k is the activity factor[1] of the modulation signal, f_0 is the frequency of modulation, C is the capacitance at that node, and ΔV is the change in the node's bias voltage upon turn ON/OFF. The loss is particularly relevant for nodes associated with large capacitance, such as the drains of M_8 (connected to a large supply switch and large bypass capacitors) and M_7 (connected to large decoupling capacitors). The pMOS supply switch must be large to have a small on-resistance to not degrade static drain efficiency. This comes at the cost of an increased parasitic capacitance, which exacerbates the switching losses as the PA is turned ON/OFF, resulting in a trade-off in its size. The input and output decoupling capacitors need to be optimized as well to minimize switching loss. The input decoupling capacitor can be conveniently absorbed in the input matching network thereby reducing its loss. A similar technique could not be utilized on the output side, and the decoupling capacitance (which has a poor quality factor at mmWave frequencies) was

[1]Defined as the average number of rising-edge falling-edge pairs per clock period.

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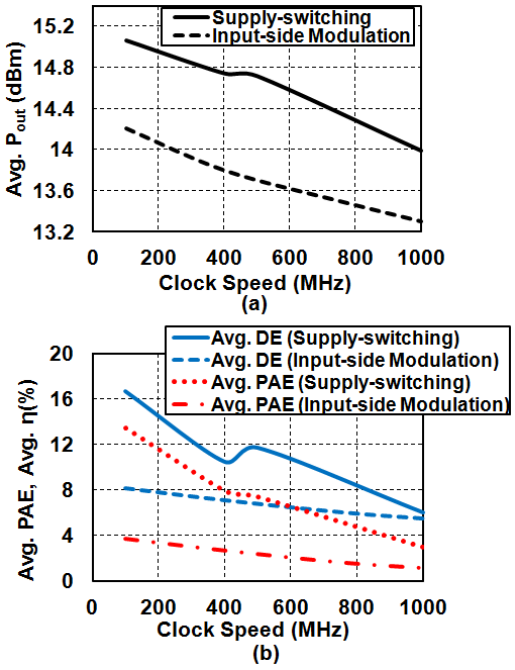

Fig. 4. Simulated average large-signal performance of the mmWave 1-bit power DAC cell at 45GHz with (a) supply-switching and (b) input-side modulation, both using a clock input with 50% duty-cycle.

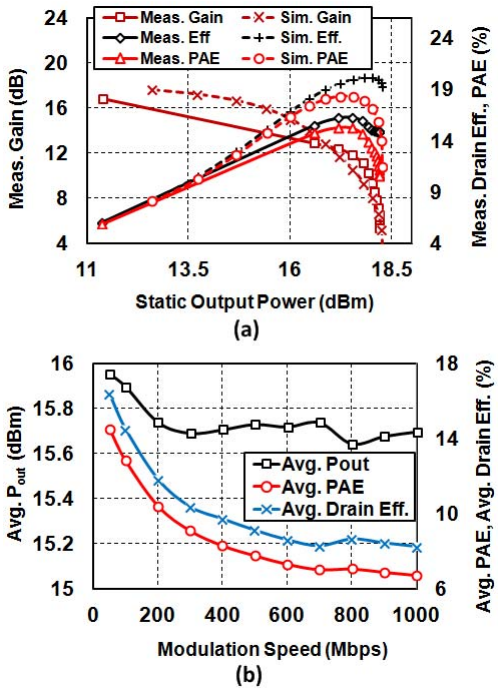

Fig. 5. (a) Measured and simulated large-signal static performance of the mmWave 1-bit power DAC cell at 47GHz, and (b) measured average large-signal metrics at 47GHz with 2^7-1 PRBS OOK at different speeds.

chosen carefully so as to minimize the degradation in static performance while not increasing dynamic power dissipation too severely. The simulated degradation in average efficiency is shown in Fig. 2(a) for a 500MHz clock input with 50% duty-cycle as the supply bypass of the main PA is increased from the nominal design point, keeping the driver's supply bypass and all other capacitors unchanged. It should be noted that a PRBS sequence has an activity factor of $\frac{1}{4}$, while that for a 50% duty-cycle clock is 1. Thus, a 500MHz clock input corresponds to a 2Gbps PRBS (assuming settling time of the circuit is $<<$ 500ps so it can support the modulation).

C. Digital Path Delays and Rise/Fall Times:

While digital path timing is critical in all high-resolution DACs, their importance within a mmWave power DAC unit cell from average efficiency and reliability points of view is described here. The delays and rise/fall times are carefully tailored so that M_8 turns OFF *before* M_5 turns ON. Otherwise, there would be a period of time when both M_8 and M_5 are ON, thereby applying a high gate bias to M_6. The resulting increase in current would degrade average efficiency and is likely to affect long term reliability as well. This phenomenon is illustrated in Fig. 3 for a 500MHz clock input with 50% duty-cycle, where slow rise time of the supply-switch control (V_{ctrl}) results in a large drain current I_{DS} being drawn by the main PA. The slow rise time is created by introducing additional interconnect between the final inverter and the supply switch.

D. Ground/Supply Bounce:

Finally, the presence of supply and ground wirebond inductances can cause the on-chip supply and ground nodes to "bounce" [5]. Ground bounce can cause changes in the instantaneous V_{GS} of devices, turning them ON/OFF unpredictably which compromises desired functionality and can pose reliability concerns as well. Furthermore, the ringing in the waveforms caused by ground bounce increases the settling time of the PA, thereby limiting modulation speed. Since the high frequency signal path conducts a large current and would exhibit largest "bounce", the impact on the digital components can be mitigated by separating the on-chip grounds for the digital and mmWave paths. In addition, by deriving all bias voltages from the on-chip power supply and ground, and using sufficient on-chip supply bypass, ground and supply bounce can be equalized so that device voltages become immune to them.

IV. Comparison with Conventional Input-side Modulation

An alternative means of accomplishing OOK is modulation exercised from the input of the PA. The supply-switched PA can be tailored to support input-side modulation by inserting a switch (controlled by the modulating signal) in series with the gate of the device M_3. The digital path is deactivated, except for the control to the input-match switch M_1, which is retained in order to present the driving source with a 50Ω load when the PA is turned OFF. Fig. 4 compares the simulated performance metrics of the supply-switched architecture with input-side modulation. Evidently, amplitude modulation via supply-switching yields higher average output power as well as average efficiency (since DC power consumption is eliminated when the PA is turned OFF) and can therefore support modulation speeds of ≈ 700Mbps with high average efficiency (≈10%).

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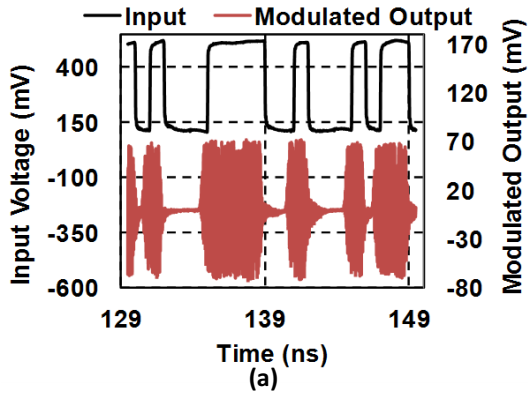
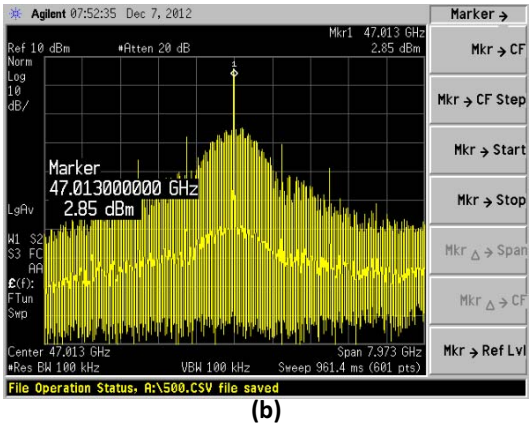


(a)

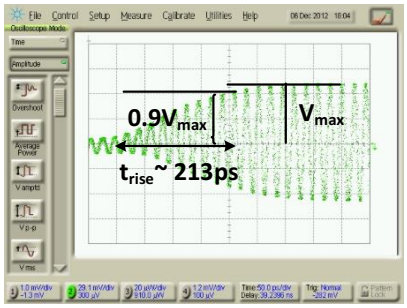


(b)

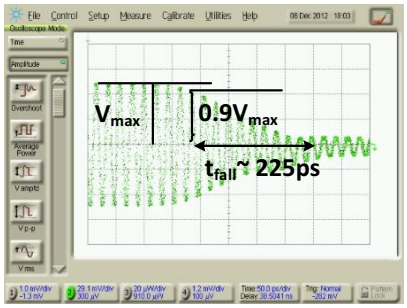
Fig. 6. (a) Measured DAC cell time-domain output with 1Gbps 2^7-1 PRBS OOK input and 47GHz carrier. (b) Measured DAC cell output spectrum with the 1Gbps OOK modulation.

V. Experimental Results

The 1-bit power DAC (Fig. 1(b)) is tested in chip-on-board configuration through on-chip probing. A R&S SMY01 signal generator serves as the input clock for an Anritsu MP1763B PPG, which provides a PRBS as the ASK control bit to the PA. The modulated waveform is displayed in an Agilent 86100B oscilloscope, which is triggered by a "Pattern Sync" signal from the PPG. Average output power is measured using Agilent N1914A power meter, while the modulated spectrum is observed on an Agilent E4448A PSA. A comparison of measured and simulated performances under static conditions is shown in Fig. 5(a). A saturated output power of 18.2dBm with a peak PAE of 15.3% is measured at 47GHz. A peak S_{21} of 20dB is measured in small signal at 51GHz. OOK modulation using a 2^7-1 PRBS was applied at modulation speeds ranging from 100Mbps to 1Gbps along with a 47GHz carrier input at the Class-E drive level. Modulation rates beyond 1Gbps could not be applied owing to the limitation of the clock generator. Fig. 5(b) summarizes the measured large-signal average performance metrics for different modulation speeds. At 400Mbps, an average output power of 15.7dBm was measured, and an average drain efficiency of $\approx$ 10% is maintained. In Fig. 6, screenshots of the time domain waveform and the modulated output spectrum are shown for a modulation rate of 1Gbps. The zoomed-in views for the time-domain output are shown in Fig. 7 from which the rise



(a)



(b)

Fig. 7. Zoomed-in view of the measured DAC cell time-domain output showing (a) rise time and (b) fall time with 1Gbps 2^7-1 PRBS OOK input and 47GHz carrier. Setup losses have not been de-embedded.

time and fall time are calculated to be $\approx$213ps and $\approx$225ps respectively. No bit errors were observed at 1Gbps, indicating that the 1-bit power DAC can be used beyond 1Gbps. The measured amplitude modulation depth (or extinction ratio) is 32dB.

VI. Conclusion

Design considerations for supply-switched mmWave power DAC cells were presented. The proposed DAC cell, in conjunction with large-scale power-combining, is suitable for implementing high power, high efficiency mmWave transmitters capable of supporting complex modulation schemes.

VII. Acknowledgements

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