Design Considerations of Time Constant Mismatch Problem for Inductor DCR Current Sensing Method

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***Abstract* - This paper identifies advantages and disadvantages of several commonly used current sensing methods such as dedicated sense resistor sensing, MOSFET $R_{DS(ON)}$ current sensing, and inductor DC resistance (DCR) current sensing. Among these current sense methods, inductor DCR current sense will become dominant one in the future. The mismatching issue between the time constant made by the current sensing RC network and the one formed with output inductor and its DC resistance is addressed. A small signal model of a buck converter using inductor DCR current sensing with mismatched time constants is presented, and the modeling has been verified experimentally.**

I. Introduction

With the development of modern technologies, there is an ever-increasing demand for high efficiency and high power density power supplies. In all the power supply and converter designs, one of key techniques is how to accurately and timely acquire current signal that will be used for current control and monitoring purpose. Although a traditional current sensing method using a dedicated sense resistor after the output inductor can achieve high accuracy in current sensing, this method would introduce quite a bit of extra power loss, especially for high output current applications. To minimize unnecessary power loss on current sensing, a MOSFET $R_{DS(ON)}$ current sensing method has been used in products. However, the accuracy of this approach strongly relies on the tolerance of the MOSFET on-state resistance ($R_{DS(ON)}$). Unfortunately, though Semiconductor manufacturers have put so much effort on improving MOSFET $R_{DS(ON)}$ tolerance, little progress has been made. The MOSFET $R_{DS(ON)}$ tolerance usually falls in 30%~40% under the current industrial gauge. For a multi-phase converter which has been widely used in today's powerful CPU voltage regulator applications, poor current sensing accuracy using MOSFET $R_{DS(ON)}$ may cause significant phase to phase current sharing unbalance.

Inductor DCR Current Sensing uses the voltage drop on the output inductor DC Resistance (DCR) to derive the output current information. Since DCR tolerance can be controlled at 5% with current process, its current sensing accuracy is much better than that from MOSFET $R_{DS(ON)}$ current sensing. Additionally, it can be implemented by just adding a couple of resistors and capacitors, which is almost a free and lossless current sensing method. This current sensing technique becomes more and more popular due to the good tradeoff between the accuracy and its lossless characteristics. However, with this current sense scheme, the sensed current signal may be distorted if the time constants mismatch between the one formed by RC sensing network and one made by the output inductor plus its DCR happens. What is more, even if the two time constants is pretty close at the initial operating point, the mismatch is still inevitable since actual inductance L and its DCR always vary with the operating point (temperature, current, et.). This paper analyzes the side effects of the time constant mismatch problem. And suggestions were made to minimize the errors introduced. Finally a small signal model with mismatched time constants is presented and verified experimentally.

II. Circuit Operation Characterization and Simulation Results

A buck converter using inductor DCR current sensing is drawn to illustrate the circuit operation. As shown in Fig. 1, SW_1 and SW_2 represent the control and freewheeling switches in a typical synchronous buck converter, respectively. L is the output filtering inductor and R_1 is the DC resistance of L. C_{OUT} and R_{ESR} represent the output capacitor and its parasitic resistance, respectively. The RC network formed by R_2 and C_1 is the current sensing circuit. R_3 is drawn in dotted line since it is not always necessary. R_3 is added only under the circumstance in which scaling down of the detected current signal or/and temperature compensation function are needed.

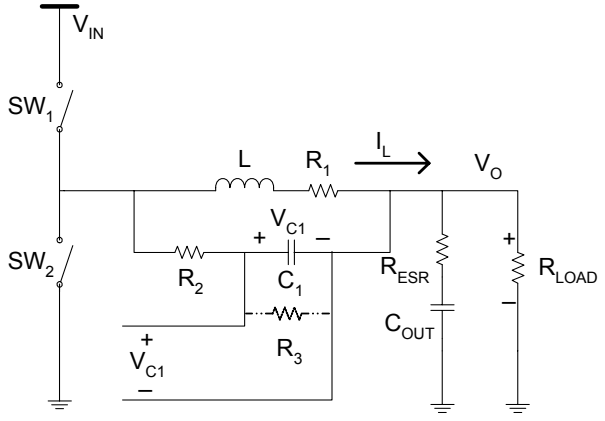

Fig. 1: Buck Converter with Inductor DCR Current Sensing

To analyze the voltage signal on C_1, the circuit as shown in Fig. 1 is investigated under four different cases. The time constant formed by the output inductor is defined as $\tau_L = L/R_1$. And the time constant composed of C_1 is defined as $\tau_{C1} = C_1 \cdot R_2$ when R_3 is not used and $\tau_{C1} = C_1 \cdot (R_2 \cdot R_3)/(R_2 + R_3)$ when R_3 is adopted. The case that we call it time constant match is when τ_L equals τ_{C1}. And the case that we call it time constant mismatch is the one when τ_L does not equal τ_{C1}.

A. Two Time Constants Match ($\tau_L = \tau_{C1}$) without R_3

This situation is the most common approach for applications using inductor DCR current sensing. As shown in Fig. 2, when the time constant τ_L equals the time constant τ_{C1}, the voltage $v_{C1}(t)$ across C_1 in dotted line, overlaps the voltage $v_{R1}(t)$ across the inductor DCR R_1 drawn with solid line. And the relationship between $v_{C1}(t)$ and $v_{R1}(t)$ can be described as in (1).

$$v_{C1}(t) = v_{R1}(t) \tag{1}$$

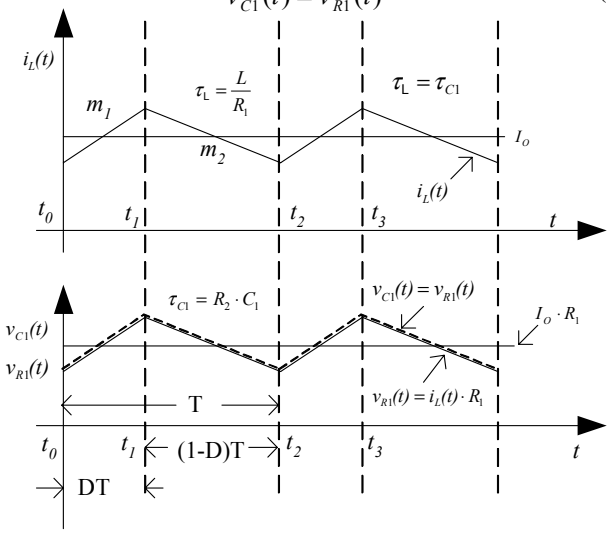

Fig. 2: Illustration of voltage signal $v_{C1}(t)$ and voltage drop $v_{R1}(t)$ without R_3 under the condition in which $\tau_L = \tau_{C1}$

With matched time constant τ_{C1}, the voltage across C_1 can 100% represents the voltage across R_1 generated by the inductor current $i_L(t)$ so that lossless current sensing can be achieved by using the voltage signal across C_1.

B. Two Time Constants Match ($\tau_L = \tau_{C1}$) with R_3

R_3 is often used to scale down the voltage signal across C_1 when either $v_{R1}(t)$ is too high or a temperature compensation function is needed. With the presence of R_3, the time constant formed by C_1 is changed and can be expressed as $\tau_{C1} = C_1 \cdot (R_2 \cdot R_3)/(R_2 + R_3)$. The voltage signals across C_1 and R_1 are illustrated in Fig. 3.

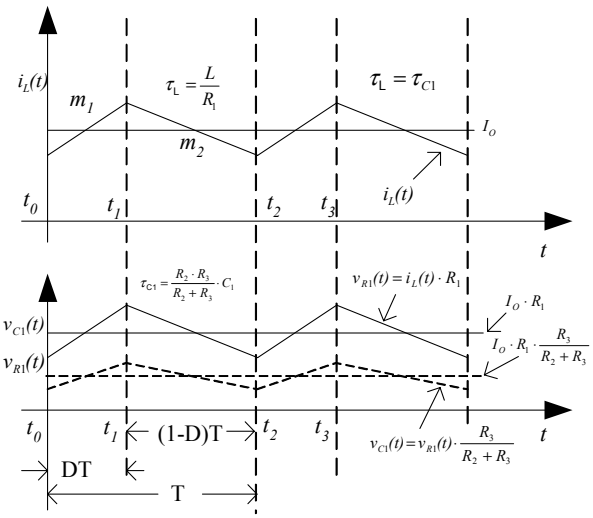

Fig. 3: Illustration of voltage signal $v_{C1}(t)$ and $v_{R1}(t)$ with R_3 under the condition in which $\tau_L = \tau_{C1}$

As shown in Fig.3, the voltage signal $v_{C1}(t)$ is not 100% of $v_{R1}(t)$ but scaled down by the factor of $R_3/(R_2 + R_3)$. The relationship between $v_{C1}(t)$ and $v_{R1}(t)$ can be written as in (2) and (3).

$$v_{R1}(t) = i_L(t) \cdot R_1 \tag{2}$$

$$v_{C1}(t) = v_{R1}(t) \cdot \frac{R_3}{R_2 + R_3} \tag{3}$$

C. Time Constants Mismatch ($\tau_L \neq \tau_{C1}$) without R_3

However, in real applications, it is very hard to match the time constant τ_L with τ_{C1} due to various limitations such as the tolerance of the used passive components and the temperature dependence of R_1. Additionally, the inductance L also changes with its DC current bias, which deteriorates the existing mismatched situation. All these realistic circumstance raises up the question on why the sensed current signal gets distorted and how this is going to affect the converter's normal operation.

The basic operation of the current sensing RC network is a process of charging and discharging on capacitor C_1. As shown in Fig. 1, when the control switch SW_1 closes, the input voltage V_{IN}, together with V_O, will be applied to the inductor L plus R_1 and the current sensing network R_2 with C_1. Since the R_1 is very small, the voltage across R_1 is very weak. So the current flowing through L, I_L, can be considered to increase linearly with the slew rate of $\frac{(V_{IN} - V_O)}{L}$. And at the same time, the voltage across the C_1 gets charged up with the time constant R_2C_1. When the control switch SW_1 is turned off and the freewheeling

switch SW_2 is turned on, only the output voltage V_O is applied to the inductor L plus R_1. I_L starts to decline with the slew rate of $\frac{-V_O}{L}$. And at the same time, C_1 gets discharged with the same time constant R_2C_1. The whole charging and discharging process is illustrated in Fig. 4.

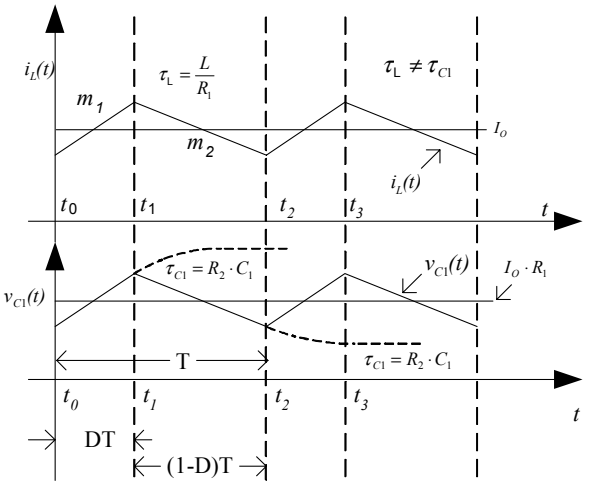

Fig. 4: Current Signal $i_L(t)$ and Voltage Waveform $v_{C1}(t)$ in Steady State

When the time constant τ_{C1} is much bigger than the switching cycle T, which is true for most of the applications in which the switching frequency is above 200kHz. During the DT and (1-D)T time, the exponential charging and discharging processes can be simplified with linearization. We can use the slew rate of the charging process at $t = t_0$ to approximate the voltage slope of $v_{C1}(t)$ during DT time. And use the slew rate of the discharging process at $t = t_1$ to approximate the voltage slope of $v_{C1}(t)$ during (1-D)T time.

Assume the initial voltage across C_1 at t_0 and t_1 is $v_{C1}(t_0)$ and $v_{C1}(t_1)$ respectively. The voltage $v_{C1}(t)$, across C_1 during DT and (1-D)T time, can be described as in (4) and (5).

$$v_{C1}(t)_{t\in[t_0,t_1]} = (V_{IN} - V_O)\cdot(1 - e^{-\frac{t-t_0}{R_2C_1}}) + v_{C1}(t_0)\cdot e^{-\frac{t-t_0}{R_2C_1}} \quad (4)$$

$$v_{C1}(t)_{t\in[t_1,t_2]} = (-V_O)\cdot(1 - e^{-\frac{t-t_1}{R_2C_1}}) + v_{C1}(t_1)\cdot e^{-\frac{t-t_1}{R_2C_1}} \quad (5)$$

At the time $t = t_0$ and $t = t_1$ the charging slew rate and the discharging slew rate are addressed in (6) and (7) respectively:

$$S_{CHARGE}(t_0) = (V_{IN} - V_O - v_{C1}(t_0))\cdot\frac{1}{R_2C_1} \quad (6)$$

$$S_{DISCHARGE}(t_1) = (-V_O - v_{C1}(t_1))\cdot\frac{1}{R_2C_1} \quad (7)$$

Since the voltage on C_1 is very small, the initial voltage across C_1, $v_{C1}(t_0)$ and $v_{C1}(t_1)$ in (6) and (7), can be omitted in the following analysis. If the time constant $\frac{L}{R_1} = R_2C_1$, then the equation (6) and (7) can be rewritten as in (8) and (9):

$$S_{CHARGE}(t_0) = (V_{IN} - V_O)\cdot\frac{R_1}{L} \quad (8)$$

$$S_{DISCHARGE}(t_1) = (-V_O)\cdot\frac{R_1}{L} \quad (9)$$

From (8) and (9), we can see that the peak-to-peak voltage ripple across C_1 is the same as the peak-to-peak voltage ripple across the inductor DC resistance R_1, which can be characterized in (10).

$$\tilde{V}_{C1\_PKPK} = (V_{IN} - V_O)\cdot\frac{R_1}{L}\cdot D\cdot T \quad (10)$$

However, in real applications, it is very hard to make $\frac{L}{R_1} = R_2C_1$. So the slew rates of the charging and discharging process need to be adjusted with a correction factor. Let first define the capacitance needed to match the time constant $\frac{L}{R_1}$ as in (11).

$$C_{DREAM} = \frac{L}{R_1\cdot R_2} \quad (11)$$

Assume C_1 is the real value selected in real applications. The slew rates of charging and discharging processes on C_1 can be modified as shown in (12) and (13).

$$S_{CHARGE}(t_0) = (V_{IN} - V_O)\cdot\frac{R_1}{L}\cdot\frac{C_{DREAM}}{C_1} \quad (12)$$

$$S_{DISCHARGE}(t_1) = (-V_O)\cdot\frac{R_1}{L}\cdot\frac{C_{DREAM}}{C_1} \quad (13)$$

Now we can see that, at $t = t_0$ and $t = t_1$, if the C_1 in a real application is less than C_{DREAM}, the peak-to-peak voltage ripple across C_1 is actually bigger than the peak-to-peak voltage ripple across R_1 generated by $\tilde{I}_L$. $\tilde{I}_L$ is the AC component of the output current flowing through L. This means that the slew rate of $v_{C1}(t)$ is actually amplified by the coefficient of $\frac{C_{DREAM}}{C_1}$. And if C_1 is bigger than C_{DREAM}, then the peak-to-peak voltage ripple across C_1 will be actually smaller than the peak-to-peak voltage ripple across R_1 generated by $\tilde{I}_L$, which means that the slew rate of $v_{C1}(t)$ is actually scaled down by the factor of $\frac{C_{DREAM}}{C_1}$.

D. Time Constants Mismatch ($\tau_L \neq \tau_{C1}$) with R_3

In some other applications, because the voltage drop across R_1 is too high or temperature compensation function is needed, another resistor R_3, as shown in Fig. 1, is adopted to level shift the DC voltage on C_1 or to provide temperature compensation. The appearance of R_3 changes the time constant previously defined by R_2 and C_1. Will this extra resistor change the slew rate of the charging and discharging C_1? To analyze the charging and discharging processes on

C1, Fig. 5 and Fig. 6 are drawn to illustrate the circuit operation during DT time and (1-D)T time. And relative waveforms are shown in Fig. 7.

With the assumption that the time constant $\frac{R_2R_3}{R_2+R_3}C_1$ is much bigger that the switching cycle of the converter, the exponential charging process can be simplified with linearization as addressed before. The voltage across C_1, $v_{C1}(t)$, can be described as the function of time t as shown in (14) and (15) during DT time and (1-D)T time with the assumption that $v_{C1}(t_0)$ and $v_{C1}(t_1)$ are so low that they can be omitted in the following analysis.

$$v_{C1}(t)_{t\in[t_0,t_1]} = (V_{IN} - V_O)\cdot\frac{R_3}{R_2+R_3}\cdot(1-e^{-\frac{t-t_0}{\frac{R_2R_3}{R_2+R_3}C_1}}) \quad (14)$$

$$v_{C1}(t)_{t\in[t_1,t_2]} = (-V_O)\cdot\frac{R_3}{R_2+R_3}\cdot(1-e^{-\frac{t-t_1}{\frac{R_2R_3}{R_2+R_3}C_1}}) \quad (15)$$

At the time $t=t_0$ and $t=t_1$ the charging slew rate and the discharging slew rate are addressed as in (16) and (17) respectively:

$$S_{CHARGE}(t_0) = (V_{IN} - V_O)\cdot\frac{1}{R_2\cdot C_1} \quad (16)$$

$$S_{DISCHARGE}(t_1) = (-V_O)\cdot\frac{1}{R_2\cdot C_1} \quad (17)$$

Based on (16) and (17), we can derive that, at the time $t=t_0$ and $t=t_1$, the slew rates of charging and discharging are not affected by the presence of R_3. The direct influence of R_3 is that the DC voltage on C_1 is level shifted by the factor of $\frac{R_3}{R_2+R_3}$. This interesting phenomenon implies that the slew rate of the voltage ripple on C_1 is only affected by R_2 and C_1. With the C_{DREAM} as predefined in (11), the slew rates of the charging and discharging process on C_1, even with the presence of R_3, can be characterized as in (18) and (19):

$$S_{CHARGE}(t_0) = (V_{IN} - V_O)\cdot\frac{R_1}{L}\cdot\frac{C_{DREAM}}{C_1} \quad (18)$$

$$S_{DISCHARGE}(t_1) = (-V_O)\cdot\frac{R_1}{L}\cdot\frac{C_{DREAM}}{C_1} \quad (19)$$

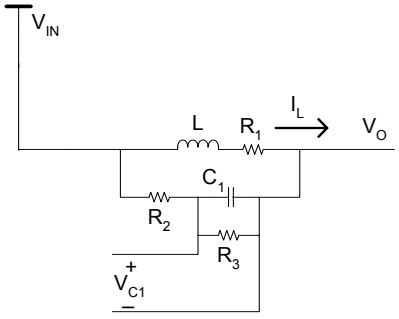

Fig. 5: Charging process on C_1 during DT time

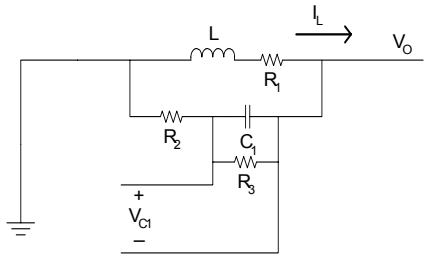

Fig. 6: Discharging process on C_1 during (1-D)T time

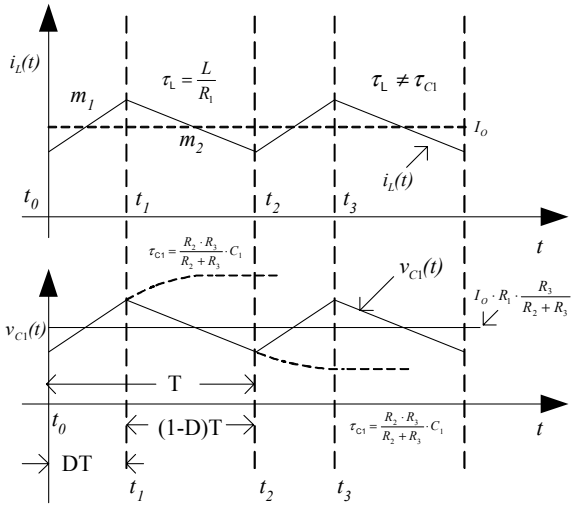

Fig. 7: Current Signal $i_L(t)$ and Voltage $v_{C1}(t)$ with R_3 in Steady State

A switching mode simulation circuit was built in spice as shown in Fig. 8. The simulation results under different time constant mismatch conditions are given in Fig.9, Fig.10 and Fig.11.

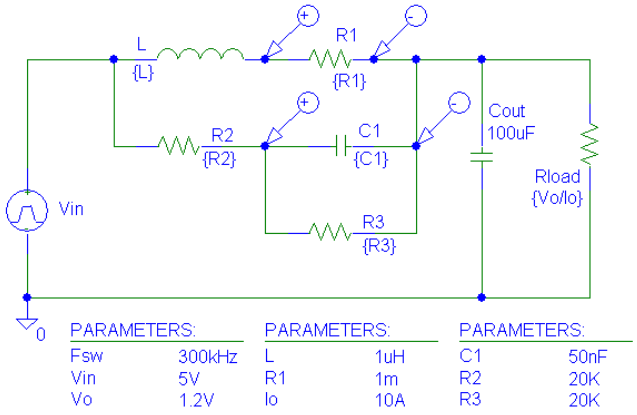

Fig. 8: Simulation Circuit

In Fig.9, Fig.10 and Fig.11, the curve on the top is the voltage drop across R_1. The curve at the bottom is the voltage across C_1. The simulation results, as listed in Fig.10 and Fig.11, clearly show that, under the conditions in which $\frac{L}{R_1} \neq R_2C_1$, the slope of the voltage across C_1 is either scaled down or scaled up by the factor of $\frac{C_{DREAM}}{C_1}$ even with

the usage of R_3. And the DC voltage on C_1 is scaled down by the factor of $\frac{R_3}{R_3+R_2}$ from $I_L R_1$ and it remains the same under those conditions as shown in Fig.9, Fig.10 and Fig.11.

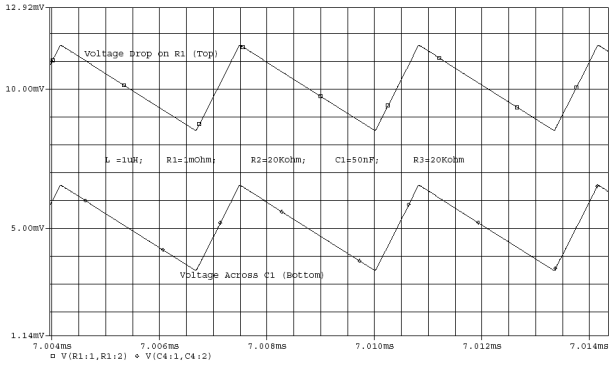

Fig. 9: Waveforms under the Condition--- $\frac{L}{R_1} = R_2 C_1$

(L=1μH; R_1=1mΩ; R_2=20KΩ; C_1=50nF; R_3=20KΩ)

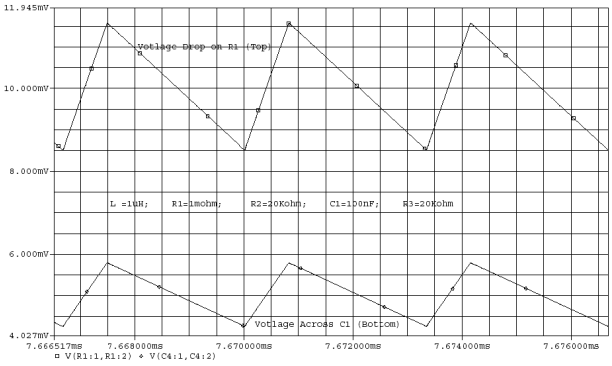

Fig. 10: Waveforms under the Condition $\frac{L}{R_1} < R_2 C_1$

(L=1μH; R_1=1mΩ; R_2=20KΩ; C_1=100nF; R_3=20KΩ)

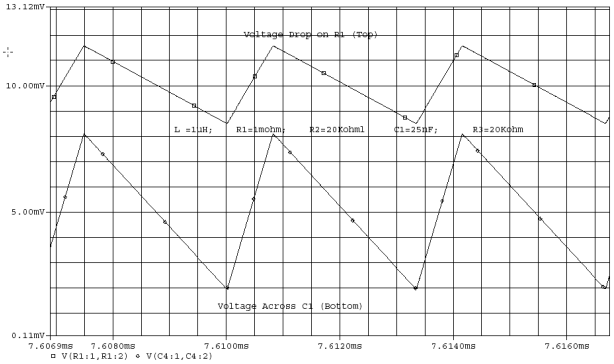

Fig. 11: Waveforms under the Condition $\frac{L}{R_1} > R_2 C_1$

(L=1μH; R_1=1mΩ; R_2=20KΩ; C_1=25nF; R_3=20KΩ)

III. Small Signal Model for Buck Converter Using Inductor DCR Current Sensing with Mismatched Time Constants

The modeling method in this paper for peak current mode control is described in chapter 11 in the book "Fundamentals of Power Electronics". Fig. 12 illustrates the variables used in the modeling. The reference designators are based on the parameters defined in Fig. 1. As shown in Fig.12, the relationships of the control variables can be expressed in (20), (21) and (22).

$$\hat{i}_L(t)\cdot\frac{R_3}{R_2+R_3} = \hat{i}_c(t) - M_a\cdot\hat{d}\cdot T - \frac{D^2\cdot\hat{m}_1\cdot T}{2} - \frac{D'^2\cdot\hat{m}_2\cdot T}{2} \quad (20)$$

$$\hat{m}_1 = \frac{\hat{v}_{IN}-\hat{v}_{OUT}}{L}\cdot\frac{C_{DREAM}}{C_1} \quad (21)$$

$$\hat{m}_2 = \frac{\hat{v}_{OUT}}{L}\cdot\frac{C_{DREAM}}{C_1} \quad (22)$$

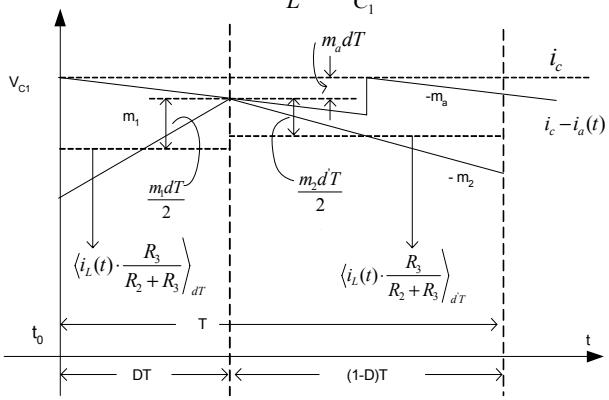

Fig. 12 Current Signal I_L and Voltage Waveform V_{C1} with R_3 in Operation

The simplified control flow chart is shown in Fig. 13.

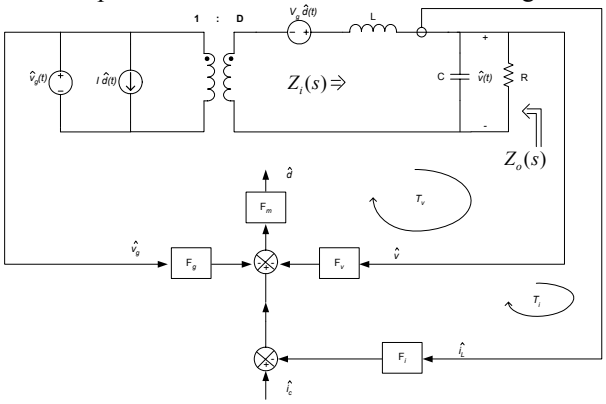

Fig. 13 Control Flow Chart

And F_g, F_m, F_v and F_i can be expressed as:

$$F_g = \frac{D^2\cdot T}{2L}\cdot\frac{C_{DREAM}}{C_1} \quad (23)$$

$$F_v = \frac{(1-2D)\cdot T}{2L}\cdot\frac{C_{DREAM}}{C_1} \quad (24)$$

$$F_m = \frac{1}{M_a T} \quad (25)$$

$$F_i = \frac{R_3}{R_2+R_3} \quad (26)$$

$$Z_i(s) = sL + (R // \frac{1}{sC}) \quad (27)$$

$$Z_o(s) = R // \frac{1}{sC} \quad (28)$$

$$T_v(s) = F_m \cdot \frac{V_{OUT}}{D^2} \cdot \frac{D}{Z_i(s)} \cdot Z_o(s) \cdot F_v \quad (29)$$

$$T_i(s) = \frac{F_i}{Z_o(s)F_v} \cdot \frac{T_v(s)}{1+T_v(s)} \quad (30)$$

So the control to output transfer function $G_{vc}(s)$ is

$$G_{vc}(s) = \frac{Z_o(s)}{F_i} \cdot \frac{T_i(s)}{1+T_i(s)} \quad (31)$$

IV. Experimental Verifications

A buck converter was built to verify the analysis of the slew rate of the voltage ripple on C_1 and its stability issue under the time constants mismatch situation. The buck converter plus its control flow chart is shown in Fig. 14. In the Fig. 14, R_a and R_b, together with EA_2 set the output voltage. The current signal is sensed through the RC network made with R_2, R_3 and C_1. V_{C1} is amplified by EA_1 and then compared with the output of EA_2 to generate the PWM signals to drive the SW_1 and SW_2, The parameters of the tested circuit are described as follows: L=1μH, R_1=1.2mΩ, R_2=20KΩ, C_1=20nF, R_3=20KΩ, C_{OUT}=200μF, R_{ESR}=1mΩ, V_{IN}=5V,V_{OUT}=1.8V, F_{SW}=750KHz.

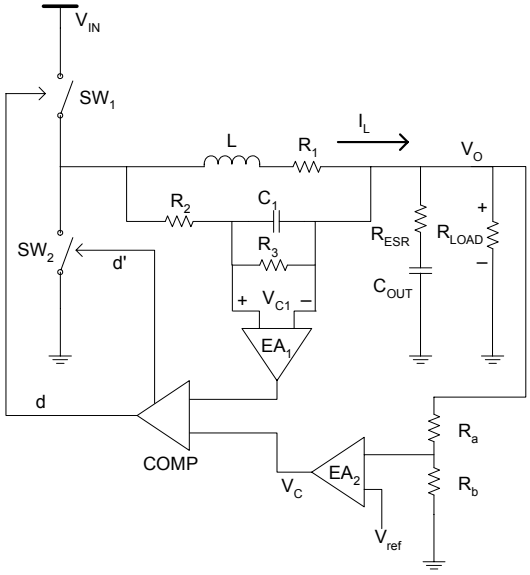

Fig.14: the Buck Converter under Test

Tests were done with 1A load to check the current signal in L and the voltage across C_1. As shown in Fig. 15, the red curve in the middle is V_{C1}. The light blue curve on the top is the zoom in of the red curve for illustration due to the limited amplitude of V_{C1}. And the dark blue curve at the bottom is the current signal I_L. The curve reading shown in Fig. 15 indicates that the voltage slope on C_1 is 9.82V/mS. The slope of the current signal in L is 3.64A/μS. So the slope of the voltage drop on R_1 is 4.366V/mS. By plugging in the correction coefficient $\frac{C_{DREAM}}{C_1} \approx 2.1$ calculated from the parameters listed above, the slope of V_{C1} (9.82V/mS) is close to the scaled up value $2.1 \times 4.366\text{V/mS} = 9.17\text{V/mS}$ calculated from the voltage slope on R_1 together with the correction factor.

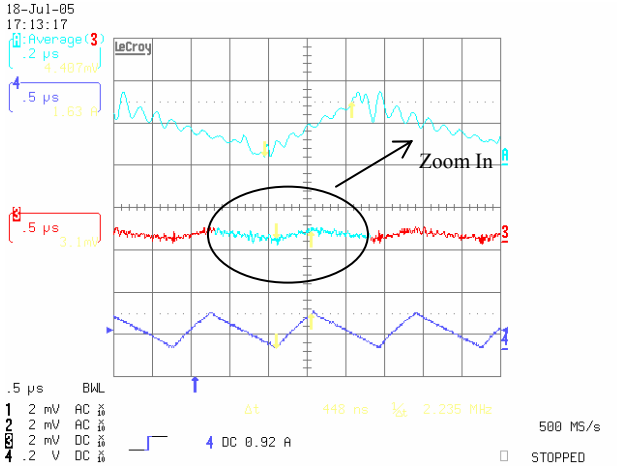

Fig.15: Current waveform in output inductor L and voltage across C_1

The gain plot and phase plot of the calculated model under 10A load condition are shown in Fig.16 and 17 respectively. And the bode plot of the tested module at 10A load condition is in Fig.18 (the Blue curve is the gain plot and the red curve is the phase plot).

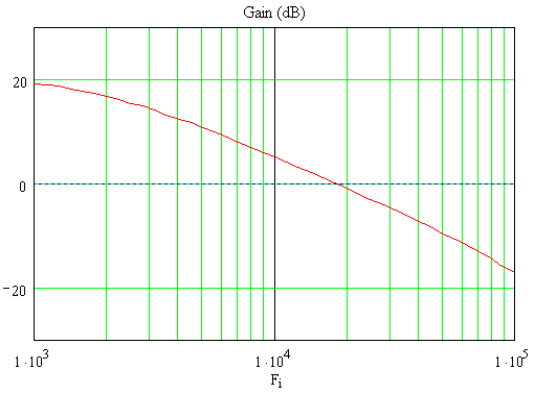

Fig.16: Calculated Gain Plot of G_{VC}

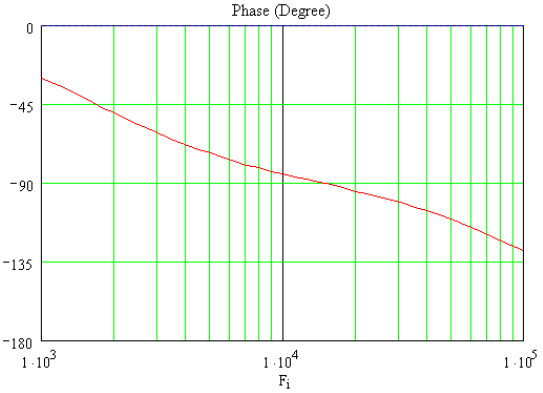

Fig.17: Calculated Phase Plot of G_{VC}

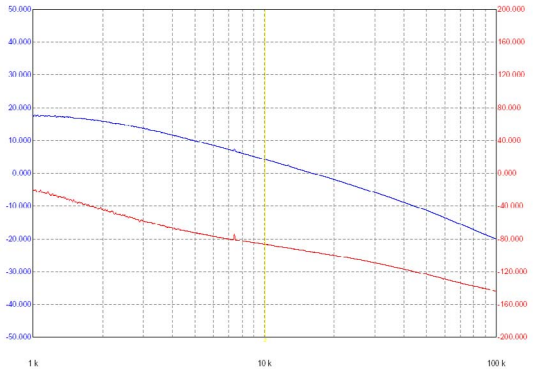

Fig.18: Bode Plot of G_{VC} of the Tested Module

V. Temperature Compensation Network

To minimize the error introduced by the temperature dependency of the R_1, a widely used three resistors network including an NTC resistor is introduced as shown in Fig. 19.

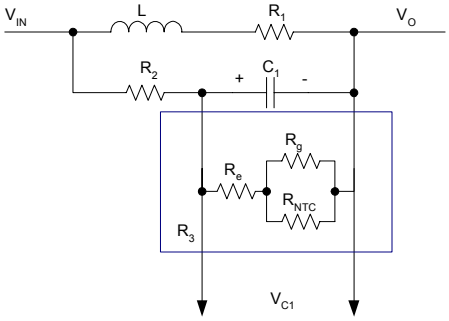

Fig.19: Inductor DCR Current Sensing Circuit with Temperature Compensation Network

As shown in Fig.19, The resistor network made of R_e, R_g and R_{NTC} is the temperature compensation network that can provide almost complete compensation for copper thermal variations. Based on the required over current protection threshold and the τ_L formed by the inductor L and R_1, R_2 and C_1 plus the equivalent R_3 of the resistor network (R_e, R_g and R_{NTC}) can be computed. It is preferable to make $R_3/(R_2+R_3)$ around 0.85. Then we pick up an NTC resistor whose value is close (within 5%) to the calculated R_3 at $25\,°C$. If not be able to find one NTC resistor, calculate another set of R_2, C_1 and equivalent R_3 until you can find one NTC resistor. Based on the characteristics of the selected NTC resistor, coefficients A and B are calculated as in (32) and (33) at $50\,°C$ and $90\,°C$:

$$A = R_{NTC}(50°C)/R_{NTC}(25°C) \quad (32)$$

$$B = R_{NTC}(90°C)/R_{NTC}(25°C) \quad (33)$$

r_1 and r_2 are calculated at $50\,°C$ and $90\,°C$ as defined in (34), (35), (36) and (37).

$$w(T) = (R_3/(R_3+R_2))/(1+0.0039\cdot(T-25°C)) \quad (34)$$

$$j(T) = w(T)/(1-w(T)) \quad (35)$$

$$r_1 = j(50°C)/j(25°C) \quad (36)$$

$$r_2 = j(90°C)/j(25°C) \quad (37)$$

Parameters such as r_e, r_g and r_{NTC} can be computed as characterized in (38), (39) and (40).

$$r_e = \frac{(A-B)\cdot r_1\cdot r_2 - A\cdot(1-B)\cdot r_2 + B\cdot(1-A)\cdot r_1}{A\cdot(1-B)\cdot r_2 - B\cdot(1-A)\cdot r_1 - (A-B)} \quad (38)$$

$$r_g = (1-A)/\left(\frac{1}{1-r_e} - \frac{A}{r_1-r_e}\right) \quad (39)$$

$$r_{NTC} = 1/\left(\frac{1}{1-r_e} - \frac{1}{r_g}\right) \quad (40)$$

Then calculate R_{NTC} as shown in (41) based on the calculated R_3. Select the closest value of one NTC thermistor available. Also compute a scaling factor k based on the ratio of the actual thermistor value used relative to the computed one as in (42).

$$R_{NTC} = r_{NTC}\cdot R_3 \quad (41)$$

$$k = R_{NTC}(Actual)/R_{NTC}(Calculated) \quad (42)$$

Based on the computed parameters as shown above, R_e and R_g can be calculated as shown in (43) and (44) based on the calculated R_3.

$$R_g = k\cdot r_g\cdot R_3 \quad (43)$$

$$R_e = ((1-k)+(k\cdot r_e))\cdot R_3 \quad (44)$$

Finally, R_e and R_g are selected from resistor bank with the resistances closest to the calculated results from (43) and (44).

VI. Summary

Inductor DCR current sensing is a common practice in high current applications. To achieve timely and accurate current sensing effect, the time constant of the current sensing RC network has to match the one formed by the inductor and its DCR. This paper analyzes, in details, the charging and discharging process of the current sensing RC network and clarifies that the slew rates of the voltage ripples on the current sensing capacitor is determined by the relationship between L/R_1 and R_2C_1 no matter whether R_3, as in Fig.1, is used or not. The consequences introduced by the time constant mismatch are summarized, simulated and tested. A small signal model for a buck converter using inductor DCR current sensing with mismatched time constants is derived and experimentally verified.

And as shown in the analysis, a little bigger value of R_2C_1 compared with the one formed by L/R_1 is recommended if a wider bandwidth and faster dynamic response is preferred. However, noise issue should be taken into account while adjusting the product of R_2C_1. And a three resistors temperature compensation network as shown in Fig.19 can be used to calibrate over current protection triggering point caused by the thermal dependency of the inductor DCR.

References

[1]. Robert W. Erickson. "Fundamentals of Power Electronics"
[2]. Ridley, R. B. "A New Continuous-Time Model for Current-Mode Control"