Design, Fabrication, and Reliability Assessment of Embedded Resistors and Capacitors on Multilayered Organic Substrates

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***Abstract*- Embedded passives provide a practical solution to microelectronics miniaturization. In a typical circuit, over 80 percent of the electronic components are passives such as resistors, inductors, and capacitors that could take up to 50 percent of the entire printed circuit board area. By integrating passive components within the substrate, embedded passives reduce the system real estate, eliminate the need for discrete components and assembly of same, enhance electrical performance and reliability, and potentially reduce the overall cost. Moreover, it is lead free. Even with these advantages, embedded passive technology is at a relatively immature stage and more characterization and optimization are needed for practical applications leading to its commercialization.**

This paper presents an entire process from design and fabrication to electrical characterization and reliability test of embedded passives on multilayered microvia organic substrate. Two test vehicles focusing on resistors and capacitors have been designed and fabricated by Packaging Research Center (PRC) and Endicott Interconnect Technologies (EI). Resistors are carbon ink based Polymer Thick Film (PTF) and NiCrAlSi, and capacitors are made with polymer/ceramic nanocomposite material. High frequency measurement of these capacitors was performed. Furthermore, reliability assessments of thermal shock and temperature humidity tests based on JEDEC standards are presented.

Index terms – BaTiO3, design, embedded capacitor, embedded passives, fabrication, high frequency, NiCrAlSi, PTF, reliability, SOP.

I. INTRODUCTION

Over the last several decades, tremendous progress has been achieved in the electronic industry. In 1959, the first integrated circuit (IC) developed by Jack Kilby contained only 2 transistors and a resistor, but now a personal computer IC contains more than a billion transistors. Cell phones that were once bulky in size are now slim and integrated with more functionality than ever. Various complex technologies are being successfully integrated together to form a remarkable stand alone system. And yet, there is a constant demand for faster, smaller, more reliable and low cost electronic systems. A potential solution to meet the current and future challenges is embedded passives technology. Although surface mount technology (SMT) is improving, embedded passives can eliminate the approaching limitations of SMT footprints. As an essential component of System-on-Package (SOP), embedded passives reduce the system real estate, eliminate the need for discrete components and assembly of same, enhance electrical performance and reliability, and potentially reduce the overall cost [1 - 5].

Current world wide passive market is approximately 25 billion USD, and although embedded passive was introduced several decades ago, currently less than 2% of components are embedded [6]. To gain more acceptance and increase market share, several technical challenges must be resolved: tight tolerance, low thermal coefficient of resistance (TCR), low thermal coefficient of capacitance (TCC), high yield and reliability, and availability of wide range of resistance and capacitance. iNEMI (International Electronic Manufacturing Initiative) projects portable and handheld product need passives with maximum resistance of 100 kohms/sq and tolerance of 5% without trim by 2007 [6]. Another major challenge for the overall success of embedded passives is reliability. Although solder joints are eliminated, rework is not a viable option. A single bad component can lead to scrapping the entire board.

This paper presents a unique design that offers low temperature processing for organic board compatibility. An entire process from design and fabrication of multilayered microvia organic substrate to extensive electrical characterization and mechanical reliability tests are presented.

II. DESIGN

Two test vehicles were designed with various sizes, geometries, and values of embedded resistors and capacitors. The Test Vehicle 1 (TV1) is a 6” x 6” epoxy based board with 8 metal layers. The core is a 6 layer subcomposite as shown

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in Fig. 1. Fig. 2 shows the cross section view. The embedded resistors and capacitors are on metal layer 7, and they are connected to probe pads on metal layer 8 by microvias. There are 4 circular and 3 rectangular geometry capacitors. Some have center probe connections to reduce the parasitic inductance, while others have edge probe connections for easier fabrication. The capacitor dielectric is based on polymer/ceramic nanocomposite, and the values of these capacitors range from 50 pF to 1.5 nF with capacitance per area of approximately 1.5 nF/cm^2. Resistors are carbon ink based Polymer Thick Film (PTF) and are designed to cover the resistance in the range of 25 ohms to 100 kohms.

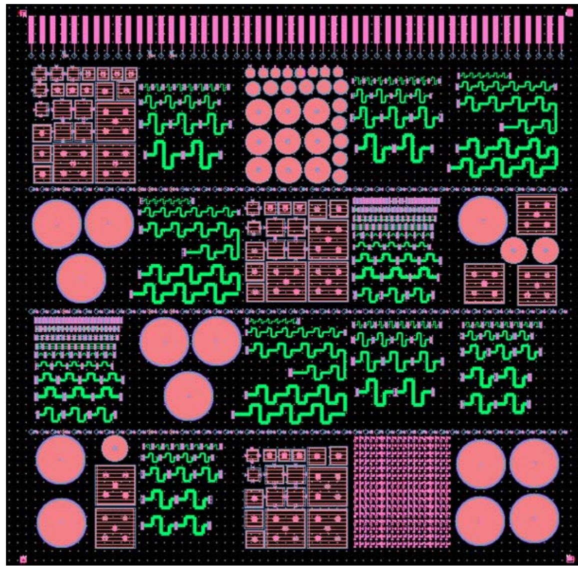

Fig.1. Top view of subcomposite at M7.

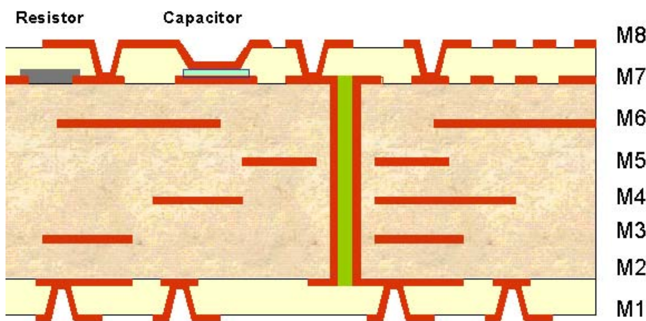

Fig. 2. Cross section view of Test Vehicle 1.

TV2 is a 12” x 12” epoxy based board with 12 metal layers. It is dedicated resistor test vehicle as shown in Fig. 3. Resistors are contained on 3 different metal layers, and each containing various sizes, geometries, and values of NiCrAlSi foil embedded resistors in the range of 5 ohms to 100 kohms.

III. FABRICATION

Test vehicles were fabricated at Packaging Research Center (PRC) and at Endicott Interconnect Technologies (EI) through partnership with PRC. There are 3 main processing steps: capacitors, resistors, and microvia with probe pads. Fig. 4 shows the general overview of each step adopted at PRC and Fig. 5 shows the fabricated prototypes.

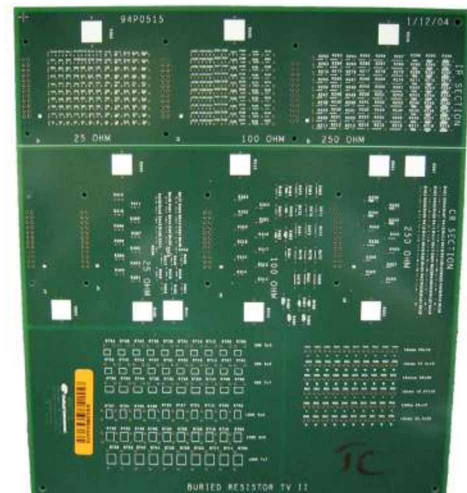

Fig. 3. Layout of Test Vehicle 2.

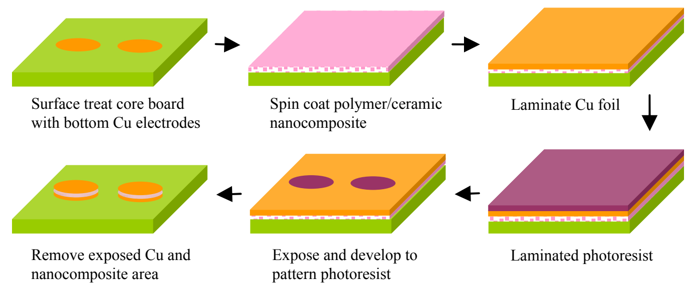

Fig. 4a. Capacitor fabrication process.

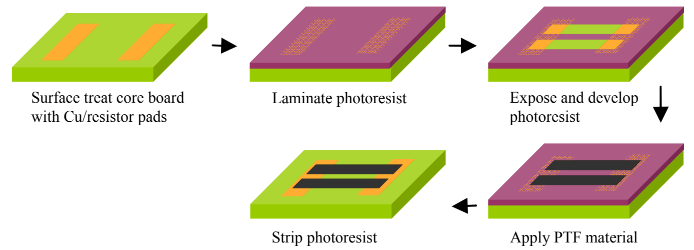

Fig. 4b. Resistor fabrication process.

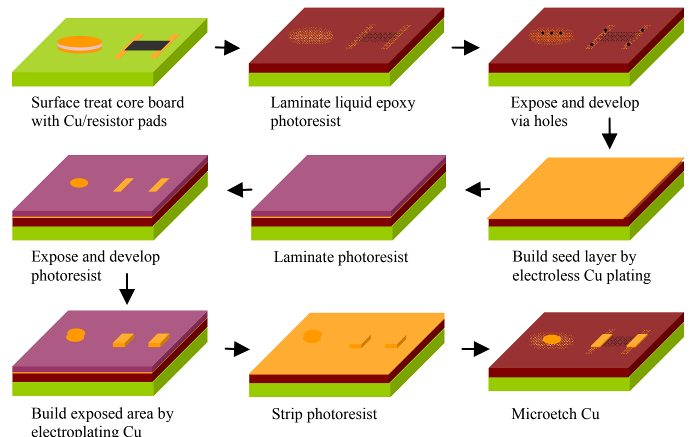

Fig. 4c. Microvia with probe pad fabrication process.

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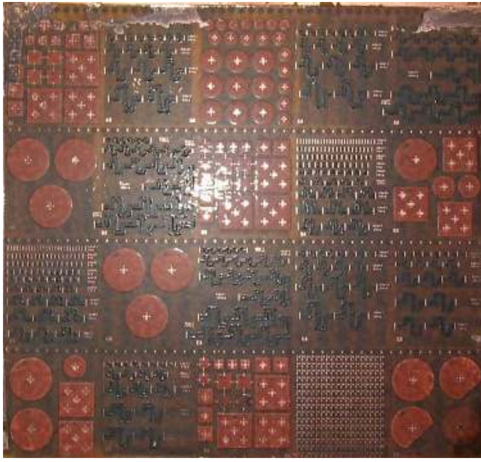

Fig. 5. Completed SOP TV1.

A. Capacitors

The bare core 6 metal layer board with bottom copper electrode was surface treated with acetone to remove any organic residues. It was then microetched, and bond film was applied to increase the adhesion with the dielectric layer. Polymer/ceramic nanocomposite dielectric was prepared by mixing 44 g of polymeric resin, which contains barium titanate, with 4.24 g of hardener and 5 g of thinner. Once these are mixed thoroughly, the nanocomposite was spin coated at 2000 rpm for 30 seconds on to the bare board to achieve a nominal thickness of 20 μm. Then, the board was soft cured at 65 ^{o}C for 45 minutes. For top copper electrode, a 10 μm copper foil was vacuum laminated, and then heat pressed (2 tons) at 70 ^{o}C was applied to strengthen the lamination. Then, conventional photolithography process was performed using Shipley SP20-29 positive photoresist. The exposed copper and nanocomposite were removed with 30% ferric chloride solution and GBL (Gamma Butyrolactone) solvent respectively to finish the capacitor process. Simple and low temperature process exhibited high yield with capacitance per area of ~ 1.5 nF/cm^2. These capacitors were also fabricated at the Endicott Interconnect using proprietary materials and processes.

B. Resistors

Conventional lift-off process was used to fabricate the embedded resistors. Initially, the board was treated with acetone and microetched to thoroughly remove any organic residue and roughen up the surface to improve adhesion. Then, conventional photolithography was performed using Dupont Riston 4615 dry film. After the photoresist is exposed and developed, carbon ink based PTF supplied by W.R. Grace was applied into the developed negative pattern of the resist trace. The resist material was soft cured at 120 ^{o}C for 1 hour. The photoresist is then stripped, and the board was fully cured at 150 ^{o}C for 1 hour to complete the resistor process. Both 10 ohms/sq and 10 kohms/sq resistance materials were used, and resulting resistor values range from 5 ohms to 400 kohms. PTF resistors were also fabricated at Endicott Interconnect using a modified version of this process.

C. Microvia with probe pads

The process of acetone clean and microetch were carried out again to thoroughly clean the surface and improve the adhesion. Then, photo-imageable liquid epoxy Vantico Probimer 7081 was spin coated at 1000 rpm for 40 seconds to achieve a nominal thickness of 30 μm. This interlayer dielectric has a dielectric constant of 3.4 and loss of 0.015 at 1 GHz. Once the board was soft cured at 90 ^{o}C for 30 minutes, UV radiation of 4 J/cm^2 was exposed to pattern the microvia structures. Then, the board was baked at 100 ^{o}C for 1 hour to fully crosslink the exposed area. GBL solvent at room temperature was used to develop the photoresist, and the board was fully cured at 160 ^{o}C for 1 hour. In order to build the vias and probing pads, conventional electroless copper plating was performed to build a thin seed layer. Probing pad pattern was developed using a conventional photolithography, and electroplating of copper was performed to build the probing pads. Finally, photoresist was stripped with 3% sodium hydroxide at 55 ^{o}C, and the copper seed layer was microetched to complete the process.

IV. ELECTRICAL MEASUREMENT

Initial measurements of capacitance were made with Hewlett Packard LCR Meter (4263B) at low frequency of 100 kHz. High frequency measurements were taken using Vector Network Analyzer (VNA) and 2 G-S (ground-signal) probes. The pitch of the probes is 500 μm, and locations of probes with respect to a capacitor are shown in Fig. 6. High frequency measurement of the 10 mm diameter circular capacitor was conducted. The capacitance was extracted by the methodology in [7]. As can be seen from Fig. 7, the structure resonates at around 900 MHz and becomes inductive after this frequency. The measurements were carried out from 50 MHz to 2GHz. The extracted capacitance is shown in Fig. 8. The value of the capacitor is 1.37 nF, and it remains relatively constant through the frequency band.

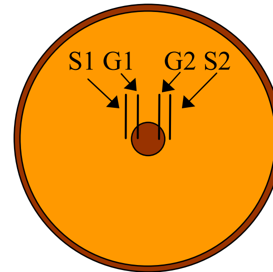

Fig. 6. Two probe locations.

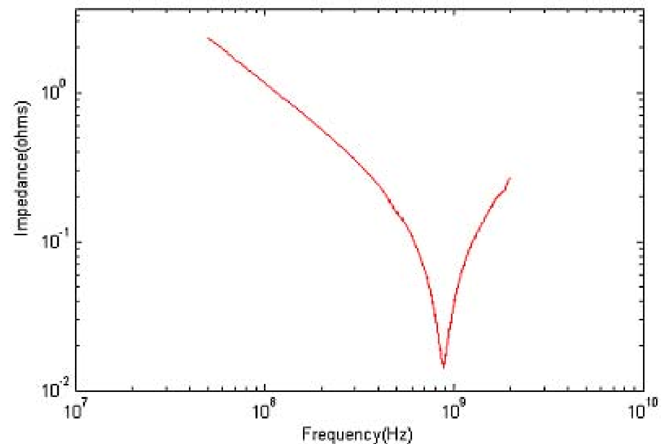

Fig. 7. Impedance profile of the capacitor.

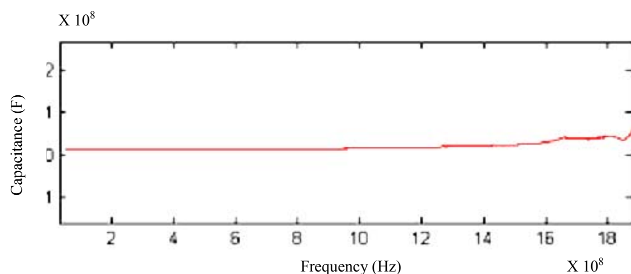

Fig. 8. Extracted capacitance of the structure.

V. Reliability Assessment

Although embedded passives are more reliable by eliminating solder joint interconnects, they also introduce other concerns such as cracks, delamination and component stability. More layers could be necessary to accommodate the embedded passives, and also, various materials within the substrate can cause significant thermo-mechanical stress due to coefficient of thermal expansion (CTE) mismatch. Unlike discrete components where defective parts can be replaced, rework is not a viable option for embedded passives and a single bad component can lead to scrapping the entire board. Consequently, reliability is a major issue in advancement and success of embedded passives technology.

A. Test Conditions

Thermal shock and constant temperature humidity tests were performed based on JEDEC standards (No. 22-A104-B and No. 22-A102-C) and others. Two thermal shock conditions were -40 to 125 °C and -55 to 125 °C. Both have dwell time of 10 minutes and tested for 1000 cycles. Moreover, two constant temperature humidity test conditions were 85 °C / 85%RH and 121 °C / 100%RH for 100 hours.

For TV1, which contains polymer/ceramic nanocomposite capacitors and PTF resistors, two thermal shock conditions and constant temperature and humidity condition of 85 °C/ 85%RH were used. For TV2, which contains only NiCrAlSi foil resistors, thermal shock condition of -55 to 125 °C and constant temperature and humidity condition of 121 °C / 100%RH were used. Table I summarizes the test conditions.

B. TV1 Resistor Results

Total of 4 boards were tested at various conditions. 3 boards have same sheet resistivity material of 10 ohms/sq, and other has 10 kohms/sq material. For each board, there are total of approximately 300 resistors, and 100 resistors divided into 6 different groups are examined during the tests. Fig. 9 shows the graphical locations of resistor groups examined, and Tables II and III summarize the results.

TABLE I
VARIOUS RELIABILITY TEST CONDITIONS

Test Cases	Temperature range	Soak Time	Humidity	Total Cycles or Hours
Thermal Shock 1	-40 to 125 °C	10 minutes	N/A	1000 cycles
Thermal Shock 2	-55 to 125 °C	10 minutes	N/A	1000 cycles
Temperature Humidity 1	85 °C	N/A	85%	100 hours
Temperature Humidity 2	121 °C	N/A	100%	100 hours

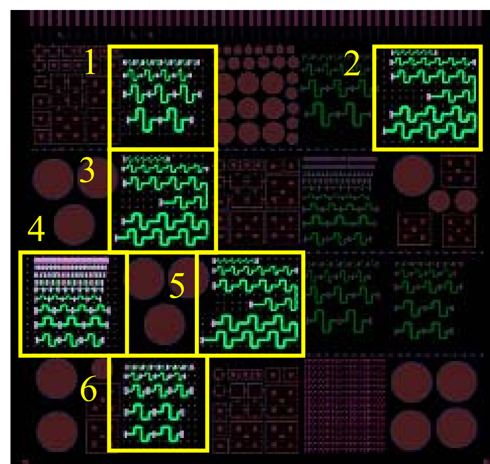

Fig. 9. TV1 resistor groups examined.

TABLE II
TV1 INITIAL TYPICAL RESISTANCE RANGE

	Typical Resistance Range	
Resistor Group	PTF 10 ohm/sq	PTF 10 kohm/sq
1	80 – 130	80 k
2	400 – 600	350 k – 400 k
3	400 – 600	350 k – 400 k
4	5 – 80	5 k – 60 k
5	400 – 600	350 k – 400 k
6	60 – 100	50 k – 60 k

TABLE III
SUMMARY OF TV1 RESISTOR RESULTS

	PTF 10 ohms/sq			PTF 10 kohms/sq
Resistor Group	Thermal Shock (-55 to 125 °C 1000 cycles)	Temperature Humidity (85 °C/85RH 100 hours)	Thermal Shock (-40 to 125 °C 1000 cycles)	Thermal Shock (-40 to 125 °C 1000 cycles)
1	-2.07%	2.21%	-0.91%	-4.29%
2	-2.19%	2.22%	-1.11%	-4.61%
3	-1.97%	2.09%	-1.12%	-4.30%
4	-3.85%	3.08%	-1.45%	-3.74%
5	-1.78%	2.16%	-1.06%	-4.37%
6	-2.15%	2.36%	-1.02%	-4.15%

The values of PTF resistors range from 5 ohms to 600 ohm with 10 ohms/sq and 5 kohms to 400 kohms with 10 kohms/sq. After 1000 cycles of thermal shock, most of the resistors experienced a slight decrease in resistance, while after 100 hours of constant temperature humidity test, most of the resistors experienced a slight increase in resistance. Both of these results are expected with PTF materials due to shrinkage and compaction of carbon particles with heating and swelling and separation of carbon particles with moisture. This effect is demonstrated in these results where a larger resistance change is observed with the more aggressive thermal shock conditions. A classic problem with PTF resistors of resistor instability due to interfacial oxidation has been overcome in these trials. Among the examined resistors, none have failed or changed more than 6%.

C. TV1 Capacitor Results

Total of 5 capacitor boards were tested at various conditions. For each board, there are total of 98 capacitors, and 68 representing various geometries, sizes, and locations

are examined. These are grouped into various geometries and sizes of capacitors. Circle 1 groups the biggest and Circle 4 groups the smallest circular capacitors. Similarly, Square 1 groups the biggest and Square 3 groups the smallest square capacitors. All the measurements were taken at low frequency of 100 kHz. Fig. 10 shows the graphical locations of capacitors examined, and Table IV summarizes the results.

TABLE IV
SUMMARY OF TV1 CAPACITOR RESULTS

Board 1: Thermal Shock (-40 to 125 °C 1000 cycles)				
Capacitor Group	Average Initial Capacitance at 100 kHz (pF)	Average % Change	Avg. Initial Q-Factor at 100 kHz	Average % Change
Circle 1	1050	-1.79%	52	52.49%
Circle 2	269	-2.20%	46	49.83%
Circle 3	73	-2.67%	44	26.89%
Circle 4	70	-2.74%	44	27.98%
Square 1	997	-1.90%	51	42.07%
Square 2	187	-2.05%	46	30.70%
Square 3	49	-3.15%	42	25.68%
Board 2: Thermal Shock (-40 to 125 °C 1000 cycles)				
Capacitor Group	Average Initial Capacitance at 100 kHz (pF)	Average % Change	Avg. Initial Q-Factor at 100 kHz	Average % Change
Circle 1	1188	-1.92%	50	43.78%
Circle 2	357	-2.62%	46	34.94%
Circle 3	129	-2.62%	40	22.04%
Circle 4	111	-2.66%	41	22.57%
Square 1	1043	-2.18%	48	33.80%
Square 2	239	-2.84%	43	27.99%
Square 3	73	-3.00%	39	19.95%
Board 3: Thermal Shock (-55 to 125 °C 1000 cycles)				
Capacitor Group	Average Initial Capacitance at 100 kHz (pF)	Average % Change	Avg. Initial Q-Factor at 100 kHz	Average % Change
Circle 1	613	-2.09%	61	42.50%
Circle 2	149	-8.88%	45	65.44%
Circle 3	61	-20.22%	38	102.20%
Circle 4	54	-22.78%	37	103.47%
Square 1	432	-3.50%	55	49.73%
Square 2	93	-13.37%	43	74.84%
Square 3	48	-24.66%	38	99.14%
Board 4: Thermal Shock (-55 to 125 °C 1000 cycles)				
Capacitor Group	Average Initial Capacitance at 100 kHz (pF)	Average % Change	Avg. Initial Q-Factor at 100 kHz	Average % Change
Circle 1	1404	-3.74%	85	-25.61%
Circle 2	376	-4.50%	72	-24.96%
Circle 3	131	-6.62%	59	-29.01%
Circle 4	107	-7.98%	60	-26.97%
Square 1	1032	-3.38%	77	-28.02%
Square 2	200	-5.26%	66	-27.69%
Square 3	91	-9.88%	58	-27.38%
Board 5: Constant Temperature Humidity (85 °C/85%RH 100 hours)				
Capacitor Group	Average Initial Capacitance at 100 kHz (pF)	Average % Change	Avg. Initial Q-Factor at 100 kHz	Average % Change
Circle 1	534	2.10%	66	-24.77%
Circle 2	131	3.95%	54	-21.11%
Circle 3	46	0.68%	54	-16.50%
Circle 4	40	1.18%	55	-18.71%
Square 1	358	4.03%	58	-21.24%
Square 2	72	1.09%	52	-14.84%
Square 3	30	0.61%	50	-9.88%

Initial values of capacitance and quality factor vary significantly in between boards due to using different materials and processes formulated by PRC and EI. The values of capacitance range approximately from 30 to 1400 pF, and quality factor range approximately from 40 to 85. After 1000 cycles of thermal shock, all the capacitors experienced decrease in capacitance, while some quality factor increased and some decreased. After 100 hours of constant temperature and humidity test, capacitance slightly increased and quality factor decreased. The primary cause of the large capacitance and Q-factor changes observed in board 3 can be attributed to the incompatibility of processing resistors and capacitors on the same layer. The fundamental problem is that resistor terminations must be protected with an anti-oxidant treatment for long term stability, while the capacitor electrodes require an oxidation coating for maximum dielectric to electrode adhesion. In general, for cost and process simplicity reasons, it is desired to place resistors on separate layers from capacitors and to place both on internal board layers. Although some capacitors were initially shorted, none that are examined failed during the reliability tests.

D. TV2 Resistor Results

Total of 4 identical boards with NiCrAlSi foil resistors were tested at various conditions. Approximately 100 out of 550 resistors were monitored from each board, and most of the resistors experienced only a slight increase of less than 1%. Overall, NiCrAlSi resistors show much more reliable results than PTF resistors. Fig. 11 shows the rough graphical locations of resistor groups examined, and Table V summarizes the results. TV2 contains various geometries, sizes, and values of NiCrAlSi foil resistors.

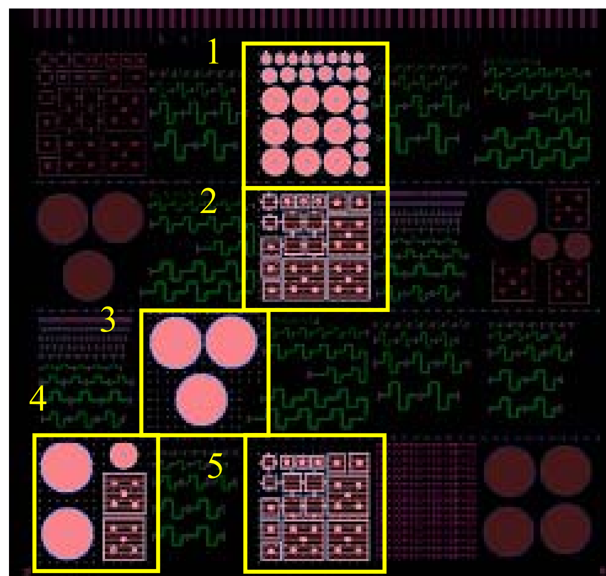

Fig. 10. TV1 capacitor groups examined.

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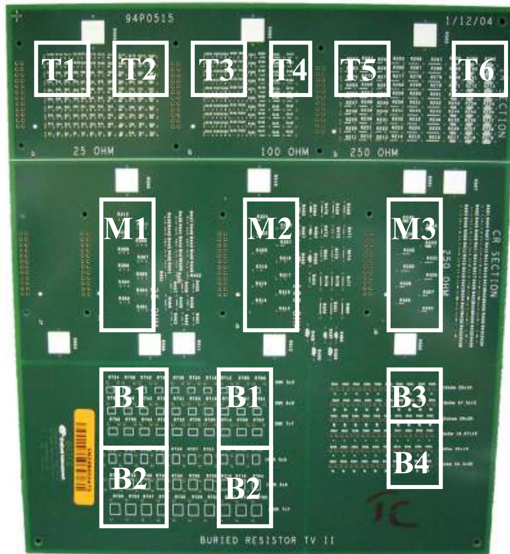

Fig. 11. TV2 resistor groups examined.

TABLE V
SUMMARY OF TV2 RESISTOR RESULTS

	NiCrAlSi foil		
Resistor Group	Typical Resistor range (ohms)	Thermal Shock (-55 to 125 °C 1000 cycles)	Temperature Humidity (121 °C/ 100RH 100 hours)
T1	~ 20	0.43%	0.38%
T2	~ 100	0.07%	0.08%
T3	~ 75	0.06%	0.05%
T4	~ 1 k	0.04%	0.09%
T5	~ 3 k	0.38%	0.84%
T6	~ 9 k	0.41%	0.69%
M1	20 – 100	0.21%	0.07%
M2	70 – 100	0.06%	0.08%
M3	~9 k	0.30%	0.70%
B1	~ 60K	0.31%	0.52%
B2	~ 100K	0.30%	0.53%
B3	5 – 10	0.51%	0.68%
B4	~ 15	0.07%	0.72%

VI. CONCLUSION

Embedded passives have been successfully designed and fabricated onto multilayered microvia organic substrate using low temperature processes. Its unique design with microvia interconnects and integration of multiple materials mimic SOP concept of package as a system to integrate digital, RF, optical, and sensor functions. High frequency measurement showed polymer/ceramic nanocomposite capacitor up to 900 MHz without resonance. Furthermore, extensive reliability tests based on JEDEC standards were performed. Both PTF and NiCrAlSi foil resistors show stable results; however, some capacitor boards show significant change in capacitance and quality factor as explained previously. Tables VI and VII summarize the results. Future work will include evaluation of effect of accelerated reliability assessments on high frequency behavior of polymer/ceramic embedded capacitors.

TABLE VI
SUMMARY OF EMBEDDED RESISTOR RELIABILITY TEST RESULTS

	Test Condition	Average % change
PTF 10 ohms/sq	TC -55 to 125 °C	-2.92%
PTF 10 ohms/sq	HAST 85/85	2.12%
PTF 10 ohms/sq	TC -40 to 125 °C	-1.24%
PTF 10 kohms/sq	TC -40 to 125 °C	3.99%
NiCrAlSi	TC -55 to 125 °C	0.16%
NiCrAlSi	121°C/100 RH	0.81%

TABLE VII
SUMMARY OF EMBEDDED CAPACITOR RELIABILITY TEST RESULTS

	Test Condition	Average % change in Capacitance	Average % change in Q-Factor at 100 kHz
Board 1 Capacitor	TC -40 to 125	-2.38%	35.18%
Board 2 Capacitor	TC -40 to 125	-2.67%	28.39%
Board 3 Capacitor	TC -55 to 125	-6.09%	-27.06%
Board 4 Capacitor	TC -55 to 125	-14.73%	78.85%
Board 5 Capacitor	HAST 85/85	2.04%	-18.20%

ACKNOWLEDGMENT

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