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# Design for Accelerated Testing of DC-link Capacitors in Photovoltaic Inverters based on Mission Profiles

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**Abstract**—The dc-link capacitor is considered as a weak component in Photovoltaic (PV) inverter systems and its reliability needs to be evaluated and tested during the product development. Conventional reliability testing methods for capacitors are typically carried out under constant loading conditions, which do not reflect the real operating conditions (e.g., mission profile) of the dc-link capacitor in PV inverters. To address this issue, a new reliability testing concept for the dc-link capacitor in PV inverters is proposed in this paper. In contrast to the conventional method, the proposed reliability testing method designs the test profile through the modification of the original mission profile (e.g., solar irradiance and ambient temperature) in order to maintain the test condition as close to the real application as possible. A certain acceleration factor is applied during the mission profile modification based on the lifetime model of the capacitor, in order to increase the thermal stress of the dc-link capacitor during test, and thereby effectively reduce the testing time.

**Index Terms**—Reliability, accelerated testing, mission profile, capacitors, PV inverters.

## I. INTRODUCTION

Reliability is one of the key performance metrics of inverters for Photovoltaic (PV) applications, and the demand has been continuously increasing, e.g., from the current lifetime expectation of 10-15 years to 20-30 years in the near future [1]. Some field experiences have indicated that PV inverters are responsible for a large share of failure events and being one of the weakest components in a PV system [2]–[4]. Such failure events can contribute to a significant loss of revenue for

the PV system owner, which is mainly due to the loss of energy yield during the downtime period of the PV power plants, but also due to the cost of inverter replacement. In order to ensure the reliability performance and to avoid unexpected failures of the PV inverters, the reliability evaluation and testing are vital during the product design and the development of them.

Among other components in PV inverters, the dc-link capacitor is one of the reliability-critical components that is highly stressed during the operation and thus it has been witnessed a high failure rate [5]–[7]. Typically, the aluminum electrolytic capacitors are adopted for the dc-link application due to their high capacitance [4], which usually gives a lower cost and volume compared to the other capacitor technologies. During the operation, the ripple current in the capacitor will inevitably induce power loss, leading to an increase in the core temperature of the capacitor (i.e., hotspot temperature) [8], [9]. In that case, the loading conditions of the PV inverter (e.g., PV power production and its variation) will certainly influence the thermal stress of the capacitor, as it has been experimentally demonstrated in [10]. Besides, the environmental condition of the installation site like the ambient temperature can also affect the hotspot temperature of the capacitor during the operation, especially for the PV inverter located outdoor (e.g., micro-inverter and string-inverter applications). The increase of the internal hotspot temperature of the aluminum electrolytic capacitor is one of the major stress factors that lead to electrolyte evaporation and contaminant (while other stress factors such as humidity are more relevant for film capacitors). This will accelerate the wear-out of the capacitor, and thus decrease the capacitor lifetime and its reliability [11]. Therefore, the reliability of the dc-link capacitor in PV inverters has been investigated in several aspects such as design for reliability [12], lifetime analysis [13]–[15], and testing [16].

Conventionally, the reliability testing of the dc-link capacitor is done under a constant electrical stress (e.g., ripple current/voltage and bias voltage) and/or environmental stress (e.g., ambient temperature) condition. For instance, a rated (constant amplitude) ripple current, rated bias voltage, and rated ambient temperature are applied to the capacitor during the accelerated lifetime testing in [16] and [17]. Similar testing condition is also considered in [18]–[20], but the ripple current is not applied during the test. In [21]–[23], only the environmental stress is considered during the accelerated test, where a constant ambient temperature condition (e.g., rated value or

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TABLE I  
COMPARISON OF VARIOUS ACCELERATED TESTING METHODS FOR ELECTROLYTIC CAPACITORS.

Testing Methods	Electrical Stress Condition	Environmental Stress Condition	Inverter Operation	Note
[16], [17]	Rated ripple current/voltage Rated bias voltage	Rated ambient temperature	No	In [16], the capacitor is punctured to emulate electrolyte evaporation
[18]–[20]	Constant bias voltage	Constant ambient temperature	No	-
[21], [22]	No	Constant ambient temperature	No	In [22], the capacitor is punctured to emulate electrolyte evaporation
[23]	No	Constant ambient temperature (overstress)	No	The capacitor is operated above SOA during the test
[24]	Constant ripple current/voltage	Constant ambient temperature	PWM	-
[25], [26]	Constant ripple current/voltage	No	PWM	-
[27], [28]	Square wave bias voltage (overstress)	Constant ambient temperature (overstress)	No	The capacitor is operated above SOA during the test
[29]	Square wave bias voltage (overstress)	No	No	The capacitor is operated above SOA during the test
[30]	Constant bias voltage	Intermittent ambient temperature	No	-
Proposed method	Ripple current and voltage bias levels are based on mission profile (with modification)	Constant ambient temperature (based on mission profile)	PWM	Testing profile has similar dynamics as mission profile. The capacitor is operated within SOA during the test

even above) is applied to the capacitor under test. The testing condition of the conventional accelerated testing method for capacitor has been summarized in Table I. The outcome of the conventional testing method, where the capacitors are stressed under a constant loading condition, is either passing a standard qualification test (e.g., after a certain number of testing hours) or obtaining a lifetime/degradation model (if the capacitors are tested until failure). The lifetime model of the capacitor with respect to the stress factors (e.g., temperature and voltage) is normally given by the capacitor manufacturer [11]. Passing the standard, e.g., IEC 62093, ensures a certain reliability performance. However, it does not reflect a quantitative measure of the PV inverter reliability in real-field operation. For instance, the inverter may be highly over-designed even though it passes the standard testing. This is mainly due to the misalignment between the testing condition and the real operating condition of the dc-link capacitor in the PV inverter. In real-field operation, the dc-link capacitor in the PV inverter will be stressed under more dynamic loading conditions (e.g., both electrical and environmental stress conditions) compared to the standard testing conditions (i.e., constant stress condition) due to the variation in the solar irradiance and ambient temperature, which is also referred to as mission profiles. This brings certain uncertainties into the reliability prediction based on the standard testing method. Moreover, the lack of a design verification method (e.g., testing under real operating condition) makes it difficult to improve the design in a cost-effective way, since the design margin cannot be easily quantified.

The above challenges raise a demand to improve testing methods for the dc-link capacitor in PV inverters to better represent similar stress conditions as in the mission profile operation. However, directly applying the mission profile as a testing condition is not practical, since the time-to-failure of the (well designed) component should be extremely long

when being stressed under the mission profile conditions (intended operating conditions). Therefore, a method to design the testing profile based on mission profile characteristic with certain acceleration factors is required. In previous studies, several concepts have been proposed for designing the testing profile where the component in the power converter (e.g., capacitors and power devices) are stressed under operating conditions close to the real application (e.g., mission profile), as it is summarized in Table I. Some of the early attempts to test and evaluate the reliability of the dc-link capacitor by considering the real application were discussed in [24]–[26], where the dc-link capacitor is stressed by operating the power converter with pulse-width modulation. However, the loading condition of the power converter during the test in [24] has been simplified (e.g., constant ripple current), which does not represent the mission profile of the PV application (e.g., dynamic loading condition). Besides, the environmental stress (e.g., ambient temperature) is not considered for the testing method in [25] and [26]. Dynamic electrical loading is used during the accelerated test in [27]–[29], where the capacitor is overstressed by the square wave bias voltage during the test. However, this loading condition only suitable for representing the voltage surge of the power supply in aircrafts, which is the target application in [27]–[29]. Moreover, the capacitor is overstressed beyond its rated voltage and/or rated ambient temperature during those test, which may risk to trigger the other failure modes which are not relevant in real-field operation. On the contrary, the intermittent ambient temperature is applied during the test in [30], while the bias voltage of the capacitor is kept constant. Therefore, a mapping between the real operating condition (e.g., mission profile) and the testing profile of the capacitors is still missing.

Recently, a reliability testing method has been applied to the PV inverters in [31], with standard accelerated testing methods (e.g., thermal cycling, damp heat, high temperature,

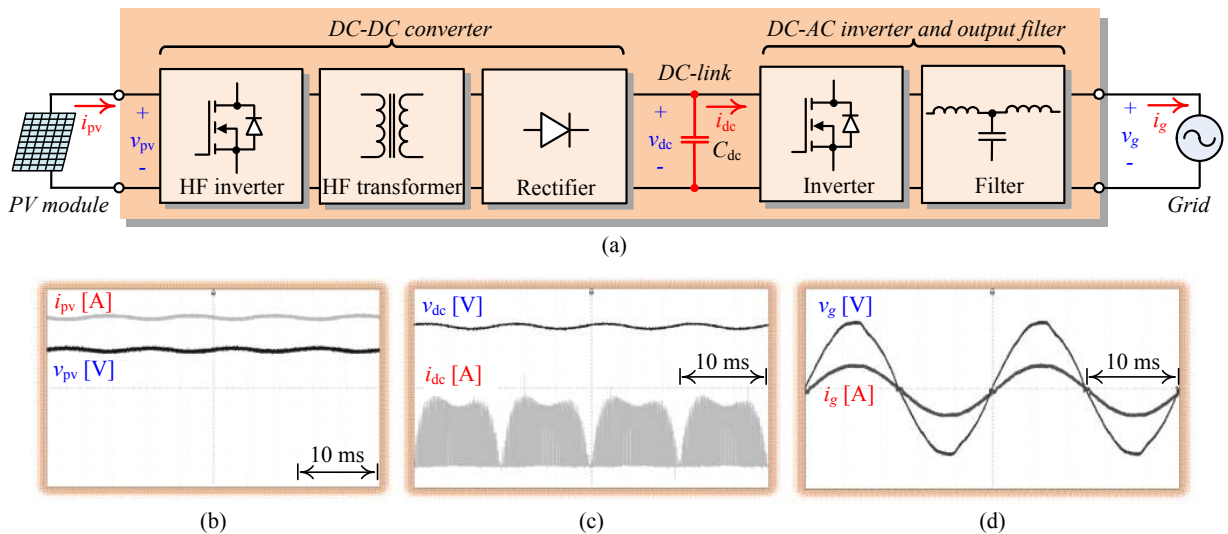


Fig. 1. A two-stage PV inverter where the dc-link capacitor  $C_{dc}$  acts as an energy buffer between the dc-side and the ac-side: (a) system diagram, (b) PV output voltage  $v_{pv}$  and current  $i_{pv}$ , (c) dc-link voltage  $v_{dc}$  and current  $i_{dc}$ , (d) grid voltage  $v_g$  and current injected to ac grid  $i_g$ .

and grid transient). Nevertheless, the mission profile of the PV system was not considered during the test. In [32], a mission profile-based accelerated test method has been applied to the power devices in PV inverters. However, the correlation between the real mission profile and the testing profile is not clearly discussed. In other words, a procedure to systematically design the test profile from the real mission profile with a certain acceleration factor is still not yet defined. In order to address the above challenges, a mission profile-based accelerated testing method for the dc-link capacitor in PV inverters is proposed in this paper. The proposed testing method is extended from a previous concept in [33] where the real mission profile of the PV system (e.g., solar irradiance and ambient temperature) is modified in a way to accelerate the degradation process of the dc-link capacitor. Compared to the existing testing methods, the proposed testing method constructs the testing profile from the mission profile by introducing a certain acceleration factor. By doing so, the operating condition of the dc-link capacitor during the test can be maintained close to the real PV inverter application, while the degradation process can still be accelerated. In this work, a comprehensive analysis including validation of thermal stress modeling is further discussed following [10].

The rest of this paper is organized as follows: A system description of the PV inverter employed in the test is provided in Section II. Then, the thermal modeling and reliability evaluation methods of the dc-link capacitor are discussed in Section III while the real-field measurement of thermal stress in the dc-link capacitor is presented in Section IV. Afterwards, the proposed mission profile-based accelerated testing concept is presented in Section V, where the possibilities for modifying the solar irradiance and ambient temperature during the test are explored. A guideline for designing the test profile is provided in Section VI, where the acceleration factors are applied to the solar irradiance and ambient temperature based on the required accumulated damage of the capacitor. Finally,

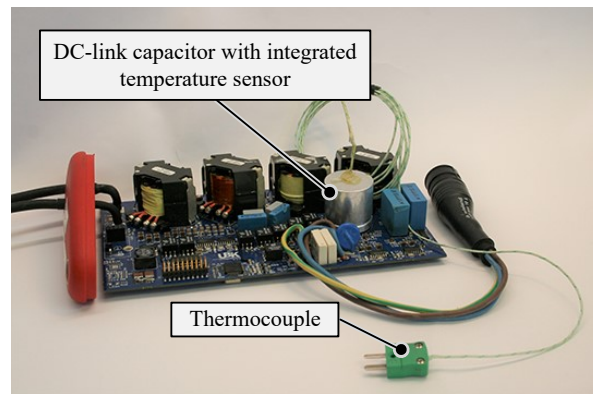


Fig. 2. Hardware prototype of the PV inverter where a thermocouple has been integrated with the dc-link capacitor.

concluding remarks are given in Section VII.

## II. PHOTOVOLTAIC INVERTERS

### A. System Description

A PV inverter is used to convert the dc power generated by PV module into the ac power and deliver it to the grid [34]. One of the commonly used system architecture is the two-stage PV system as shown in Fig. 1, where the two power conversion stages are used: 1) the dc-dc converter and 2) the dc-ac inverter. In this configuration, the dc-dc converter is responsible for extracting the power generated by the PV module using Maximum Power Point Tracking (MPPT) operation. It is also required to convert the PV module output voltage  $v_{pv}$  (e.g., 10-60 V) to a regulated dc-link voltage level  $v_{dc}$  (e.g., 400 V). Then, the dc-ac inverter converts the extracted dc power into ac power and delivers it into the grid. The hardware prototype of the PV inverter is shown in Fig. 2 and the system parameters are given in Table II.

TABLE II  
PARAMETERS OF THE TWO-STAGE PV INVERTER (FIG. 1).

Input voltage range $v_{pv}$	10-60 V
Rated power	300 W
Switching frequencies	DC-DC converter: 105 kHz, DC-AC inverter: 20 kHz
DC-link capacitor $C_{dc}$	180 $\mu$ F, 500-V electrolytic capacitor
$LCL$ -filter	$L_{inv} = 2.6$ mH, $L_g = 1.8$ mH $C_f = 470$ nF
Grid nominal voltage (RMS)	$V_g = 230$ V
Grid nominal frequency	$\omega_0 = 2\pi \times 50$ rad/s
Peak efficiency of power circuit	96.2 %
Peak MPPT efficiency	99.5 %

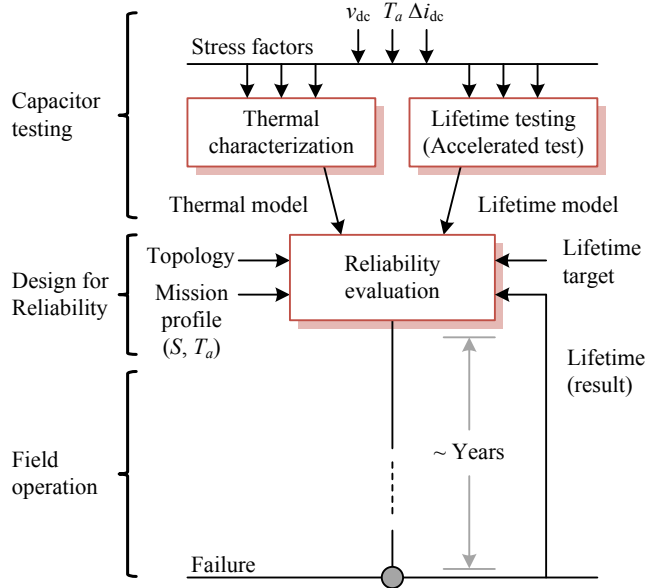


Fig. 3. Conventional method to evaluate the reliability of the dc-link capacitor (e.g., aluminum electrolytic capacitor) during the design phase of PV inverters ( $v_{dc}$ : dc-link voltage,  $\Delta i_{dc}$ : ripple current,  $S$ : solar irradiance,  $T_a$ : ambient temperature).

### B. Design of DC-link Capacitor

Between the two power conversion stages, the dc-link capacitor is required to maintain a relatively constant dc-link voltage. Inevitably, the instantaneous power from the single-phase ac grid induces the double-line frequency (e.g., 100 Hz) power fluctuation to the dc-side. This double-line frequency power oscillation needs to be suppressed at the dc-link to ensure the tracking performance of the MPPT algorithm [7]. Therefore, the dc-link capacitor of the single-phase system is normally designed according to the dc-link voltage ripple  $\Delta v$  requirement as

$$\begin{aligned}
 C_{dc,min} &> \frac{P_{pv}}{\omega_0 \cdot \Delta v \cdot v_{dc}} \\
 &= \frac{300}{(2\pi \cdot 50) \cdot (0.04 \cdot 400) \cdot 400} \\
 &= 150 \mu\text{F}
 \end{aligned} \tag{1}$$

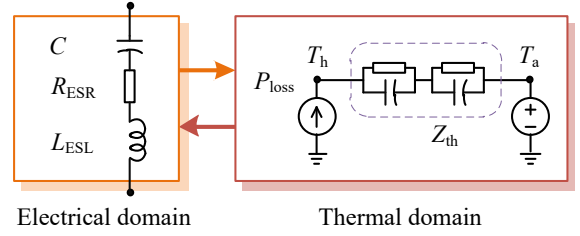


Fig. 4. Electro-thermal model of the electrolytic capacitor, where  $C$  is the capacitance,  $R_{ESR}$  and  $L_{ESL}$  are the equivalent series resistance and inductance,  $P_{loss}$  is the power loss,  $T_h$  and  $T_a$  are the hotspot and ambient temperature, and  $Z_{th}$  is the thermal impedance.

where  $C_{dc,min}$  is the minimum dc-link capacitance,  $P_{pv}$  is the rated output power,  $\omega_0$  is the grid nominal frequency, and  $v_{dc}$  is the nominal dc-link voltage [12].

### III. RELIABILITY MODELING OF DC-LINK CAPACITORS

In this section, a conventional method to evaluate the reliability of the dc-link capacitor in a PV inverter is discussed. A general diagram of the assessment procedure is illustrated in Fig. 3, which includes the characterization of the capacitor in terms of thermal and lifetime modeling as well as reliability evaluation based on the mission profile.

#### A. Thermal Modeling of DC-link Capacitors

Since the thermal stress is one of the dominant factors that accelerates the degradation process of the electrolytic capacitor, it is necessary to model the thermal characteristic of the dc-link capacitor in order to assess its reliability. The thermal behavior of the dc-link capacitor can be modeled with a thermal network as it is illustrated in Fig. 4. During the operation, the ripple current (RMS) in the capacitor  $\Delta i_{dc}$  induces power loss  $P_{loss}$  due to the equivalent series resistance  $R_{ESR}$  following:

$$P_{loss} = \sum_{i=1}^n (\Delta i_{dc}(f_i))^2 \cdot R_{ESR}(f_i) \tag{2}$$

where  $\Delta i_{dc}(f_i)$  and  $R_{ESR}(f_i)$  are the ripple current and equivalent series resistance at the frequency  $f_i$ , respectively, while  $n$  is the number of frequency components. In this study, the equivalent series resistance parameter  $R_{ESR}$  has been measured experimentally at different frequencies and temperature conditions, as it is shown in Fig. 5.

Following the thermal model in Fig. 4, the power loss  $P_{loss}$  causes the internal temperature  $T_h$  to rise according to

$$T_h = \frac{d}{dt} Z_{th} * P_{loss} + T_a \tag{3}$$

where  $T_a$  is the ambient temperature and  $Z_{th}$  is the capacitor thermal impedance [12]. The thermal impedance of the capacitor  $Z_{th}$  is measured from an experiment for a given power loss (e.g., dissipated in the equivalent series resistance) and ambient temperature  $T_a$  as discussed in [35]. When the supply of the power loss (e.g., the ripple current injection) is removed, the (normalized) cooling behavior of the dc-link capacitor

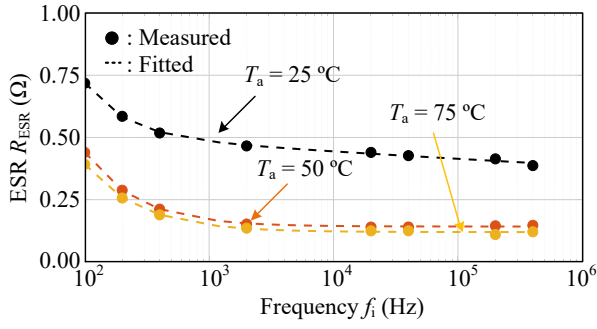


Fig. 5. Equivalent series resistance parameter  $R_{ESR}$  of the dc-link capacitor at different frequencies and temperature conditions.

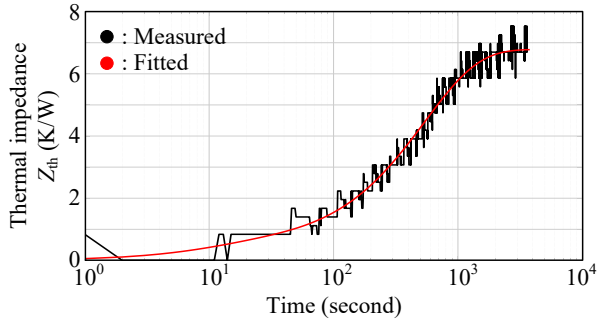


Fig. 6. Thermal impedance of the dc-link capacitor  $Z_{th}$  characterized by applying a ripple current of 2 A (RMS) with a frequency of 100 Hz.

represents the thermal impedance. The thermal impedance of the dc-link capacitor used in this paper is obtained as

$$Z_{th} = 6.3 \cdot (1 - e^{-(t/543.3)}) + 0.483 \cdot (1 - e^{-(t/10.06)}) \quad (4)$$

which is based on fitting the measurement results shown in Fig. 6 using the Foster thermal network [36].

### B. Lifetime Modeling of DC-link Capacitors

In general, the hotspot temperature and the applied voltage are the two main stress factors that affect the degradation process of electrolytic capacitors [8]. These stress factors lead to the acceleration of the chemical process (e.g., electrolyte evaporation), which consequently results in a decrease of the capacitance  $C$  and an increase of the equivalent series resistance  $R_{ESR}$ . For electrolytic capacitors, the reliability testing is normally done by applying a relatively high constant operating temperature and voltage [18] in order to accelerate the degradation process of capacitors. Afterwards, the lifetime model of the capacitor with respect to these stress factors can be obtained as given in the following

$$L_f = L_0 \times 2^{\frac{T_0 - T_h}{10}} \times \left(\frac{V}{V_0}\right)^{-5} \quad (5)$$

where  $L_f$  is the lifetime under the thermal and electrical stresses  $T_h$  and  $V$  (e.g., real operating condition),  $L_0$  is the lifetime under the reference temperature  $T_0$  and the nominal voltage  $V_0$  [37]–[39]. The lifetime model parameter of the capacitor used in this paper is specified in Table III.

TABLE III  
PARAMETERS OF THE LIFETIME MODEL OF A CAPACITOR [39].

Parameter	Symbol	Value
Rated lifetime (at $V_0$ and $T_0$ )	$L_0$	3000 hours
Rated operating voltage	$V_0$	500 V
Rated operating temperature	$T_0$	105°C

For the dynamic operating condition (e.g., mission profile), the Miner's rule can be employed to accumulate the damage occurred during the operation [40], which is calculated as

$$D = \sum_i \frac{l_i}{L_{fi}} \quad (6)$$

in which  $l_i$  is the time duration when the capacitor operates at a specific hotspot temperature  $T_h$  and voltage  $V$  while  $L_{fi}$  is the time-to-failure calculated from (5) at that specific stress condition. The lifetime of the capacitor is then determined when the damage is accumulated to  $D = 1$ .

It is worth to mention that the same methodology can also be applied to other capacitor technologies (and inverter topology). In that case, the lifetime model of the relevant degradation mechanism and their corresponding stress factors should be considered (in addition to the temperature and voltage stress).

### C. Design for Reliability of DC-link Capacitors

Once the thermal model and the lifetime model of the dc-link capacitor have been obtained, the design for reliability approach can be applied in order to ensure the reliability performance of the dc-link capacitor under a given mission profile. Normally, the mission profile needs to be converted into the loading condition of the capacitor (e.g., power losses). This calculation requires the knowledge of the topology and operation of the PV inverter, as discussed in Section II. Then, the obtained power loss profile is applied to the thermal model in order to estimate the hotspot temperature of the capacitor during the operation. Afterwards, the lifetime of the dc-link capacitor can be estimated from the lifetime model together with Miner's rule for accumulating the damage during the entire operation (e.g., mission profile). If the estimated lifetime is below the lifetime target, either the capacitor or the overall PV inverter needs to be re-sized.

However, the validation of the design for reliability approach discussed above is challenging. More specifically, it is difficult to experimentally validate if the lifetime of the dc-link capacitor can be achieved in the real operation according to the estimation, especially with a limited testing time. Typically, the reliability-related tests after the design phase are more relevant to the qualification of the PV inverter. Thus, very limited information about the wear-out lifetime can be obtained, especially when considering the operation under the specified mission profile. In many cases, the failure from field operation is the only indicator of the real lifetime of the component, but this information can normally be obtained after certain years of operation while the product development cycle is much shorter.



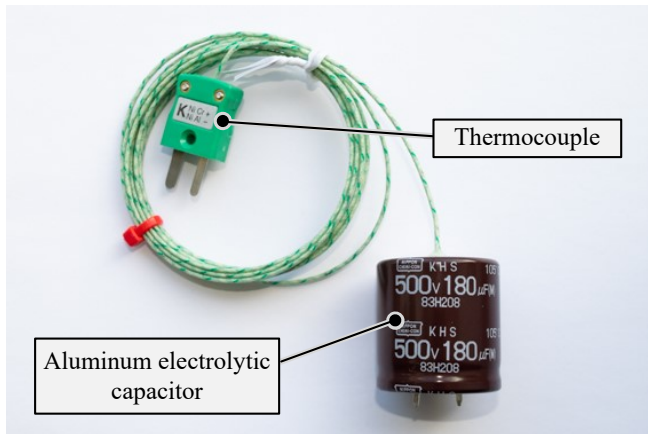


Fig. 7. A sample of aluminum electrolytic capacitor used in the dc-link with integrated temperature sensor.

#### IV. REAL-FIELD THERMAL STRESS OF DC-LINK CAPACITORS IN PV INVERTERS

In order to investigate the impact of mission profile on the thermal stress and reliability of dc-link capacitor, three daily mission profiles are used as case studies. For each case study, the hotspot temperature of the dc-link capacitor is measured experimentally and compared.

##### A. Hotspot Temperature Measurement

The temperature measurement is based on thermocouple sensor (i.e., Type-K with an accuracy of 0.75 %), which has been integrated to the dc-link capacitor (i.e., testing sample from manufacturer), as shown in Fig. 7. The placement of the sensor is approximately at the core (middle) of the capacitor, which is normally referred to as the hotspot/core temperature. This is normally the area with the highest thermal stress for the capacitor due to its lower thermal conductivity compared to, e.g., the surface area of the capacitor [41], [42]. A similar temperature measurement method for the dc-link capacitor has also been employed in the previous studies [36], [43].

The dc-link capacitor is placed on the printed circuit board inside the enclosure, as it is shown in Fig. 2, and filled up with an encapsulation compound, which is shown in Fig. 8. By doing so, the hotspot temperature profile can be directly measured during the operation including the thermal-coupling effect among different components. This result will be used as a benchmark case to validate the thermal modeling accuracy under real-field operation.

##### B. Mission Profiles

For PV inverters, the mission profile parameter consists of solar irradiance and ambient temperature, since they have a strong influence on the electrical and thermal loading of the inverter. The mission profiles used in this paper have been recorded at Aalborg University, Denmark [44]. Three representative daily mission profiles are shown in Fig. 9, which are recorded under different environmental conditions of the PV inverters. For instance, the mission profile in Fig. 9(a)

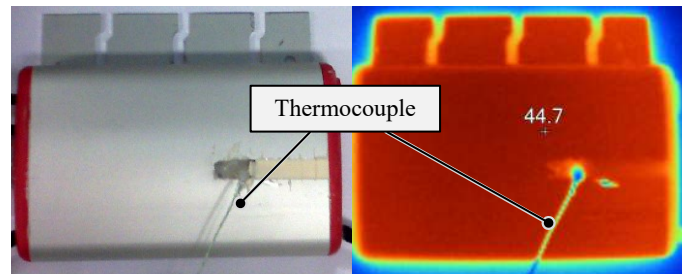


Fig. 8. Hardware prototype of the PV inverter: (a) picture of the prototype with integrated thermal sensor for the dc-link capacitor and (b) the thermal image acquired at the rated power and ambient temperature of 28°C.

represents the operating condition during a clear day, where the solar irradiance changes smoothly and slowly during the day. This is a typical operating condition of the PV inverter during the clear-sky condition. The cloudy-day condition is also considered during the test, as it is demonstrated by the mission profile in Fig. 9(b). In this case, the solar irradiance, and thereby the output power of the PV inverters, fluctuates considerably during the entire day. Another operating condition considered in the test is shown in Fig. 9(c), where the mission profile during a low-irradiance day is considered. This mission profile represents the operating condition where the solar resources are relatively low during the entire day.

##### C. Thermal Stress of DC-link Capacitors

The thermal stress profiles of the dc-link capacitor from the experimental measurements are shown in Fig. 10, which are obtained by applying the mission profiles shown in Fig. 9 to the PV inverter test-bench. The same mission profiles are also applied to the thermal model of the dc-link capacitor in the PV inverter and the estimated thermal stress profiles are also shown together with the experimental ones. It can be seen from the results that the thermal stress profiles obtained from the thermal model are well aligned with the experimental results. Thus, the thermal model used in this work is capable of estimating the thermal stress dynamics of the dc-link capacitor under mission profile operation.

In general, the thermal stress of the capacitor is the highest during the clear-day condition due to the high power production of the PV module and high power losses generated by the PV inverter, where the maximum hotspot temperature of the capacitor reaches 50°C. The thermal stress level is reduced in the case of cloudy-day and low-irradiance day conditions due to a considerable reduction in the PV power production and thus the power loss dissipated in the dc-link. In the cloudy day, due to its thermal capacitance as shown in Fig. 6, the dc-link capacitor still has relatively slow dynamics in its thermal profile in Fig. 10(b), compared to that in the mission profile shown in Fig. 9(b). Its thermal time-constant effectively acts as a low-pass filter in the temperature rise when the power loss is applied. This result leads to a conclusion that a fast thermal stress dynamic is not required for accelerated testing of the dc-link capacitor even under a fast variation in the mission profile of PV applications, which can simplify the test requirement

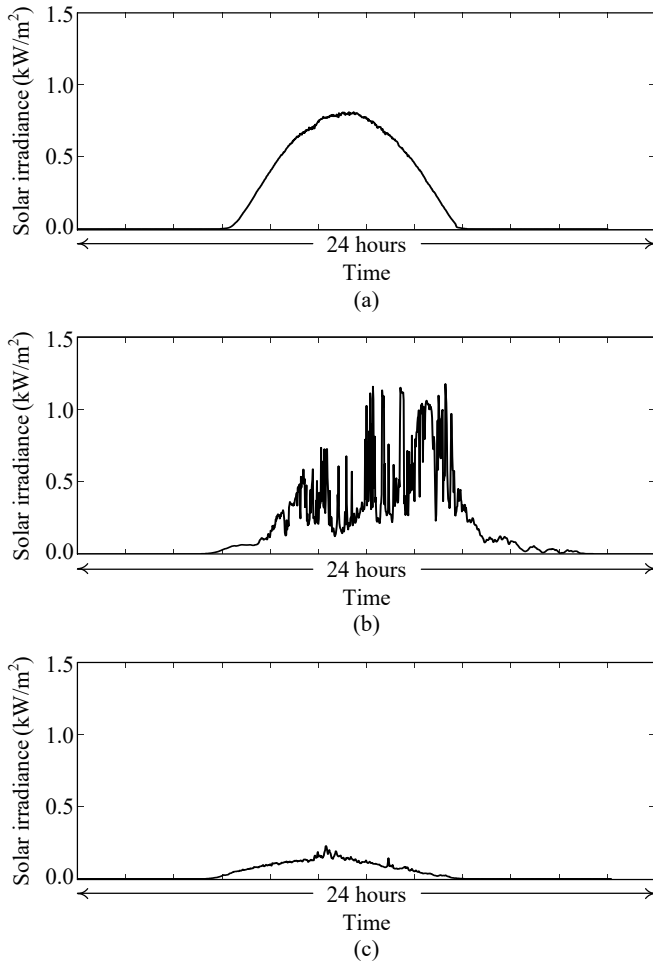


Fig. 9. One-day mission profile (i.e., solar irradiance profile) used in the case study: (a) Clear day, (b) Cloudy day, and (c) Low-irradiance day.

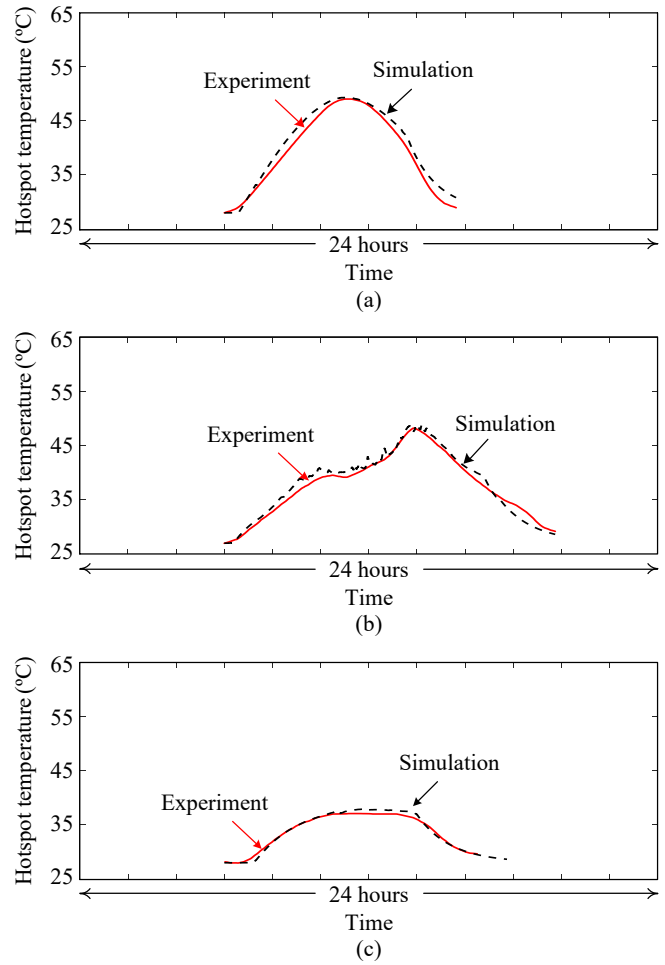


Fig. 10. Experimental and simulation results of the thermal stress of dc-link capacitor during: (a) Clear day, (b) Cloudy day, and (c) Low-irradiance day.

regarding the temperature elevation, which will be discussed in the next part.

## V. PROPOSED MISSION PROFILE BASED ACCELERATED TESTING METHOD FOR CAPACITORS

In the following, the new reliability testing concept for the dc-link capacitor in PV inverter is proposed. The methodology of the proposed testing strategy and a method to modify the mission profile with certain accelerated stress conditions are discussed.

### A. Methodology

To address the challenge discussed previously, a new reliability testing method for the dc-link capacitor in the PV inverter is needed. This testing method should be applied as part of the design verification as illustrated in Fig. 11. The requirements of such testing method are

- The degradation process of the dc-link capacitor should be accelerated during the test
- The dc-link capacitor should be stressed under the operating condition close to the real mission profile

One possibility to maintain the stress condition of the dc-link capacitor during the test similar to that in the real application is by realizing the test profile through the modification of the original mission profile [33]. Afterwards, the modified mission profile can be applied to test the prototype of the PV inverter, and the degradation of the dc-link capacitor can be measured. The concept of the proposed mission profile-based accelerated testing of dc-link capacitor is illustrated in Fig. 12.

Clearly, the original mission profile needs to be modified with a certain acceleration factor in a way to accelerate the degradation process of the dc-link capacitor during the test and thereby reduce the testing time. For PV systems, the solar irradiance and ambient temperature are considered as the mission profile parameters, as they strongly affect both the electrical and thermal loading conditions of the components in the PV inverter. The modification of these two parameters needs to consider the impact on the degradation of the dc-link capacitor according to the lifetime model in (5).

### B. Modifying the Solar Irradiance Profile

In general, the solar irradiance is the mission profile parameter that strongly affects the dynamics of the PV power



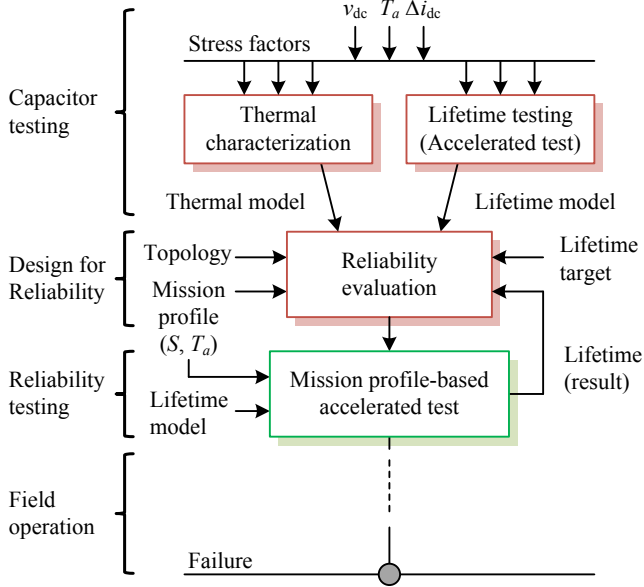


Fig. 11. Proposed method to evaluate the reliability of the dc-link capacitor in PV inverters through mission profile-based accelerated testing ( $v_{dc}$ : dc-link voltage,  $\Delta i_{dc}$ : ripple current,  $S$ : solar irradiance,  $T_a$ : ambient temperature).

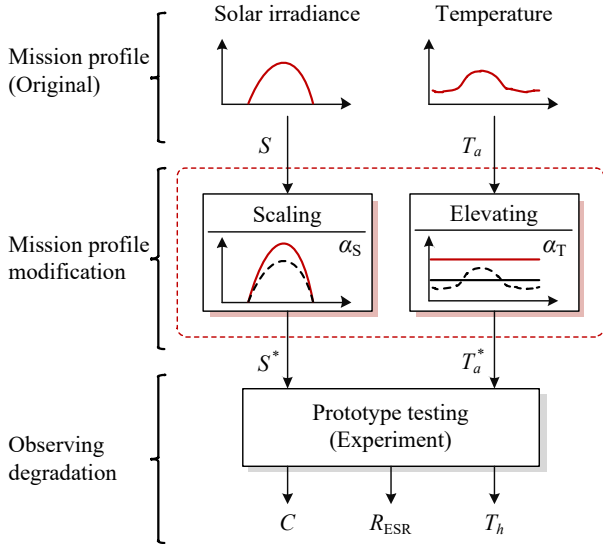


Fig. 12. Mission profile-based accelerated testing of the dc-link capacitor in PV inverters, where  $(S, T_a)$  and  $(S^*, T_a^*)$  are the original and the modified mission profiles, respectively.

production, and thereby the loading of the dc-link capacitor. Thus, it has a direct impact on the power losses  $P_{loss}$ , which in turn contributes to the hotspot temperature of the dc-link capacitor  $T_h$  according to the thermal model in Fig. 4.

In order to accelerate the degradation of the dc-link capacitor during the test, the solar irradiance profile needs to be modified in a way to increase the loading and thereby the power losses in the dc-link capacitor. This can be achieved by multiplying the original solar irradiance profile with a certain

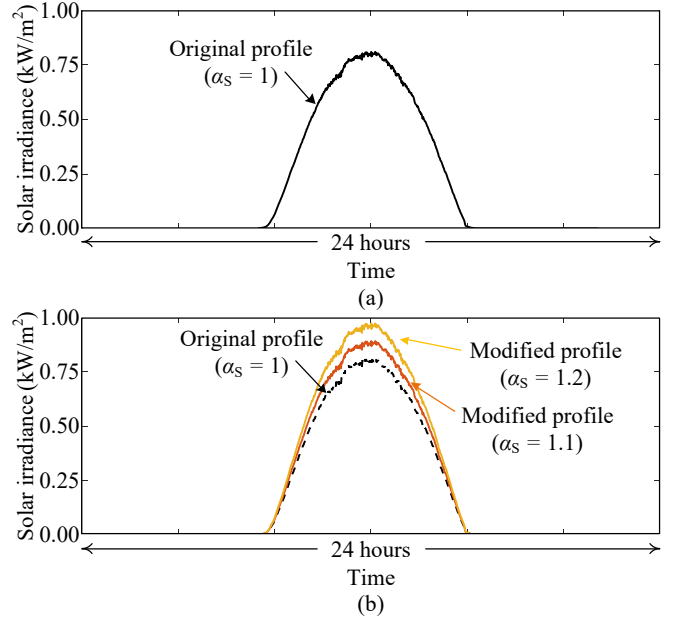


Fig. 13. Daily solar irradiance profile: (a) original profile and (b) modified profile with different amplitude scaling factors  $\alpha_S$ .

amplitude scaling factor  $\alpha_S$ , which is defined as

$$\alpha_S = \frac{S^*}{S} \quad (7)$$

where  $S$  and  $S^*$  are the original solar irradiance and the modified solar irradiance, respectively.

An example of the solar irradiance amplitude modification is illustrated in Fig. 13, where the original daily solar irradiance profile (e.g., collected from the field operation) is modified with different amplitude scaling factors  $\alpha_S$  (e.g., increase the solar irradiance amplitude by 10% and 20% for  $\alpha_S = 1.1$  and 1.2, respectively). By doing so, the loading condition of the dc-link capacitor during the test is increased while its dynamic operation (e.g., shape) remains the same as the original one. As a result, the dc-link capacitor will degrade with a faster rate compared to the original mission profile, and thereby reduce the testing time. Notably, the maximum amplitude scaling factor is limited by the rated power of the PV inverter. When the solar irradiance is over-scaled, the loading of the PV inverter will be limited to its rated power and thus the dynamics (e.g., shape) of the mission profile will be affected.

### C. Modifying the Ambient Temperature Profile

According to the thermal model of the dc-link capacitor in Fig. 4, the ambient temperature  $T_a$  has a direct influence on the hotspot temperature of the dc-link capacitor  $T_h$ . Thus, increasing the ambient temperature for the test is an effective way to accelerate the degradation process of the capacitor.

Normally, the ambient temperature profile varies to a certain extent during the day, as it is demonstrated in Fig. 14(a). However, the slow response of the thermal impedance of the dc-link due to the thermal capacitance limits the dynamics of thermal stress in real application. This has been demonstrated in Fig. 10 and also discussed in [36] that the fast variation

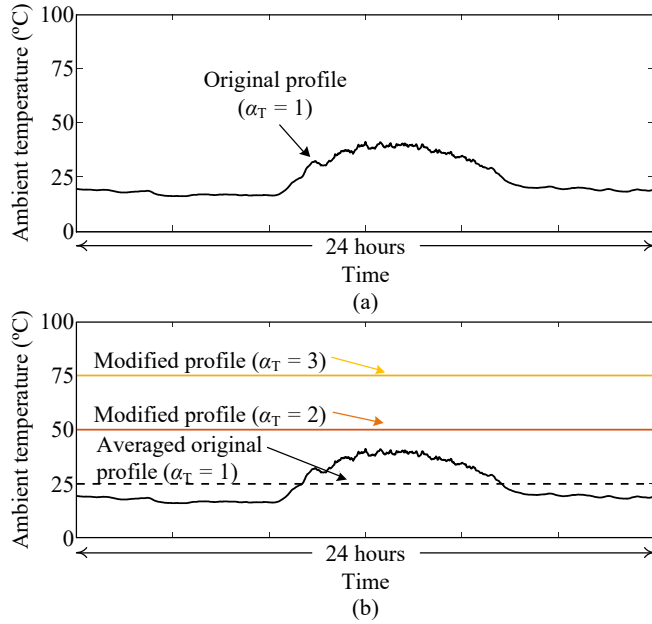


Fig. 14. Daily ambient temperature profile: (a) the original profile and (b) the modified profile with different temperature scaling factors  $\alpha_T$ .

in the ambient temperature does not have a direct impact on the dynamics of thermal stress in the dc-link capacitor. With this consideration, using a constant ambient temperature to simplify the test facility requirement (e.g., response time of the oven) is a reasonable assumption for the dc-link capacitor, as its degradation mechanism is related to the average value of the hotspot temperature [8]. The initial value of the ambient temperature can be obtained from the average value of the original profile, as it is shown in Fig. 14(b).

In order to reduce the testing time, an ambient temperature level should be elevated during the test in order to accelerate the degradation process of the capacitor [24]. A scaling factor for the ambient temperature during the test is defined as

$$\alpha_T = \frac{T_a^*}{T_a} \quad (8)$$

where  $T_a$  and  $T_a^*$  are the original averaged ambient temperature and the modified ambient temperature, respectively.

An example of the modified ambient temperature with different scaling factors  $\alpha_T$  is shown in Fig. 14(b), where the original averaged ambient temperature of 25 °C is elevated to 50 °C (i.e.,  $\alpha_T = 2$ ) and 75 °C (i.e.,  $\alpha_T = 3$ ). By elevating the ambient temperature during the test, the damage of the dc-link capacitor during the test can be increased significantly compared to the original mission profile. Notably, the de-rating strategy is not considered during the test, as it will counter-act the purpose of accelerated testing. This principle is applied to most of the accelerated testing methods (e.g., standard power cycling test) where the component under test should be stressed higher than the intended operating condition, in order to accelerate the degradation process and thereby reduce the testing time. However, the maximum temperature scaling factor is limited by the maximum operating temperature of the dc-link capacitor (and also the surrounding components).

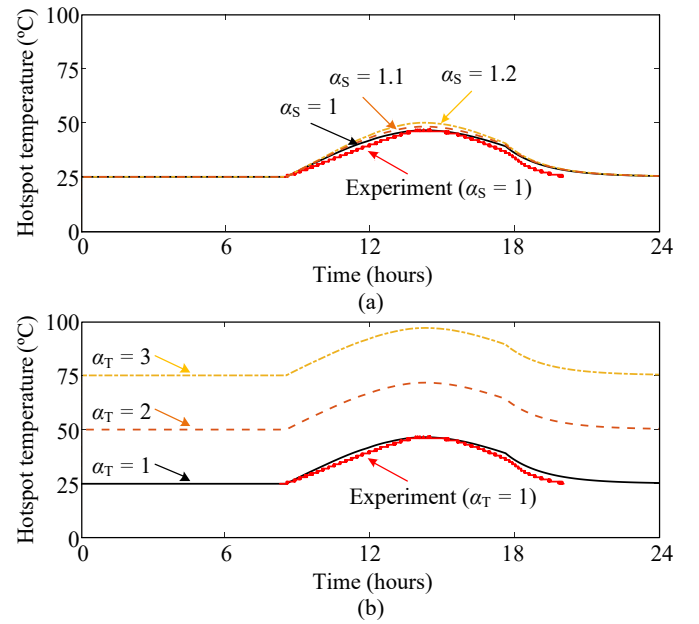


Fig. 15. Daily hotspot temperature of the dc-link capacitor with different: (a) amplitude scaling factors  $\alpha_S$  and (b) temperature scaling factors  $\alpha_T$ .

In this case, the maximum temperature limit of the dc-link capacitor is 105 °C [39]. Applying an ambient temperature higher than the maximum limit should be avoided, as it may trigger other failure mechanisms that are not related to the wear-out failure of the capacitor in real application and thereby introduce erroneous in the reliability evaluation.

## VI. DESIGN GUIDELINE

In this section, a guideline for designing a test profile according to the proposed mission profile-based accelerated testing is provided. The selection of scaling factor parameters for a certain required accumulated damage is discussed, where the original mission profiles in Figs. 13(a) and 14(a) are considered.

### A. Thermal Stress Analysis

The thermal stress of dc-link capacitor during the test is an indicator to demonstrate the effectiveness of the proposed testing method. According to the test requirements discussed in Section V, the thermal stress of the dc-link capacitor should be increased in a way to accelerate the capacitor degradation, while its dynamics should be maintained close to the real operation (e.g., the original mission profile).

The hotspot temperature of the dc-link capacitor under the original mission profile is shown in Fig. 15(a) (for the case of  $\alpha_T = 1$ ), where the result obtained from the simulation is closely aligned with the experiments (under similar operating conditions) and validating the thermal modeling. It can be seen from the same figure that the hotspot temperature of the dc-link capacitor reaches a higher peak value as the amplitude scaling factor increases to  $\alpha_S = 1.2$ , which is the maximum limit where the peak PV output power reaches the PV inverter rated power during midday. In this case, the modification of

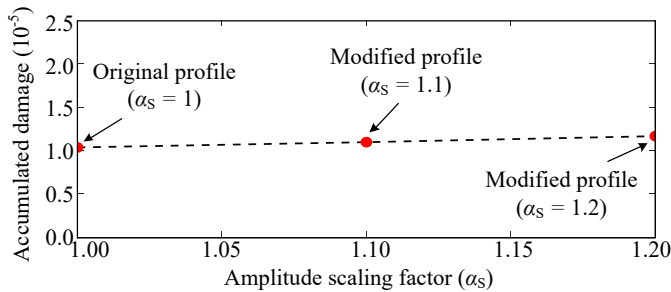


Fig. 16. Accumulated damage of capacitor under daily mission profile with different solar irradiance amplitude scaling factors (ambient temperature of  $T_a = 25^\circ\text{C}$ ).

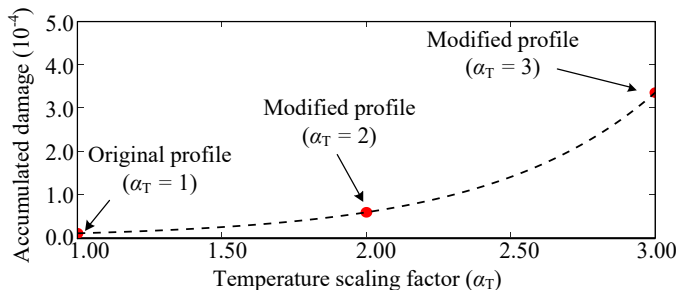


Fig. 17. Accumulated damage of capacitor under daily mission profile with different ambient temperature scaling factors (original solar irradiance profile).

the solar irradiance only affects the thermal stress of the dc-link capacitor during the day (e.g., from 8.00 to 18.00). On the other hand, the modification of the ambient temperature can effectively elevate the hotspot temperature of the dc-link capacitor during the entire testing period, as it can be seen in Fig. 15(b). In both cases, the dynamics of the hotspot temperature is similar to that in the original profile.

### B. Parameter Sensitivity Analysis

To quantify the impact of the mission profile acceleration on the damage of the dc-link capacitor, the sensitivity analysis of the two scaling factors is necessary. In this case, the accumulated damage of the dc-link capacitor under daily mission profile with different scaling factors (e.g.,  $\alpha_S$  and  $\alpha_T$ ) are evaluated and compared, since it is a reliability metric that indicates the time-to-failure of the capacitor during the test. More specifically, the required testing time is inversely proportional to the damage accumulated during the test. Therefore, the test condition with high accumulated damage indicates a shorter testing time.

The accumulated damage of the capacitor under different amplitude scaling factors  $\alpha_S$  is shown in Fig. 16, which is obtained by applying the thermal stress profile in Fig. 15(a) to the lifetime model and the damage model in (5) and (6), respectively. It can be seen from the results in Fig. 16 that the amplitude scaling factor has an insignificant impact on the accumulated damage of the capacitor. Thus, its effectiveness to increase the damage during the test is limited. In contrast, the accumulated damage of the capacitor increases significantly as the temperature scaling factor  $\alpha_T$  increases, as it is shown in

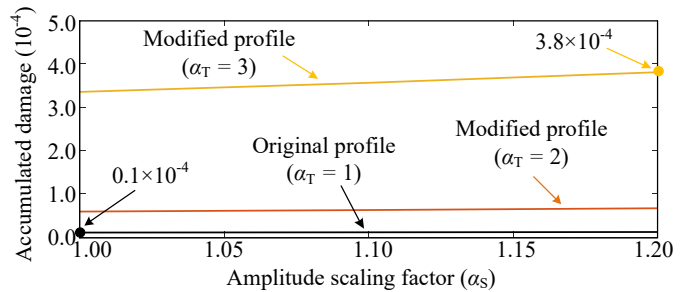


Fig. 18. Accumulated damage of capacitor under daily mission profile with different solar irradiance amplitude scaling factors  $\alpha_S$  and ambient temperature scaling factors  $\alpha_T$ .

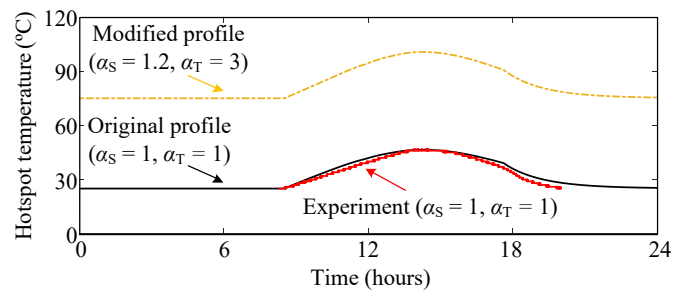


Fig. 19. Daily hotspot temperature of the dc-link capacitor with the amplitude scaling factors of  $\alpha_S = 1.2$  and temperature scaling factors of  $\alpha_T = 3$ .

Fig. 17. In fact, the increase in the accumulated damage follows an exponential function. Therefore, elevating an ambient temperature can effectively accelerate the reliability testing of the dc-link capacitor.

### C. Scaling Factor Design

In order to design the scaling factor for the test profile, the impact of both solar irradiance amplitude and temperature scaling factors need to be considered together. The accumulated damage of the dc-link capacitor when considering both solar irradiance and ambient temperature modifications are shown in Fig. 18. Similarly to the sensitivity analysis, the ambient temperature elevation is more effective than the solar irradiance amplitude modification in terms of accelerating the damage (and thereby reducing the testing time). Nevertheless, the impact of the solar irradiance amplitude scaling factor is more pronounced at the high ambient temperature, as it can be seen from the slope of the accumulated damage at different temperature scaling factors. Therefore, at the elevated ambient temperature condition, the impact of the modified solar irradiance should not be neglected.

The results in Fig. 18 can be used for designing the scaling factors based on the desired accumulated damage level. In general, the ratio between the accumulated damage of the modified and the original mission profiles indicates the acceleration factor in terms of the testing time. For instance, by applying the scaling factor of  $\alpha_S = 1.2$  and  $\alpha_T = 3$ , the dc-link capacitor is highly stressed during the test compared to the original mission profile, as it can be seen in Fig. 19. This test condition of the modified mission profile results in the accumulated damage of  $D = 3.8 \times 10^{-4}$ , while the accumulated

damage of the original mission profile is  $D = 0.1 \times 10^{-4}$ . Thus, applying the modified mission profile can induce an accumulated damage which is 38 times higher than the case of the original mission profile. This also means that the testing time will be much shorter compared to the time-to-failure in the real-field operation (while the mission profile dynamic are similar) to emulate the same degradation level. Notably, the stress condition during the test may be further increased (and thereby the testing time will be reduced) by applying a higher temperature scaling factor (since the maximum value of  $\alpha_S$  is 1.2) as long as it is within the maximum operating temperature of the capacitor (e.g., 105 °C) and also other components in the system. For a certain stress condition (e.g., damage), the combination of the scaling factors (e.g.,  $\alpha_S$  and  $\alpha_T$ ) can be selected following the results shown in Fig. 18.

## VII. CONCLUSIONS

In this paper, a method to design a testing profile based on the real mission profile seen in the field is proposed for the dc-link capacitor in PV inverters. In contrast to the conventional reliability testing method where a constant testing condition is usually applied, the proposed one realizes the testing conditions through the modification of the original mission profile in order to be more close to the real application. More specifically, the solar irradiance profile is modified by introducing an amplitude scaling factor while the ambient temperature is elevated for the test. This leads to an increase in the thermal stress (e.g., the hotspot temperature) of the dc-link capacitor, and thereby accelerating the degradation process. A design guideline for selecting the scaling factors is also provided based on the acceleration level of the damage and the mission profile dynamics. The proposed mission profile-based accelerated testing method can be used as part of the design verification, e.g., to verify if the expected lifetime can be met for a certain mission profile. This gives a possibility to bridge the gap between design for reliability and real-field experimental validation.

## REFERENCES

- [1] National Renewable Energy Laboratory, "On the path to sunshot: The role of advancements in solar photovoltaic efficiency, reliability, and costs," Tech. Rep. No. NREL/TP-6A20-65872, 2016.
- [2] G. Petrone, G. Spagnuolo, R. Teodorescu, M. Veerachary, and M. Vitelli, "Reliability issues in photovoltaic power processing systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2569–2580, Jul. 2008.
- [3] Solar Bankability, "Technical risks in PV projects. report on technical risks in PV project development and PV plant operation," 2016.
- [4] P. Hacke, S. Lokanath, P. Williams, A. Vasani, P. Sochor, G. Tamizhmani, H. Shinohara, and S. Kurtz, "A status review of photovoltaic power conversion equipment reliability, safety, and quality assurance protocols," *Renewable and Sustainable Energy Reviews*, vol. 82, no. 1, pp. 1097–1112, Feb. 2018.
- [5] L. M. Moore and H. N. Post, "Five years of operating experience at a large, utility-scale photovoltaic generating plant," *Progress Photovoltaics: Res. Appl.*, vol. 16, no. 3, pp. 249–259, 2008.
- [6] Enphase Energy, "Reliability study of electrolytic capacitors in a microinverter," Sep. 2008.
- [7] J. Flicker, R. Kaplar, M. Marinella, and J. Granata, "PV inverter performance and reliability: What is the role of the bus capacitor?" in *Proc. of PVSC*, pp. 1–3, Jun. 2012.
- [8] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters - an overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep. 2014.
- [9] Y. Yang, K. Ma, H. Wang, and F. Blaabjerg, "Mission profile translation to capacitor stresses in grid-connected photovoltaic systems," in *Proc. of ECCE*, pp. 5479–5486, Sep. 2014.
- [10] A. Sangwongwanich, Y. Shen, A. Chub, E. Liivik, D. Vinnikov, H. Wang, and F. Blaabjerg, "Reliability of dc-link capacitors in two-stage micro-inverters under different PV module sizes," in *Proc. of ICPE 2019 - ECCE Asia*, pp. 1867–1872, May 2019.
- [11] *Application guide, Aluminum Electrolytic Capacitors*, Cornell Dubilier, Liberty, SC, USA. [Online]. Available: <http://www.cde.com/catalogs/AEappGUIDE.pdf>
- [12] H. Wang, Y. Yang, and F. Blaabjerg, "Reliability-oriented design and analysis of input capacitors in single-phase transformer-less photovoltaic inverters," in *Proc. of APEC*, pp. 2929–2933, Mar. 2013.
- [13] A. Sangwongwanich, Y. Yang, D. Sera, F. Blaabjerg, and D. Zhou, "On the impacts of PV array sizing on the inverter reliability and lifetime," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3656–3667, Jul. 2018.
- [14] Y. Shen, A. Chub, H. Wang, D. Vinnikov, E. Liivik, and F. Blaabjerg, "Wear-out failure analysis of an impedance-source PV microinverter based on system-level electro-thermal modeling," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3914–3927, 2019.
- [15] J. M. Lenz, J. R. Pinheiro, and H. C. Sartori, "Dc-link electrolyte capacitor lifetime analysis for a PV boost converter," in *Proc. of PEDG*, pp. 1–6, Apr. 2017.
- [16] S. Gulbrandsen, J. Arnold, N. Kirsch, and G. Caswell, "A new method for testing electrolytic capacitors to compare life expectancy," *Additional Conferences (Device Packaging, HITEC, HiTEN, & CICMT)*, vol. 2014, no. DPC, pp. 001 759–001 786, 2014.
- [17] *Technical Note – Judicious use of Aluminum Electrolytic Capacitors*, Nippon Chemi-Con. [Online]. Available: <https://www.chemi-con.co.jp/e/catalog/pdf/al-e/al-sepa-e/001-guide/al-technote-e-2018.pdf>
- [18] G. J. Levenbach, "Accelerated life testing of capacitors," *IRE Trans. Reliab. Qual. Control*, vol. PGRQC-10, pp. 9–20, Jun. 1957.
- [19] A. Lahyani, P. Venet, G. Grellet, and P. Viverge, "Failure prediction of electrolytic capacitors during operation of a switchmode power supply," *IEEE Trans. on Power Electron.*, vol. 13, no. 6, pp. 1199–1207, 1998.
- [20] A. Dehbi, W. Wondrak, Y. Ousten, and Y. Danto, "High temperature reliability testing of aluminum and tantalum electrolytic capacitors," *Microelectron. Reliab.*, vol. 42, no. 6, pp. 835 – 840, 2002.
- [21] R. Shukla, M. W. Ahmad, N. Agarwal, and S. Anand, "Accelerated ageing of aluminum electrolytic capacitor," in *Proc. of 7th Nat. Power Electron. Conf.*, pp. 1–5, 2015.
- [22] D. Boby, M. W. Ahmad, N. Agarwal, and S. Anand, "Correlation of accelerated lifetime in punctured capacitor with normal operating lifetime," in *Proc. of CPE-POWERENG*, pp. 353–357, 2016.
- [23] C. S. Kulkarni, J. R. Celaya, K. Goebel, and G. Biswas, "Physics based electrolytic capacitor degradation models for prognostic studies under thermal overstress," in *Proc. of First European Conference of the Prognostics and Health Management Society*, 2012.
- [24] V. A. Sankaran, F. L. Rees, and C. S. Avant, "Electrolytic capacitor life testing and prediction," in *Proc. of 32nd IEEE IAS Annu. Meeting*, vol. 2, pp. 1058–1065, Oct. 1997.
- [25] K. Zhao, P. Ciufo, and S. Perera, "Lifetime analysis of aluminum electrolytic capacitor subject to voltage fluctuations," in *Proc. of ICHQP 2010*, pp. 1–5, 2010.
- [26] Y. Ko, H. Jedtberg, G. Buticchi, and M. Liserre, "Topology and control strategy for accelerated lifetime test setup of dc-link capacitor of wind turbine converter," in *Proc. of APEC*, pp. 3629–3636, 2016.
- [27] J. R. Celaya, C. S. Kulkarni, S. Saha, G. Biswas, and K. Goebel, "Accelerated aging in electrolytic capacitors for prognostics," in *Proc. of Annu. Rel. Maintainability Symp.*, pp. 1–6, 2012.
- [28] C. S. Kulkarni, J. R. Celaya, G. Biswas, and K. Goebel, "Accelerated aging experiments for capacitor health monitoring and prognostics," in *Proc. of IEEE AUTOTESTCON*, pp. 356–361, 2012.
- [29] C. S. Kulkarni, G. Biswas, X. Koutsoukos, J. Celaya, and K. Goebel, "Integrated diagnostic/prognostic experimental setup for capacitor degradation and health monitoring," in *Proc. of IEEE AUTOTESTCON*, pp. 1–7, 2010.
- [30] R. Jánó and D. Pitică, "Accelerated ageing tests for predicting capacitor lifetimes," in *Proc. of SIITME*, pp. 63–68, 2011.
- [31] J. Flicker, G. Tamizhmani, M. K. Moorthy, R. Thiagarajan, and R. Ayyanar, "Accelerated testing of module-level power electronics for long-term reliability," *IEEE J. of Photovolt.*, vol. 7, no. 1, pp. 259–267, Jan. 2017.
- [32] M. Dbeiss, Y. Avenas, H. Zara, and L. Dupont, "A method for accelerated ageing tests of photovoltaic inverters considering the application's mission profiles," in *Proc. of EPE*, pp. 1–10, Sep. 2017.

- [33] A. Sangwongwanich, Y. Shen, A. Chub, E. Liivik, D. Vinnikov, H. Wang, and F. Blaabjerg, "Mission profile-based accelerated testing of dc-link capacitors in photovoltaic inverters," in *Proc. of APEC*, pp. 2833–2840, Mar. 2019.
- [34] S.B. Kjaer, J.K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep. 2005.
- [35] Z. Sarkany, G. Farkas, and M. Rencz, "Thermal characterization of capacitors," in *Proc. of ICEP*, pp. 200–203, Apr. 2016.
- [36] H. Wang, R. Zhu, H. Wang, M. Liserre, and F. Blaabjerg, "A thermal modeling method considering ambient temperature dynamics," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 6–9, Jan. 2020.
- [37] S. G. Parler, "Deriving life multipliers for electrolytic capacitors," *IEEE Power Electron. Soc. Newsl.*, vol. 16, no. 1, pp. 11–12, Feb. 2004.
- [38] A. Albertsen, "Electrolytic capacitor lifetime estimation," 2017. [Online]. Available: <https://www.jianghai-america.com/>.
- [39] Nippon Chemi-con, "Large capacitance aluminum electrolytic capacitors, downsized snap-ins, 105°C KHS series," 2020. [Online]. Available: <http://www.chemi-con.co.jp/e/catalog/pdf/al-e/al-sepa-e/005-snapin/al-khslug-e-2020.pdf>.
- [40] M. Miner, "Cumulative damage in fatigue," *J. Appl. Mech.*, vol. 12, pp. 159–164, May 1945.
- [41] S. G. Parler, "Thermal modeling of aluminum electrolytic capacitors," in *Proc. of Thirty-Forth IAS Annual Meeting*, vol. 4, pp. 2418–2429 vol.4, 1999.
- [42] Z. Na, "A study of electrolytic capacitor's thermal conductivity, behavior and measurement," in *Proc. of THERMINIC*, pp. 315–318, 2016.
- [43] P. Freiburger, "Transient thermal modeling of aluminum electrolytic capacitors under varying mounting boundary conditions," in *Proc. of THERMINIC*, pp. 1–5, 2015.
- [44] *PV outdoor test and monitoring platform*, Aalborg University. [Online]. Available: <https://www.et.aau.dk/laboratories/renewable-energy-conversion-storage/PV+outdoor+test+and+monitoring+platform/>.



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