# Design Methodologies for Soft Switched Inverters

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***Abstract*—This paper presents a detailed design methodology for soft-switched inverters. The actively clamped resonant dc link and the resonant pole inverters are taken as illustrative design examples with detailed enumeration of component design rules, switching loss calculations, and system optimization. The soft-switched circuits are then compared with a conventional hard switched voltage source inverter under identical operating conditions.**

## I. Introduction

THE CONCEPT OF soft switching in high-power inverter circuits is attracting a lot of attention as shown by recent literature [1]–[5]. A soft switching converter is characterized by intrinsic modes of operation that allow an automatic and lossless resetting of the snubber elements by appropriate recirculation of the trapped energy. Reactive elements in these circuits principally shape the device switching loci and play only a minor role in the power transfer process. These circuits hold the promise of substantially higher switching frequencies with minimum penalties in terms of rating and cost.

The resonant dc link inverter (RDCLI) and the quasiresonant current mode or resonant pole inverter (RPI) are two examples of such soft-switched inverters [5]. These circuits have already been shown to be viable with BJT's and GTO's at up to the 40-kW level with strong potential for reaching power levels greater than 200 kW. However, much confusion still persists regarding the operation, control, efficiency, and performance characteristics of such converters. This paper attempts to specify in detail, a methodology for the design and control of such converters for maximizing performance, with particular emphasis on the RDCLI and RPI. Because one of the major aims is the realization of low-loss switching, efficiencies of the converters are compared with those of comparably rated hard switched voltage source inverters. Equations are developed for analytically estimating system losses and for guiding the choice of circuit components. The various tradeoffs inherent in the design process are detailed, and the impact of modulation strategy is discussed. It is hoped that this paper will establish the framework for evaluating and comparing various soft-switched inverter topologies.

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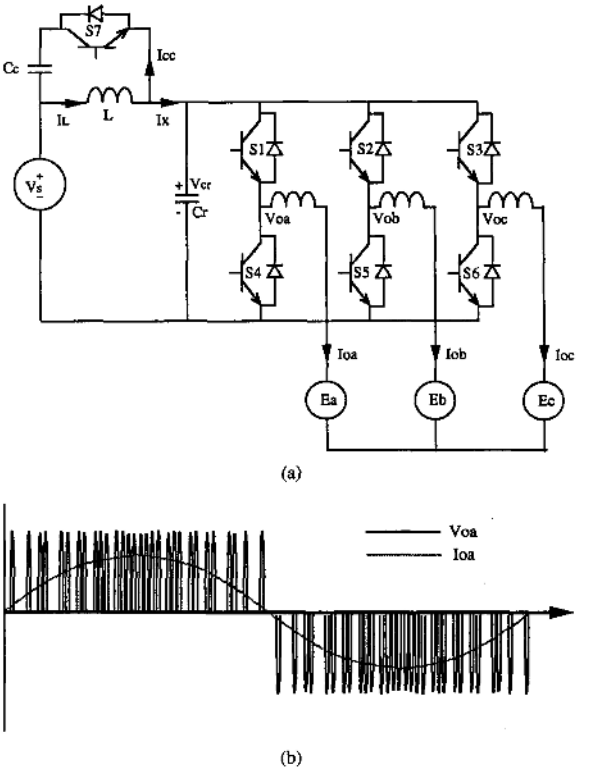


Fig. 1. (a) Circuit schematic of an actively clamped resonant dc link inverter; (b) typical output voltage and output current waveforms.

## II. Soft Switching Inverter Control Issues

A circuit schematic of the actively clamped resonant dc link inverter is shown in Fig. 1 as the preferred topology [5]. The circuit operates by setting up a resonating dc link that periodically returns the dc bus voltage to 0 V. During the interval that the diodes in antiparallel with the main inverter devices are conducting, all inverter devices may be turned off, if desired, with minimal turn-off losses. At the same time, all incoming devices may be turned on with zero turn-on losses. The concept was introduced in [1] and was developed in [5] to include the active clamp. The use of a seventh device $S_7$ restricts voltage stresses to less than twice the dc supply voltage and increases the applications potential of the circuit.

The introduction of the active clamp has a dramatic impact on the way the inverter can be controlled. It is clear that the clamp should be lossless and should not need a continuous

power feed from an auxiliary supply. One possible control approach was detailed in [5]. In a manner similar to the unclamped RDCL inverter, the resonating bus is held shorted for sufficient time to ensure that at least the minimum required energy is pumped into the clamp capacitor $C_c$. Turnoff of the clamp device $S_7$ in turn regulates the energy drawn from the clamp capacitor over a cycle. Consequently, by controlling the turnoff of $S_7$, it is possible to maintain zero average power flow into $C_c$ and the regulate the clamping voltage at a preset desired value.

The problem with this scheme is that the resonating bus needs to be shorted every resonant cycle by a turnoff of all inverter devices or, alternatively, by an additional device in parallel. This, of course, has to be followed by turnoff of three of the main devices. The higher switching rates implies higher gate drive losses. Of even more importance is the storage time of the device. The finite, and often large, storage time results in bus shorting durations that are longer than desired and substantially reduce the maximum frequency of possible operation.

An alternate means of control is possible and is described below. The major problem with the above scheme is the required turnon of all inverter devices to ensure a precharge of the energy to be dissipated in the subsequent resonant cycle. With clamping voltage levels of 1.3–1.8 $V_s$, it is clear that the $LC$ resonant circuit can reach the clamping voltage even with zero initial current. The critical resonant transition occurs when the clamp device is turned off. As shown in [5], the minimum current in the inductor $I_{LM}$ at that instant needs to be

$$I_{LM} = I_x - \frac{V_s}{Z_o}\sqrt{K(2-K)} \tag{1}$$

where $I_x$ is the dc link current during that resonant cycle, $V_s$ is the supply voltage, $Z_o = (L/C_R)^{1/2}$, and $KV_s$ is the clamping voltage. Maintaining inductor trip current $i_L = I_T > I_{LM}$ ensures that the resonant bus shorting interval is not very critical and does not need to be controlled.

The presence of modulation in the inverter section causes the current $I_x$ to change by large quantum jumps on a resonant cycle-to-cycle basis. For example, if inverter switches $S_1S_2S_6$ in Fig. 1(a) are conducting with a resulting $I_{xo}$ in the link, turning them off and turning on $S_3S_4S_5$ in the next cycle forces $I_x = -I_{xo}$. At the instant just before switching, $i_L = I_x$. Consequently, $2I_x$ flows into the capacitor $C_R$ for the next resonant cycle and pumps substantial energy into the clamp capacitor $C_C$. On the other hand, if the transition has been from $-I_{xo}$ to $I_{xo}$, the bus would have remained shorted, allowing $i_L$ to build up to $I_{xo}$ before the resonant cycle would start. The net initial current into $C_R$ would then be zero, and insufficient energy would be transferred to $C_c$. However, if $C_c$ is large enough, then energy balance over a few cycles would be possible, and the trip current $I_T$ could be regulated through a $PI$ loop to effect energy balance and clamp voltage regulation. Fig. 2 shows waveforms depicting the two modes of operation.

Consequently, under modulation conditions, the clamp can be self sustaining and does not need an auxiliary supply except for precharging prior to startup. If operation under zero load current conditions is anticipated, then the auxiliary supply needs to be sized to handle resonant circuit losses. With this control strategy, the main inverter devices do not need to be turned on during the bus shorting interval. This results in a simpler, decoupled control strategy, where link control is accomplished via control of the clamp device $S_7$, and modulation control is from the main inverter devices $S_1$–$S_6$. A block schematic of the new controller is shown in Fig. 3. This also yields a 30% increase in the attainable link switching frequency.

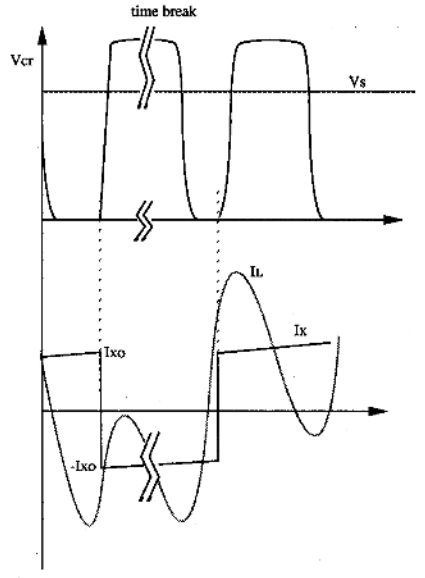


Fig. 2. Link waveforms of the RDCL inverter in the two modes of operation.

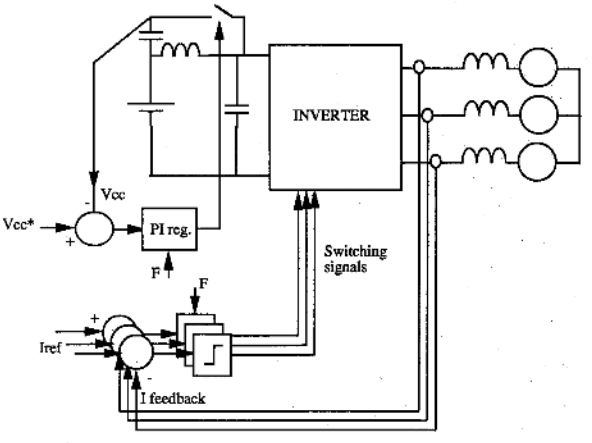


Fig. 3. Block schematic of controller for RDCL inverter.

Another inverter control issue concerns the modulation strategy. Given the discrete pulse modulation (DPM) on the inverter output, a new class of modulator is required. The sigma delta modulator ($\Sigma\Delta$M) [1], [2], [6] and the current regulated delta modulator (CR$\Delta$M) [7] are good examples of effective control strategies. More recently, it has also been shown that real-time optimal discrete pulse modulation

strategies are relatively easy to implement [4], [8]. In a manner similar to hard switching PWM systems, it has been shown that line-line switching functions that avoid $\pm 1$ to $\mp 1$ transitions demonstrate improved performance. This has a major impact on the operation of the resonant link itself. The sizing of the $LC$ components is done dependent on the device switching losses, which are a function of the maximum reapplied $dv/dt$ at the start of the resonant cycle, which in turn is dependent on the maximum current in $C_R$. Looking at the waveforms in Fig. 2, it can be seen that eliminating $\pm 1$ to $\mp 1$ transitions by switching $S_1S_2S_3$ on in the next cycle would reduce the peak current in $C_R$ from $2I_x$ to $I_x$, which is a 50% reduction in $dv/dt$ and in device switching losses. Consequently, it is desirable to adopt modulation strategies that do not allow such transitions.

The resonant dc link inverter behaves almost exactly like a hard-switched PWM inverter operated off the same supply voltage $V_s$. It is characterized by the same output-voltage-to-supply-voltage ratio. It generates a voltage source output and is ideally suited for drives applications where load inductance provides sufficient filtering. For UPS-type applications, where an $LC$ filter needs to be used, it is possible that the resonant pole inverter (RPI) would also be a suitable candidate [5]. A circuit schematic and waveforms are shown in Fig. 4. The RPI works on the principle that soft switching implies device turn-on with the antiparallel diode conducting. Consequently, whenever a diode (say $D_1$ from Fig. 4(a)) conducts, the current in $L_1$ ramps up until the device $T_1$ is forced into conduction. At this point, the device can be turned off, forcing the current to commutate to the diode $D_2$. Provided sufficient current exists in $L_1$, it resonates with $C_R$ and forces the bus voltage transition. With $D_2$ conducting, $T_2$ can be turned on with no turn-on losses. The process can now be repeated. The use of purely capacitive lossless snubbers implies that oversized snubbers can be used to get substantially higher switching frequencies. Control of the RPI is fairly simple and has been discussed in [5].

Of vital importance to all soft switched inverters is the design of the $LC$ components and an appreciation of all the tradeoffs involved in the design process. Of primary importance is the issue of higher switching frequencies, which is a factor that is completely limited by device characteristics and system losses. These aspects are considered next.

## III. Device Losses Under Soft Switching

Inverter design commences with the selection of devices. Given the device switching characteristics, the $L$ and $C$ elements can then be chosen to minimize the sum of conduction and switching losses in the devices as well as losses occuring in the ESR of the reactive components. Further, device specifications directly translate into a switching frequency limit that can be achieved, giving an indication of the possible spectral performance. The strong interactions between various parameters makes the analysis fairly complex and often counterintuitive. It is important that these interactions be properly understood if a design methodology is to be formulated.

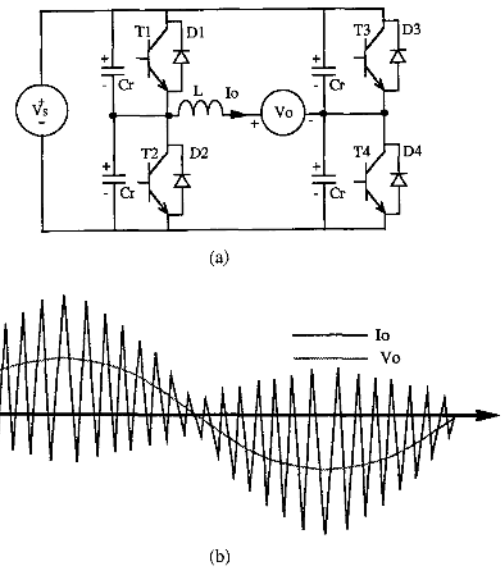


Fig. 4. (a) Circuit schematic of a single-phase resonant pole inverter; (b) typical output voltage and output current waveforms.

This paper will assume that BJT darlington transistors are the device of choice, although similar procedures could be applied to any gate turn-off device. Device behavior under soft switching conditions needs to be understood and has been characterized in [9]. The important differences compared with hard switching are the elimination of RBSOA constraints permitting higher reverse-base currents and smaller storage time. It was also found that no dynamic saturation exists at device turn-on with the diode conducting. The higher peak voltage and current stresses resulting from diode recovery are also no longer relevant.

Consequently, for the purposes of soft switching, only the turn-off switching losses need to be calculated differently. Turn-on losses are zero, whereas conduction losses correspond to the dc current curve [9]. In order to maximize the benefits of soft switching, $C_R$ is chosen to operate in the oversnubbed mode. This implies that the device current reaches zero before the voltage across the device has reached its clamping level. Fig. 5 shows typical switching waveforms for a soft-switched device, including capacitive snubber.

It is assumed that the resonant inductor current does not change appreciably during device current turnoff. The device current $i_D$ can be approximated to

$$i_D = I_p\left(1 - \frac{t}{t_f}\right). \tag{2}$$

The capacitor current $i_C$ and capacitor voltage $V_C$ then become

$$i_C = I_p\frac{t}{t_f} \tag{3}$$

$$V_C = \frac{I_p t^2}{2C_R t_f}. \tag{4}$$

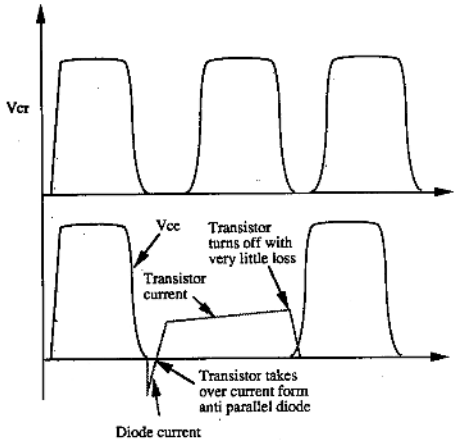


Fig. 5. Typical device voltage and current waveforms in RDCL converter.

Dissipation in the device can thus be found

$$P_d = V_C i_D = \frac{I_p^2}{2C_R t_f} t^2 \left(1 - \frac{t}{t_f}\right). \tag{5}$$

The instantaneous device dissipation has a maximum of $P_{dm}$ at $t = 2t_f/3$

$$P_{dm} = \frac{2I_p^2 t_f}{27C_R}. \tag{6}$$

The turn-off switching locus for various values of $C_R$ is shown in Fig. 6. Given an oversnubbed case, the average device switching losses can then be calculated for an average switching frequency $f$ to be

$$P_{sw} = \frac{I_p^2 t_f^2}{24C_R} f. \tag{7}$$

Under typical operating conditions, the expressions for $P_{sw}$ and $P_{dm}$ are accurate to within a few percentage points of values calculated from exact analytical expressions. That is considered sufficiently accurate for the application.

## IV. Losses in the RDCL Inverter

The motivation for the use of soft-switched inverters stems from a desire to increase the switching frequency to realize higher performance and power density. It is clear that the choice of link frequency and $LC$ component values will ultimately be dependent on the device characteristics itself. The complex tradeoffs involved often make the process counterintuitive at first glance. However, in an effort to develop a methodology for the design of soft-switched inverters, an analytical estimate is developed for losses in the RDCL inverter.

The circuit considered is a single-phase H-bridge inverter with an active clamp device as shown in Fig. 7. The supply voltage is $V_s$, and the clamp voltage is $KV_s$. The load is

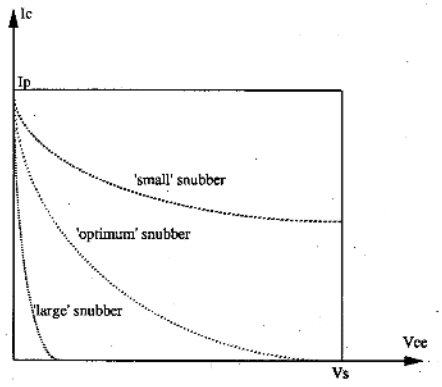


Fig. 6. Device turn-off switching loci for various $Cr$.

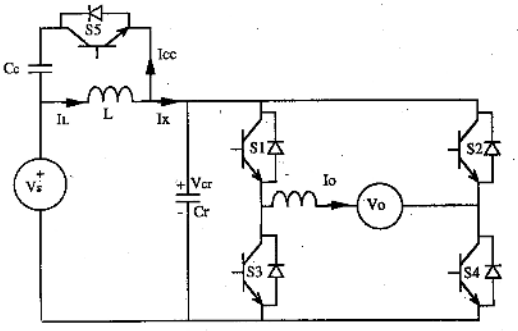


Fig. 7. Circuit schematic of the single-phase resonant dc link inverter.

modeled by a sinusoidal current source and the output voltage is modulated with a strategy that avoids $b + 1$ transitions in the line-line switching function. The ESR associated with the reactive components is predominantly in $L$. The resonant capacitor $C_R$ is represented as a lumped element. All devices are assumed to have a constant forward voltage drop of $V_D$ and a current fall time of $t_f$. Device storage time is neglected in the loss calculations.

For the ideal RDCL inverter with lossless $LC$ elements and devices, the minimum value of trip current $I_T = I_{LM}$ is adequate to keep the link functioning. This corresponds to the case when shorting time for the resonant bus approaches zero. Under these conditions, for a clamping level $KV_s$, the link switching frequency can be found to be [5]

$$f_L = \frac{1}{T_T} = \frac{1}{2\sqrt{LC_R}\left[\cos^{-1}(1-K) + \dfrac{\sqrt{K(2-K)}}{K-1}\right]} = \frac{K_1}{\sqrt{LC_R}}. \tag{8a}$$

For a typical value of $K = 1.5$, the following corresponds to zero excitation:

$$T_T = 7.652\sqrt{LC_R}. \tag{8b}$$

Total system losses are make up of conduction and switching losses in the five devices and losses in the inductor ESR. These are individually calculated below.

### A. Main Device Conduction Loss ($P_{CM}$)

The conduction losses in $S_1$–$S_4$ are almost independent of $L$ and $C$ and are governed by the load current $i_o = I_o \sin \omega t$. As the load current always flows in two devices, we have

$$P_{CM} = \frac{4}{\pi} V_D I_D = K_2. \tag{9}$$

### B. Main Device Switching Loss ($P_{SM}$)

Main device switching losses depend primarily on $C_R$ and indirectly on $L$. Switching losses occur whenever the bus voltage is rising at the time the device is being turned off. This corresponds to the case where $i_L > I_x$ immediately after switching, and minimum time is spent with the bus shorted. For the case where $i_L < I_x$, the bus automatically remains shorted until $i_L = I_x$, and the clamp on the bus voltage resulting from the main diodes is released. Under these conditions, device turn-off has already been accomplished with the diodes conducting, i.e., no switching losses. Consequently, assuming that the worst-case current $I_o$ is turned off in half of the switching cycles, we can estimate the main device switching losses to be

$$P_{SM} = \frac{1}{2} \frac{I_o^2 t_f^2}{24 C_R} \frac{K_1}{\sqrt{LC_R}} = \frac{K_3}{\sqrt{LC^{3/2}}}. \tag{10}$$

### C. Clamp Device Conduction Loss ($P_{CC}$)

The current in the clamp device has a profile given in Fig. 8. Assuming charge balance energy cycle, the peak currents in the diode and device are equal and have peak magnitudes of $I_{CM}$

$$I_{CM} = (I_{L2} - I_x) = \pm \frac{V_s}{Z_o} \sqrt{K(2-K)}. \tag{11}$$

The current flows first through the diode and then through the device. Assuming equal voltage drops of $V_D$ across each, we can calculate the average clamp conduction loss by finding the average current through the diode and device, respectively. The shaded area in Fig. 8 represents the current through the diode and corresponds to a net charge transferred to clamp capacitor of $q_{cl}$, where

$$q_{cl} = \frac{1}{2} \sqrt{LC_R} \frac{\sqrt{K(2-K)}}{(K-1)} V_s \sqrt{\frac{C_R}{L}} \sqrt{K(2-K)} \tag{12a}$$

$$\therefore\ q_{cl} = V_s C_R \frac{K(2-K)}{2(K-1)}. \tag{12b}$$

The average current is then found by dividing $q_{cl}$ by $T_T$. Now, the total conduction losses in the clamp can be found to be

$$P_{CC} = V_D V_s \sqrt{\frac{C_R}{L}} * \frac{K(2-K)K_1}{(K-1)} \cong K_4 \sqrt{\frac{C_R}{L}}. \tag{13}$$

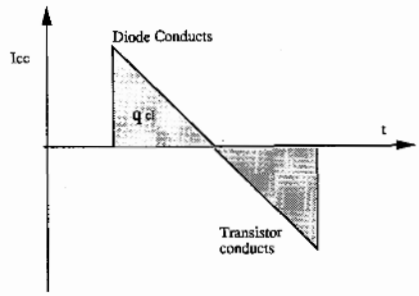


Fig. 8. Typical waveform in the clamp capacitor.

### D. Clamp Device Switching Losses ($P_{SC}$)

The peak current being turned off in the clamp device depends on the control strategy being implemented. The actual current at turn off is $-I_{CM}$ from (11). In actual practice, the current at turnoff may be selected to be higher, corresponding to an overexcited case for the resonant link. To turn-off current $I_{CM}$, the average switching loss incurred can be found from (7) to be

$$P_{SC} = V_s^2 \frac{K(2-K)t_f^2}{24L} \frac{K_1}{\sqrt{LC_R}} \tag{14a}$$

$$\therefore\ P_{SC} = \frac{K_5}{L^{3/2}\sqrt{C_R}}. \tag{14b}$$

### E. ESR Losses ($P_L$)

The loss in the ESR elements is predominantly in the inductor and has two identifiable components: the dc load current and the ac circulating current. Under worst-case conditions, corresponding to a unity $pf$ load with square wave output voltage, the dc current is a rectified sinusoid with a peak of $I_o$, whereas the circulating current is $V_s/Z_o$. This loss is most difficult to estimate with accuracy as it is dependent on the modulation strategy, which cannot be factored in except in numerical computation. Under these assumptions, $P_L$ can be calculated to be

$$P_L = \frac{I_o^2}{2Q} \sqrt{\frac{L}{C_R}} + \frac{V_s^2}{2Q} \sqrt{\frac{C_R}{L}} \tag{15a}$$

$$\therefore\ P_L = K_6 \sqrt{\frac{L}{C_R}} + K_7 \sqrt{\frac{C_R}{L}} \tag{15b}$$

where $Q$ is the quality factor of the resonant tank. $Q$ factors of 200 are easily attained in the laboratory.

### F. Total System Losses ($P_T$)

The total RDCL system losses can now be calculated by summing the various components

$$P_T = K_2 + \frac{K_3}{\sqrt{LC_R}} + K_4 \sqrt{\frac{C_R}{L}} + \frac{K_5}{L^{3/2}\sqrt{C_R}} + K_6 \sqrt{\frac{L}{C_R}} + K_7 \sqrt{\frac{C_R}{L}}. \tag{16}$$

The expression confirms our original suspicion that system optimization involves a wide variety of tradcoffs. Equation (16) relates the link frequency and losses to *real* system parameters such as the clamping level $K$, device current fall time $t_f$, $V_D$, $V_s$, and $Q$. Factors such as storage time and modulation are difficult to handle analytically and require numerical methods. It is interesting to observe the following trends in the individual loss components:

$P_{CM}$ independent of $L$ and $C_R$ $P_{CC}$ increases with circulating current $P_{SM}$, $P_{SC}$ decreases with increasing $C_R$ and increases with link frequency $P_L$ insensitive to link frequency, given $Q$.

### G. Selection of L and $C_R$

Given (16), the next step is the selection of best values of $L$ and $C_R$. Examining the expression for $P_T$, it can be seen that the absolute minimum occurs as the $LC_R$ product becomes infinite. A more reasonable optimization strategy would thus find optimal values of $L$ and $C_R$ at a specified link frequency (given by (8a)). Thus, using (8a) as a constraint, (16) is differentiated to find and extremum point. Thus, rewriting (8a)

$$\sqrt{C_R} = \frac{K_1}{f\sqrt{L}} \tag{17}$$

$$P_T = \left(\frac{K_4K_1}{f} + \frac{K_5 f}{K_1} + \frac{K_7K_1}{f}\right)\frac{1}{L} + \left(\frac{K_6 f}{K_1} + \frac{K_3 f^3}{K_1^3}.\right)L + K_2. \tag{18}$$

Differentiating with respect to $L$ and equating to zero, we can find the values of inductance $L_M$ and capacitance $C_{RM}$, which gives the lowest losses at a specified link frequency.

$$L_M = \left(\frac{K_4K_1^4 + K_5K_1^2f^2 + K_7K_1^4}{K_3f^4 + K_6K_1^2f^2}\right)^{1/2} \tag{19}$$

$$C_{RM} = \frac{K_1^2}{f^2L_M}. \tag{20}$$

The minimum power loss $P_{TM}$ can then be found by reevaluating (16). The accuracy of these estimated values is compared with detailed simulation results later in the paper. A complete comparison of soft switched inverters requires similar development for the RPI, which is attempted next.

## V. System Optimization for the RPI

Examining the single phase RPI shown in Fig. 4a, it can be seen that device turnoff needs to be done with sufficient current in $L$ to ensure that the voltage resonates to the other bus. This turns on the diode and allows a lossless turnon of the incoming device. The value of the minimum inductor current $I_M$ required for zero voltage turnon is [5].

$$I_M = \pm\frac{2\sqrt{V_sV_o}}{Z_o} \tag{21}$$

where $Z_o = \sqrt{L}/C_R$. In the presence of a modulation strategy, where $I_r$ is the output current to be synthesized, the positive and negative peak values of inductor current $I_p$ and $-I_M$ for positive $I_r$ are

$$I_p = 2I_r + I_M. \tag{22}$$

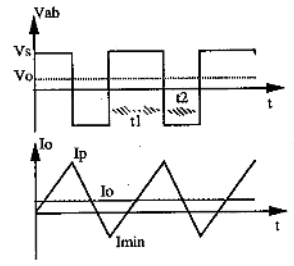


Fig. 9. Expanded idealized pole voltage and current waveforms in RPI.

For negative $I_r$, the values are $Im$ and $-I_p$, where assuming that the output voltage $V_o$ varies slowly as compared with the pole switching frequency and that bus voltage transitions occur very fast compared to the period of the traingular wave $T_T$, $T_T$ can be found to be

$$T_T = \frac{1}{f} = 4V_s\left(\frac{I_rL + 2\sqrt{V_sV_o}\sqrt{LC_R}}{V_s^2 - V_o^2}\right). \tag{23}$$

It can be seen that $T_T$ depends on $V_o$, $V_s$, $I_r$, and $C_R$. Consequently, the switching frequency varies dynamically during a cycle and maximum at no load with zero output voltage and is minimum at full load and maximum output voltage. With low-frequency ac modulation, the system behaves similarly to a PWM system and generates harmonics close to the switching frequency defined by (23) under rated conditions. Fig. 9 shows the envelope of the inductor current waveform showing the lower and upper boundaries. For similar switching frequencies, the RPI possesses vastly superior spectral characteristics as compared with the RDCL inverter.

Optimization of the RPI is even more complex than for the RDCLI. The task can be simplified by choosing $L$ and $C_R$ based on efficiency constraints and the filter capacitor $C_f$ based on harmonic specifications. In a manner similar to the RDCLI, the energy loss terms can be developed for the devices and the inductor ESR. Assuming a forward voltage drop in the devices of $V_D$, the main device conduction losses $P_{CM}$ and switching losses $P_{SM}$ can be calculated to be

$$P_{CM} = \frac{V_DV_sf}{(V_s^2 - V_o^2)}\left[LI_p^2 + 4C_RV_sV_o + 4\sqrt{LC_RV_sV_o}I_p\right] + \frac{V_DI_pf}{V_s + V_o}\left[LI_p + 2\sqrt{V_sV_oLC_R}\right] \tag{24}$$

$$P_{SM} = \frac{ft_f^2}{24}\left[\frac{I_p^2}{C_R} + \frac{4V_sV_o}{L}\right]. \tag{25}$$

By substituting the expression for $C_R$ obtained from (23), on can rewrite (24) and (25) in terms of $L$ only, as in (18). This would then permit the calculation of an analytical estimate of the inductance $L_M$, which gives the minimum device loss point. The expression for $L_M$ is fairly complex and it is difficult to obtain a closed-form solution.

The remaining loss component is in the inductor ESR. This is found by finding the r.m.s. current in the inductor and calculating the $I^2R$ loss $P_R$ at the rated operating point.

$$P_R = \frac{2}{3} f R_1 V_s L \frac{(I_p + I_M)^3}{V_s^2 - V_o^2} - f R_1 L \frac{I_p I_M (I_p + I_M)}{V_s + V_o} \tag{26}$$

where $R_1$ is the ESR of the inductance. Summing the three loss components than gives the total system loss. The optimization can be done either for minimum overall loss or minimum device loss.

The above procedure is similar to that for the RDCLI and allows calculation of the $L$ and $C_R$ components in the RPI. The output of the inverter is the filter capacitor voltage, and the total harmonic distortion constraint on the output would determine choice of $C_f$. In order to choose $C_f$, let us examine the neutral voltage as seen in Fig. 4(b). Assuming a large frequency differential between the switching and output frequencies, we can approximate the pole output voltage by a duty cycle modulated waveform as shown in Fig. 9. The dominant frequency component in the pole voltage that is to be filtered is at the switching frequency $f$ given by (23). This fundamental component amplitude is

$$a_1 = \frac{4V_s}{\pi} \sqrt{\frac{1 - \cos \pi(1-d)}{2}} \tag{27}$$

where $d = V_o/V_s$. Assuming 40-dB/decade attenuation with the $LC_f$ combination, this gets attenuated to an output voltage ripple

$$\Delta V_r = \frac{a_1}{(2\pi f)^2 L C_f}. \tag{28}$$

The total harmonic distortion (THD) may than be approximated by

$$\text{THD} = \frac{\Delta V_r}{V_o} \cong \frac{1}{d\pi^3 f^2 L C_f} \sqrt{\frac{1 - \cos \pi(1+d)}{2}}. \tag{29}$$

Consequently, given THD, $L$, $f$, and $d$, the required value of $C_f$ can be found. It can be seen that higher switching frequencies require smaller values of $L$, giving larger values of $C_f$. For very large $C_f$, the reactive current consumed by $C_f$ may become excessive at the desired output frequency $f_s$, requiring derating of the inverter. This implies that the RPI has minimum frequency ratio $\rho = f/f_s$. A typical value for $\rho$ is 60–65.

## VI. Comparison of Soft-Switched Converters

In order to evaluate the validity of the proposed design methodologies, a detailed comparison was undertaken for a single-phase $H$-bridge inverter rated at 10 kW. The inverters compared included the RDCLI, the RPI, and the hard-switched PWM voltage source inverter (HSI). All inverters were operated off a supply voltage of 300 V and delivered output power at 60 Hz to a unity power factor load. For the RDCLI and the HSI, the output was assumed to be a sinusoidal current source with peak amplitude of 100 A. The inverters were modulated using a modified $\Sigma\Delta$ M [8] and sine-triangle PWM, respectively to generate 200 V peak fundamental output voltage. The RPI was assumed to have a voltage source load, and the current in the output was controlled to satisfy identical load conditions. Fig. 10 shows circuit schematics and waveforms for each type of converter.

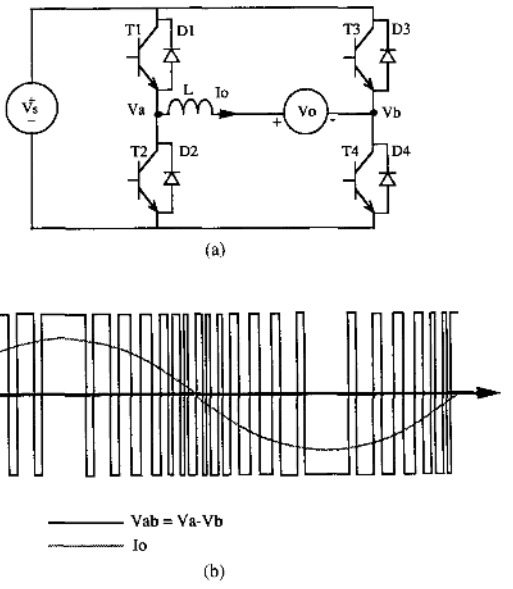


Fig. 10. (a) Circuit schematic of a single-phase hard switched PWM inverter; (b) typical output voltage and output current waveforms.

The devices used in the simulation were assumed to be BJT darlingtons with $V_D = 1.8$ V and $t_f = 2$ $\mu$ s. The RDCLI was assumed to clamp at 450 V ($K = 1.5$). Diodes used in the HSI simulation were assumed to have a reverse recovery time of 500 ns. All inductors were assumed to have a $Q = 200$. The operation of each inverter was simulated using the advanced continuous simulation language (ACSL) on an Apollo workstation. Each run involved detailed computation of component losses over an entire 60-Hz cycle. For the RDCLI, the modulation strategy avoided $\pm 1$ to $\mp 1$ switching transitions to ease stresses on the link.

One of the more important goals was to verify the validity of the loss estimates on which the design methodologies were based. For the conditions specified above, Fig. 11 shows comparisons of total system losses versus $L$ for the RDCLI operating a $t$ 10, 25, and 40 kHz. The optimal choice of $L$ is seen to be accurate to within 2–3%, whereas the estimate on system loss is within 10%. The accuracy of these estimates is more than adequate given the shallow extremum exhibited by the various curves. Given the fact that each optimization run took well over 8 hr on the computer, the importance of the estimates may be appreciated.

Fig. 12 shows the variation of the system losses with the link frequency for the RDCLI. Each point represents the optimum design point at that frequency. It is interesting to note that a 400% increase in frequency from 10 to 40 kHz increased total losses by only 22% from 447 to 546 W under indentical load conditions.

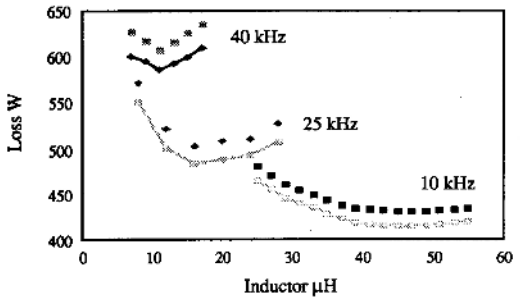


Fig. 11. Variation of losses with inductor for RDCLI at different link frequencies estimated (solid) and simulated (Scatter).

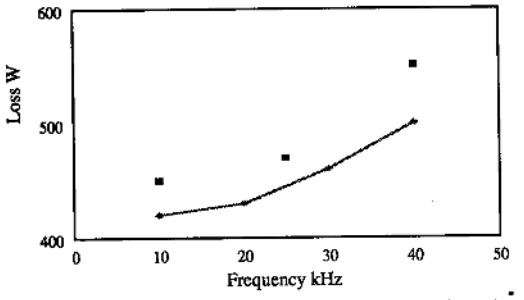


Fig. 12. Variation of minimum losses with link frequency estimated (solid) and simulated (Scatter).

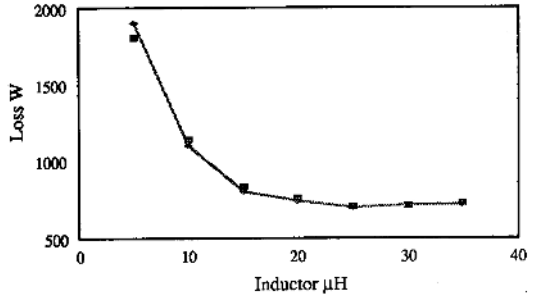


Fig. 13. Variation of losses in RPI with inductor at minimum switching frequency 12 kHz estimated (solid) and simulated (Scatter).

TABLE I
SUMMARY OF VARIOUS LOSS COMPONENTS FOR DIFFERENT TOPOLOGIES

| Inverter | Frequency kHz | Conduction Loss W | Switching Loss W | Device Loss W | ESR Loss W | Total Loss W |
|---|---|---|---|---|---|---|
| HSI | 5 | 225 | 434 | 659 | - | 659 |
| | 10 | 220 | 896 | 1116 | - | 1116 |
| RDCLI | 10 | 301 | 8 | 309 | 137 | 447 |
| | 25 | 283 | 48 | 331 | 134 | 465 |
| | 40 | 270 | 159 | 429 | 117 | 546 |
| RPI | 18(Avg) | 300 | 284 | 584 | 372 | 956 |

TABLE II
STRESSES ON VARIOUS COMPONENTS FOR DIFFERENT TOPOLOGIES (Rated Conditions $V_s = 300$ V, $V_o = 200$ V(Pk), $I_o = 100$ A(Pk), $P_o = 10$ kW, Q factor = 200)

| INVERTER | HSI | | RDCLI | | | RPI |
|---|---|---|---|---|---|---|
| Frequency (kHz) | 5 | 10 | 10 | 25 | 40 | 18 (Avg) |
| Current Stress (A): | | | | | | |
| Resonant Inductor (μH) | - | - | 50 | 26 | 14 | 25 |
| RMS | - | - | 144 | 90 | 81 | 121 |
| Peak | - | - | 300 | 215 | 197 | 317 |
| Resonant Capacitor | - | - | 3.4 | 1 | .76 | .16 |
| RMS | - | - | 113 | 50 | 45 | 15 |
| Peak | - | - | 208 | 133 | 125 | 317 |
| Device (tf=2μs, Vf=1.8V) | | | | | | |
| RMS | 44 | 45 | 49 | 48 | 48 | 69 |
| Avg | 25 | 25 | 31 | 30 | 30 | 29 |
| Peak | 150 | 150 | 128 | 136 | 124 | 315 |
| Diode (Storage time=500ns) | | | | | | |
| RMS | 23 | 23 | 32 | 31 | 31 | 42 |
| Avg | 7 | 7 | 15 | 14 | 14 | 15 |
| Peak | 100 | 100 | 100 | 108 | 99 | 307 |
| Clamp Device and Diode | | | | | | |
| RMS | - | - | 47 | 33 | 26 | - |
| Avg | - | - | 19 | 15 | 11 | - |
| Clamp Capacitor (μF) | - | - | 50 | 50 | 50 | - |
| RMS | - | - | 67 | 47 | 37 | - |
| Peak | - | - | 172 | 119 | 110 | - |
| DC Bus Capacitor | ∞ | ∞ | ∞ | ∞ | ∞ | ∞ |
| RMS | 62 | 62 | 122 | 70 | 65 | 111 |
| Peak | 243 | 220 | 300 | 215 | 197 | 315 |
| Output Filter Capacitor | - | - | - | - | - | ∞ |
| RMS | - | - | - | - | - | 107 |
| Peak | - | - | - | - | - | 249 |
| Peak Voltage Stress | 300 | 300 | 460 | 460 | 460 | 300 |

For the RPI, Fig. 13 shows a comparison of the estimated and simulated device losses as a function of $L$. Once again, the validity of the technique is clearly apparent. The switching frequency of the RPI varies from 40 to 12 kHz with an average value of 18 kHz under the given conditions. As discussed earlier, all estimated losses are computed at 12 kHz. Designing the output filter $C_f$ with component values of $L = 25$ μH, $d = 0.66$, $C_R = 0.16$ μF, $f = 12$ kHz, THD $= 0.05$, and $V_s = 300$, we get, from (29) $C_f = 135$ μF. At $f_s = 60$ Hz, the capacitor conducts 100 A peak, which corresponds to 10% of rated current. This is certainly acceptable.

Table I gives a summary of various loss components for the topologies and switching frequencies considered. It can be seen that the RDCLI is most effective at reducing switching losses and permits operation at substantially higher switching frequency. The losses in the RDCLI actually include a fifth device and indicate that the losses per device are even lower. For the HSI as expected, switching losses completely dominate and limit the performance level achievable. For the RPI, switching losses are substantially reduced, compared with the HSI, but are greater than for the RDCLI. The use of a PWM strategy as opposed to a DPM strategy may provide the only reason for selecting the RPI over the RDCLI.

Table II shows details of peak, average, and rms stresses on the various components. The biggest penalty faced by the RDCLI is obviously the 1.5-$V_s$ voltage stress. The peak device current stresses in the RDCLI are actually lower than for the HSI. The RPI peak device current seems to be very high at 315 A. However, the average device current that governs conduction losses is very similar to the RDCLI. Consequently, using a device with a good peak turn-off capability, such as a GTO, would maximize RPI performance.

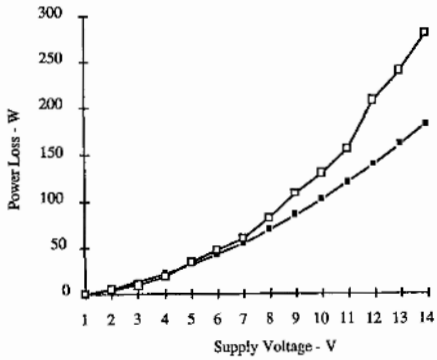


Fig. 14. Comparison of calculated and measured losses at no load.

TABLE III
COMPARISON OF MEASURED AND CALCULATED DATA FOR RDCL INVERTER

| Parmeter | Measurement | Calculation |
|---|---|---|
| Supply voltage | 650 V | 650 V |
| Clamp voltage | 850 V | 850 V |
| Peak Inductor Current | 46 A | 45.5 A |
| Bus Zero Period | 1.9 μs | 1.9 μs |
| Resonant Transition Period | 1.7 μs | 1.7 μs |
| Clamp Period | 10 μs | 10.8 μs |
| Link Frequency | 65 kHz | 62.2 kHz |

( reproduced from [9] )

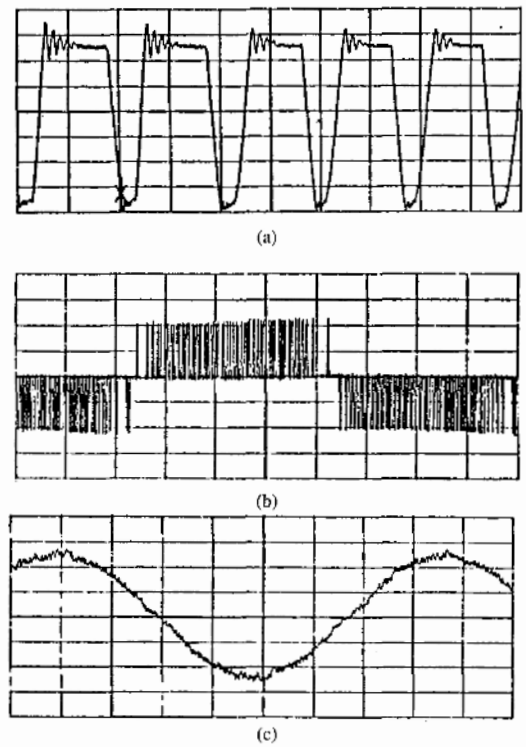


Fig. 15. Oscillograms depicting (a) link voltage, (b) output line-line voltage, and (c) load current for a resonant dc link inverter.

An experimental verification of the entire design methodology would be a highly impractical venture due to the need to vary of $L$ and $C$ values over a wide range in order to obtain enough data. A more practical approach measures the losses in an inverter designed using the methodology and compares the results. Fig. 14 and Table III have been reproduced from [9] and these show a comparison of calculated and experimental measurement of no-load losses and waveform parameters, respectively. The inverter, which is rated at 40 kVA, operating at about a 60-kHz link frequency uses IGBT's for switches. One can easily observe the excellent agreement between the theoretical and measured values of the losses in the circuit.

## VII. Conclusions

This paper has taken a detailed look at developing systematic design methodologies for soft-switched inverters. The design approach integrates component loss calculations with device characteristics, system control, and modulation strategies and formulates a simple analytical approach to a design problem that otherwise appears complex and almost intractable. Using system losses as a primary criteria for choice of $LC$ components, approximate expressions were derived for losses incurred within different devices and ESR elements. This approach has since been extended to other soft-switching converters with great success [10].

The validity of the loss models was extensively tested through comparisons with detailed simulations. The accuracies of the estimated losses and optimum $LC$ values calculated were found to be more than adequate and laid a sound basis for inverter design. For applications that are not sensitive to system efficiency, an alternate criteria may be considered if so desired.

Detailed comparisons of the hard switched inverter, the resonant dc link inverter, and the resonant pole inverter clearly demonstrate the superior loss characteristic of the RDCLI. At a switching frequency of 40 kHz, the switching loss per device in the RDCLI was approximately equivalent to that in a device in a HSI switching at 370 Hz. All component stresses are seen to be moderate and well controlled, where the higher voltage stress is a well-known penalty. An experimental RDCL inverter has been designed and constructed based on the proposed methodology. Fig. 15 shows oscillograms depicting link voltage, output line-line voltage, and load current for a resonant dc link inverter. The devices used are Mitsubishi BJT darlingtons rated at 1000 V, 150 A. The values of reactive components are $L = 20\ \mu$H and $C_R = 0.75\ \mu$F, giving a link frequency of approximately 31 kHz.

## Acknowledgment

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