DESIGN OF 16-BIT LOW POWER ALU - DBGPU

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Abstract

Arithmetic and Logic Unit (ALU) is one of the common and the most crucial components of an embedded system. Power consumption is a major design issue in the case of embedded systems. Usually ALU's consists of a number of functional units for different arithmetic and logic operations which are realised using combinational circuits. Each of the functional unit performs a specific arithmetic or logic operation. In this paper the main concern is given for reducing the power of the adder and multiplier modules which are important functional units of ALU thereby reducing the overall power consumption without compromising the speed of the processor. The ALU circuit ensures the execution of either arithmetic or logic operation only at a time so that only one set of circuits is active at a time thus ensuring low power consumption. The entire ALU circuit is realised using Verilog HDL and power analysis is obtained through same.

Keywords: Adder/Subtractor, Column Bypassing, Compressor

1. ALU

1.1 Introduction

The design of low power and high speed microprocessors requires that its components should consume less power. Arithmetic and Logic Unit (ALU) is one of the most power consuming components in a microprocessor. So, to reduce the power consumption of the entire ALU each of its components should consume less power.

Here we concentrate on a 16 bit ALU implementation which includes an ADDER/SUBTRACTOR module using carry look ahead adder, a MULTIPLIER module using column bypassing with inbuilt compressor, a SHIFTER with 8 different shift operations and a LOGIC unit.

Carry Look Ahead adder module consumes very less power and is much faster compared to Ripple Carry Adder. Likewise the multiplier module using compressor has reduced the usage of full adders for column wise addition, thereby reducing power consumption effectively.

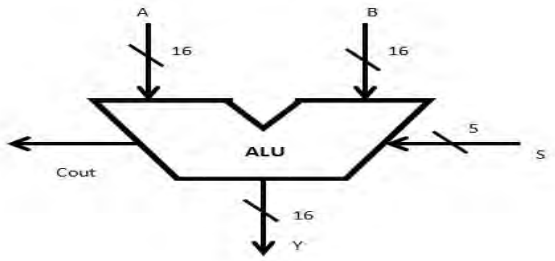


Fig 1. Symbol

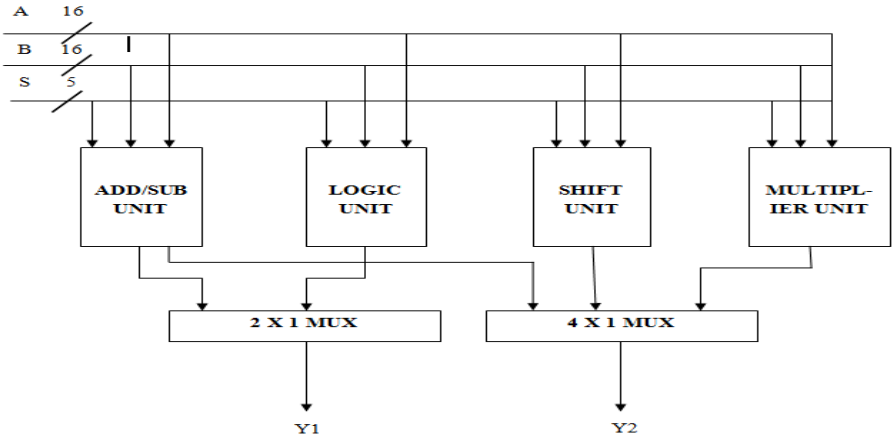


Fig 2. Block Diagram

1.2 ALU Operations

Control signals					
S[4]	S[3]	S[2]	S[1]	S[0]	OPERATION
0	0	0	0	0	Half Adder
0	0	0	0	1	Half Subtractor
0	0	0	1	0	Full Adder
0	0	0	1	1	Full Subtractor
0	0	1	0	0	Logical AND
0	0	1	0	1	Logical OR
0	0	1	1	0	XOR
0	0	1	1	1	Compliment
0	1	0	0	0	No Shift
0	1	0	0	1	Arithmetic Left Shift
0	1	0	1	0	Arithmetic Right Shift
0	1	0	1	1	Logical Left Shift
0	1	1	0	0	Rotate Left
0	1	1	0	1	Rotate Right
0	1	1	1	0	Rotate Left Through Carry
0	1	1	1	1	Rotate Right Through Carry
1	0	0	0	0	Multiplication

Control logic of control unit :Table 1

2. 16-bit Carry Look Ahead Adder/Subtractor

The carry look ahead adder reduces the consumption of power without compromising the speed of the adder. This is achieved by generating carry simultaneously from all the bits. An n-bit carry look-ahead adder is formed from n stages, where each stage is a full adder modified by replacing its carry output line C_i by two auxiliary signals, generate (G) and propagate (P), where

$G_i = X_iY_i$ (1)

$P_i = X_i \wedge Y_i$

The carry in i^{th} stage, $C_i = G_i + P_iC_{i-1}$ (2)

Similarly $C_{i-1} = G_{i-1} + P_{i-1}C_{i-2}$ (3)

Substituting,equation (3) in equation (2),

$C_i = G_i + P_iG_{i-1} + P_iP_{i-1}C_{i-2}$ (4)

That is, C_i can be expressed as function of the P and G outputs of all the previous stages.

Carry look-ahead can be extended to larger adders. For example, four 1bit adder can be connected to form a 4bit adder and such four 4-bit adders can be connected to form the 16-bit adder.

In our ALU we have used the concept of adder-subtractor where the same circuit performs the functions of both adder and subtractor. The adder functions based on the concept of look ahead carry adder. The subtractor just uses an xor gate as an extra circuitry. The block diagram for an adder-subtractor circuit thus can be as below.

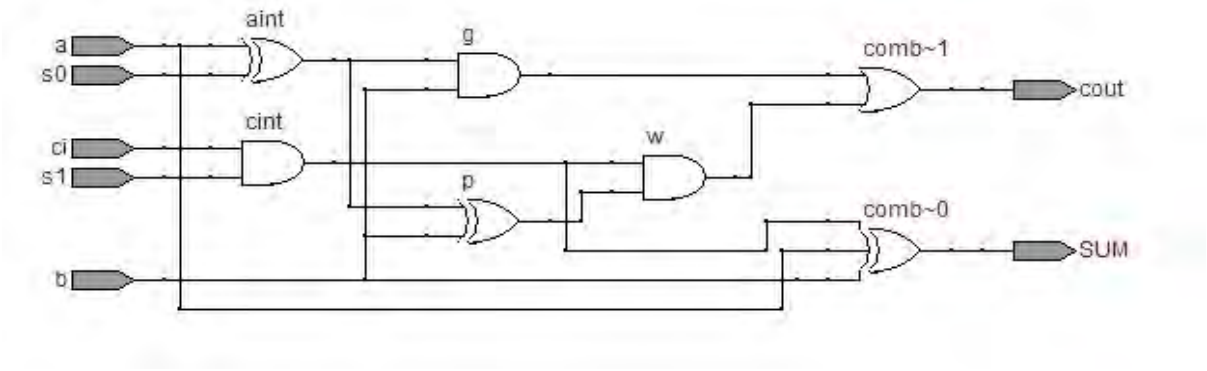


Fig 3. RTL view of adder subtractor

This is extended to 16 bits of data. The use of a single circuit for both adder and subtractor reduces power consumption and also area. The operation of the adder-subtractor is based on the S1 and S0 control bits.

S1	S0	Operation
0	0	Half Adder
0	1	Half Subtractor
1	0	Full Adder
1	1	Full Subtractor

Table 2

3. 8*8 Multiplier

The multiplier can multiply two 8 bit numbers resulting in a 16 bit product. We use coloumn bypass technique which reduces power consumption. A compressor module is used to calculate each bit in the product. This helps to reduce power. Thus power reduction is obtained through the two methods.

3.1 Column Bypassing

The column bypassing technique is advantageous over row bypassing in power reduction. It does not perform shifting and use partial products as in row bypassing. The circuit of the column bypassing scheme is smaller than that of the row bypassing scheme. We perform normal multiplication of two 8 bit numbers. First multiply each bit of the multiplier with that of the multiplicand and displayed as in usual multiplication. Then last bit position is taken as the LSB of the product. All other bits are obtained by addition using full adder and compressor along with carry propagated from previous states.

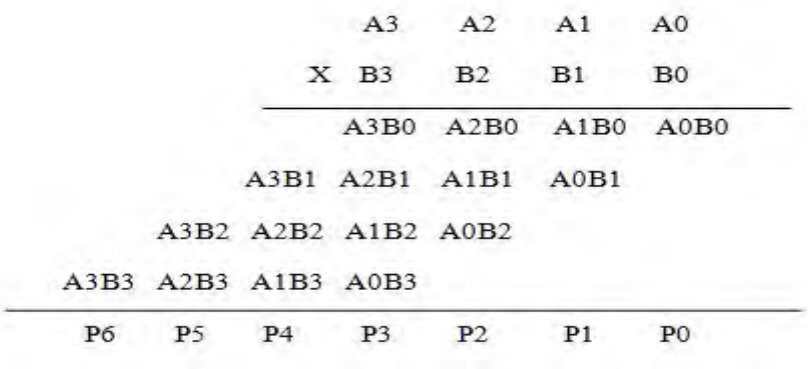


Fig 4.Multiplication

3.2 Compressor

Most digital signal processing (DSP) circuits use adder compressors for low power and high performance. Compressors can be used in multiplier architectures also. Multipliers are usually structured into three functions: partial-product generation, partial-product accumulation and final addition. The main source of power, delay and area is the partial-product accumulation stage .Compressors reduce the number of adders required at the final stage and thus reduces power consumption. Also it contributes to reduce the critical path and thus maintains the performance of the circuit. Here we have used a 4-2 compressor and 5-2 compressor to perform addition.

3.3 4-2 Compressor

The 4-2 Compressor has 5 inputs P, Q, R,S and Cin and has 3 outputs Sum, Carry1 and Carry2 as shown in Figure 4. The input Cin is the output from a previous lower significant compressor and the Cout output is input for the compressor in the next significant stage. The 4-2 compressors is with 2 full adders connected serially as shown in Figure 4.

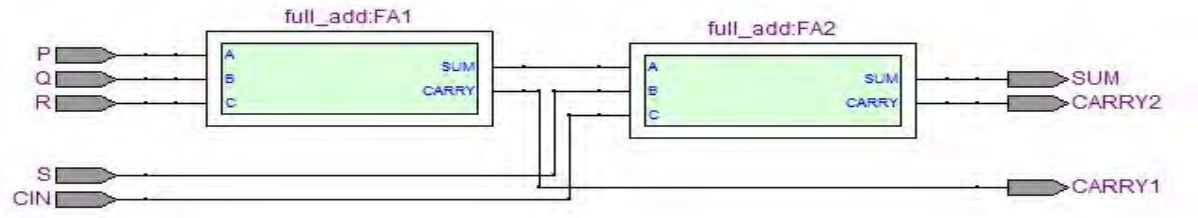


Fig 5. 4-2 Compressor using 2 full adders

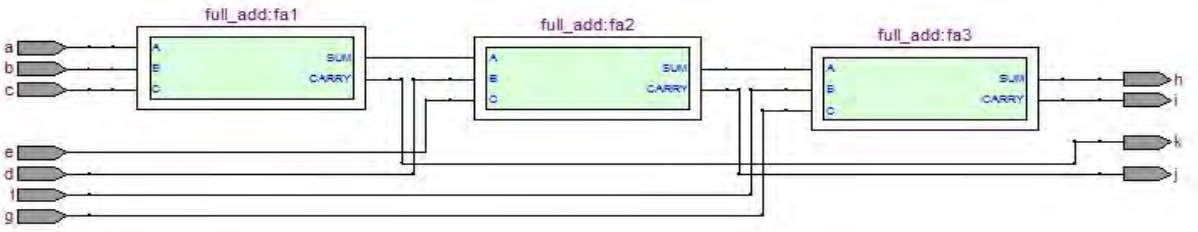


Fig 6. 5-2 Compressor using 3 full adders

4. Logic Unit

The logical functions performed are AND, OR, XOR and NOT. Bitwise operation is performed on the two inputs. The operation to be performed is decided by the 2 least significant bits of the decoder output.

S[1]	S[0]	Logical Operation
0	0	A.B
0	1	A+B
1	0	A^B
1	1	~A

Table 3

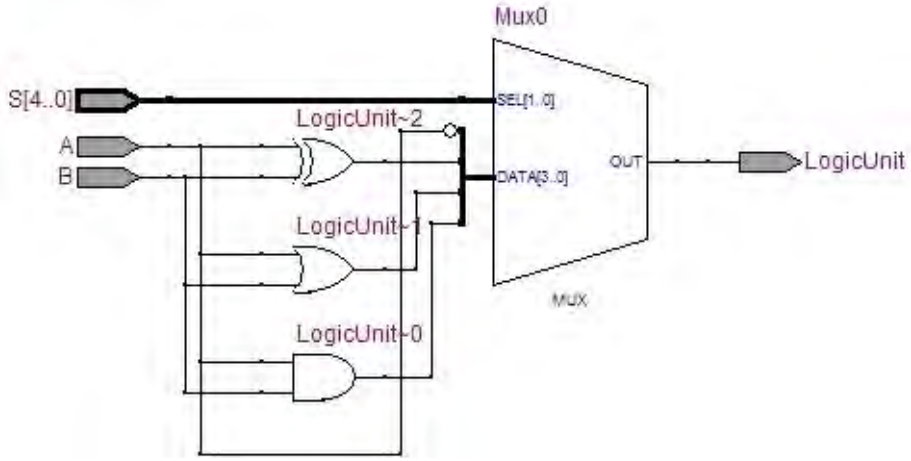


Fig 7.Logic unit

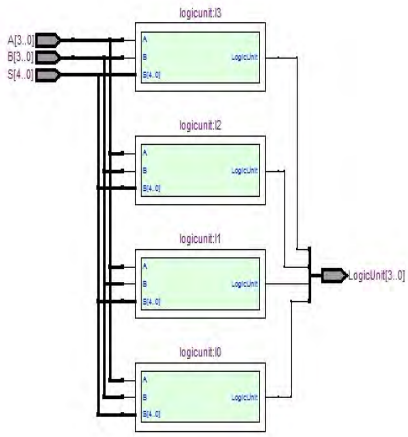


Fig 8. 4 bit logic unit

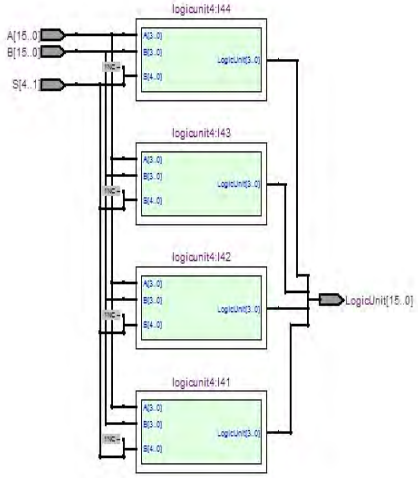


Fig 9. 16bit logic unit

5. Shifter

The ALU designed performs 7 Shift/Rotate Operations namely arithmetic left shift(same as logical left shift),arithmetic right shift, logical right shift ,rotate and rotate through carry.The logical shift operation shifts each bit of the operand. In logical shift a number's sign bit is not preserved. and each bit in the operand is moved a specified number of bit positions. The vacant bit-positions are filled with zeros. In arithmetic shifts, the shifted bit is retained.

Logical shift is an efficient way to perform division and multiplication of integers by powers of two. Shifting left by k bits on a binary number is equivalent to multiplying it by 2^k.Similarly shifting right by *k* bits on an binary number is equivalent to dividing it by 2^k.

For example, consider the binary number 0001 0111.

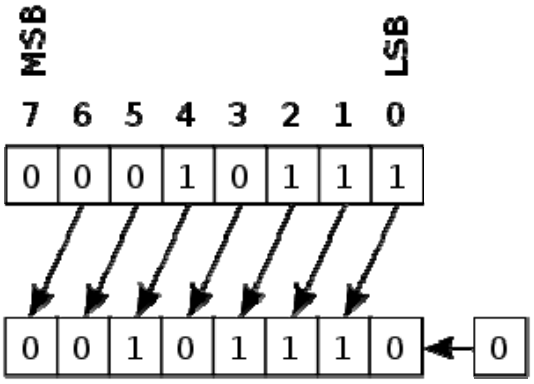


Fig 10. Logical left shift

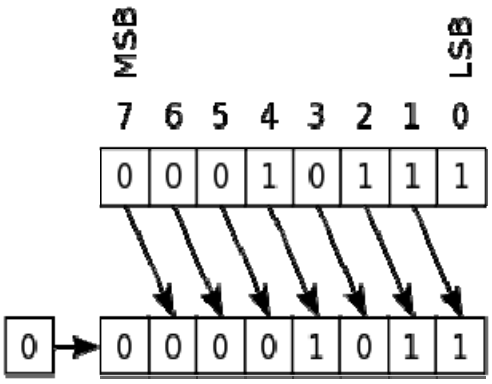


Fig 11. Logical Right Shift

The shift/rotate operation is performed based on the 3 lower significant bits of the select line

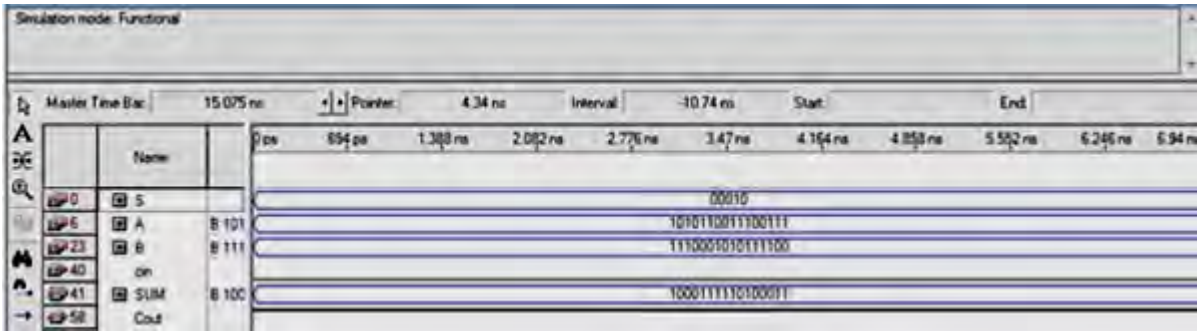
5.1 Shift Operations

S[2]	S[1]	S[0]	OPERATION
0	0	0	No Shift
0	0	1	Arithmetic(logical)Left Shift
0	1	0	Arithmetic Right Shift
0	1	1	Logical Right Shift
1	0	0	Rotate left shift
1	0	1	Rotate Right shift
1	1	0	Rotate left through carry
1	1	1	Rotate right through carry

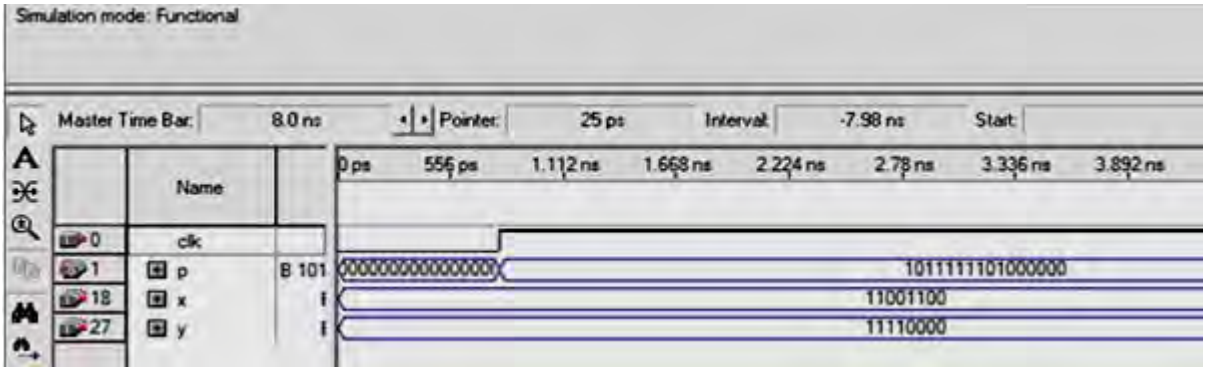
Table 4

6. Simulation Results

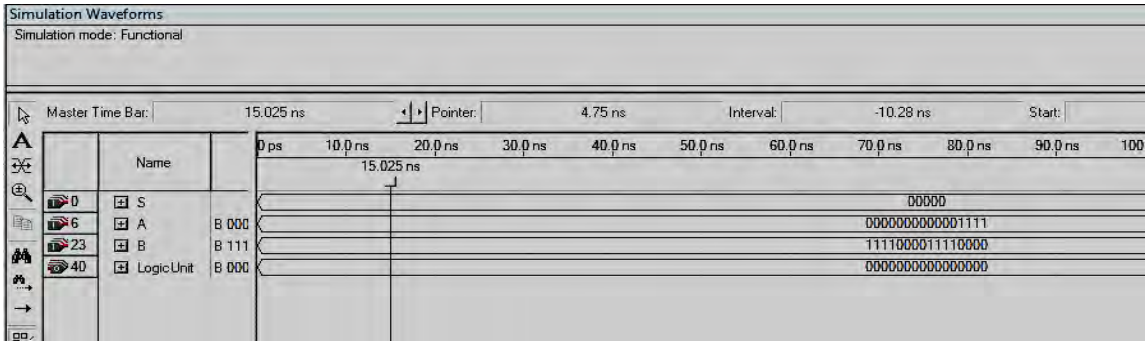
6.1 Adder/Subtractor



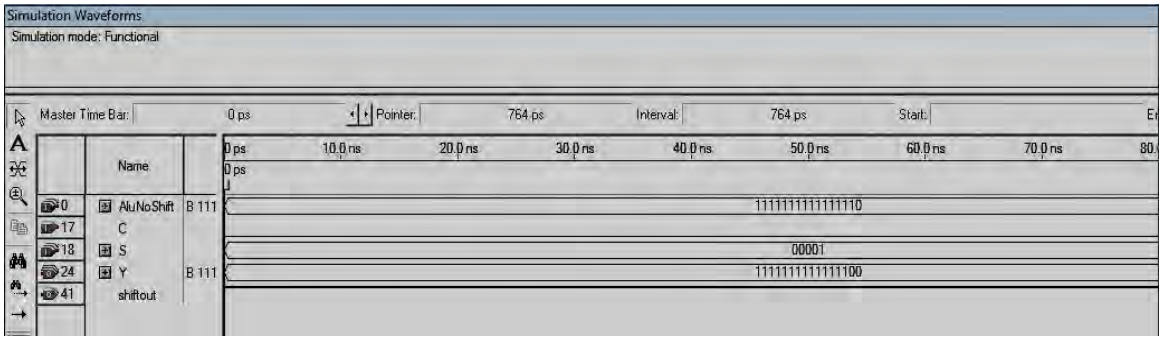
6.2 Multiplier



6.3 Logic Unit -AND-operation



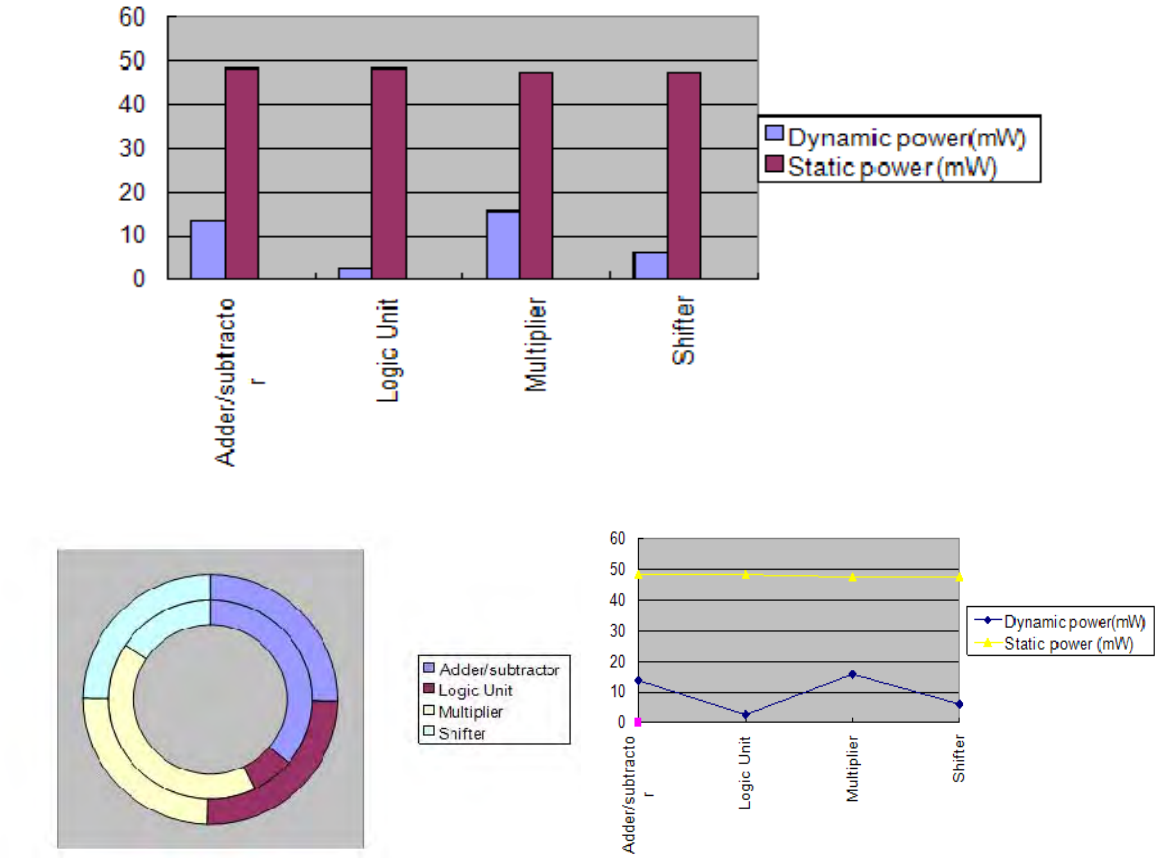
6.4 Shifter-Left Shift



7. POWER ANALYSIS

MODULE	Dynamic power(mW)	Static power (mW)
Adder/subtractor	13.76	48.31
Logic Unit	2.61	48.20
Multiplier	15.80	47.41
Shifter	6.04	47.57

Table 5



Total power consumption split up for ALU

8. Conclusion

The proposed ALU is designed with low power performance. The individual blocks within the ALU such as the adder, multiplier, logical unit and the shifter are low power units thereby reducing the power of the entire ALU unit. The adder used is a carry look ahead adder performing both addition and subtraction operations thus avoiding the need of a separate block for subtractor as in usual ALU designs. Power analysis and simulation was done on each block and found that power is low for each block. Integrating all the blocks in an ALU thus reduces the overall power.

9. Future Enhancement

Multiplier-Accumulator(MAC) is the essential elements of the digital signal processing. Multiplication involves two basic operations: the generation of partial products and their accumulation. The addition and multiplication of two binary numbers is the fundamental and most often used arithmetic operation in microprocessors, digital signal processors, and data processing application-specific integrated circuits. . Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier.In this MAC architecture a new Radix-4 modified booth algorithm is used for high speed multiplication. The Radix-4 MBA reduce N-bits of partial products to n/2 partial products. The parallel multipliers like Radix-4 modified booth multiplier do the computations using lesser adders and lesser iterative steps. This is very important criteria because in the fabrication of chips and high performance system requires components which has area as small as possible. The Multiplier and Accumulator can be adapted to various fields requiring high performance such as signal processing areas. Thus in above ALU ,MAC unit can be included for fast multiplication processing.

10. References

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