Design of 754 IEEE by The Multiplier of Floating Point

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Abstract:- **In the computation of the data processing signal in the environment of the digitized phenomena plays a crucial role in its application include the multiplication of the floating point under the computation of the scientific research oriented strategy respectively. In terms of the computational strategy multiplications plays a crucial role in its implication of the operation of the arithmetic scenario. Here the implementation of the multiplier with the high precision of the floating point value of improvement in the speed relative to the FPGA vertex 6. And under the further research strategy there is an integration of the 754 IEEE standard plays a crucial role I the applicability by the order of design and flow handling under the conditionality of the different multiple expectation respectively. Here there is an improvement in the performance and also the storage capabilities by the present method in a well efficient way. Simulations have been conducted on the present method where it completely overcome the drawbacks of the several previous methods in a well oriented fashion respectively.**

Keywords: **FPGA, Verilog, Multiplier, Adder, Multiplier of floating point, Precision data, IEEE 754, Virtex 6, Clock pulse and Core multiplier respectively.**

I. INTRODUCTION

Here the numbers of the floating point are considered of the type in which it includes the numbers of the binary aspect under the integration of the real numbers[1].

Under the standards of the 754 IEEE formats of the floating data are broadly divided with respect to the format interchange of the decimal and binary in a predefined fashion respectively. Under the applications of the processing of the signal relative to the digitized scenario it plays a crucial role and is a major challenge for the analysis point of view related to the multipliers of the floating data effectively. Here the focus of the paper includes the structural aspects of the normalized precision of the format of the binary digits of interchance which is shown in the block diagram shown below [3][4]. Under the implementation of FPGA by the data of the floating scenario in which in terms of the research point of view is a major concern. FPGA based implementation of the data parallelism under the effect of the pipelining plays a major role of the multiplier of the floating data under the standard of 754 IEEE respectively.

BLOCK DIAGRAM

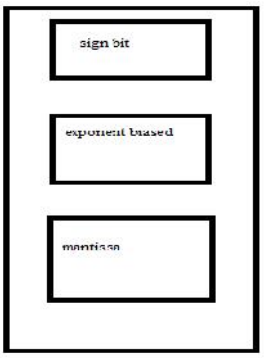

Fig 1: shows the representation of the floating precision

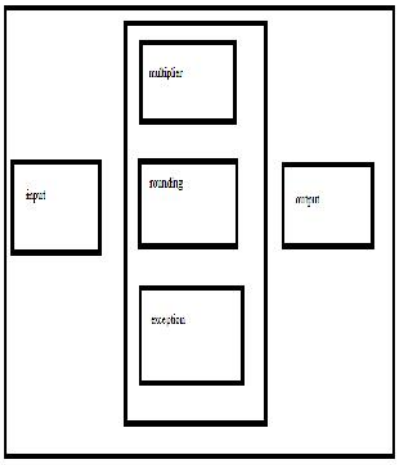

Fig 2: Shows the block diagram of the present method respectively

II. METHODOLOGY

Here in the implementation of the proposed method include the rounding and the exceptions of the multiplier of the floating data related to the scenario of the structural aspects aiming for the double precision implementation respectively. Here the implementation of the proposed method is shown by the above figure in the summarized fashion[2]. Where it includes the applicability of the rounding exception followed under the structural aspects of the pipelining plays a crucial role in its implacability that too in a simultaneous fashion respectively. Here the multiplier related to the floating data of the double precision which was included in the black box where it has the capability of size of the storage of 64 bits in terms of the receiving standards. Here the data received are classified as per the block diagram one under the three layered constraints respectively [5]. Then after the completion of the entire process there is a necessity of the normalization of the processed data that's is the final outcome of the system. Then it is applied in the cascaded fashion for the block diagram two and the process proceeds and finally the results are evaluated.

III. EXPECTED RESULTS

In this paper a new technique is proposed based on the precision of the design oriented multiplier of the floating data with respect to the double precision plays a crucial role in its analysis. Here the complete simulation takes place in the software of the Xilinx under the coding aspect of the VHDL terminology respectively. The entire code is dumped in the kit of the FPGA where the results are evaluated o the kit of FPGA under the precision of the floating data 64 bits respectively. Here finally the outcome of the present method is shown by the above diagram where the pulses are generated for the proposed method.

IV. CONCLUSION

In this paper a proposed algorithm is implemented which is effective and efficient in terms of the performance and the data storage followed by the speed of the process in an analogous fashion respectively. Under the format of interchange where the data related to the binary fashion by which under the standard support of the IEEE 754 of floating data of double precision respectively. Here the system is operated under the frequency of the 414 mega hertz and followed by the slices of the 648 in area in a most efficient fashion.

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