Design of a 100-MHz 10-mW 3-V Sample-and-Hold Amplifier in Digital Bipolar Technology

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***Abstract*—This paper describes the design of an all-npn open-loop sample-and-hold amplifier intended for use at the front end of analog-to-digital converters. Configured as a quasidifferential topology, the circuit employs capacitive coupling between the input and output to achieve differential voltage swings of 3 V in a 3.3-V system. It also exploits the high speed of bipolar transistors to attain a sampling rate of 100 MHz with a power dissipation of 10 mW. A prototype fabricated in a 1.5-μm 12-GHz digital bipolar technology exhibits harmonics 60 dB below the fundamental with a 10-MHz sinusoidal input. The hold-mode feedthrough is less than -60 dB and the droop rate is 100 μV/ns.**

I. Introduction

THE TREND toward implementing systems with low supply voltages has created challenging tasks in the design of analog and mixed-signal circuits. Dynamic range limitations have become more apparent in 3.3-V applications because neither the "turn-on" voltage of transistors nor the magnitude of noise and offsets has scaled proportionally. In particular, despite their high transconductance, the unscalable base-emitter voltage of bipolar devices has made their use more difficult in low-voltage systems.

This paper introduces a low-voltage open-loop sample-and-hold technique that is compatible with all-npn digital bipolar technologies [1]. Isolating the dc levels of the input and output stages by means of the sampling capacitor, the sample-and-hold amplifier (SHA) achieves differential voltage swings of 3 V with a 3.3-V supply. It also exploits the high speed of bipolar transistors to attain a sampling rate of 100 MHz while dissipating 10 mW. The SHA is intended for use at the front end of low-voltage high-speed analog-to-digital converters (ADC's), especially multistep architectures with resolutions on the order of 10 b. The proposed sampling technique may also prove useful in heterojunction bipolar technologies that do not provide high-performance pnp devices.

In the next section of the paper, two conventional all-npn SHA's are examined for low-voltage operation, and their shortcomings are illustrated. In Section III, parallel and series sampling techniques are described and compared. The SHA architecture and its implementation are presented in Section IV and design issues are detailed in Section V. Experimental results are summarized in Section VI.

II. Conventional All-NPN SHA's

High-speed sample-and-hold amplifiers in all-npn technologies have achieved sampling rates in excess of 100 MHz with resolutions of 10 b [2]. In this section, we consider two such circuits for low-voltage operation.

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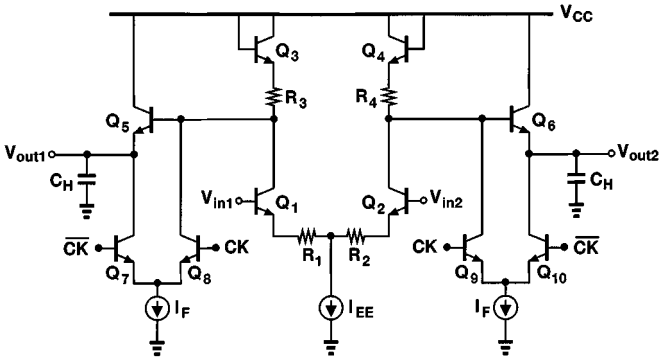


Fig. 1. All-npn sampling circuit in [2].

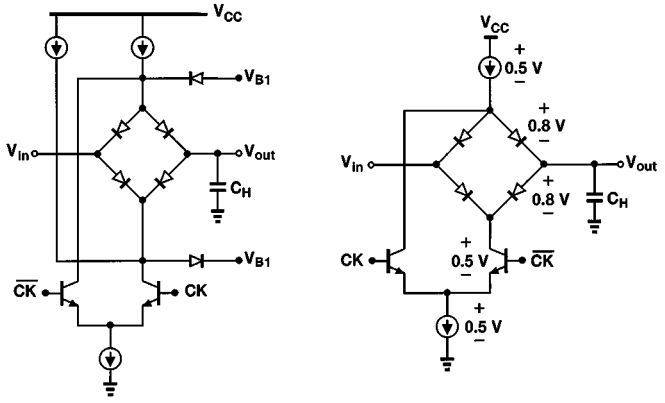
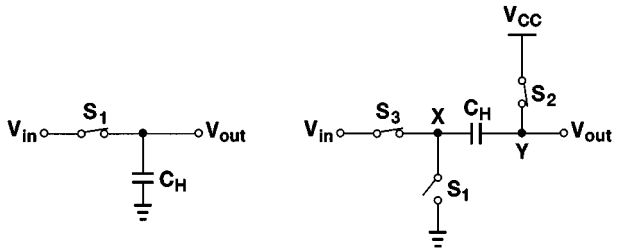


Fig. 2. Diode bridge sampler.

Shown in Fig. 1 in simplified form is an all-npn SHA topology proposed by Vorenkamp *et al.* [2]. This circuit consists of a linearized unity-gain amplifier Q_1–Q_4 and clocked emitter followers Q_5–Q_6 operating as sampling switches. To calculate the minimum supply voltage, we note that typically $I_F \geq I_{EE}$ and when the circuit is in the *hold* mode, both I_{EE} and I_F can flow from R_3 (or R_4). Thus, $V_{CC,\min} = V_{BE3} + (I_{EE} + I_F)R_3 + V_{CE1} + I_{EE}R_1 + V_{IEE}$. For $R_1 = \cdots = R_4 = R$, $V_{BE} \approx 0.8$ V, $I_{EE}R = I_FR = 0.5$ V, $V_{CE,\min} = 0.5$ V, and $V_{IEE} = 0.5$ V, we obtain $V_{CC,\min} = 3.3$ V. In practice, when designed for 10-b linearity, the circuit accommodates a 1-V differential input swing with a 5-V supply [2].

Fig. 2(a) depicts a sample-and-hold topology employing a diode bridge and hold mode clamp devices [3]. To calculate the minimum supply voltage, the circuit can be simplified as



(a) (b)

Fig. 3. Sampling techniques. (a) With parallel capacitor. (b) With series capacitor.

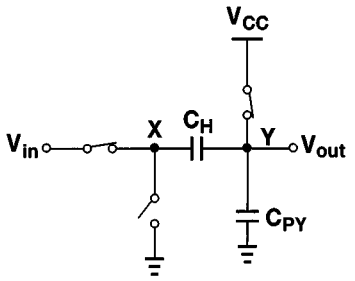


Fig. 4. Effect of parasitic capacitance in series-capacitor scheme.

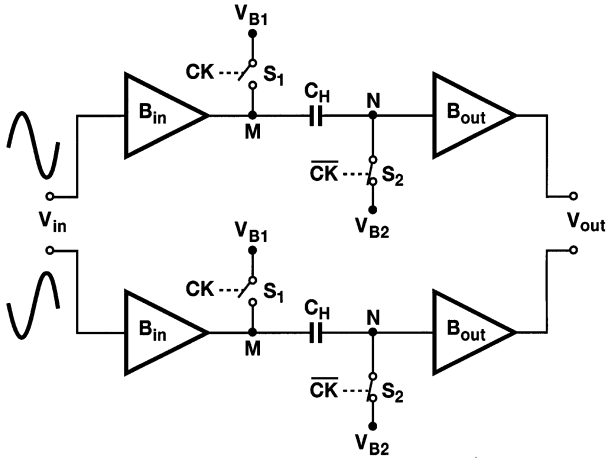


Fig. 5. Conceptual block diagram of SHA.

shown in Fig. 2(b), yielding $V_{CC,\min} \approx 3.1$ V with the same assumptions as above.

The circuits in Figs. 1 and 2 exemplify the difficulties in scaling the supply voltage of bipolar SHA's, indicating the need for low-voltage sampling techniques.

III. Parallel and Series Sampling Techniques

Sampling techniques can be broadly classified as depicted in Fig. 3. In the circuit of Fig. 3(a), the sampling capacitor is *in parallel* with the signal and the input and output are dc-coupled. This technique offers limited flexibility in low-voltage design because consecutive stages must provide opposite common-mode level shifts so as to provide reasonable voltage swings.

In the circuit of Fig. 3(b), the sampling capacitor is *in series* with the signal [3], thereby isolating the common-mode levels of the input and the output. Here, during the acquisition mode, S_2 is on, connecting node Y to V_{CC}, and S_3 is also on, allowing node X to track the input. In the transition to the hold mode, first node Y is released from V_{CC} and subsequently node X is shorted to ground, producing a voltage *change* at the output equal to the instantaneous value of the input.

In addition to isolated input and output common-mode levels, the circuit of Fig. 3(b) has another advantage over its counterpart in Fig. 3(a). While the parallel-capacitor scheme suffers from input-dependent charge injection due to S_1, the series-capacitor technique does not exhibit such behavior because S_2 turns off before S_3, thus injecting a constant charge onto Y.

Another point of contrast between the two sampling techniques lies in their hold-mode feedthrough behavior. In the parallel-capacitor configuration, C_H forms an attenuator with the feedthrough capacitances of the sampling switch, whereas in the series-capacitor topology, C_H has little effect on the feedthrough signal. This point is especially critical in bipolar sampling circuits because the junction capacitances of bipolar devices conduct appreciably.

It is also important to note that the series sampling scheme is susceptible to any capacitance seen from node Y to ground. Resulting from the fact that Y is not a virtual ground, this effect manifests itself when the voltage change at the input is coupled to the output. As shown in Fig. 4, the voltage division between C_H and the parasitic capacitance C_{PY} introduces gain error and, if C_{PY} is voltage-dependent, nonlinearity. While gain error can be corrected elsewhere in the system, the nonlinearity must be minimized by making C_H sufficiently larger than C_{PY}.

The SHA architecture to be described is based on the series-capacitor scheme, with the primary challenge being the implementation of S_1–S_3 in bipolar technology.

IV. SHA Architecture and Implementation

As mentioned in the introduction, the sample-and-hold circuit is intended for use in ADC's. Such an environment has two properties that relax the SHA design in comparison with a stand-alone sampling circuit: 1) the ADC digitizes only the *held* levels at the SHA output, allowing the acquisition behavior to be chosen somewhat arbitrarily; 2) the SHA need not drive a 50-Ω resistive load, although it must provide enough drive for the input capacitance of the converter.

A conceptual block diagram of the SHA is shown in Fig. 5. It employs two channels in a quasidifferential architecture to improve the overall linearity, minimize the effect of common-mode pedestal and noise, and lower the effective droop rate. Each channel consists of an input buffer B_{in}, a sampling capacitor C_H, and an output buffer B_{out}. Switches S_1 and S_2 connect nodes M and N to fixed voltages V_{B1} and V_{B2}, respectively. The input buffer is designed such that it is disabled when S_1 is on, thus operating as S_3 in Fig. 3(b). This point is clarified below.

In contrast with the fully differential circuit of Fig. 1, the proposed SHA incorporates two independent channels. Nevertheless, if the two channels are laid out symmetrically and in close proximity, they benefit from the same advantages as the fully differential case.

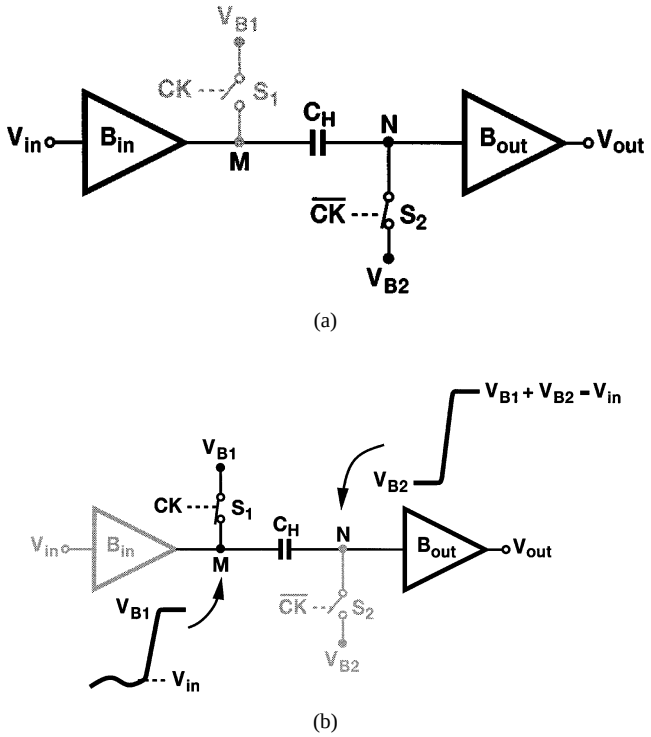


Fig. 6. Operation of SHA. (a) Acquisition mode. (b) Hold mode.

The operation of the circuit can be explained with the aid of Fig. 6. In the acquisition mode (Fig. 6(a)), S_1 is off and S_2 is on, holding node N at V_{B2}. Thus, if the offset and gain error of B_{in} are neglected, then $V_M = V_{in}$. In the transition to the hold mode (Fig. 6(b)), S_2 turns off and S_1 turns on, pulling node M to V_{B1} and disabling the input buffer at the same time. The change in V_M is therefore equal to $V_{B1} - V_{in}$. This change is coupled to node N, forcing V_N to go from V_{B2} to $V_{B1}+V_{B2}-V_{in}$. We see that the sampling operation inverts the input voltage and shifts it by $V_{B1}+V_{B2}$. The level shift can be chosen so as to maximize the input and output voltage swings.

The circuit implementation of one channel is shown in Fig. 7. In correspondence with Fig. 5, we note that emitter follower Q_1 operates as B_{in}, Q_2 as S_1, Q_3 as S_2, and emitter follower Q_4 as B_{out}. The circuit is in the acquisition mode when CK is high and in the hold mode when CK is low.

We illustrate the circuit's operation using Fig. 8. In the acquisition mode (Fig. 8(a)), Q_5 is on, drawing current from R_1 such that $V_P \approx -2$ V. Thus, Q_2 is off and Q_1 is on if V_{in} remains greater than V_P by a few hundred millivolts (Condition 1). During this mode, Q_6 is also on, allowing Q_3 to clamp node N at $-(V_{D1} + V_{BE3}) = -2V_{BE}$. (The voltage across R_2 is negligible.) The small current I_F lowers the impedance of D_1 and hence the inductive component seen at N.

In the transition to the hold mode, Q_5 and Q_6 turn off and Q_7 turns on. Consequently, V_P rises to the ground potential, pulling node M high and turning Q_1 off if V_{in} remains less than zero by a few hundred millivolts (Condition 2). Also, Q_7 draws current from R_2, turning off Q_3 rapidly.

From Conditions 1 and 2, we note that each channel can accommodate input/output swings of approximately 1.5 V, thus providing an overall differential full scale of 3 V with a 3.3-V supply.

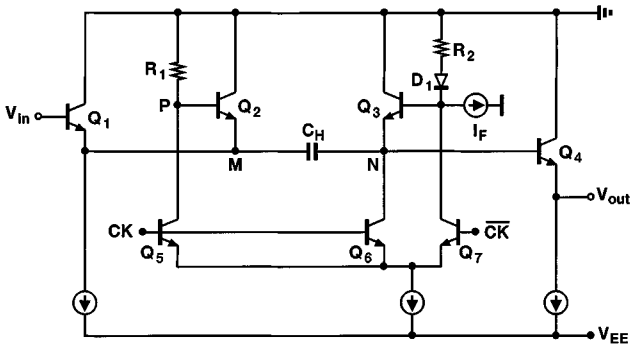
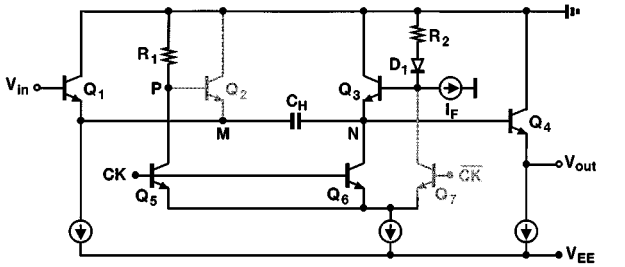
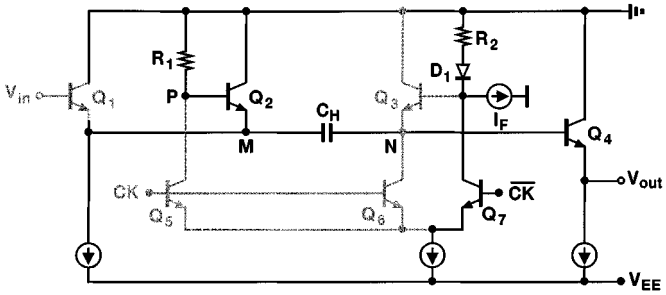


Fig. 7. Implementation of one channel.



(a)



(b)

Fig. 8. Operation of one channel. (a) Acquisition mode. (b) Hold mode.

Shown in Fig. 9 are the simulated input/output waveforms of the circuit. The input differential sinewave is 3 V_{PP} at 10 MHz and the clock frequency is 100 MHz. The output of each channel is depicted at the bottom. Note that in the acquisition mode, the output is reset to a fixed value; thus, the acquisition behavior is not observable at the output. This is a fundamental property of sampling circuits with series capacitors.

Simulations predict 10-b acquisition and hold settling times of approximately 4 ns and 2.5 ns, respectively.

V. Design Issues

While the series sampling technique easily lends itself to all-npn implementation, it nevertheless entails two important issues: hold-mode feedthrough and capacitance nonlinearity.

A. Hold-Mode Feedthrough

In the circuit of Fig. 7, Q_1 is off in the hold mode but its base-emitter junction capacitance introduces significant feedthrough (Fig. 10). In this mode, C_H is in series with Q_4 and hence does not attenuate the feedthrough signal. Nevertheless, since Q_2 is on, it provides a relatively low

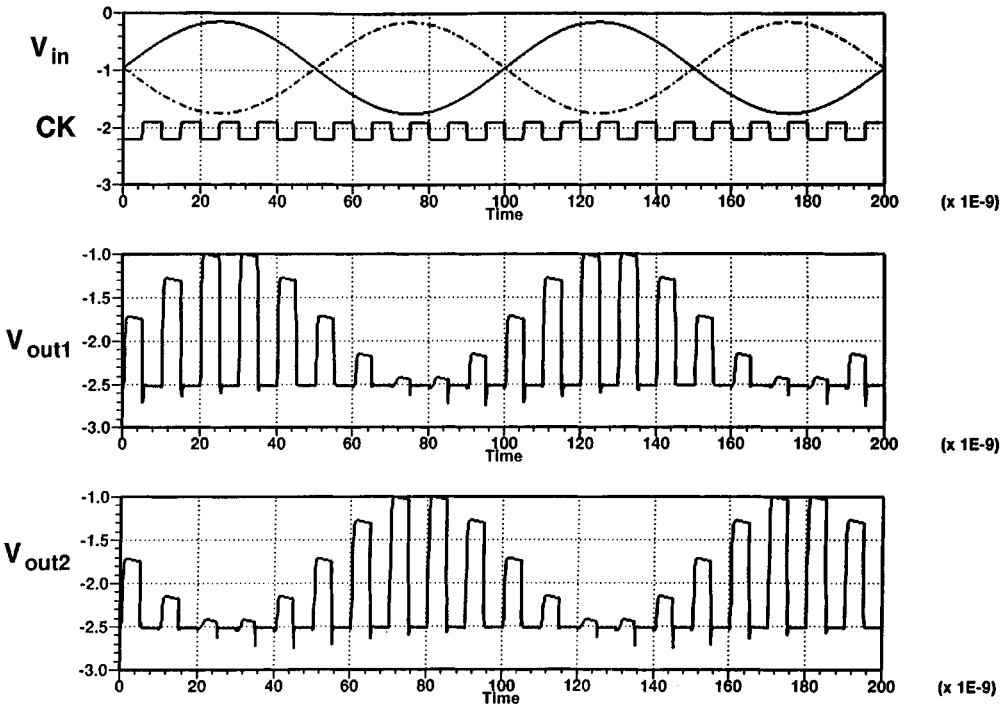


Fig. 9. Simulated input and output waveforms of the SHA.

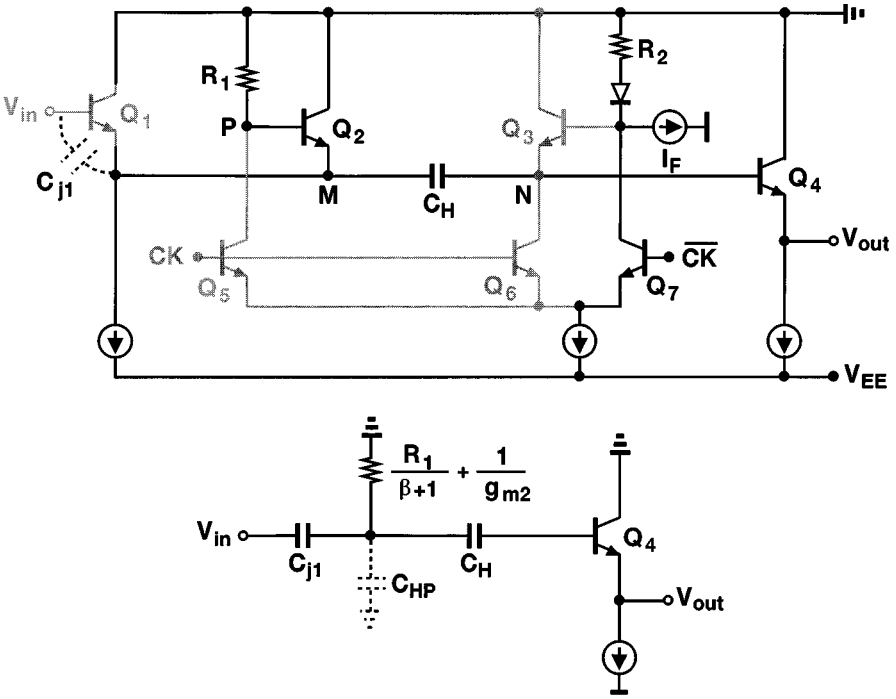


Fig. 10. Feedthrough in the hold mode.

impedance from M to ground, forming a high-pass filter with C_{j1}. For $R_1/(\beta+1) \approx 80\,\Omega$, $1/g_{m2} \approx 50\,\Omega, C_{j1} \approx 20$ fF, and frequencies less than 100 MHz, the feedthrough transfer function can be approximated as

$$H(s) \approx \left(\frac{R_1}{\beta+1} + \frac{1}{g_{m2}}\right) C_{j1} s. \tag{1}$$

For a sinusoidal input at 50 MHz, $|H(j\omega)| \approx 8.2 \times 10^{-4} \approx -62$ dB. The bottom plate parasitic capacitance of C_H, denoted by C_{HP} in Fig. 10, further suppresses the feedthrough signal.

B. Capacitance Nonlinearity

As explained in Section III, sampling circuits that employ the series technique of Fig. 3(b) are susceptible to the nonlinearity of any parasitic capacitance seen at the floating output node. In the circuit of Fig. 7, the capacitance loading node N originates from collector-base and collector-substrate junctions

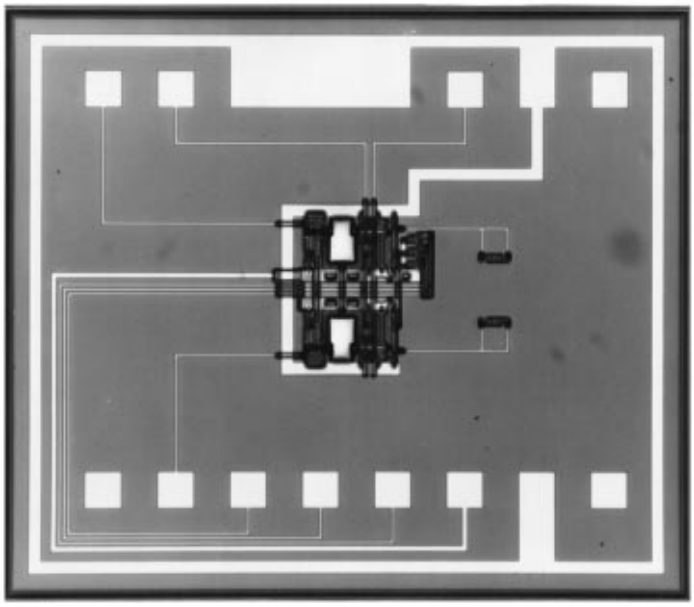


Fig. 11. SHA die photograph.

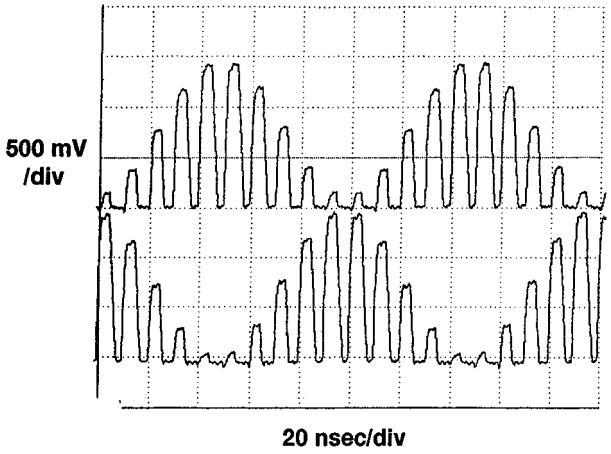


Fig. 12. Measured output in the time domain.

of Q_6, base-emitter junction of Q_3, and base-collector junction of Q_4. The voltage-dependence of this capacitance results in harmonic distortion, thereby imposing a lower limit on the value of C_H for a given precision. The analysis presented in the Appendix and simulations indicate that the quasidifferential architecture suppresses the second harmonic. Therefore, the third harmonic is the dominant component. With $C_H = 0.5$ pF, the total harmonic distortion remains below -65 dB.

VI. Experimental Results

The sample-and-hold circuit has been fabricated in a 1.5-μm 12-GHz digital bipolar technology [4]. Fig. 11 is a photograph of the die, whose active area measures 300 μm $\times$ 360 μm. All tests are performed with a 3-V supply while each channel dissipates 5 mW.

Fig. 12 depicts the measured output of each channel at a sampling rate of 100 MHz. The sinusoidal input has a differential swing of 3 V and a frequency of 10 MHz. Since the circuit cannot drive a 50-Ω load, accurate measurement of the hold settling time has not been possible. Instead, the output has been examined in the frequency domain to assess the circuit's dynamic performance.

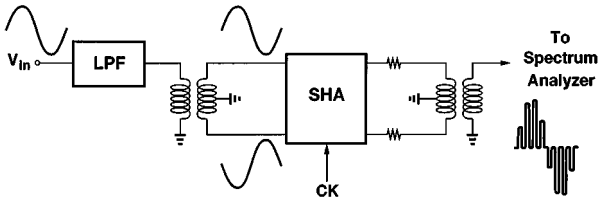
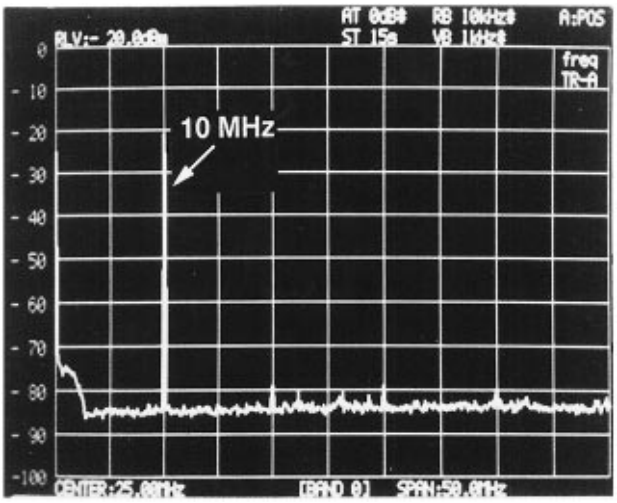
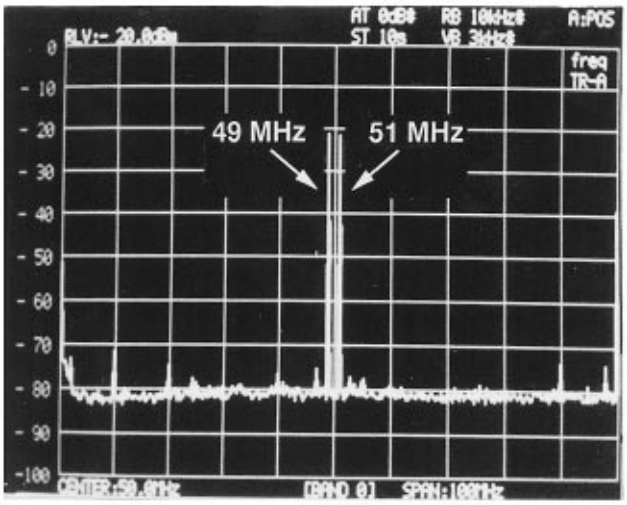


Fig. 13. Setup for frequency-domain measurement.



(a)



(b)

Fig. 14. Output spectra for 10-MHz and 49-MHz inputs.

Shown in Fig. 13 is the setup used for the frequency domain measurement. A filtered sinewave is split into differential signals and applied to the circuit. The SHA outputs are fed to a power combiner driving a spectrum analyzer. It is important to note that in this test, the entire output waveform is analyzed in the frequency domain, whereas in an ADC environment only the held values of the output are of interest. Since the waveform exhibits slewing at both the beginning and the end of the hold mode, this test overestimates the harmonic distortion.

Fig. 14 shows the output spectra at 100-MHz sampling rate. In Fig. 14(a), the analog input sinewave is at 10 MHz and

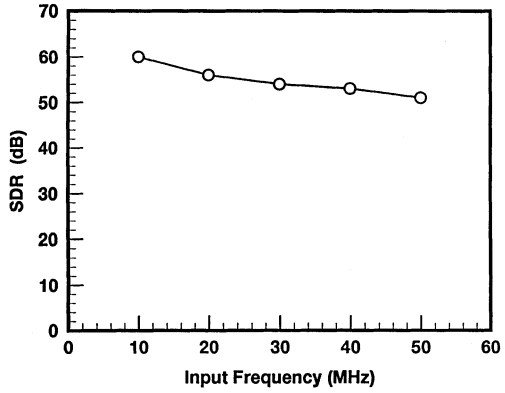


Fig. 15. Measured harmonic distortion versus analog input frequency.

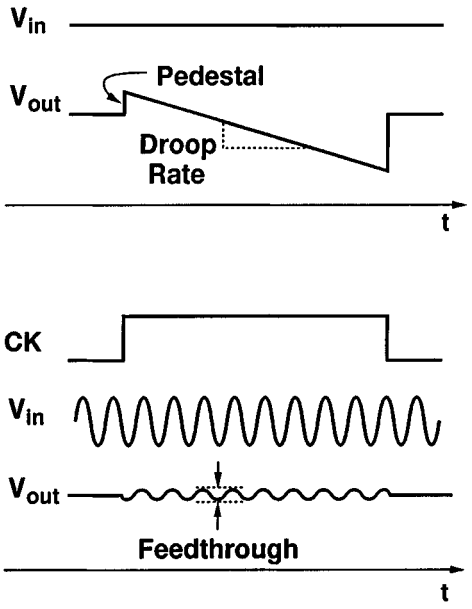


Fig. 16. Timing diagram for measurement of hold mode parameters.

the harmonic components are approximately 60 dB below the fundamental. In Fig. 14(b), the analog input is at 49 MHz and appears along with the aliased component at 51 MHz. Here, the second harmonic is at 98 MHz and about 53 dB below the fundamental.

Plotted in Fig. 15 is the measured harmonic distortion as a function of the analog input frequency with a 100-MHz sampling rate. Most of the degradation near the Nyquist rate is attributed to slewing at the beginning and the end of the hold mode. It is expected that if only the held values are considered, higher linearity will be obtained [5].

To evaluate the hold mode parameters, the timing arrangement shown in Fig. 16 is used. With a dc input, both the pedestal and the droop rate can be measured. To observe the feedthrough, a full-scale high-frequency sine input is applied and a low sampling rate is used so that several cycles of the feedthrough signal appear at the output.

Fig. 17 shows the output of each channel (the top two waveforms) along with the difference between the two. The common-mode (single-ended) droop is approximately 5 mV/ns while the differential droop is only 100 μV/ns. The differential pedestal error is about 6 mV.

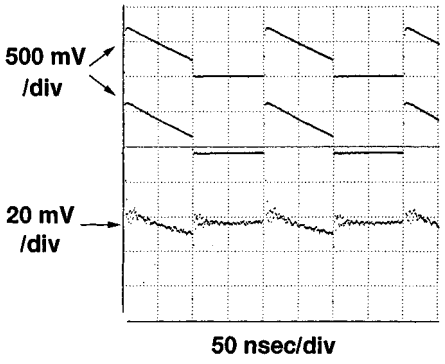


Fig. 17. Measured waveforms for pedestal and droop rate calculation.

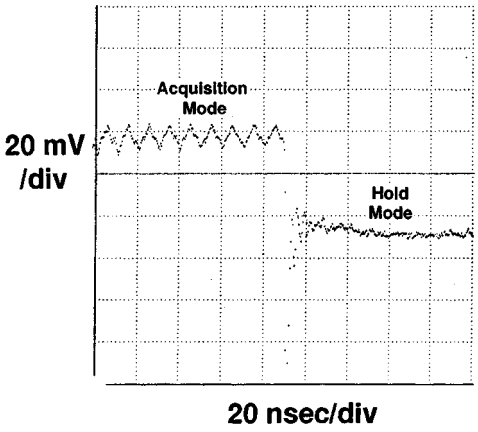


Fig. 18. Measured feedthrough in the hold mode.

TABLE I
SHA CHARACTERISTICS

Sampling Rate	100 MHz
Harmonic Distortion	–60 dB @ 10 MHz
Feedthrough	–60 dB @ 50 MHz
Droop	100 μV/nsec
Voltage Swing	3 V
Pedestal	6 mV
Power Dissipation	10 mW
Supply	3 V
Technology	12-GHz Bipolar

The feedthrough behavior of the circuit is depicted in Fig. 18. For a 100-MHz, 3-V sinusoidal input, the feedthrough suppression is better than 60 dB. We also note that in the acquisition mode the output experiences some variation. This effect is due to the finite impedance of the clamping transistor, Q_3, in the circuit of Fig. 7, but it has little significance in this application.

Table I summarizes the performance of the circuit.

VII. CONCLUSION

The series-capacitor sampling technique proves useful in low-voltage applications. While isolating the dc levels of the input and output, this topology lends itself to implementation in all-npn bipolar technologies.

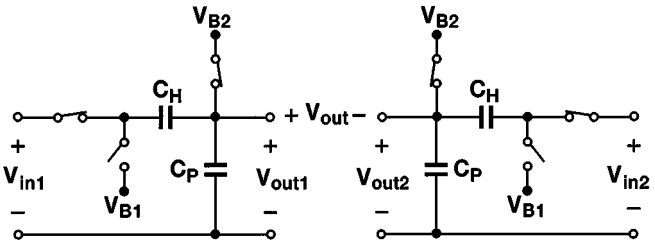


Fig. 19. Simplified quasidifferential sampling circuit.

A quasidifferential sample-and-hold amplifier based on the series sampling scheme has been described that achieves a sampling rate of 100 MHz while dissipating 10 mW from a 3-V supply. The circuit accommodates differential input/output swings of 3 V and exhibits more than 60 dB attenuation of the hold-mode feedthrough signal. The output harmonic distortion is about −60 dB for an analog input frequency of 10 MHz.

APPENDIX
HARMONIC DISTORTION IN SERIES SAMPLING

Consider the quasidifferential sampling circuit in Fig. 19. The voltage-dependence of the parasitic capacitance C_P introduces harmonic distortion in the output waveform. Assuming sinusoidal inputs and $C_P(V) = C_0 + \alpha_1 C_0 V + \alpha_2 C_0 V^2$, we can estimate the harmonic components in V_{out1}, V_{out2}, and V_{out}.

Let us first analyze the left part of the circuit. When the SHA enters the hold mode, the voltage across C_H goes from $V_{in1} - V_{B2}$ to $V_{B1} - V_{out1}$, while that across C_P changes from V_{B2} to V_{out1}. Thus,

$$\int_{V_{in1}-V_{B2}}^{V_{B1}-V_{out1}} C_H\, dV = \int_{V_{B2}}^{V_{out1}} (C_0 + \alpha_1 C_0 V + \alpha_2 C_0 V^2)\, dV, \tag{2}$$

which yields

$$C_H(V_{B1} - V_{out1} - V_{in1} + V_{B2}) = C_0 V_{out1} + \tfrac{1}{2}\alpha_1 C_0 V_{out1}^2 + \tfrac{1}{3}\alpha_2 C_0 V_{out1}^3 - f(V_{B2}), \tag{3}$$

where $f(V_{B2}) = C_0 V_{B2} + \alpha_1 C_0 V_{B2}^2/2 + \alpha_2 C_0 V_{B2}^3/3$. While it is desirable to solve (3) such that V_{out1} is expressed in terms of V_{in1}, the third order of the equation makes this approach difficult. We therefore apply an approximation as follows.

Suppose $\alpha_1 = \alpha_2 = 0$; then

$$V_{out1} = \frac{C_H(V_{B1} + V_{B2} - V_{in1}) + C_0 V_{B2}}{C_H + C_0}. \tag{4}$$

If α_1 and α_2 are not zero but sufficiently small, then we can assume that V_{out1} is still close to that given by (4) and hence can be substituted as such in the second- and third-order terms of (3). In other words,

$$\begin{aligned} -(C_H + C_0)V_{out1} &= -C_H(V_{B1} + V_{B2} - V_{in1}) \\ &+ \frac{1}{2}\alpha_1 C_0 \left[\frac{C_H(V_{B1} + V_{B2} - V_{in1}) + C_0 V_{B2}}{C_H + C_0}\right]^2 \\ &+ \frac{1}{3}\alpha_2 C_0 \left[\frac{C_H(V_{B1} + V_{B2} - V_{in1}) + C_0 V_{B2}}{C_H + C_0}\right]^3 \\ &- f(V_{B2}). \end{aligned} \tag{5}$$

For $V_{in1} = A\cos\omega t$, the second and third harmonics in V_{out1} can be easily calculated. In quasidifferential operation, $V_{in2} = -V_{in1}$ and $V_{out} = V_{out1} - V_{out2}$. It follows from (5) that if $C_0 \ll C_H$, then

$$V_{out} \approx -2A\cos\omega t + \frac{2}{3}\alpha_2 \frac{C_0}{C_H} A^3 \cos^3 \omega t. \tag{6}$$

Thus, the magnitude of the third harmonic normalized to the fundamental is

$$HD_3 \approx \frac{\alpha_2}{12}\frac{C_0}{C_H} A^2. \tag{7}$$

Simulations indicate that (7) predicts the distortion with a few dB of error.

We note that in the implementation of Fig. 7, other sources of distortion exist in the tracking mode. The finite bias currents of Q_1 and Q_3 impose an upper bound on the input slew rate for a given distortion. The analysis is similar to that in [2].

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Behzad Razavi (S'87–M'91), for a photograph and biography, see p. 109 of the February 1995 issue of this JOURNAL.