Design of a Boost Power Factor Correction Converter Using Optimization Techniques

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Abstract— This paper presents a procedural approach for the design optimization of a boost power factor correction front-end converter with an input electromagnetic interference filter. The system design variables are first identified. The relevant system responses and component costs are then expressed as a function of these design variables. Finally, by using mathematical optimization techniques, the design variable values that minimize the total system component cost are obtained, given practical constraints on these design variables and system responses.

Index Terms — Design optimization, continuous optimization, power factor correction, boost, electromagnetic interference, electromagnetic compatibility.

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Abstract— This paper presents a procedural approach for the design optimization of a boost power factor correction front-end converter with an input electromagnetic interference filter. The system design variables are first identified. The relevant system responses and component costs are then expressed as a function of these design variables. Finally, by using mathematical optimization techniques, the design variable values that minimize the total system component cost are obtained, given practical constraints on these design variables and system responses.

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I. INTRODUCTION

The design of power electronics systems involves large numbers of design variables and the application of knowledge from several different engineering fields (electrical, magnetic, thermal, mechanical). In order to simplify the design problem, traditional design procedures fix a subset of the design variables and introduce assumptions (simplifications) based on the designer's understanding of the problem. These simplifications allow an initial design to be obtained in a reasonable amount of time, but further iterations through hardware prototype testing are usually required. The ability and expertise of the designer usually leads to good designs, but not optimum designs.

Mathematical optimization techniques offer an organized and methodical way of approaching the design problem. This allows the designer to use more design variables and fewer simplifications. This, in turn, reduces the number of iterations during the hardware-testing phase. The increasing speed of computer hardware and the development of faster computational models allow optimum designs to be

obtained in a relatively short time. Furthermore, the application of the optimization techniques can provide a better understanding of the tradeoffs involved in the design, and even highlight some that were initially ignored.

In this paper, a continuous variable optimization approach is applied to the design of a 1.15 kW boost power factor correction (PFC) front-end converter including the input electromagnetic interference (EMI) filter. Even though most of the design variables of the system are essentially discrete and would therefore benefit from a discrete variable optimization approach [1], some of these discrete design variables (such as devices) are fixed and the others (such as capacitances) are converted to continuous design variables. This approach allows continuous optimization techniques to be applied to the problem. It also leads to a better understanding of the design tradeoffs and resulting system responses.

The organization of the paper is as follows. In Section II, the optimization problem is defined. First, the system under study, specifications, and fixed design variables are presented. Next, the design variables are identified and the objective function and constraints are described. Finally, the models and assumptions considered for the computation of the system responses are discussed. In Section III, the optimization algorithms employed are briefly described. In Section IV, the optimization results are presented and the paper is concluded in Section V.

II. DEFINITION OF THE OPTIMIZATION PROBLEM

A. System under Study, Specifications and Fixed Design Variables

The system to be designed consists of a boost PFC front-end converter plus an ac side EMI filter, as shown in the schematics of Fig. 1.
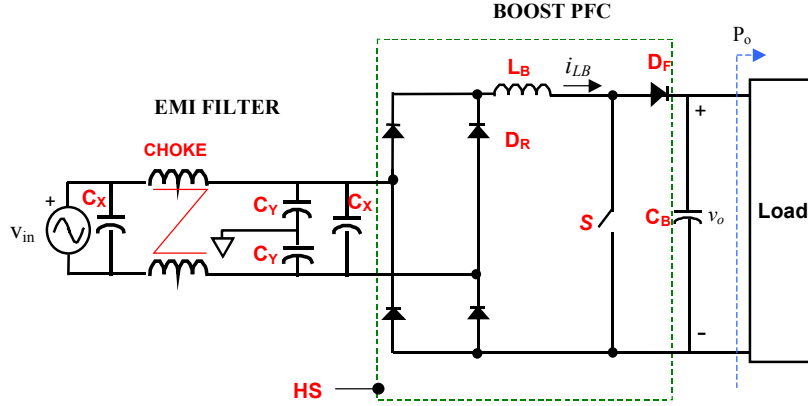
Fig. 1. EMI filter and boost PFC stage schematic.

The system cost must be minimized assuming the following assumptions:

1. The following design specifications are fixed: output power (P_o), input voltage range (V_{in_min}, V_{in_nom}, V_{in_max}), line frequency (F_{line}), maximum value of the output voltage (v_{o_max}), ambient temperature ($T_{ambient}$), and maximum temperature of the heat sink (T_{HS_max}).

2. The design must also meet the corresponding PFC [2] and EMI [3] standards.

3. The constant-frequency average-current-mode control for continuous-current-mode operation was chosen as the control strategy for the switch. This control was fixed during the optimization process.

4. The output capacitor C_B and the average value of the output voltage (v_o) are determined independently considering v_{o_max}, the maximum peak value of the input voltage ($V_{in\_max\_pk}$) and controller tolerances.

5. For the implementation of the common-mode choke, it was decided to choose among commercially available designs.

6. The core shape of the boost inductor L_B was considered to be toroidal and the core material was selected.

7. For the viability of the application of a continuous variable optimization approach, all devices (rectifier diodes D_R, fast diode D_F, and controlled switch S) were fixed. The cheapest devices meeting the

requirements of the system under study were chosen. In particular, for the controlled switch S, an IGBT with an external anti-parallel diode was selected. However, other analyses considering a MOSFET have been performed.

8. A single heat sink for all devices was considered.

9. A final simplification is made by assuming the layout to be fixed throughout the design process. The parasitics shown in Fig. 2 are estimated according to the layout and component characteristics of the common-mode choke and boost inductor. This is required information for the accuracy in the estimation of the EMI levels.
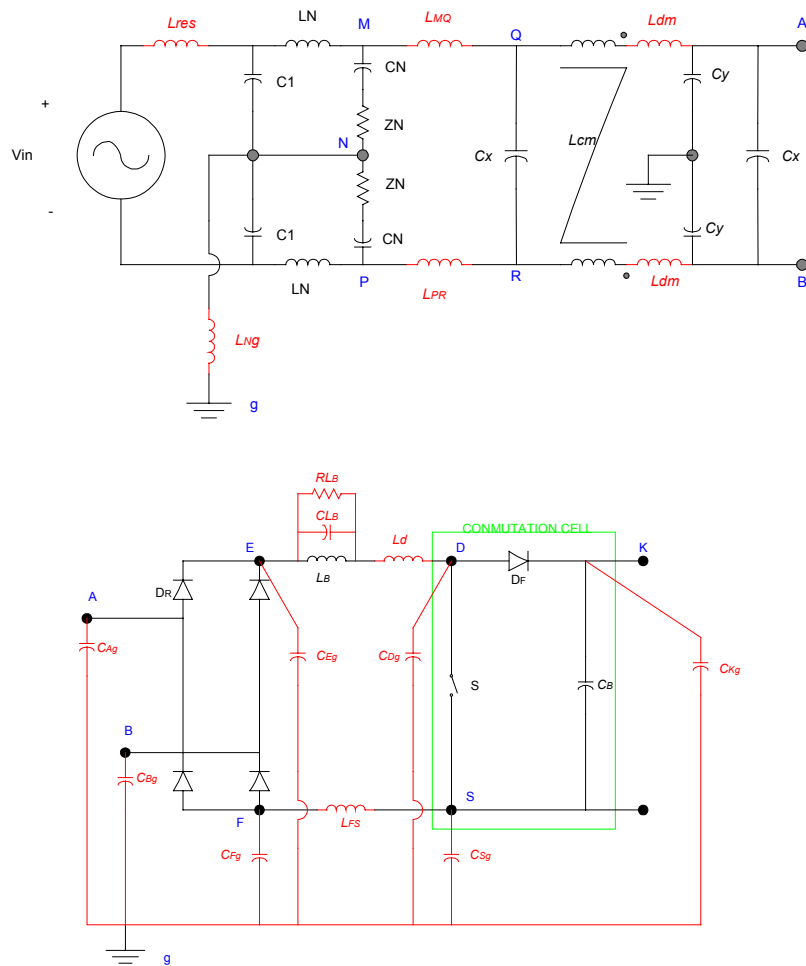

Fig. 2. System schematic including LISN, EMI filter and single-phase boost PFC stage. The circuit shows the components and parasitics considered.

B. Design Variables

The remaining variables of the system constitute the set of continuous design variables to consider in the optimization design problem. These are detailed in Table I.

TABLE I
DESIGN VARIABLES

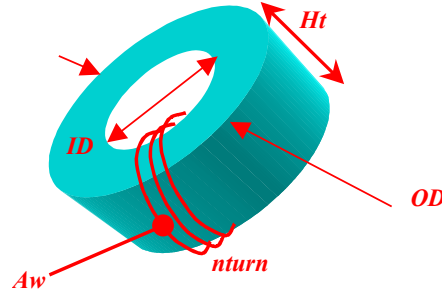|	
	Lcm: Common-mode choke inductance
EMI Filter	*Cx*: Differential-mode capacitance
	Cy: Common-mode capacitance
	OD: Outside diameter of the core
Boost	*ID:* Inside diameter of the core
Inductor	*Ht*: Height of the core
(see Fig. 3)	*Aw*: Area of the wire copper
	nturn: Number of turns
Fs: Switching frequency	
Rth_hs_a: Thermal resistance of the heat sink to the ambient	

Fig. 3. Boost inductor design variables.

C. Objective Function

In an optimization problem, the design variable values that maximize or minimize a given objective function must be determined. In our case, the objective function is the component cost of the system expressed as a function of the design variables

$$Sys\_Cost^* = Cost\_Choke + 2*Cost\_Cx + 2*Cost\_Cy + Cost\_L_B\_core + Cost\_L_B\_wiring + \quad (1)$$

$$+ Cost\_S + Cost\_D_F + 4*Cost\_D_R + Cost\_HS + Cost\_C_B.$$

The goal is to obtain the set of design variable values that minimize this function.

The cost of the different components has been approximated as a polynomial function of the design variable expressions shown in Table II, based on a given a set of actual components and their costs.

TABLE II
COMPONENT COST APPROXIMATION

Cost	Polynomial function of
Cost_Choke	Lcm
Cost_Cx	Cx
Cost_Cy	Cy
Cost_L_B core	Core volume
Cost_L_B wiring [a]	Wire volume
Cost_HS	1/Rth_hs_a

[a] Includes estimation of boost inductor manufacturing costs

D. Constraints

The design variable values that minimize the objective function must be found subject to several constraints defined according to the design specifications, physical limitations, etc. These constraints are discussed in the following:

1. The maximum peak-to-peak current ripple in the boost inductor cannot be higher than 150 % of the peak average (in a switching period) boost inductor current. This constraint is set to limit the amount of time the converter is operating in discontinuous current mode.

2. The peak value of the flux density in the boost inductor core cannot exceed the maximum value defined for its material.

3. The current density in the boost inductor wire cannot exceed the maximum current density considered for copper (600 A/cm^2).

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[*] *Italics:* costs function of the design variable values.

4. The wire should fit in the available window area of the core, according to the filling factor ($Ku = 0.3$) considered. The area occupied by the wire is considered to be the area of a square with side length equal to the diameter of the wire.

5. The inside diameter of the core must be smaller than the outside diameter minus 0.5 cm.

6. The rms (MOSFET switches, Cx capacitors, Cy capacitors, and common-mode choke) and average (IGBT switches, fast diode and rectifier diode) current in the components cannot exceed the maximum allowed rms/average current.

7. The junction temperatures of the switch, fast diode, rectifier diode, and the temperatures of the boost inductor core and heat sink should be lower than their corresponding maximum values.

8. The differential and common-mode disturbance levels for the group of harmonics around the first multiple of the switching frequency above the minimum frequency where the EMI standard limits are defined (currently 150 kHz), should be lower than the standard level defined for its frequency minus 3 dB (see section E).

9. The capacitance of the common-mode capacitor Cy should not exceed 10 nF due to the maximum leakage current allowed in the ac line.

10. The lower boundary for the switching frequency is 20 kHz (audible range limit) and the upper boundary is 150 kHz.

11. The minimum bare area of the wire copper is $0.0202*10^{-3}$ cm^2 (corresponding to an AWG 44).

E. Models and Assumptions Considered

For computing the value of the various constraints as a function of the design variables, worst-case steady-state algebraic models including second order effects have been applied. Here, the interest is to obtain a computationally efficient way of computing the system responses to evaluate the constraints.

This is desirable because optimization algorithms typically require that a large number of constraint evaluations be performed for different sets of design variable values.

1) Boost PFC Stage:

a) Assumptions:

1. The voltage drop across the EMI filter and diode bridge is negligible.

2. The change in boost inductor core permeability due to ac flux density has been neglected (conservative assumption).

3. A *di/dt* =200 A/μs is assumed for the computation of the losses due to the reverse recovery of the fast diode.

4. Fifty per cent of the reverse recovery losses are dissipated in the fast diode and fifty per cent in the controlled switch.

b) Computations:

The maximum and minimum values of the instantaneous current waveform through the boost inductor in each switching period along half a line cycle are computed, taking into account the effect of saturation of the boost inductor core (a different value of inductance is obtained for each switching cycle). The saturation of the core can be significant at the peak value of the input voltage, when the average current is maximum, as shown in the experimental results of Fig. 4. Modeling the saturation is therefore required to obtain accurate predictions of the system behavior.

The computation of the maximum and minimum values of the instantaneous current waveform through the boost inductor allows computing both the conduction and switching losses of the devices (controlled switch, fast diode and rectifier diodes). The switching losses include the losses due to the reverse recovery of the fast diode and the switching losses in the controlled switch due to the overlap of the voltage and current waveforms. The losses in the boost inductor core and wire are also calculated. From this loss

information, the temperature of the different devices and the temperature of the core can be computed. These computations, together with other conventional formulas, are used to check that constraints 1 through 7 are satisfied.
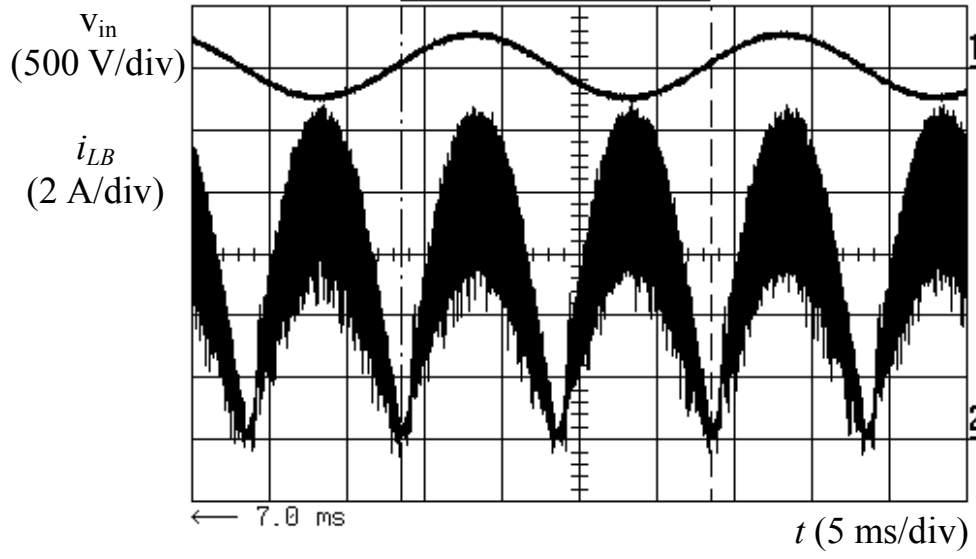

Fig. 4. Experimental waveforms for the input voltage v_{in} and boost inductor current i_{LB} (prototype tested at $V_{in} = 180$ Vrms and $P_o = 1.15$ kW).

2) EMI Filter:

a) Assumptions:

1. The voltage waveform across terminals D and S in Fig. 2 is that shown in Fig. 5. Only constant slopes have been considered for the rising and falling edges. No ringing has been considered.

2. According to the methodology used to estimate the EMI levels, we need to consider only one value of the boost inductance. We cannot use the different values of inductance obtained due to the effect of saturation of the core. We assumed that the value of the boost inductance was the minimum value of the inductance during the line cycle (conservative assumption).

3. The system configuration between mains and the bridge rectifier is assumed to be symmetrical with respect to ground.

4. If the group of LISN resistor voltage harmonics around the first multiple of the switching frequency above the minimum frequency for which the standard is defined comply with the standard, then all subsequent groups of harmonics will also verify the standard.

b) Computations:

To estimate the EMI levels in the LISN resistors, the model presented in [4] has been considered. The fundamentals of this procedure for estimating the value of the constraints number 8 are presented next.

In Fig. 2, all the system components and parasitics considered are presented. To account for the effects of the commutation cell with regard to the rest of the system placed between this cell and the mains, the commutation cell can be replaced by an equivalent voltage source with the time domain voltage waveform of Fig. 5 (this voltage waveform represents the voltage across the switch). In fact, in steady state, the duty ratio of the switch varies for each switching period during half a line cycle. As a result, the period of the voltage waveform $v_{ds}(t)$ is equal to half of the line period. But since the rectifier bridge will change the polarity of the voltage each half line period, this voltage will propagate to the system located before the bridge rectifier with a period equal to the line period.
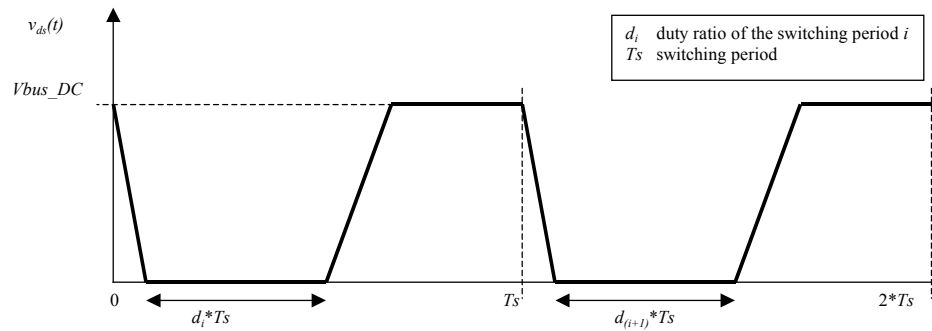

Fig. 5. Time domain evolution of the equivalent conducted EMI voltage source related to the commutation cell (represented here for only two switching periods).

We can characterize appropriately this voltage source in the frequency domain by means of the Laplace transform, first, and then applying the appropriate conversion to the Fourier representation. In essence, by

means of these steps, the previous voltage waveform is represented by an addition of sinusoids, each at a multiple of the fundamental frequency (in our case, the line frequency). For each of these frequencies, and assuming that the system is symmetric between the mains and the rectifier bridge (with respect to ground), we can derive from Fig. 2 an impedance diagram, in which the commutation cell is replaced with a sinusoidal voltage source (V_{pert}) corresponding to the harmonic of $v_{ds}(t)$ at the frequency considered. The different impedances will correspond to the system component and parasitic impedances at this frequency.

Hence, by using standard electrical network analysis methods, we can now compute, for each frequency desired, the perturbation voltage levels in the LISN resistors (ZN, in Fig. 2). According to [5], those harmonics that are even multiples of the switching frequency correspond to common-mode noise and those odd multiple of the switching frequency correspond to differential-mode noise.

In the case of the perturbed voltage model of Fig. 5, we will observe that the only significant harmonics at high frequency are centered around the multiples of the switching frequency. In our case, we select for the comparison with the standard limits the group of harmonics around the first multiple of the switching frequency above the initial frequency for which the standard limits are defined (150 kHz) (see Fig. 6).
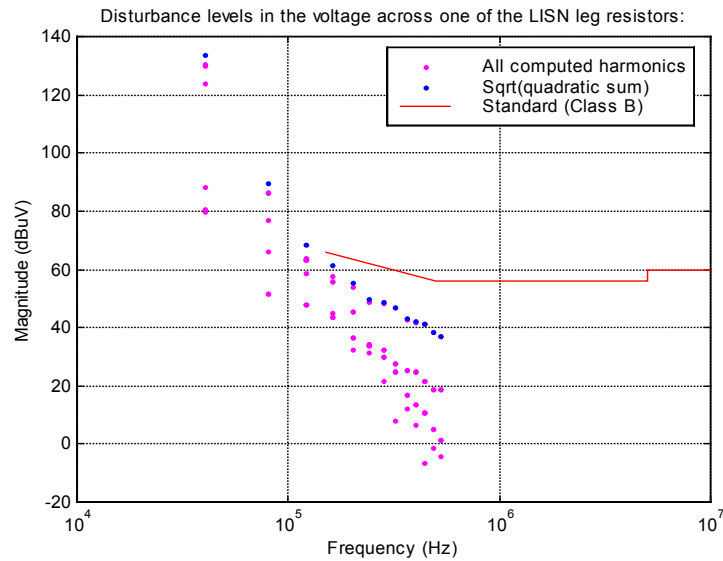

Fig. 6. Example of disturbance levels in the voltage across one of the LISN resistors for a switching frequency Fs = 40 kHz (the highest group of harmonics shown is the tenth above 150 kHz).

To verify that this group of harmonics meets the standard, the square root of the quadratic sum of the amplitudes of the harmonics contained in a 9 kHz band can be compared with the standard limit for the frequency considered (this emulates the measurement results obtained by the spectrum analyzer). This would constitute the only EMI constraint to be verified for this group of harmonics. However, in order to facilitate the identification by the optimizer of the dependence of the different harmonic levels (common and differential) on the different design variables, this single constraint was split into two. The square root of the quadratic sum of the harmonics corresponding to differential-mode noise, on one hand, and common-mode noise, on the other, are computed.

In fact, not all the harmonics in the 9 kHz band are considered for these computations, just the six harmonics most significant. A correction in the noise level is then introduced to account for the rest. Finally, both quantities are compared to the standard limits minus 3 dB as specified in constraints 8. The 3 dB difference is the minimum difference insuring that the total noise level be below the standard limit.

The fourth assumption is established in order to decrease the time needed for the evaluation of a design. The level of one group of harmonics centered around one multiple of the switching frequency is in general higher than the level of the group of harmonics centered at the next multiple of the switching frequency. Additionally, it has also been observed that this reduction on the level is greater than the decrease in the required standard level. Therefore, if the first group of harmonics verifies the standard there is no need to check subsequent groups.

In Fig. 7, the predicted and experimental results for both the differential and common mode EMI noise levels of a prototype are presented. It can be seen that the model is able to provide fairly accurate predictions of the levels of the first groups of harmonics above 150 kHz, especially in the case of the common mode noise. The predicted and experimental values for the first group of harmonics above 150 kHz, which is the critical group to meet the standard, are quite similar.
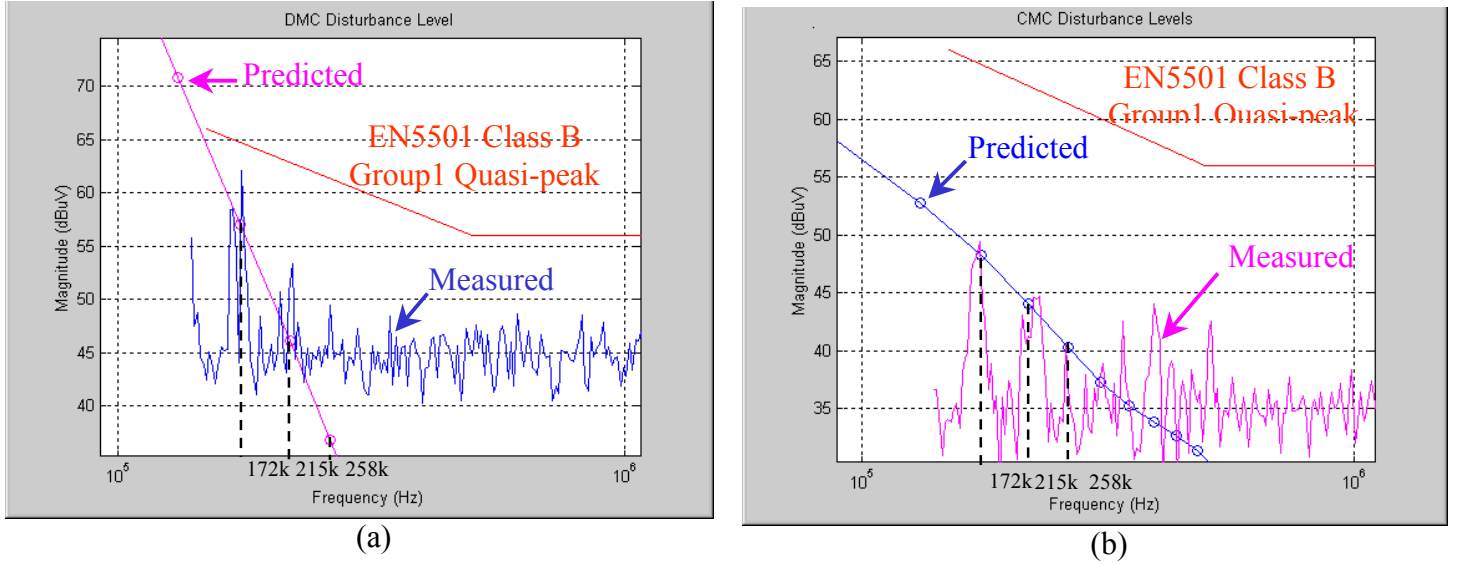
Fig. 7. Comparison of predicted and experimental results. (a) Differential mode noise. (b) Common mode noise.

The models discussed in this section were used to construct a MATLAB function. The inputs to this function are the values of the design variables for a given design. The function returns an output vector containing the value of the objective function and the values of the various constraints. The evaluation of one design takes less than one second on an Intel Pentium III microprocessor - 600 MHz.

III. OPTIMIZATION ALGORITHMS

The MATLAB function mentioned previously was linked to the commercial optimization software code VisualDOC (VMA Engineering) [6]. Both the Sequential Quadratic Programming [7] and Modified Method of Feasible Directions [7] algorithms were utilized in obtaining the results presented in Section IV. Constraint derivatives were computed using finite differences.

The optimization algorithms used for the present work belong to a class of optimization algorithms termed "gradient based methods". In order to begin the optimization process, these algorithms are typically provided with an initial design. Once an initial design is specified, gradients of the objective

function and constraints are computed with respect to the design variables to compute a search direction in the design space. Next, the design space is searched along the computed direction so as to minimize the objective function while satisfying all the constraints. Gradients are then recomputed at the new design point, and the process continues until no further improvements are possible. If the design space contains several local minima, there is a possibility that a gradient-based optimizer may be trapped by a local minimum, and the answer will depend on the selection of the initial design point. In order to increase the probability of finding the point with the smallest objective function value (the global minimum), it is customary to execute the optimization algorithm starting from several different initial designs. In the present work, it was found that there were local minima in the design space, although in all cases studied, the local minima were less expensive than the manual design. The results reported in Section IV correspond to the best designs found during the course of the study and are likely to be the globally optimum design.

IV. OPTIMIZATION RESULTS

Optimization runs were performed to design a 1.15 kW unit. The design specifications are summarized in Table III.

TABLE III
SPECIFICATIONS SUMMARY

P_o	1.15 kW
V_{in_max}	254 Vrms
V_{in_nom}	230 Vrms
V_{in_min}	180 Vrms
F_{line}	50 Hz
v_{o_max}	375 V
$T_{ambient}$	40 °C
T_{HS_max}	100 °C
Standards to comply with	IEC 61000-3-2: Input Harmonic Current, Class A [2].
	EN 55011: Conducted EMC emission, Class B [3].

In Table IV, the value of the design variables for a manual design and the design obtained by means of the optimization are presented. The value of the objective function of both designs is also specified. Aiming to reproduce a traditional design methodology, the manual design has been obtained by initially fixing the value of the switching frequency and choosing a commercial core, according to the designer's intuitive understanding of the problem. All the other design variables have been adjusted manually with the aid of the MATLAB function developed, trying to minimize the cost as much as possible while meeting the different constraints.

TABLE IV
DESIGN VARIABLE VALUES AND COST FOR THE MANUAL AND OPTIMUM DESIGNS

Design variable	Manual Design	Optimum Design
Lcm (mH)	1.50	0.97
Cx (µF)	2.8	2.23
Cy (nF)	5	7.58
OD (cm)	4.45	4.62
ID (cm)	2.72	2.33
Ht (cm)	1.65	1.62
Aw (cm^2)	$11.20*10^{-3}$	$11.41*10^{-3}$
$nturn$	122	88
Fs (kHz)	40	29.78
Rth_hs_a (°C/W)	2.20	2.38
$Cost$ [a]	100	90.64

[a] Percentage with respect to the manual design cost

A constraint is considered to be active when the boundary specified on the design response is reached. It will be inactive if the boundary specified is not reached and violated if the response value goes beyond the boundary. In the manual design, constraints 3, 4, 8 (both common and differential-mode noise), and the temperature of the heat sink are active. All the others are inactive. In the optimum design the only difference is that the common-mode noise constraint is inactive and the core temperature becomes active.

In the optimization runs performed, several tradeoffs and system behavior characteristics have been identified. Some of them are discussed in the following.

For a given switching frequency Fs, there is a tradeoff among the design variables common mode inductance Lcm, differential mode capacitance Cx and the boost inductor design variables, since all of them contribute to reduce the differential-mode noise (a leakage inductance of value $Ldm = 0.002 * Lcm$ has been assumed for the common-mode choke). The common mode capacitance Cy also slightly affects the differential-mode level. The relative cost-effectiveness of these components will determine the optimum set of values that meet the constraint specified for the differential-mode noise. A variation in the design of the boost inductor will vary the optimum heat sink size due to the variation in the peak-to-peak current waveform that will in turn vary the switching losses. Therefore, for the estimation of the cost-effectiveness of the boost inductor, the cost of the heat sink should be included.

Similarly, for a given switching frequency Fs, there is also a tradeoff between the common mode inductance Lcm and the common mode capacitance Cy since both design variables contribute to the reduction of the common-mode noise.

The selection of the optimum value of the switching frequency is not obvious. In the optimization runs, several local minima were detected at specific values of the switching frequency. In order to gain some insight into the effect of the value of the switching frequency Fs on the design, several optimization runs were then made by fixing this design variable and finding optimal values for the remaining variables. From the analysis of these results, we can observe the cost behavior sketched in Fig. 8 (qualitative cost pattern) for the EMI filter, heat sink and boost inductor.

The heat sink cost increases with an increase in the switching frequency due to an increase of the switching losses. The boost inductor cost increases as the switching frequency Fs decreases, due to an increase in the ac flux density and the current ripple that leads to an increase in the power lost in the core and wire, respectively, and therefore to a higher core temperature. Consequently, the inductor cost must increase in order to meet the constraint in the core temperature.
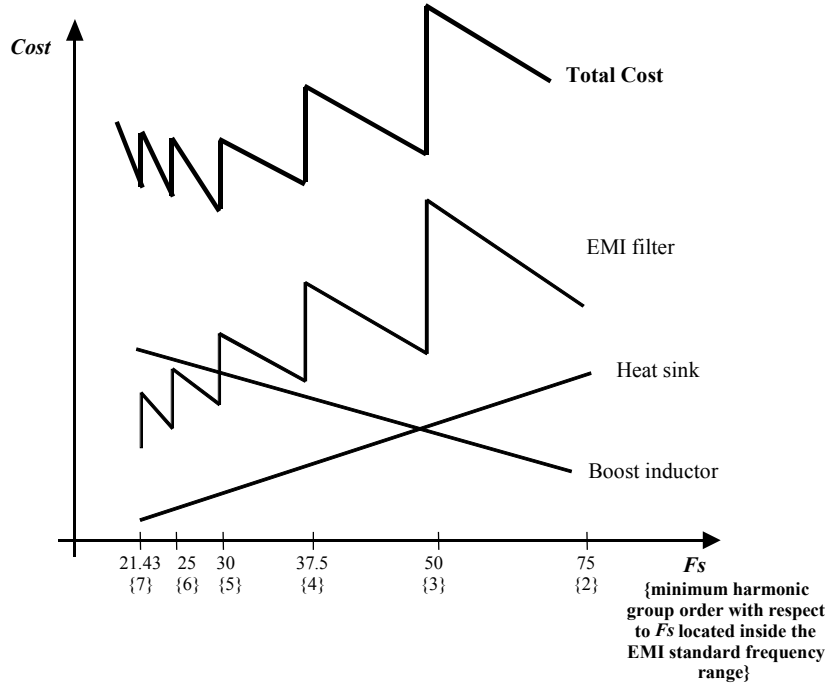
Fig. 8. Qualitative cost patterns of the optimum component and system costs as a function of the switching frequency.

The cost of the EMI filter depends essentially on the amplitude of the minimum-order harmonic (group of harmonics centered at multiples of the switching frequency) of the perturbation voltage V_{pert} that enters into the frequency range where the standard limits are defined (150 kHz - 30 MHz). Typically, this harmonic is placed between 150 kHz and 500 kHz, a range where the standard limit has a slope of approximately 20 dB/dec. As we increase the switching frequency Fs, this harmonic moves towards a higher frequency, where the standard limit is lower. But since the attenuation of the EMI filter considered is higher than 20 dB/dec, the resulting cost of the EMI filter needed is lower. The discontinuities in the EMI filter cost are due to the fact that, as the switching frequency Fs increases, new lower order harmonics (with an increasing amplitude) enter into the standard limit frequency range. For instance, at Fs = 21.43 kHz (= 150 kHz / 7) the 7th harmonic needs to be limited to the standard level at 150 kHz. Similarly for the 6th harmonic at Fs = 25 kHz, for the 5th at Fs = 30 kHz, etc.

The minimum of the total cost as a function of the switching frequency Fs will determine the optimum value of this design variable. One of the most valuable results of the presented optimization is the identification of this minimum and the pattern of the total cost as a function of the switching frequency Fs, which in general points as best choices for this design variable those values that are slightly lower than the discontinuities (at 21.43 kHz, 25 kHz, etc.).

V. Conclusions

A continuous optimization approach has been applied to the design of a 1.15 kW boost PFC front-end converter with an input EMI filter. The value of the considered design variables that minimizes the system cost subject to several constraints has been obtained. The results, although highly dependent on the accuracy of the cost information and models considered, highlight the main features of the system. The methodology applied allows obtaining improved solutions with respect to traditional design procedures and also reduces the design time required. A special feature of the procedure applied is that new optimum designs for different specifications can be obtained (almost) immediately.

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