Design of a Capacitor-Supported Dynamic Voltage Restorer (DVR) for Unbalanced and Distorted Loads

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***Abstract*—The paper discusses the operating principles and control characteristics of a dynamic voltage restorer (DVR) that protects sensitive but unbalanced and/or distorted loads. The main aim of the DVR is to regulate the voltage at the load terminal irrespective of sag/swell, distortion, or unbalance in the supply voltage. In this paper, the DVR is operated in such a fashion that it does not supply or absorb any active power during the steady-state operation. Hence, a dc capacitor rather than a dc source can supply the voltage source inverter realizing the DVR. The proposed DVR operation is verified through extensive digital computer simulation studies.**

***Index Terms*—Deadbeat control, distribution system, dynamic voltage restorer, unbalanced and distorted load, voltage source inverter.**

I. Introduction

A dynamic voltage restorer (DVR) is a power electronic converter-based series compensator that can protect critical loads from most common supply side disturbances other than outages [1]–[3]. The basic operating principle of a DVR is to insert a voltage of required magnitude and frequency in series with a distribution feeder. Thereby the DVR can restore the voltage on the load side to the desired amplitude and waveform even when the source voltage is unbalanced or distorted.

Usually a voltage source inverter (VSI) realizes a DVR. The output of the VSI is connected in series with a distribution feeder through a transformer. This device employs IGBTs that are operated in a pulse-width modulated (PWM) fashion. The VSI is supplied by a dc source [4]–[6]. With this, the DVR can regulate the load voltage at any given magnitude and phase angle. This can be accomplished through real power exchange between the dc source and the ac system through the inverter.

An alternative scheme is to provide real power exchange with the ac system through a separate rectifier. In this scheme, the power may be drawn from the ac system during normal operation and during voltage sag or load application. However, during load rejection, the excess power must be sent back to the ac lines. This may require a four-quadrant rectifier using two bridges. Alternately, a damping resistor may be switched in to dissipate the excess energy. Thus, this ac supported DVR is an expensive proposition and requires additional control for the rectifier.

It has been shown that the DVR can be operated in such a fashion that it does not supply or absorb any average real power in the steady state [7], [8]. However, in [7], [8] the load was assumed to be balanced and linear. In this paper, we propose a generalized algorithm to maintain balanced sinusoidal load voltage with a desired magnitude even when the load is unbalanced and nonlinear. The load voltage is regulated against all supply side voltage disturbances. The DVR is operated such that the load voltage magnitude is held constant but its phase angle is allowed to vary, while the average real power absorbed/supplied by it is zero in the steady state.

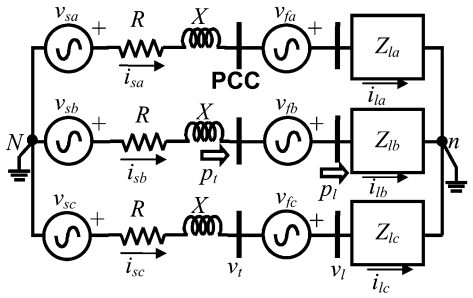

Fig. 1. Schematic diagram of a series-compensated distribution system.

The proposed algorithm is validated through extensive digital computer simulation studies, first with an ideal DVR model. In this, a hybrid structure of an ideal DVR will be proposed in which a shunt capacitor filter is used to provide a low impedance path for the harmonic components in the load and source currents. We shall then discuss the structures of a DVR using voltage source inverters. Three different DVR configurations will be investigated. It will be shown that only one of them is suitable for performing the desired task.

II. DVR Reference Voltage Generation

The schematic diagram of a series compensated distribution system is shown in Fig. 1. In this, the DVR is connected in series between the point of common coupling (PCC) and the load. With respect to this figure, we define the following:

- ideal series compensator: represented by the instantaneous voltage sources v_{fa}, v_{fb} and v_{fc};
- supply voltages: represented by the instantaneous voltage sources v_{sa}, v_{sb}, and v_{sc};
- load voltages: represented by the instantaneous voltages v_{la}, v_{lb}, and v_{lc};
- terminal (PCC) voltages: represented by the instantaneous voltages v_{ta}, v_{tb}, and v_{tc};
- line currents: represented by i_{sa}, i_{sb}, and i_{sc}. Note that these currents will also flow through the load and, therefore, we might also call them load currents;

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- sensitive loads: represented by the impedances Z_{la}, Z_{lb}, and Z_{lc}. In addition, the load may also contain rectifier-type loads.

The subscripts a, b, and c denote the phases. However, in the following, these are omitted if any discussion (or equation) applies to all three phases. The source is connected to the DVR terminal by a feeder with an impedance of $R+jX$. Using KVL at PCC we get

$$v_t + v_f = v_l. \tag{1}$$

The main aim of the DVR is to make the load voltage a strictly positive sequence. Furthermore, the DVR must not supply or absorb any real power. To force v_l to be positive sequence, from (1) we see that v_f must cancel the zero- and negative-sequence components of v_t. In addition, the positive sequence component of v_f must be chosen such that the load voltage is regulated at a prespecified value.

Since the DVR must operate in zero power mode, we get the following relation from Fig. 1:

$$p_{lav} = p_{tav} = v_{ta}i_{sa} + v_{tb}i_{sb} + v_{tc}i_{sc} \tag{2}$$

where p_{tav} is the average value of the instantaneous power (p_t) entering the terminal and p_{lav} is the instantaneous power (p_l) supplied to the load. Let us denote the phasor load voltage as $\boldsymbol{V_l} = |V_l|\angle\theta$, where $|V_l|$ is a prespecified magnitude and θ is an unknown angle to be computed. Note that since the load voltage is strictly positive sequence, the average power to the load is also positive sequence. We then get

$$p_{lav} = |V_l|\,|I_{l1}|\cos(\theta - \phi) \tag{3}$$

where $|I_{l1}|\angle -\phi$ is the phasor positive sequence component of the load current.

Combining (2) and (3) we get

$$\theta = \cos^{-1}\left(\frac{p_{tav}}{|V_l|\,|I_{l1}|}\right) + \phi. \tag{4}$$

Among the quantities on the right-hand side of (4), $|V_l|$ is known, p_{tav} can be calculated from the instantaneous measurements of terminal voltage and load current using half-cycle averaging. The rms phasor positive-sequence component of the load current (or terminal voltage) can be extracted from the sampled values of the load current (or terminal voltage), which may contain harmonics, using the procedure given in [9]. Denoting the zero, positive, and negative phasors by the subscripts 0, 1, and 2, respectively, these components are given by

$$\begin{bmatrix} \boldsymbol{I_{l0}} \\ \boldsymbol{I_{l1}} \\ \boldsymbol{I_{l2}} \end{bmatrix} = \frac{\sqrt{2}}{T\sqrt{3}} \int_t^{t+T} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix} e^{-j(\omega t - 90^\circ)} dt \tag{5}$$

where $a = e^{j120^\circ}$ and T are the integration interval that is chosen as half a cycle to eliminate all harmonic components.

Once θ is obtained from (4), the reference phasor sequence components of the DVR voltages are obtained from (1) as

$$\boldsymbol{V_{f0}^*} = -\boldsymbol{V_{t0}}, \boldsymbol{V_{f1}^*} = |V_l|\angle\theta - \boldsymbol{V_{t1}} \text{ and } \boldsymbol{V_{f2}^*} = -\boldsymbol{V_{t2}}. \tag{6}$$

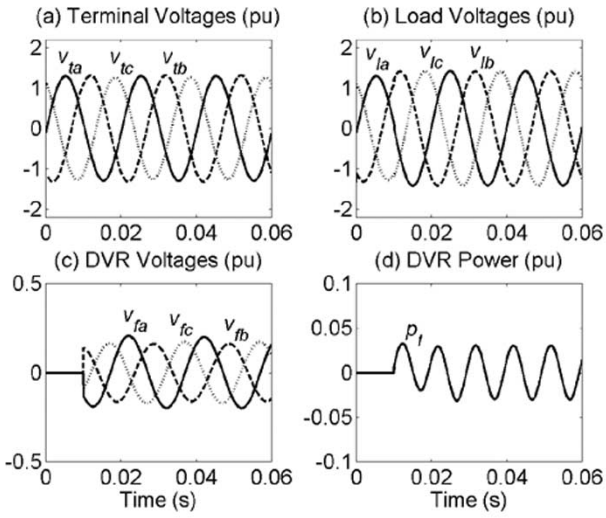

Fig. 2. System response with unbalanced load and ideal DVR.

TABLE I
SYSTEM PARAMETERS

System quantities	Values
System Frequency	50 Hz
Feeder impedance	$0.05 + j0.3$ per unit
Load impedance	
Phase-a	$2.0 + j1.5$ per unit
Phase-b	$2.5 + j2.0$ per unit
Phase-c	$1.0 + j2.5$ per unit
Desired load voltage $\|V_l\|$	1.0 per unit

An inverse symmetrical component transformation of (6) will then produce the reference phasor voltages of the DVR. The instantaneous phase voltages then can be obtained from the phasor voltages. Note that the entire operation is synchronized with an arbitrary phase reference.

III. NUMERICAL RESULTS WITH IDEAL DVR

In this section, we shall present numerical results with an ideal DVR. It means that the DVR is realized by an ideal voltage source that follows the reference voltage generated by (6) accurately. The system parameters chosen for the simulation studies are given in Table I. We shall demonstrate the functioning of the DVR with the help of the following examples.

A. Example 1

In this example, we assume that the source voltage is 1.0 p.u. rms (i.e., $\sqrt{2}$ per unit peak) and balanced. The system response is shown in Fig. 2. In this, the compensator is connected at the end of the first half cycle (10 ms) after the integration (5) is performed through moving average. It can be seen that the load voltages become balanced almost as soon as the compensator is connected. The DVR power ($p_f = v_{fa}i_{sa} + v_{fb}i_{sb} + v_{fc}i_{sc}$) shown in Fig. 2(d) is oscillating with a mean of zero. ΔΔΔ

B. Example 2

We now introduce a nonlinear load that draws a 120° square-wave current with a peak of 0.35 p.u. in addition to the unbalanced load given in Table I. To accommodate this load, we have

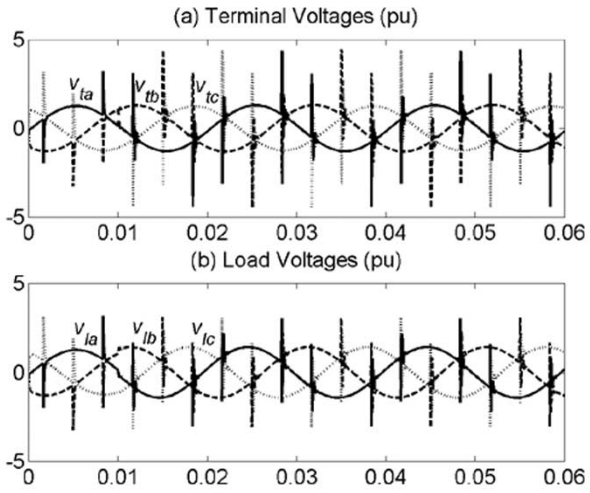

Fig. 3. System response with unbalanced and distorted load and ideal DVR.

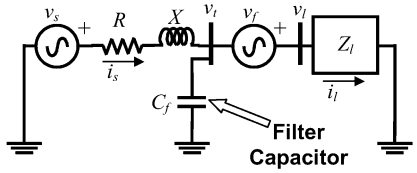

Fig. 4. Modified compensator structure with filter capacitor.

to modify the reference algorithm. The harmonic in the load current will distort the terminal voltage. Since the DVR only cancels the zero and negative sequences, the harmonic component of the terminal voltage will be passed on to the load voltage. To avoid this, we can separate the terminal voltage as

$$v_t = v_{tf} + v_{th} \tag{7}$$

where v_{tf} is the fundamental component and v_{th} is the harmonic component of the terminal voltage. The fundamental component can be obtained using the same procedure as given in (5) and the harmonic component can be obtained by subtracting the fundamental component from the actual signals. The desired DVR voltage is then given by

$$v_f^* = v_{ff}^* - v_{th} \tag{8}$$

where v_{ff}^* is the instantaneous values obtained from (6), after inverse transform.

The system response is shown in Fig. 3 in which the terminal and load voltages are shown. It can be seen that these contain high-frequency harmonics and spikes due to discontinuous changes in the load. The magnitudes of the spikes are unacceptable. We must therefore provide a low impedance path for these high-frequency harmonic currents to flow. To accomplish this, we connect a filter capacitor in shunt at the PCC. The single line diagram of this configuration is shown in Fig. 4 in which the filter capacitor is denoted by C_f. Note that the terminal or PCC voltage (v_t) is the voltage across C_f. Also note that the source current (i_s) is no longer equal to the load current (i_l).

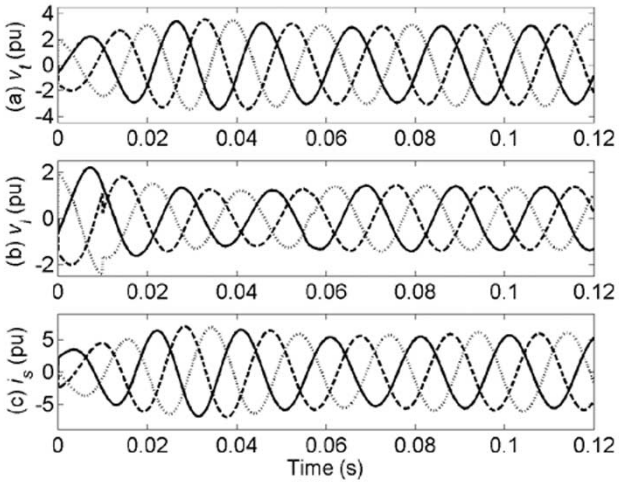

Fig. 5. System response with ideal DVR for $X_{cf} = 0.5$ per unit.

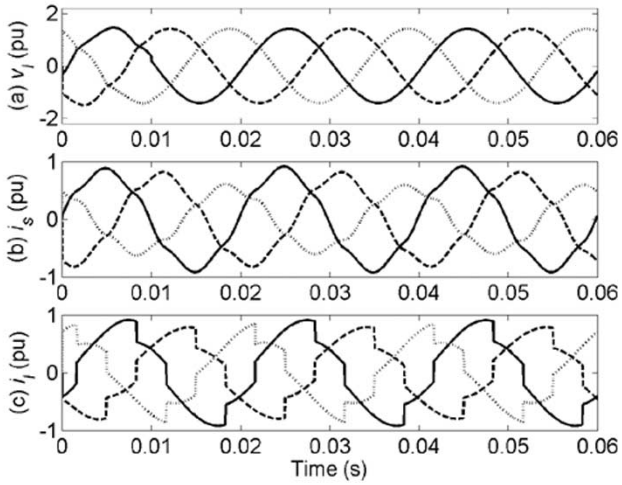

Fig. 6. System response with ideal DVR for $X_{cf} = 3.0$ per unit.

The choice of the value of C_f is very crucial. To illustrate this, we have chosen two different values of C_f. These are given by

$$X_{cf} = \frac{1}{\omega C_f} = 0.5 \text{ per unit and } 3.0 \text{ per unit.}$$

The results with X_{cf} of 0.5 p.u. are shown in Fig. 5. It can be seen that due to the large value of capacitance, the load voltage settles after five cycles (0.1 s). Furthermore, the peak of the terminal voltages and source currents is excessively high. In fact, the peak of the source current is about 6 p.u., which clearly is totally undesirable. The results with X_{cf} of 3.0 p.u. are shown in Fig. 6. It can be seen that the load voltage settles within one cycle of the connection of the DVR at 0.01 s. Also, the peak of the source current is comparable to that of the load current. We shall therefore choose this value of X_{cf} in all our further studies as a compromise between high current and inadequate filtering. $\Delta\Delta\Delta$

C. Example 3

For the same system of example 2, let us assume that the source voltage is unbalanced as well as distorted. The peak of the fundamental component of the source voltages are $\sqrt{2}$,

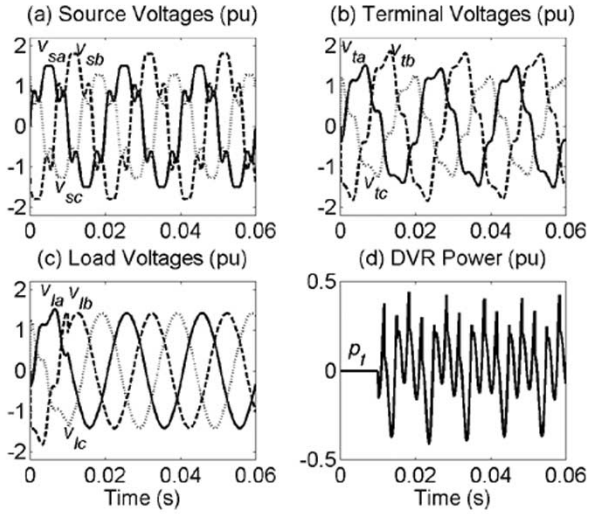

Fig. 7. System response with ideal DVR when both source and load are unbalanced and distorted.

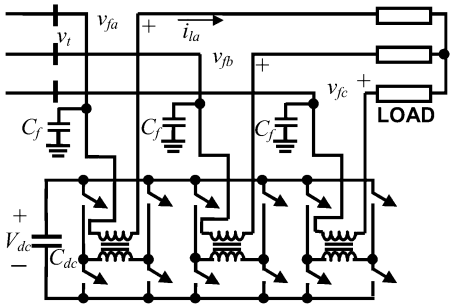

Fig. 8. Schematic diagram of the DVR with capacitor filter.

$1.2\times\sqrt{2}$ and $0.85\times\sqrt{2}$ for phases a, b, and c, respectively. In addition, each phase voltage contains fifth and seventh harmonics with their magnitudes being inversely proportional to their harmonic number. The system response with DVR for the unbalanced and distorted load mentioned above is shown in Fig. 7. It can be seen that DVR performs as expected with the DVR power being zero-mean. $\Delta\Delta\Delta$

From the above examples, we conclude that ideal DVR configuration of Fig. 4 is capable of nullifying the poor quality of source. The implementation of DVR is discussed next.

IV. DVR Structure

The DVR structure is shown in Fig. 8. It contains three H-bridge inverters that are connected to a common dc storage capacitor (C_{dc}). The voltage V_{dc} across this capacitor is the dc supply voltage input to the inverters. The output of each inverter is connected to a single-phase transformer. The outputs of the three transformers are then connected in series to the three phases of the distribution feeder.

The single-phase equivalent circuit of the DVR of Fig. 8 is shown in Fig. 9. In this, L_d represents the leakage reactance of the transformer and R_d represents the losses in the inverter circuit. The term $u \cdot V_{dc}$ represents the inverter output voltage where V_{dc} is the voltage across the dc capacitor and $u = \pm 1$ is the switching function. From Fig. 9, we get the following equation:

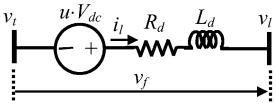

Fig. 9. Single-phase equivalent circuit of the DVR of Fig. 8.

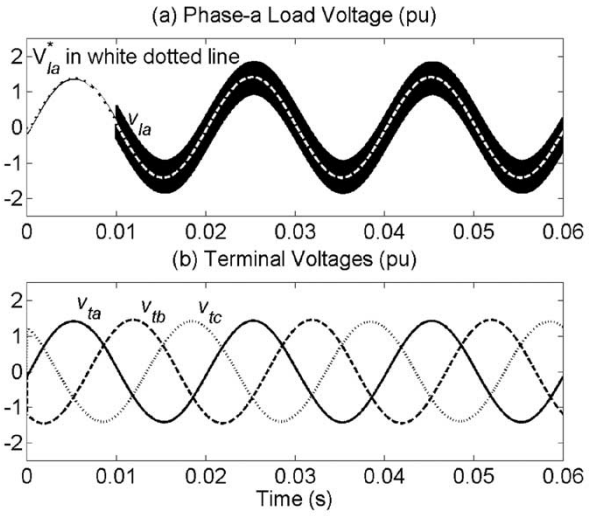

Fig. 10. Compensation using the DVR structure of Fig. 8.

$$v_f = u \cdot V_{dc} - R_d i_l - L_d \frac{di_l}{dt}. \tag{9}$$

Let us assume that R_d is negligible and L_d is small. Then, $u \cdot V_{dc}$ will be the dominant term on the right-hand side of (9). Therefore, to increase v_f, we choose $u = +1$ and to decrease it, we choose $u = -1$. This gives the following switching law:

$$u = \begin{cases} -1 & \text{for } v_f - v_f^* \geq h \\ +1 & \text{for } v_f - v_f^* < -h \end{cases} \tag{10}$$

where $2h$ is the width of a hysteresis band.

A. Example 4

Let us consider the same system as in Example 2 except that the unbalanced load is harmonic free. We assume that the three inverters are supplied by a dc source with a magnitude of 0.5 p.u. The DVR parameters are chosen as

$$R_d = 0 \text{ per unit and } X_d = \omega L_d = 0.1 \text{ per unit}$$

with the value of X_{cf} being 3.0 p.u. The phase-a of the load voltage is shown in Fig. 10(a) along with its reference value (shown in the white dotted line). Here, the reference (i.e., ideal) load voltage is given by

$$v_l^* = v_t + v_f^*. \tag{11}$$

It can be seen that the load voltage contains very high frequency switching components around the ideal value. The terminal

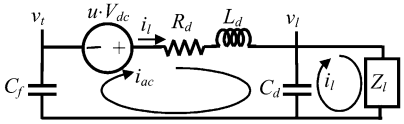

Fig. 11. Single-phase equivalent circuit of the DVR with filter connected in shunt with the load.

voltage is, however, not affected by the switching frequency harmonics. This is evident from Fig. 10(b). ΔΔΔ

Clearly, the configuration of Fig. 8 is unacceptable due to the presence of switching components in the load voltage. We must therefore provide a path for these harmonic components to flow. A possible configuration is shown in Fig. 11 in which a capacitor (C_d) is connected in parallel to the load. This capacitor provides a path for the switch frequency harmonic components to flow. Note that the load voltage v_l is also the voltage across the capacitor C_d. We shall now use a deadbeat output feedback controller [9] to track the reference load voltage given by (11).

Consider the equivalent circuit of Fig. 11. Defining a state vector $x^T = [v_l \quad i_{ac}]$, the state space equation of the system is

$$\dot{x} = Ax + Bz \tag{12}$$

where

$$A = \begin{bmatrix} 0 & \frac{1}{C_d} \\ -\frac{1}{L_d} & -\frac{R_d}{L_d} \end{bmatrix},\ B = \begin{bmatrix} 0 & -\frac{1}{C_d} & 0 \\ \frac{V_{dc}}{L_d} & 0 & \frac{1}{L_d} \end{bmatrix}$$
$$\text{and } z^T = [u_c \quad i_l \quad v_t].$$

Note that in the above equation, i_l and v_t are assumed as forcing functions and the switching function u is considered as a continuous variable u_c. The purpose of the deadbeat controller is to determine u_c.

Discretization of (12) results in the following equation:

$$x(k+1) = Fx(k) + Gz(k) = \begin{bmatrix} f_{11} & f_{12} \\ f_{21} & f_{22} \end{bmatrix} x(k) + \begin{bmatrix} g_{11} & g_{12} & g_{13} \\ g_{21} & g_{22} & g_{23} \end{bmatrix} z(k) \tag{13}$$

where the matrices F and G are given by

$$F = e^{A\Delta T} \text{ and } G = \int_0^{\Delta T} e^{At} B dt.$$

ΔT being the sampling time. From (13), the load voltage equation is given as

$$v_l(k+1) = f_{11}v_l(k) + f_{12}i_{ac}(k) + g_{11}u_c(k) + g_{12}i_l(k) + g_{13}v_t(k). \tag{14}$$

In deadbeat control, a cost function of the form

$$J = \{v_l(k+1) - v_l^*(k+1)\}^2 \tag{15}$$

is chosen and minimized with respect to $u_c(k)$. This gives the following control law [9]:

$$u_c(k) = \frac{1}{g_{11}}[v_l^*(k+1) - f_{11}v_l(k) - f_{12}i_{ac}(k) - g_{12}i_l(k) - g_{13}v_t(k)]. \tag{16}$$

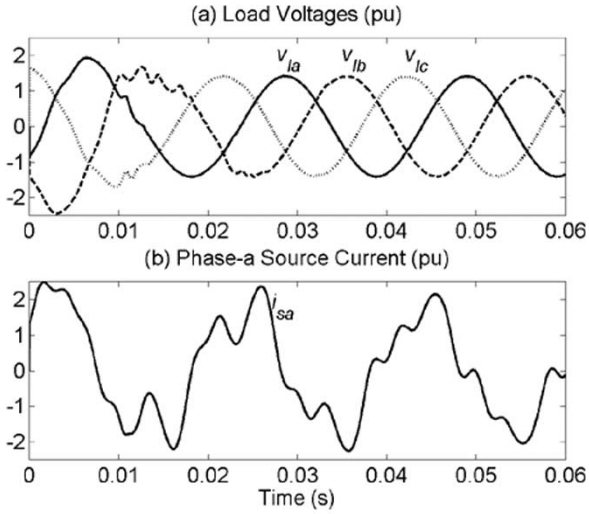

Fig. 12. System response with the DVR structure of Fig. 11 for $X_{cd} = 1.0$ per unit.

With the value of u_c computed above, the switching law is given by [9]

$$u = \begin{cases} +1 & \text{for } u_c \geq 0 \\ -1 & \text{for } u_c < 0 \end{cases}. \tag{17}$$

B. Example 5

Let us consider the same system as given in example 3 where both load and source are unbalanced and distorted. It is assumed that the inverters are supplied by a dc source with a magnitude of 1.5 p.u. The DVR and filter parameters are chosen as

$$R_d = 0.15 \text{ per unit},\ X_d = \omega L_d = 0.1 \text{ per unit and } X_{cd} = \frac{1}{\omega C_d} = 1.0 \text{ per unit}.$$

The value of X_{cf} remains the same as before. The system response with the deadbeat controller is shown in Fig. 12. It can be seen from Fig. 12(a), that the load voltages become balanced sinusoids once the DVR is connected. However, the magnitude of the source current becomes high. The peak of the phase-a source current is over 2.0 p.u. in the steady state as shown in Fig. 12(b). This is clearly unacceptable.

To check whether a suitable value of X_{cd} exists, further studies are performed with $X_{cd} = 0.75$ and 5.0 p.u. The waveforms of load voltage and phase-a source current are shown in Fig. 13. It can be seen that the lower value of X_{cd} improves load voltage waveform but increases the current drawn from the source, while the reverse effect is seen with the higher value of X_{cd}. Thus, no suitable value of X_{cd} can be found for the structure of Fig. 11. Furthermore, the use of capacitor in parallel with the load makes the choice of X_{cd} load sensitive. Therefore, we shall not advocate this configuration. ΔΔΔ

We now investigate an alternate DVR structure in which the filter capacitor (C_d) is connected in parallel with the DVR [7]. This is shown in Fig. 14. In this, the voltage v_f is the voltage across the filter capacitor C_d. Defining a state variable as $x^T =$

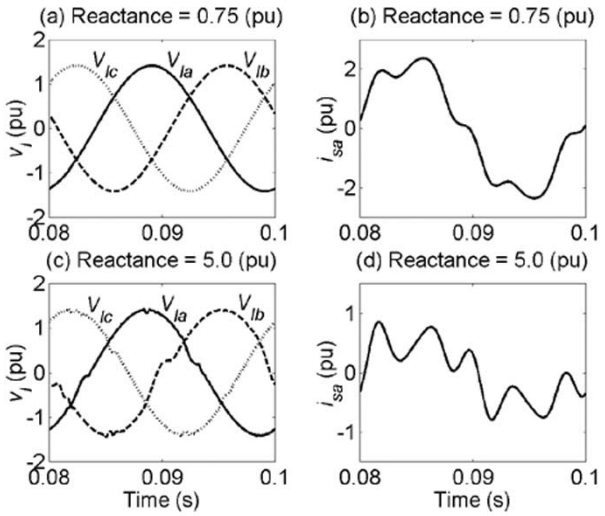

Fig. 13. Steady-state response with the DVR structure of Fig. 11 for $X_{cd} = 0.75$ and 5.0 p.u.

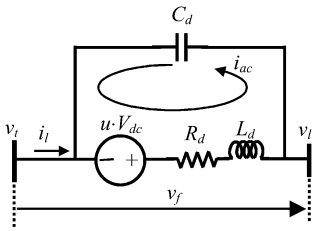

Fig. 14. Single-phase equivalent circuit of the DVR with filter capacitor connected in shunt with the DVR.

$[v_f \quad i_{ac}]$, we can write the state space equation of the system of the form (12) where

$$A = \begin{bmatrix} 0 & \frac{1}{C_d} \\ -\frac{1}{L_d} & -\frac{R_d}{L_d} \end{bmatrix},\ B = \begin{bmatrix} 0 & -\frac{1}{C_d} \\ \frac{V_{dc}}{L_d} & 0 \end{bmatrix}$$
$$\text{and } z^T = [u_c \quad i_l]. \tag{18}$$

In (18), the load current is a forcing function along with u_c. The deadbeat performance index is then

$$J = \left\{v_f(k+1) - v_f^*(k+1)\right\}^2. \tag{19}$$

The resulting control equation is similar to the one given in (16) [7] and the switching law is then given by (17).

C. Example 6

In this example, we consider the system of example 3. The DVR (Fig. 14) parameters of R_d and X_d are as given in example 5 while X_{cd} is chosen as 1.0 p.u. The inverters are supplied by a dc source of magnitude 1.5 p.u. The results are shown in Fig. 15. It can be seen that the peak of the phase-a source current has reduced considerably compared to that shown in Fig. 12(b) and it is now around 1.0 p.u.

To check whether the value of X_{cd} of 1.0 p.u. is optimum, further studies are performed with $X_{cd} = 0.75$ and 5.0 p.u. The waveforms of load voltage and phase-a capacitor current (i_{ac} of Fig. 14) are shown in Fig. 16. It can be seen that for the lower value of X_{cd}, the capacitor current is high, while this current reduces with the increase in the value of X_{cd}. The load voltage,

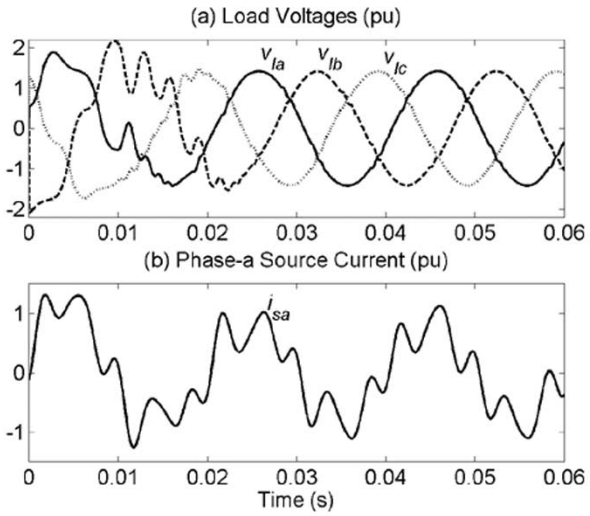

Fig. 15. System response with the DVR structure of Fig. 14.

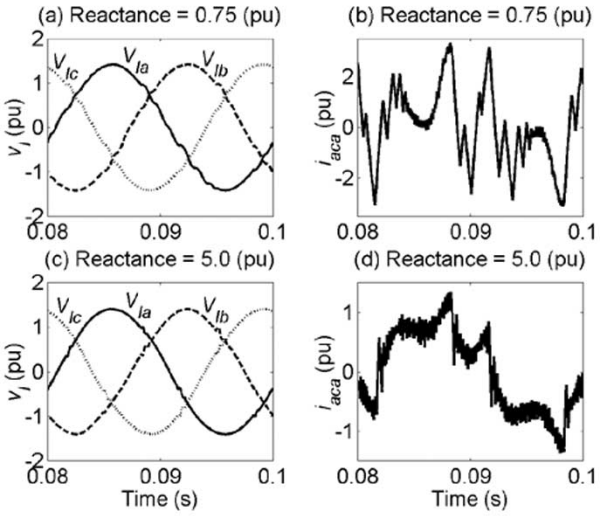

Fig. 16. Steady-state response with the DVR structure of Fig. 14 for $X_{cd} = 0.75$ and 5.0 p.u.

however, is distorted in both cases. In effect, reduction in the value of X_{cd} shorts the DVR, while large value of X_{cd} makes the filtering inadequate. ΔΔΔ

Therefore, we find that the structure of Fig. 14 with X_{cd} of 1.0 p.u. is the best among the three DVR structures discussed. We shall now design the dc capacitor control loop for this structure.

V. DC Capacitor Control

In Examples 4–6 we have assumed that the inverters are supplied by a dc source rather than a dc storage capacitor. In this section, we shall remove this assumption. The dc capacitor must operate in such a way that the voltage across it is maintained constant. To accomplish this, we use a proportional plus integral controller of the form

$$p_{loss} = K_P(V_{ref} - V_{dcav}) + K_I \int (V_{ref} - V_{dcav})\, dt \tag{20}$$

where V_{dcav} is the average of the dc capacitor voltage over a cycle and V_{ref} is a reference value. Note that the dc capacitor

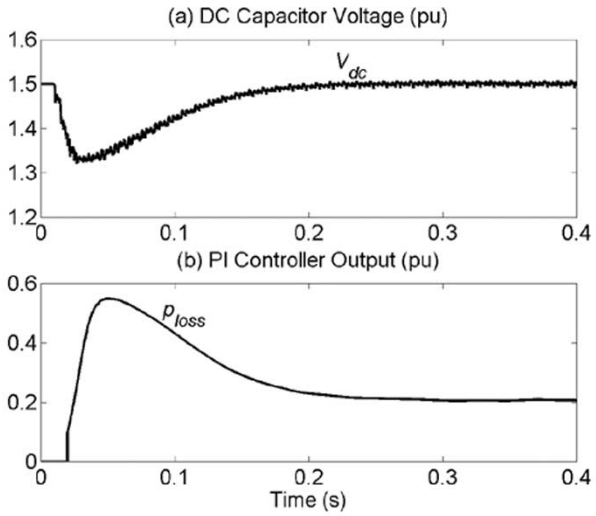

Fig. 17. Performance of the dc capacitor controller.

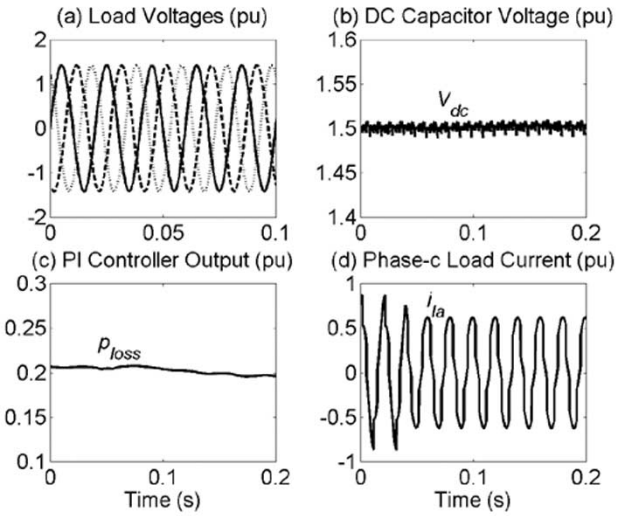

Fig. 18. Performance during load change.

voltage contains the switching frequency ripple. Therefore, its measurements are smoothed by the averaging process. Here, we can use a moving average filter which, at any given time, averages the measurements of the last one cycle.

Note that a drop/rise in the dc capacitor voltage indicates a real power supply/absorption by the capacitor. Therefore, p_{loss} in (20) defines the power loss in the inverter circuit. Since the loss can only be supplied by the ac system, we must modify the reference generation scheme to accommodate p_{loss}. Note from Fig. 1 that the average of the power supplied to the load p_{lav} is equal to the difference of the average power entering the terminal p_{tav} and the power consumed by the DVR, which is p_{loss}. Therefore, we can modify (3) as

$$p_{tav} - p_{loss} = |V_l|\,|I_{l1}|\,cos\,(\theta - \phi)\,. \tag{21}$$

The remaining equations remain unaltered. The following example demonstrates the dc capacitor control function.

A. Example 7

For this example, we consider the system of example 6 with $X_{cd} = 1.0\ \text{per unit}$. The dc capacitor value must be so chosen that it can ride through any transient without substantial fall or rise in the voltage during this period. For this simulation, we have chosen a capacitor, the reactance of which has a per unit value of 0.0318 at the system frequency of 50 Hz. It is assumed that the capacitor is precharged such that its voltage has a value of 1.5 p.u. before the compensator is connected. The PI controller parameters are chosen as

$$K_P = 3 \text{ and } K_I = 15.$$

It is assumed that the control loop is activated at the end of the first half cycle (0.01 s) along with the DVR. The dc capacitor voltage and the PI controller output are shown in Fig. 17. It can be seen that the V_{dc} drops as soon as the DVR is connected as it momentarily needs to supply power to the system. However, the PI controller brings it back to steady state within about ten cycles (0.2 s). Moreover, since the dc capacitor voltage does not drop significantly during the transient, the load voltages remain balanced. ΔΔΔ

VI. Performance Evaluation

The DVR with capacitor control loop incorporated is tested for various disturbance conditions. The results are discussed in this section in which we shall consider the same system and parameters as in example 7.

A. Performance During Load Change

With the system operating in the steady state, the RL load of phases a and c are changed suddenly at the end of the second cycle. These parameters are changed to $1.0 + j2.5\ \text{per unit}$ in phase-a and $5.0 + j1.5\ \text{per unit}$ in phase-c. The phase-b RL load and the nonlinear load remain unchanged. The system response is shown in Fig. 18. It can be seen that the load change has no significant impact on the system performance even though the magnitude of the phase-c load current has reduced considerably.

B. Performance During Voltage Sag

With the system operating in the steady state for two cycles, an eight-cycle sag occurs in which all phases of the supply voltage drop to 0.85 times their nominal values. The sag is cleared after ten cycles when the nominal supply voltages are restored. The system response is shown in Fig. 19. It can be seen that during the sag, p_{loss} reduces and, consequently, V_{dc} increases. However, they return to their nominal values after the nominal voltages are restored. Moreover, the sag and the voltage recovery have no impact on the load voltages as they are maintained during the entire period.

C. Performance Limits

When a deep voltage sag occurs, the DVR may fail to maintain the load voltage to the prespecified value. Since the negative and zero sequences of the DVR voltage only cancel the

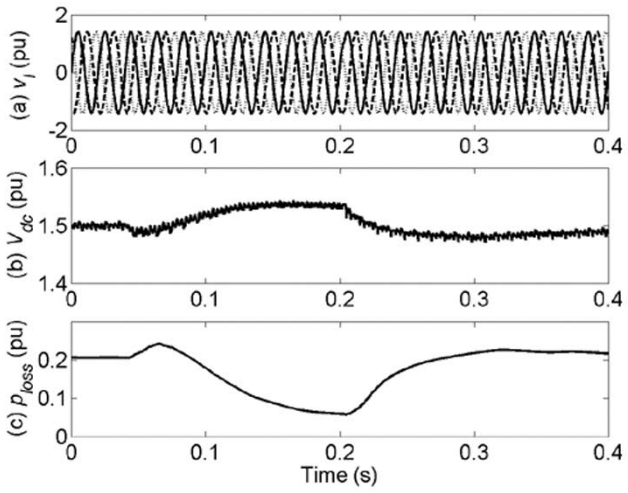

Fig. 19. Performance during 85% voltage sag.

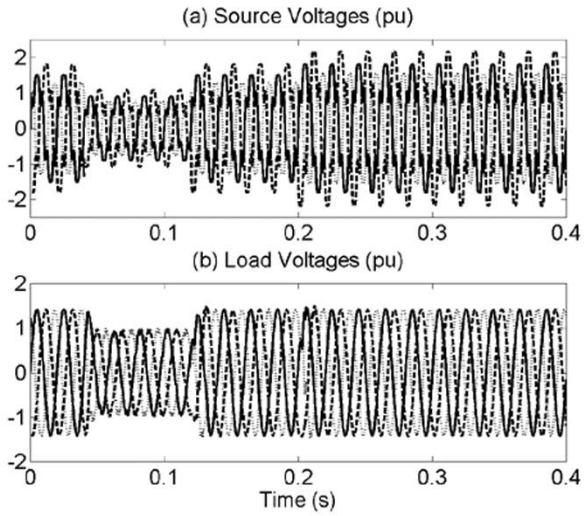

Fig. 20. Source and load voltages during voltage sag and swell.

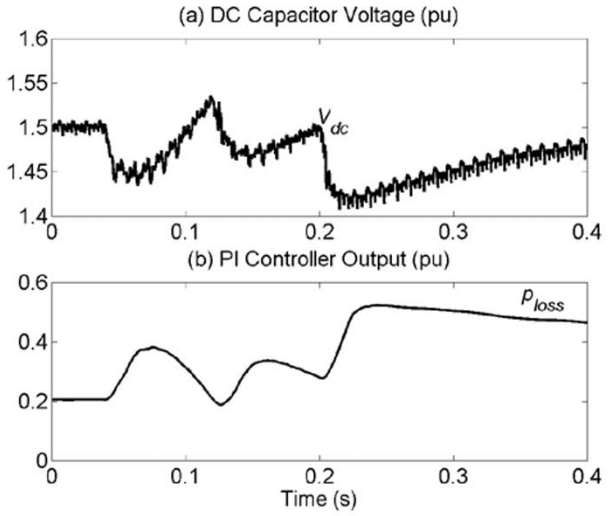

Fig. 21. DC voltage and controller output during voltage sag and swell.

corresponding sequences of the terminal voltage, it is the positive sequence that creates a problem. Let us consider the phasor relationship between the positive sequence voltages

$$\boldsymbol{V_{t_1}} + |V_{f1}|\,(a + jb) = \boldsymbol{V_l} \tag{22}$$

where $a+jb$ is a unit vector that leads the positive-sequence load current $\boldsymbol{I_{l_1}}$ by 90°. This implies that the positive sequence of the DVR voltage leads that of the load current by 90° and, hence, the real power flowing through this sequence is zero. Assuming $\boldsymbol{V_l} = |V_l|\angle 0°$ (22), results in the following quadratic [9]:

$$|V_{f1}|^2 - 2a\,|V_l|\,|V_{f1}| + |V_l|^2 - |V_{t1}|^2 = 0. \tag{23}$$

The above quadratic must have two real solutions of $|V_{f1}|$ for an achievable target load voltage. In case of a complex conjugate pair of roots, the target load voltage is not achievable and its magnitude must be reduced. From (23), $|V_{f1}|$ will have two real identical solutions when the following condition is true [9]:

$$|V_l| = \frac{|V_{t1}|}{\sqrt{1-a^2}}. \tag{24}$$

Equation (24) gives the maximum achievable target load voltage for a voltage sag. Note that a can be calculated from the angle of $\boldsymbol{I_{l_1}}$ given by (5).

With the system operating in the steady state, a voltage sag occurs after two cycles in all three phases of the source voltages in which their magnitudes are reduced to 60% of their nominal values. The source voltages are restored to their nominal values after six cycles. Then a voltage swell occurs after ten cycles in which the magnitudes of the source voltages increase to 1.2 times their nominal values. This voltage swell condition persists for a long time. The source voltages are shown in Fig. 20(a).

The DVR is operated with the voltage limit given by (24). The reference voltage is fixed at this limit if the quadratic (23) fails to produce two real roots. The resulting load voltages are shown in Fig. 20(b). It can be seen that the load voltage reduces during the sag. However, these voltages are unaffected by the voltage swell.

The dc capacitor voltage and PI controller output are shown in Fig. 21. It can be seen that dc capacitor voltage tries to recover once the sag is cleared. Furthermore, it also comes back to its steady state value of 1.5 p.u. during the persistent voltage swell. During the voltage swell, the loss in the inverter increases as the RL load now draws more power. This is evident from Fig. 21(b).

VII. Conclusion

This paper discusses the operating principles, structure, and control of a DVR that is supplied by a dc capacitor. It has been shown that when the load is nonlinear, even an ideal DVR may not be able to suppress voltage spikes unless a low impedance path from the PCC to ground is provided through a shunt capacitor. Three different configurations are analyzed. It is shown that the DVR with a capacitor connected in shunt with it gives the best performance. It has been shown that the success of the DVR depends on the choice of these two capacitors. Their values must be chosen judiciously as discussed in the paper. Furthermore,

the value of the dc capacitor also plays an important role. This value is chosen such that the DVR can ride through and provide voltage support during transients.

The DVR algorithms discussed in [7] and [8] are valid only for systems with balanced and linear loads. Since the proposed algorithm can handle more general types of load, the algorithms of [7] and [8] are subsets of the proposed algorithm.

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