DESIGN OF A CMOS BANDGAP REFERENCE WITH LOWTEMPERATURE COEFFICIENT AND HIGH POWER SUPPLY REJECTION PERFORMANCE

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ABSTRACT

A high precision temperature compensated CMOS bandgap reference is presented. The proposed circuit employs current-mode architecture that improves the temperature stability of the output reference voltage as well as the power supply rejection when compared to the conventional voltage-mode bandgap referenc. Using only first order compensation the new architecture can generate an output reference voltage of 550mV with a peak-to-peak variation of 400µV over a wide temperature range from -25°C to +100°C which corresponds to a temperature coefficient of 5.8ppm/°C. The output reference voltage exhibits a variation of 2.4mV for supply voltage ranging from 1.6V to 2.0V at typical process corner. A differential cascaded three-stage operational amplifier is included in the bandgap circuit to improve the power supply rejection of the BGR. Simulation result shows that the power supply rejection ratio of the proposed circuit is 79dB from DC up to 1kHz of frequency. The proposed bandgap reference is implemented using UMC 0.18µm CMOS process and it occupies an active layout area of 0.14mm^2.

KEYWORDS

BGR, Temperature coefficient, PSRR.

1. INTRODUCTION

Bandgap reference (BGR) is an important building block which is required in many analog and mixed-signal systems such as communication systems and data acquisition systems, as well as some digital systems such as dynamic random access memories (DRAMs). A voltage reference circuit must be, inherently, well-defined and insensitive to temperature, power supply and load variations. The accuracy of high performance analog circuits such as A/D and D/A converters, filters etc. are often limited by the precision of their reference voltage over the circuit's operating temperature range. Therefore, a good bandgap reference circuit is required to have a high power supply rejection ratio (PSRR) and a very low temperature coefficient (TC) over a large temperature range. Recently, different techniques have been proposed to design precise voltage references at low supply voltages which is in great demand in low-voltage battery-operated

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portable devices and systems. In order to reduce the temperature coefficient, several compensation schemes i.e. quadratic temperature compensation [1], exponential temperature compensation [2] and piece-wise linear temperature compensation [3] have been reported. Other than this, PSRR improvement is another challenge for a BGR [4].

In this paper, a bandgap reference with very high temperature-stabilty and high PSRR performance is proposed. Conventional BGR architecture [5] employs voltage-mode to produce a stable voltage reference. The proposed architecture incorporates current-mode operation, where two currents having complementary type TC are added to generate a temperature independent current and thereby, producing a temperature independent voltage reference. Compared to the traditional BGR circuit , the proposed circuit can produce reference voltages less than 1.2V to meet the requirements of designs under low supply voltages. With the help of resistors and bipolar transistors, the proposed circuit can produce a very low TC of V_{ref} with only first-order temperature compensation. As there are no high-order curvature compensations employed, the structure of proposed circuit greatly reduces the circuit complexity. Compared to the traditional BGR circuit that uses a two-stage operational amplifier, the proposed circuit employs a differential cascaded three-stage operational amplifier [6] to get higher gain to improve PSRR of the BGR. At the same time, the Miller compensation technique is incorporated in the opamp circuit to improve the stability of the circuit.

2. CONVENTIONAL BGR PRINCIPLE

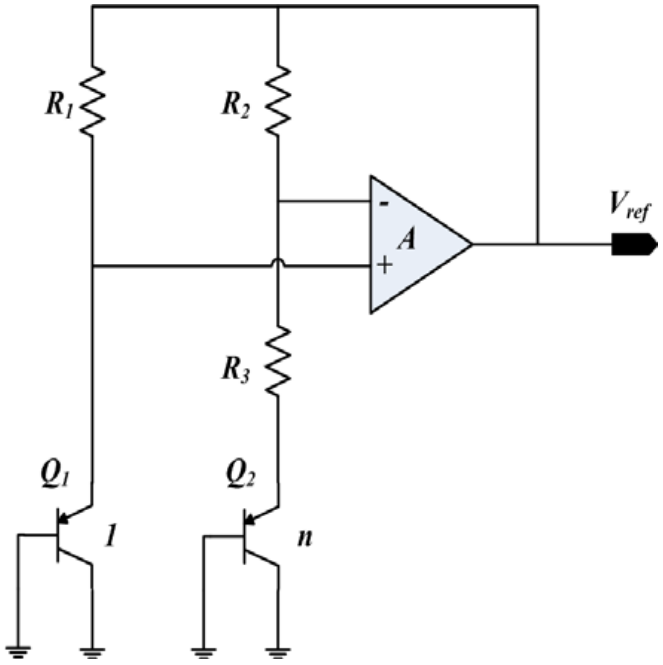

Figure 1. Conventional BGR architecture

Figure 1 shows a conventional voltage-mode BGR architecture [5]. The basic idea of BGR in CMOS technology is to add a proportional to absolute temperature (PTAT) voltage to the base-emitter voltage (V_{EB}) of a bipolar transistor, so that the first-order temperature dependency in V_{EB}

is compensated by the PTAT voltage, resulting in a nearly temperature-independent output voltage. Typical output voltage of BGR is about 1.2 V at room temperature, which is close to the bandgap voltage of silicon. The difference between the base-emitter voltages (ΔV_{EB}) of two bipolar transistors has a positive temperature coefficient (positive TC) and, therefore, can be treated as a PTAT voltage. On the other hand, the base-emitter voltage of a single bipolar transistor (V_{EB}) can act as a negative TC voltage.

For a bipolar device the collector current is given by,

$$I_C = I_S \left| . e^{V_{EB}/V_T} \right.$$

$$\Rightarrow V_{EB} = V_T ln(\frac{I_C}{I_S}) \quad (1)$$

Where, V_T =Thermal voltage= kT/q, and

I_S =The saturation current= $bT^{4+m}e^{\frac{-E_g}{kT}}$, ($b$ is a proportionality factor and m is a material (Si) constant related to electron mobility in it).

Therefore, the negative TC can be given as,

$$\frac{\delta V_{EB}}{\delta T} = \frac{V_{EB} - (4+m)V_T - E_g/q}{T} \quad (2)$$

(*Assuming I_C to be constant*)

$$\frac{\delta V_{EB}}{\delta T} = \frac{V_{EB} - (3+m)V_T - E_g/q}{T} \quad (3)$$

(*Assuming I_C to be a function of temperature*)

While, the postive TC can be found as,

$$\Delta V_{EB} = V_{EB1} - V_{EB2} = V_T ln(n)$$

$$\frac{\delta \Delta V_{EB}}{\delta T} = \frac{V_T}{T} ln(n) \quad (4)$$

Now, the BGR reference voltage is described as,

$$V_{ref} = V_{EB} + \frac{R_2}{R_3} \Delta V_{EB} \quad (5)$$

Here, the first term i.e. V_{EB} has a negative temperature coefficient of −2 mV/^{o}C, whereas the second term ΔV_{EB} has a positive temperature coefficient of +0.086 mV/^{o}C. So, proper choice of the resistor ratio (R_2/R_3) gives a reference voltage which has theoretically a zero TC value. Combining eqn (3)-(5), the final temperature coefficient of the reference voltage can be formulated as,

$$\frac{\delta V_{ref}}{\delta T} = \frac{V_{EB} - (3+m)V_T - E_g/q}{T} + \frac{R_2}{R_3}\frac{V_T}{T}ln(n) \quad (6)$$

After imposing the constraint of zero TC i.e. $\frac{\delta V_{ref}}{\delta T} = 0$, the reference voltage of the BGR becomes,

$$V_{ref} = \frac{E_g}{a} + (3+m)V_T \quad (7)$$

Here, E_g=bandgap energy of Si=1.12eV, V_T=25mV at room temperature and m = −3/2 for Si. Putting this values we get $V_{ref} \approx 1.25V$. Thus, the reference voltage of a conventional BGR that exhibits a nominally-zero TC is controlled to be about 1.25V. This limits the range of reference voltage as well as the operational voltage V_{dd} which can not be lowered than 1.25V. Obviously, these limitations are not welcomed in the low-voltage CMOS design.$_TV$

3. PROPOSED BGR PRINCIPLE

The drawbacks of the conventional BGR are overcome in the new architecture. The current-mode operation of the proposed BGR produces a temperature independent current which when passes through a resistor gives a temperature independent voltage. Since, the controlled quantity for the circuit is current, any reference voltage less than 1.2V can easily be generated. Moreover, the supply voltage limitation faced in the conventional voltage-mode circuit is removed in the new current-mode architecture. The details of the architecture are discussed here.

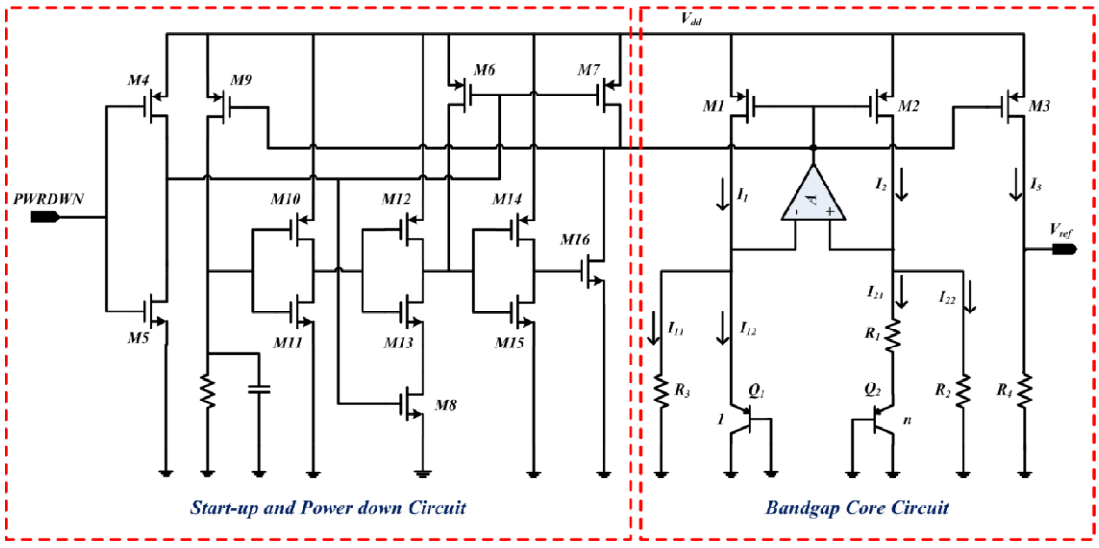

Figure 2: The proposed current-mode BGR architecture

3.1. Core BGR Circuit

Figure 2 shows the core of the proposed bandgap reference circuit. In the circuit, two currents which are proportional to V_{EB} and ΔV_{EB} are generated. The size of the transistors M1-M3 are identical. The gates of the transistors are connected to a common node to provide the current-mirror connection. Therefore, the current through them are same, i.e.

$$I_1 = I_2 = I_3 \tag{7}$$

I_1 and I_2 are further divided into two branches containing resistors and bipolar transistors, as shown in Figure 2. The currents are divided in such a way that,

$$I_{11} = I_{22} \qquad I_{12} = I_{21} \tag{8}$$

Now, to make the voltages at node A and node B equal, the resistors through which I_1 and I_2 are flowing are made to be equal.

$$R_3 = R_2 \tag{9}$$

$$\Rightarrow I_{11}R_3 = I_{22}R_2$$

$$\Rightarrow V_A = V_B$$

The opamp in the circuit is so controlled that the voltages at its two inputs are equalized. From the Figure 2, $V_A = V_{EB1}$. Therefore,

$$I_{22}R_2 = V_B = V_A = V_{EB1} \tag{10}$$

$$\Rightarrow I_{22} = \frac{V_{EB1}}{R_2}$$

And,

$$I_{21}R_1 = V_B - V_{EB2} \tag{11}$$

$$= V_A - V_{EB2}$$

$$= V_{EB1} - V_{EB2} = \Delta V_{EB}$$

$$\Rightarrow I_{21} = \frac{\Delta V_{EB}}{R_1}$$

So, the output reference voltage of the proposed BGR can be obtained as,

$$V_{ref} = R_4 I_3 = R_4 I_2 \qquad (12)$$
$$= R_4 (I_{21} + I_{22})$$
$$= R_4 \left(\frac{\Delta V_{EB}}{R_1} + \frac{V_{EB1}}{R_2}\right)$$

As already known from the conventional BGR operation, V_{EB1} has a negative TC, while ΔV_{EB} has a positive TC. So, V_{ref} becomes almost independent of temperature. But, unlike the conventional BGR, where the temperature-independent voltage is given by the bandgap voltage and some other constant factors, the proposed BGR can produce a range of voltages which are independent of temperature by simply varying the values of resistor R_4. Moreover, V_{ref} is little influenced by the absolute value of the resistors R_1, R_2 or R_4 since it is the resistor ratio that controls V_{ref} (see (12)). It should be noted that the pMOS transistors (M1-M3) are required to operate in the saturation region for proper operation of the circuit. The transistors M4-M6 are added in the circuit as cacode connection to improve the PSRR of the BGR.

3.2. Start-up and Power down circuit

The PWRDWN signal is an active high signal that can switch ON or OFF the whole circuit whenever necessary. When PWRDWN=1, M6 and M7 are ON. Due to M6, the gate of M16 goes LOW and M16 becomes OFF. Since M16 is OFF and M7 is ON, the gates of M1-M2 go HIGH and, thereby, ceases the operation of the core circuit.

The start-up circuit of BGR is composed of M9 - M16. PWRDWN is made low for the circuit to operate properly. When the power is just turned on, no current flows through M1, M2 or M9. So, the drain of the pMOS transistor M9 is initially at LOW voltage which after passing through the transistor network M10-M15 reaches the gate of M16 as a HIGH signal. Thus, M16 becomes ON, which, in turn, switches ON transistors M1-M2. Current starts to flow through M1-M2 and the operation of BGR gets started. Now, this start-up circuit must be switched OFF automatically once the transients of the BGR reference generation are settled. When current starts to flow through M1-M2, M9 also starts to carry the initial current which rises the drain voltage of M9 when it flows through the resistor R_5. When the drain voltage becomes sufficiently HIGH, it switches OFF the nMOS (M16) and thereby, ceases the further operation of the start-up circuit without affecting the core circuit.

3.3. Operational Amplifier

The opamp circuit [6] used in the proposed bandgap reference is a three-staged CMOS amplifier with high gain and CMRR. Sufficient high gain of the opamp improves the PSRR of the BGR. Figure 3 shows the simplified schematic of the amplifier. The first stage (formed by transistors M1-M5) and second stage (formed by transistors M6-M10) are standard differential amplifier stages while the third stage (formed by transistors M11-M12) is a class-A output stage. The Nested-Miller compensation technique is employed for frequency compensation. The compensation resistor R_{C1} is added to improve the stability performance.

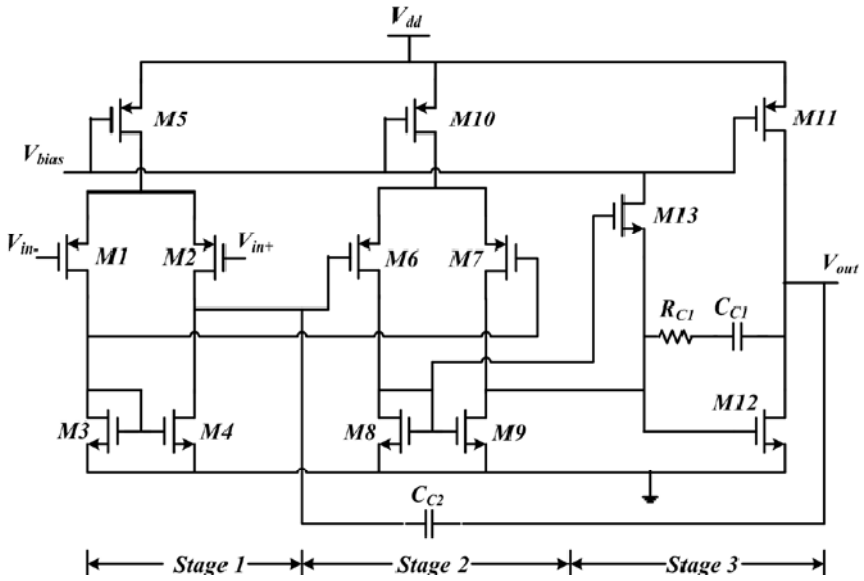

Figure 3: Schmetic of the opamp used in the proposed BGR

4. SIMULATION RESULTS

Simulations have been carried out using a 0.18 µm CMOS technology under the operating voltage of 1.8V and simulation results are obtained by spectre. The operational amplifier used in the proposed BGR circuit gives a gain of 62dB and a phase margin of 80 degree which are enough for this application (see Figure 4).

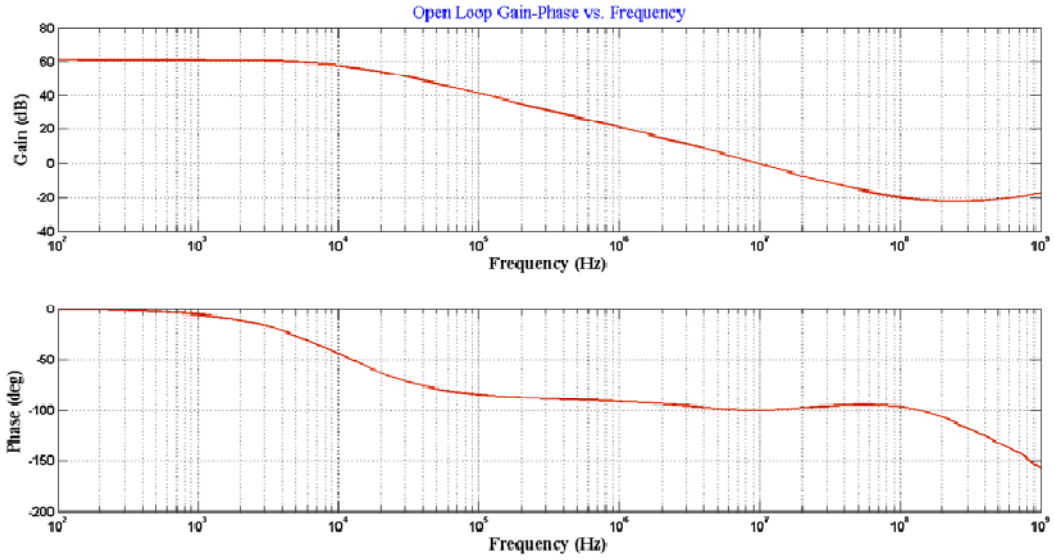

Figure 4: Gain and phase plot of the opamp

Figure 5 shows the simulated output reference voltage (550mV) of the proposed bandgap reference as a function of temperature over the range -25oC to 100°C. The variation of the V_{ref} for different process corners (i.e. typ, fast, slow) are shown in the same figure over the aforesaid temperature range. The curves exhibit a variation of 400 µV, 470 µV and 260 µV for typ, fast and slow corners respectively. The corresponding temperature coefficients are 5.81ppm/°C, 6.84ppm/°C and 3.78ppm/°C respectively.

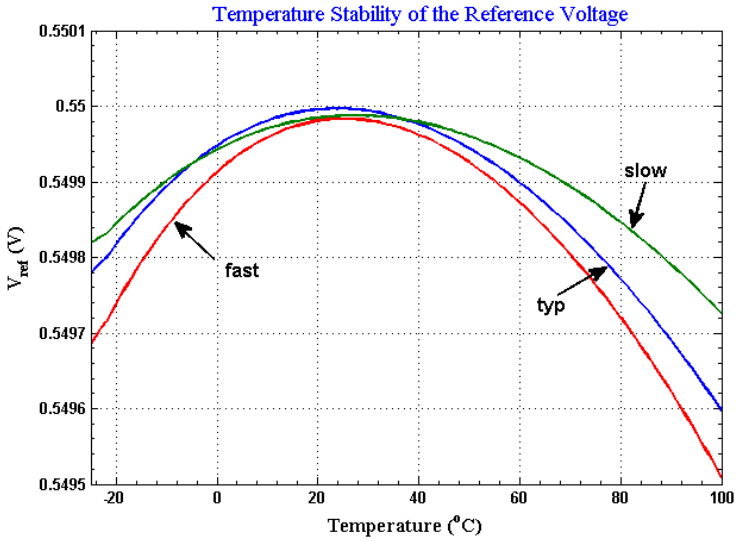

Figure 5: Variation of V_{ref} over different process corners

Time required for the BGR to produce a stable output is ~900ns (typ, 27°C,1.8V). It is found from the transient simulation of the BGR output voltage when the supply voltage V_{dd} is given as a ramp signal. This simulation of the proposed BGR has been carried out for ramp inputs that goes from 0V to V_{dd} within 10nS, 100nS and 500nS and the corresponding output voltage waveforms are shown in Figure 6.

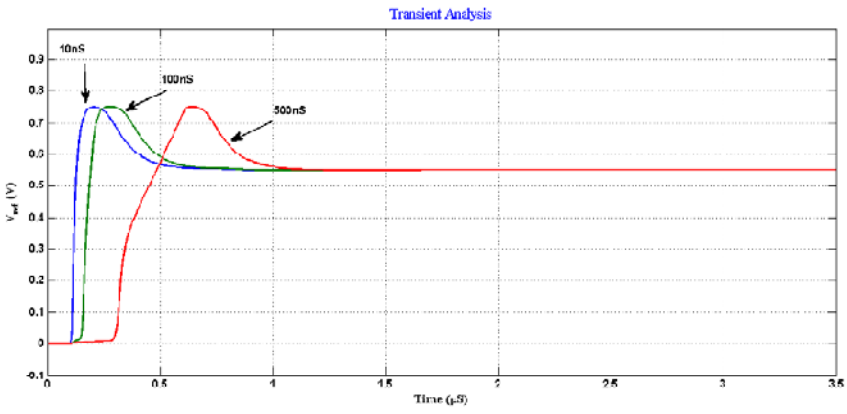

Figure 6: Start-up behaviour of the BGR output voltage with a V_{dd} ramp

Figure 7 shows the output variation with the supply voltage over a range of 1.6V-2.0V. The simulations are performed over all the process corners at 27°C and at 80°C . As seen from the plot, the variation of V_{ref} is within 2.4mV at typical corner at both the temperature point.

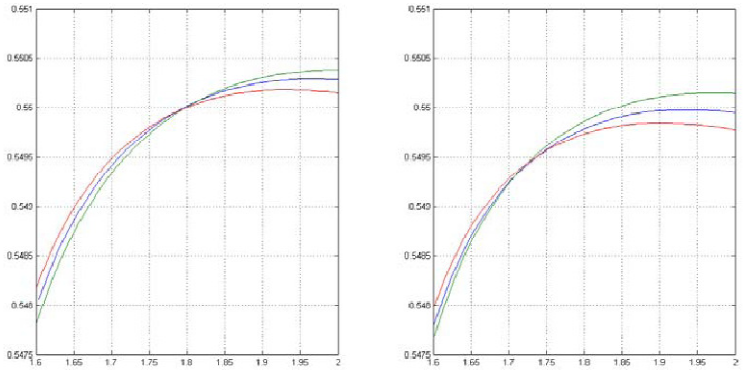

Figure 7: Variation of V_{ref} with power supply (V_{dd}) at 27oC and at 80oC

The PSRR Vs. frequency plot is shown in Figure 8, from which it can be found that PSRR of the proposed BGR is 79dB at typical process corner at 27°C at low frequency and is stable up to 1kHz. The values of PSRR over different process corners at 27°C and 80°C are given in Table 1.

Table 1. PSRR over process corners

Process corner	**At 27oC**	**At 80oC**
ff	82.02 dB	87.17 dB
typ	79.10 dB	81.60 dB
ss	76.41 dB	77.46 dB

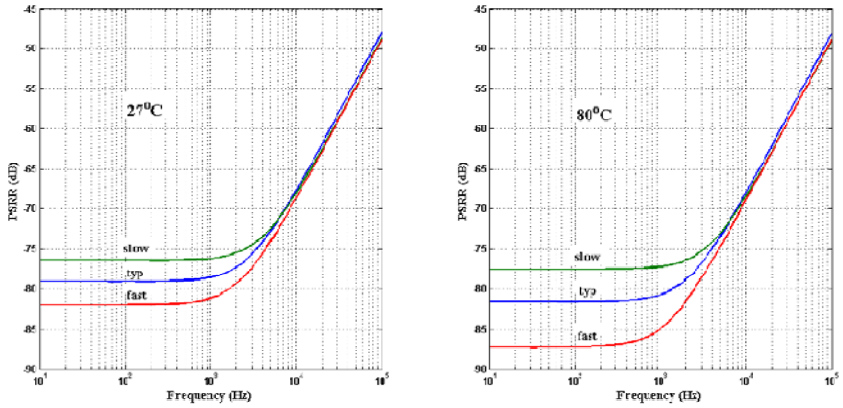

Figure 8: PSRR of the proposed BGR at 27oC and at 80oC

The performance metrics of different state-of-the-art bandgap circuits along with the proposed one are shown in Table 2. From the table, it can be seen that the proposed BGR has got a very low temperature coefficient and a high PSRR compared to other architectures. Figure 9 shows the layout of the proposed bandgap reference which occupies an area of ~0.14mm^2.

Table 2. Performance comparison of Bandgap reference circuits

Parameters	[7]	[4]	[8]	[9]	[10]	[11]	Proposed design
Technology	0.8 μm BiCMOS	0.8 μm BiCMOS	0.6 μm CMOS	0.35 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
V_{dd}	1V	-	2V	3.3V	1.8V	1.8V	1.8V
V_{ref}	536mV	1.207V	1.142V	1.183V	615.1mV	500mV	550mV
V_{ref} variation	300 μV	2.8mV	2.85mV	1mV	1.4mV	900 μV	400 μV
Temp. Range	0°C/ +80°C	-40°C/ +125°C	0°C/ +100°C	10°C/ +90°C	0° C/ +70°C	-40°C/ +125°C	-25°C/ +100°C
TC	7.5 ppm/°C	14 ppm/°C	5.3 ppm/°C	10.5 ppm/°C	32.5 ppm/°C	9 ppm/°C	5.8 ppm/°C
PSRR	-	110dB	47dB	-	35dB	108dB	79dB

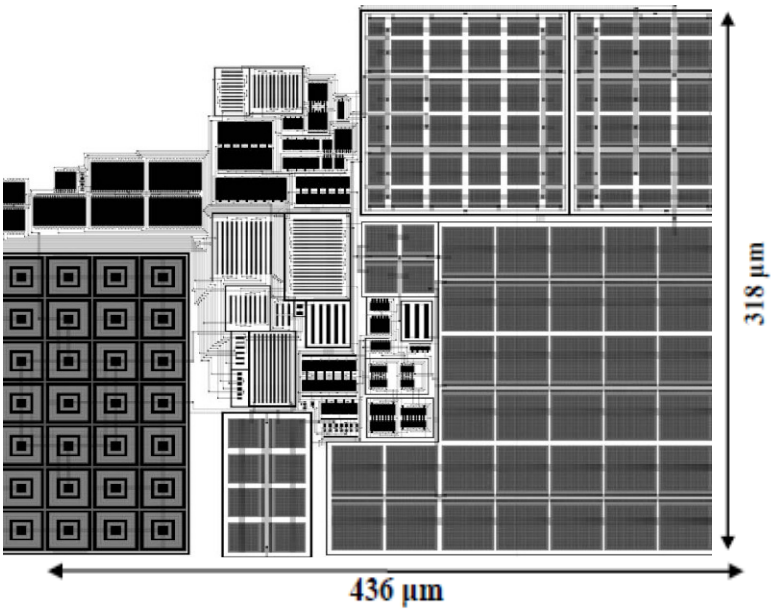

Figure 9: Layout of the proposed bandgap reference

4. CONCLUSION

A CMOS current-mode bandgap reference with high PSRR and low temperature coefficient is presented and verified. Using a 1.8V supply, a reference voltage of 550mV has been generated, which shows a TC of 5.8ppm/^{o}C over a wide temperature range from -25^{o}C to 100^{o}C. The proposed circuit registers a PSRR of more than 79dB at low frequency at typical process corner. So, it can fairly be concluded that this BGR circuit is well suited for the CMOS system-on-chip (SoC) applications for its power supply flexibility, temperature-stability of the reference voltage and high power supply rejection ratio.

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