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Design of a Dual Change-Sensing 24T Flip-Flop in 65 nm CMOS Technology for Ultra Low-Power System Chips

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Abstract: In this paper, a flip-flop (FF) that minimizes the transition of internal nodes by using a dual change-sensing scheme is discussed. Further, in order to reduce power consumption, a new technique to eliminate short-circuit currents is described. The proposed dual change-sensing FF (DCSFF) composed of 24T (T: number of transistors) has the lowest dynamic power consumption among conventional FFs, independent of the data activity ratio. According to the measured results with a 65 nm CMOS process, the power consumption of DCSFF is reduced by 98% and 32%, when the data activity is close to 0% and 100%, respectively, compared to that of conventional transmission gate FF. Further, compared to that of change-sensing FF, the power consumption of DCSFF is reduced by 26% when the data activity is close to 100%.

Keywords: flip-flop; dual change-sensing flip-flop (DCSFF); internal transitions; ultra low-power system chip

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1. Introduction

The rapid development of CMOS process technology has facilitated the design of high-performance and highly integrated circuits and systems [1]. Further, it is essential to apply the CMOS process technology for many kinds of low-power digital basic building blocks, such as flip-flop (FF), memory, arithmetic logic unit, and so on [2]. Among them, the design of an FF, which represents the primary synchronous logic component of system-on-chip frameworks, has been widely studied [3–20]. Figure 1 shows the circuit diagram of transmission-gate flip-flop (TGFF), which has been widely used in the field of digital systems [3]. It is composed of conventional 24T (T: number of transistors) and two latches. When CLK (or CLKa) is high, the first latch at the left side holds the previous input data. Then, it is transferred to the second latch on the right side when CLK is low. It means the output, Q, is holding the input data until the next CLK is high. Thus, a positive edge-triggered data FF is easily obtained with the circuit diagram of TGFF, as shown in Figure 1. However, TGFF has a high power dissipation due to a large number of complementary clock nodes. Whenever clock nodes are changed, huge short-circuit currents are generated at the transistors. Thus, TGFF has a drawback of large power consumption. In order to overcome the disadvantage of TGFF, an 11T flip-flop shown in Figure 2 has been reported [4]. While TGFF uses a dual-phase clock, Figure 2 uses only a single-phase clock. Thus, it is called a true single-phase clock flip-flop (TSPCFF). The TSPCFF has a lower power consumption due to single-phase clock operations and the use of fewer transistors compared to TGFF. However, this scheme of TSPCFF undergoes a performance degradation due to sub-nanometer CMOS technology with a low supply voltage under 1.8 V. Further, it has many glitches and non-static behaviors, because there are a lot of internal floating nodes. Even though it has less internal nodes, many internal floating nodes generate huge short-circuit currents and large power consumption.

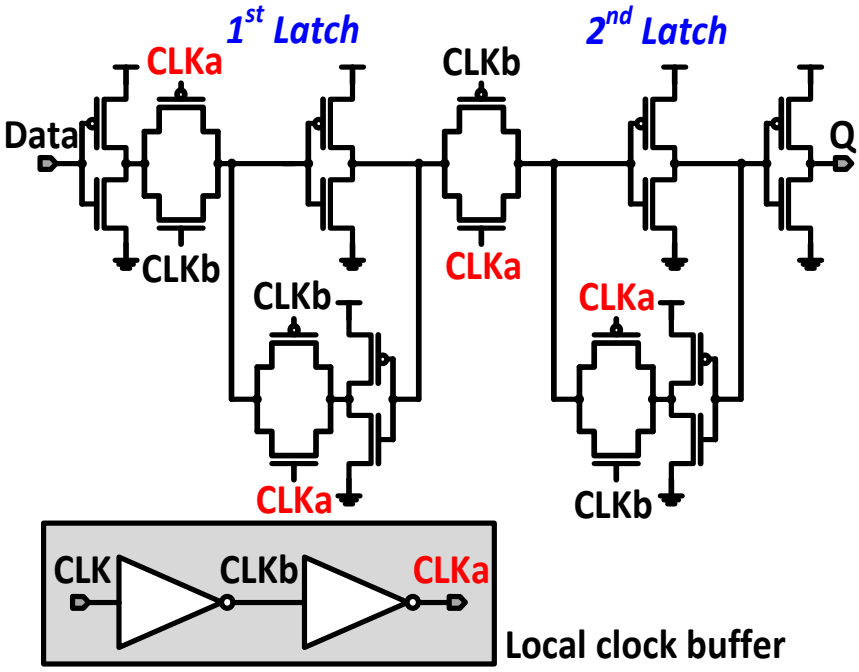


Figure 1. Transmission Gate Flip-Flop (TGFF).

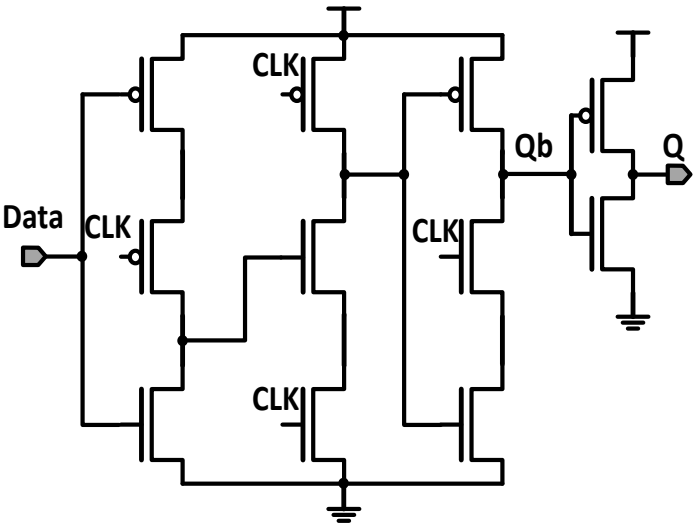


Figure 2. True Single Phase Clock Flip-Flop (TSPCFF).

To improve the circuit performance at low power supply voltage, a 24T static single-phase contention-free flip-flop (S^2CFF) shown in Figure 3 has been published [5]. The S^2CFF can eliminate many glitches and maintain single-phase clock operation. Thus, the authors have described that the performance of S^2CFF is much better than that of TSPCFF. However, it is still suffering from high power consumption because the continuous internal transitions of the node (the red line of net2 in Figure 3) are lastly undergoing. When the input data is low, the net2 is just following the clock. It means there is high power consumption. To minimize those internal transitions of S^2CFF, a 24T change-sensing flip-flop (CSFF) shown in Figure 4 has been proposed [6]. Since the CSFF uses a change-sensing scheme, it can reduce the internal transitions. However, the power consumption might be significantly increased if the short circuit currents are generated at the node (the blue line of DNCS in Figure 4). The timing diagram of internal node (net2) transitions is shown in Figure 5. The timing diagram of CSFF is also shown in Figure 5. When the input data is high, the CS

node (the red line in Figure 4) fluctuates. It means that huge power consumption can be generated at the high data activity ratio.

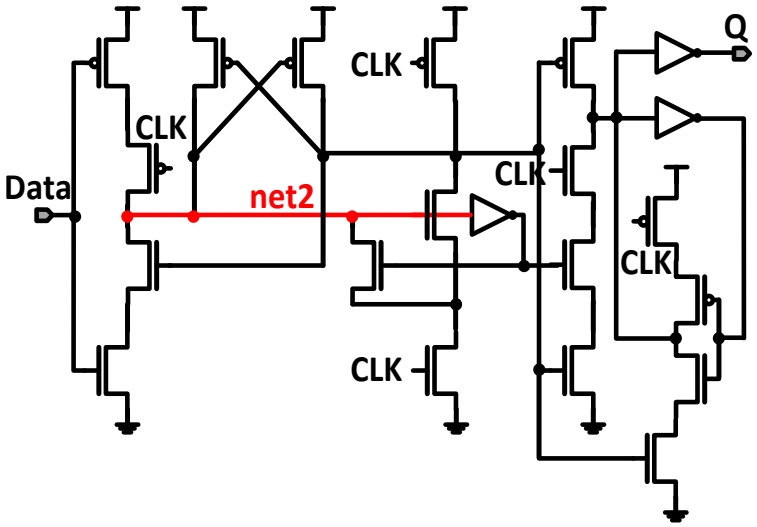


Figure 3. Static Single-phase Contention-free Flip-Flop (S^2CFF).

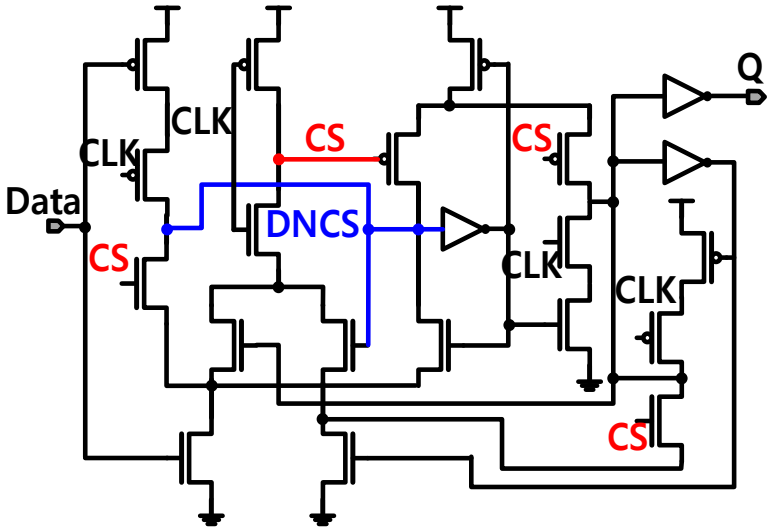


Figure 4. Change-Sensing Flip-Flop (CSFF).

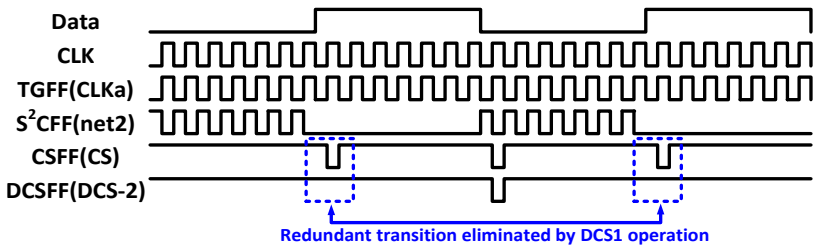


Figure 5. Timing Diagram of Redundant Transitions between the Proposed One and Others.

In order to reduce power consumption with a wide dynamic voltage range, a flip-flop should satisfy the design requirements as follows. (1) Static operation: dynamic nodes are susceptible to process, voltage, and temperature variations at low power supply voltages. (2) contention-free transitions: ratioed logics may have serious unstable conditions with the wide range voltage swing. (3) Single-phase clocking: it avoids toggling the internal

clock inverters and corresponding power penalty. (4) Small chip area: the chip size of the new FF should be smaller than that of conventional FFs. Even though various kinds of FFs to satisfy the requirements have been reported [8–16], a new scheme is proposed in this paper. The contents of this paper are as follows. In Section 2, a new FF is described and analyzed. The measured results are discussed in Section 3, and the conclusions are described in Section 4, respectively.

2. Proposed Dual Change-Sensing Flip-Flop (DCSFF)

Figure 6 shows the circuit diagram of the proposed dual change-sensing flip-flop (DCSFF). The aim of DCSFF is to minimize the power consumption by the reduction of internal transitions and the elimination of short-circuit currents that generate glitches in CSFF. Notably, since the continuous internal transitions are caused by CLK without the influence of output node, Q of FFs, those redundant transitions result in an increase of dynamic power consumption. The timing diagram which demonstrates the redundant transitions of conventional FFs is shown in Figure 5. The TGFF shows continuous redundant transitions due to the local clock buffer (CLKa and CLKb), whereas net2 of S^2CFF involves continuous redundant transitions only when the data are "0". The CS nodes of CSFF shown in Figure 4 reduce the redundant transitions compared to those of S^2CFF because the redundant transitions only occur at the data transitions. To significantly minimize those redundant transitions, the proposed DCSFF divides CS nodes into two nodes (DCS-1 and DCS-2). DCS-1 and DCS-2 replace CS nodes when the data are rising and falling, respectively. The redundant transitions of CSFF and DCSFF generated by the data and CLK have four states shown in Figure 7. DCS-1 can eliminate the redundant transition when the input data are rising (Data = "0" to "1"). Compared to the conventional FFs, therefore, the proposed DCSFF has the least redundant transitions, which results in the minimum dynamic power consumption.

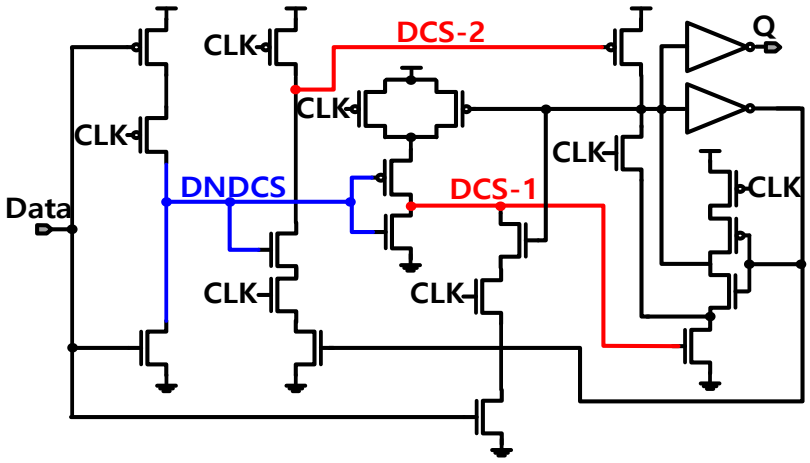


Figure 6. Circuit Diagram of Proposed Dual Change-Sensing Flip-Flop (DCSFF).

Internal Toggle (CSFF)	Data= 0 to 1	Data= 0 to 1
CLK=0	O	O
CLK=1	O	O

Internal Toggle (DCSFF)	Data= 0 to 1 (DCS1)	Data= 0 to 1 (DCS2)
CLK=0	X	O
CLK=1	X	O

Figure 7. Comparison of Internal Toggle Transitions between DCSFF and CSFF.

The left side of Figure 8a shows the process of glitch generation due to the short-circuit current in the CSFF. When the CLK maintains the "1" state, the CS node is discharged to

detect the input data rising. As the input data changes "0" to "1", the discharge path of DNCS is generated. Thus, a huge short-circuit current is generated with the glitch of DNCS, although the CS is discharged before the DNCS is discharged to maintain a value of "1". Further, the DNCS should not retain the "1" state to eliminate the mechanism by which the short-circuit current in the CSFF is generated. On the contrary, the operation principle of the proposed DCSFF is shown in Figure 8b. The DNDCS of DCSFF is a similar node to the DNCS. In the same way, the DCSFF allows DCS-1 to hold "0", even if the DNDCS is discharged without maintaining "1". Therefore, no additional operation is required to maintain "1" in the DCSFF. As shown in Figure 8c, while DNCS has a serious short-circuit current, the DNDCS does not generate a short-circuit current, even if CLK remains in the "1" state when data are rising with DCS-1. Therefore, the proposed DCSFF reduces the dynamic power consumption by half compared to CSFF. Furthermore, the proposed DCSFF consumes less power than that of CSFF when the data activity ratio is high.

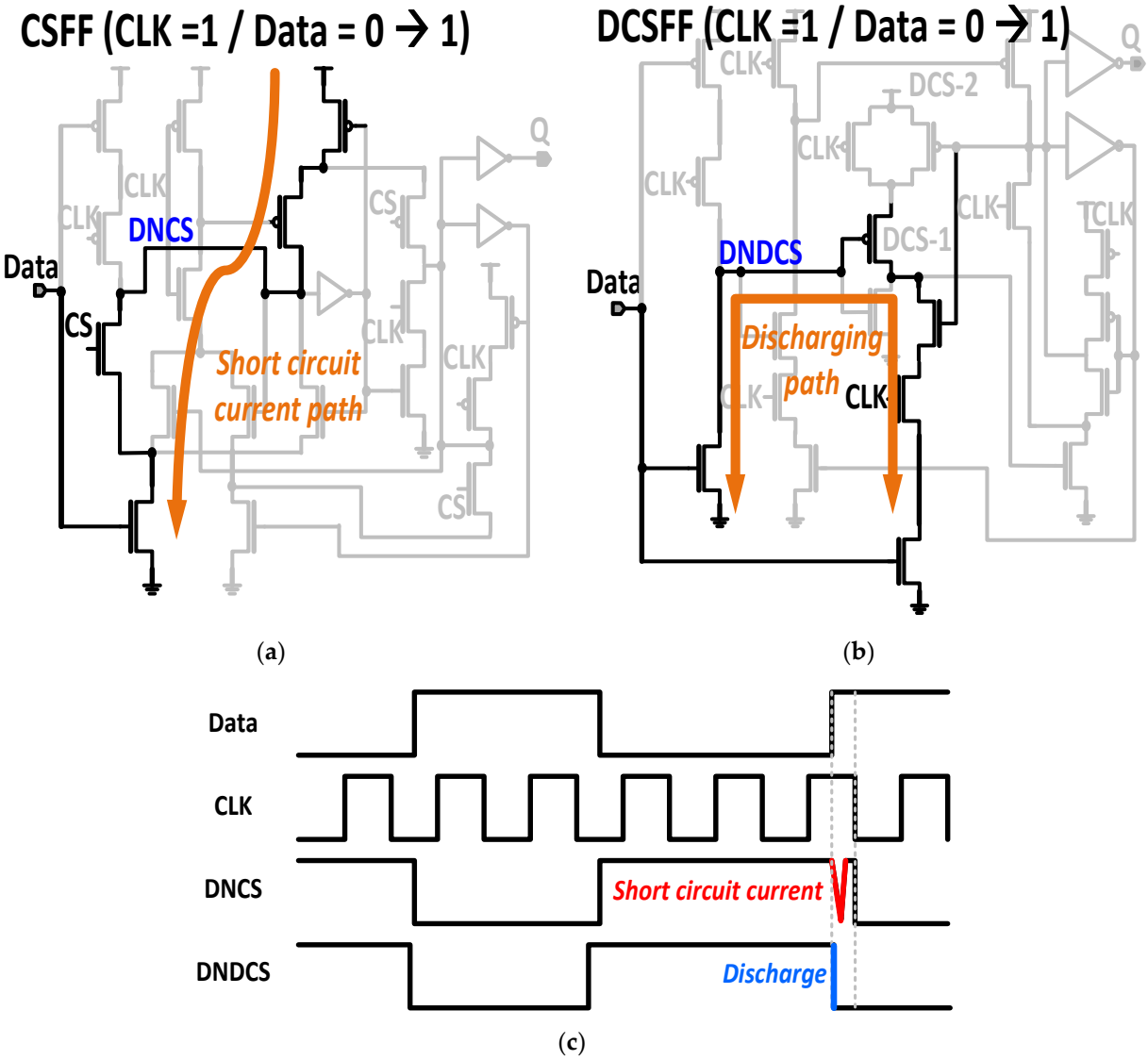


Figure 8. Circuit Diagram of (**a**) CSFF and (**b**) DCSFF and (**c**) Comparison of Timing Diagram.

3. Measured Results

In order to implement an accurate comparison between conventional FFs and the proposed DCSFF, efficient on-chip testing circuits to measure many performance parameters should be considered. For example, the considered parameters are the power consumption,

setup time, hold time, C-Q delay, data activity factor, etc. The measurement blocks are designed to realize the on-chip testing of each parameter. The setup and hold time measurement block is shown in Figure 9, which consists of a delay chain and an external monitoring block to encode the outputs and predict the internal skews [17]. Figure 10 shows the C-Q delay measurement block [18–20]. It has a ring oscillator structure, and the C-Q delay can be measured when we consider the difference in the frequency between the device under test (DUT) and reference rings. Figure 11 shows the power consumption measurement block. For the power consumption measurement block, the data activity factor is designed to be regulated. The initial external patterns are applied to the DUT periodically with a constant pulse signal. The data activity can be adjusted to range from 0% to 100% in 10% intervals.

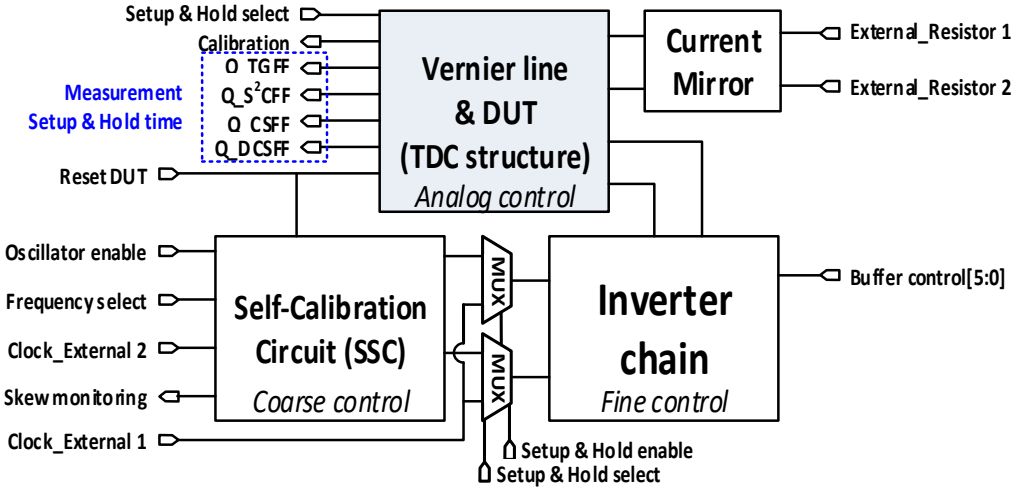


Figure 9. Block Diagram for Setup and Hold Time Measurement.

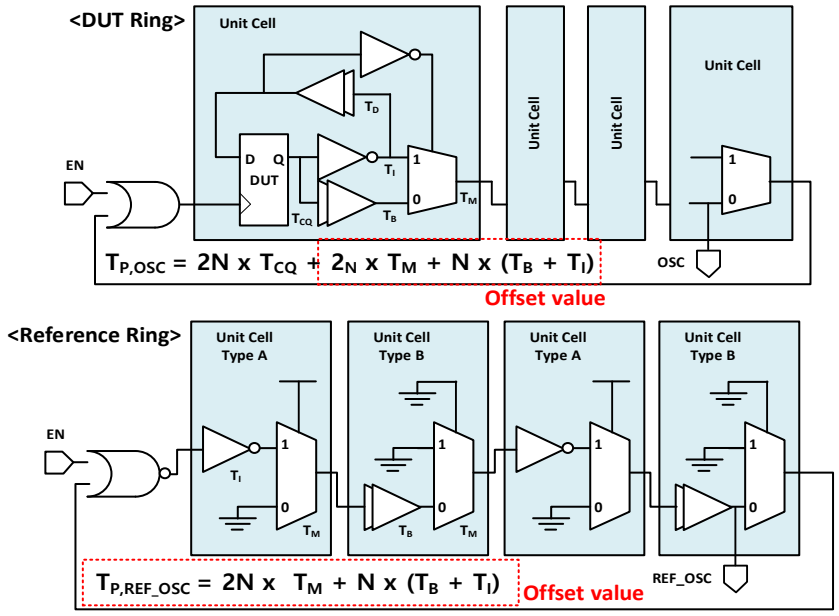


Figure 10. Block Diagram of Power Measurement.

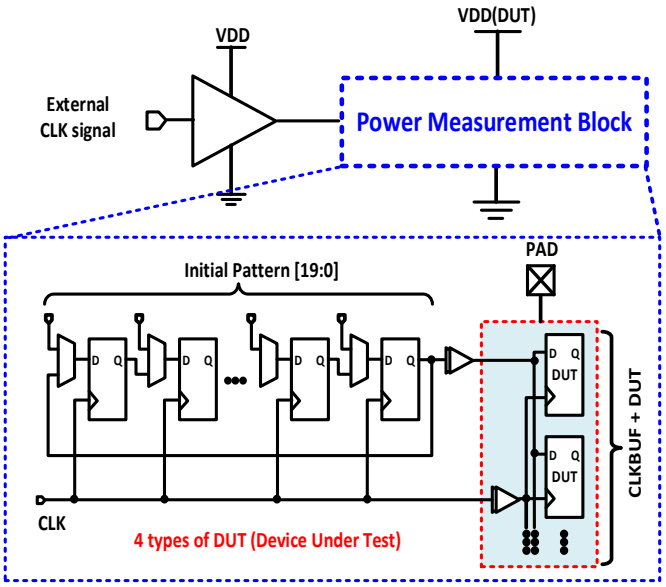
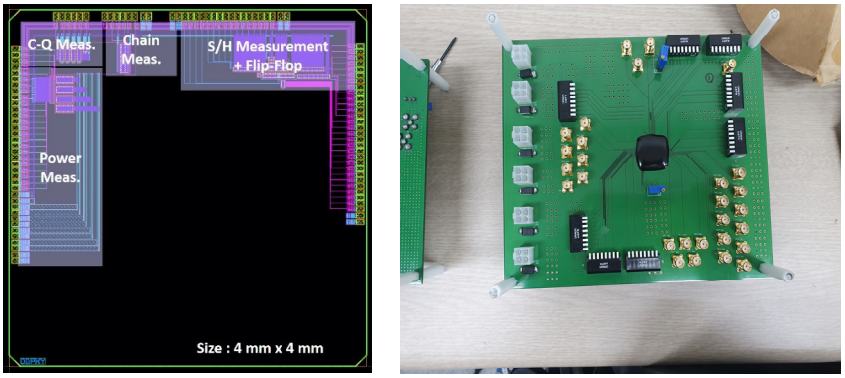


Figure 11. Block Diagram of Power Measurement.

The layout drawing of the fabricated chip and testing PCB is shown in Figure 12. The proposed DCSFF has been fabricated with a Samsung 65-nm CMOS process with TGFF, S^2CFF, and CSFF. All of them have been measured on the same chip. The setup and hold time measurement block shown in Figure 9 is placed at the right top side of Figure 12a. C-Q delay measurement block shown in Figure 10 is placed at the left top side of Figure 12a. Finally, the power measurement block shown in Figure 11 is placed at the left middle side of Figure 12a. Each block has the conventional FFs and the proposed DCSFF. The testing printed circuit board (PCB) with a fabricated chip is shown in Figure 12b.

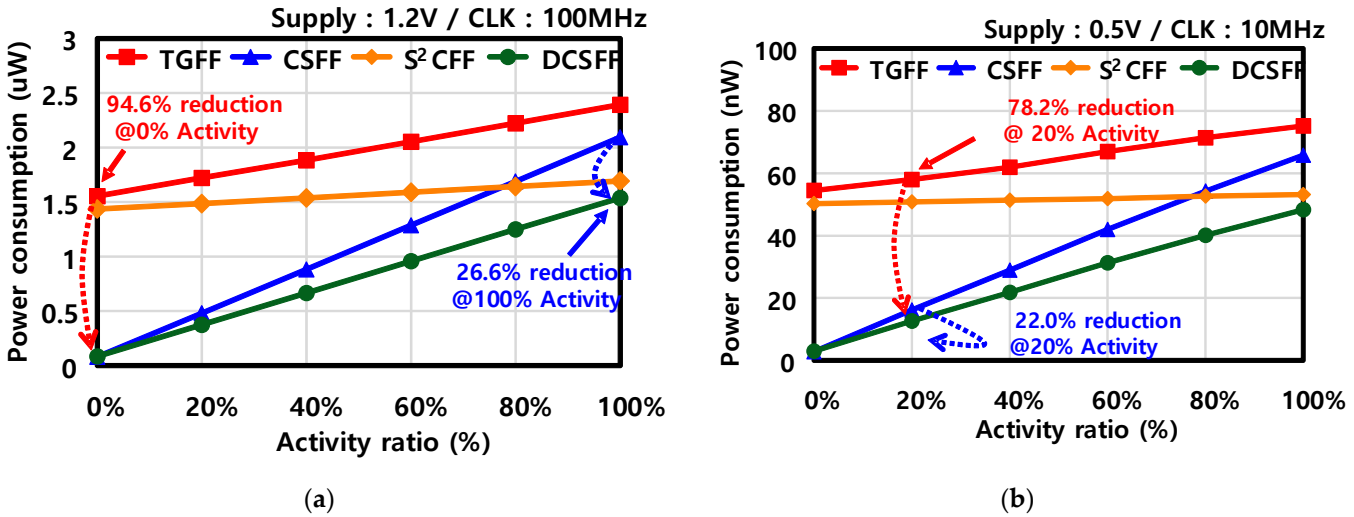


(**a**) (**b**)

Figure 12. (**a**) Chip Layout; (**b**) Testing PCB with a Fabricated Chip.

Figure 13 shows the measured power consumption, according to the increase of data activity ratio from 0% to 100%. The power consumptions of each FF have been measured under two conditions: (a) 1.2 V/100 MHz and (b) 0.5 V/10 MHz. In terms of data activity ratios, the CSFF and DCSFF almost do not consume power at 0% data activity ratio (=no leakage) because the drastic reduction of internal transition nodes is available. Thus, the CSFF and DCSFF have low absolute power consumption, even though the TGFF and S^2CFF have a large power consumption when the data activity ratio is low. At the data activity ratio of 0%, for example, the power consumption of DCSFF is smaller by 94% than that of S^2CFF from Figure 13a,b. Further, at the data activity ratio of 20%, for example, the power consumption of DCSFF is smaller by 78% than that of S^2CFF from Figure 13a,b. By the way, since the CSFF is more sensitive to the data activity ratio than that of DCSFF, the slope of

power consumption of CSFF is steeper by about 26% than that of DCSFF. When the data activity is 20%, the DCSFF has a 22.1% and 22% lower power consumption at 1.2 V/100 MHz and 0.5 V/10 MHz, respectively, compared to the CSFF. When the data activity is 100%, the power consumption of DCSFF is smaller by 26% than that of the CSFF.



(**a**) (**b**)

Figure 13. Measured Power Consumption. (**a**) 1.2 V Supply and 100 MHz Clock (**b**) 0.5 V Supply and 10 MHz Clock.

However, the slope of power consumption of CSFF and DCSFF is two or three times steeper than that of TGFF and S^{2}CFF, according to the increase of data activity ratios. At the data activity ratio of 100%, the power consumption of CSFF is bigger by 20% than that of S^{2}CFF, and smaller by 15% than that of TGFF. However, the power consumption of the proposed DCSFF is always smaller than that of TGFF, S^{2}CFF, and CSFF. Figure 14 shows the comparison data of the active energy consumption at the data activity ratio of 100%. The active energy of DCSFF is reduced by 35.7% and 26.6% compared to that of the TGFF and CSFF, respectively. Further, the active energy consumption of DCSFF is smaller by 11% than that of S^{2}CFF. Therefore, the proposed DCSFF has the lowest power consumption among other conventional ones.

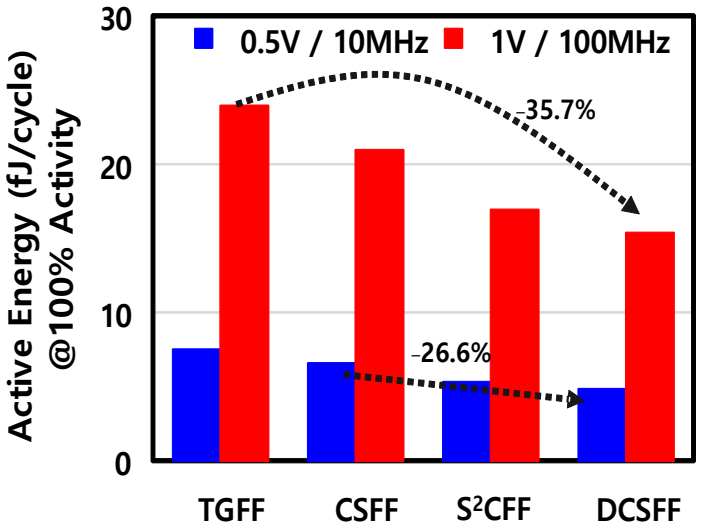


Figure 14. Comparisons for Measured Active Energy.

Table 1 shows the measurement comparison table between the proposed DCSFF and other FFs. Since the proposed DCSFF is contention-free and composed of 24 transistors

with a single phase clock, it is easy to design a circuit diagram and a layout drawing. When the layout size of the TGFF is normalized to 1, the area is increased by 5% for S^2CFF, by 13% for CSFF, and by only 4% for DCSFF. It means the layout size of DCSFF is smaller by 8% than that of CSFF. The measured C-Q delay of DCSFF is 112.7 pico-seconds, which is the shortest among other FFs. However, the measured setup time and hold time is 216 pico-seconds and 49 pico-seconds, respectively. It means the proposed DCSFF has a disadvantage from the viewpoint of operating speed. At 100 MHz clock with 1.2 V power supply, the measured power consumption is 0.37 μW and 1.54 μW at the activity ratio of 20% and 100%, respectively. At 10 MHz clock with a 0.5 V power supply, the measured power consumption is 0.013 μW and 0.048 μW at the activity ratio of 20% and 100%, respectively. Further, the measured leakage power consumption is only 0.084 μW at a 1.2 V power supply. It means, in terms of power consumption, the proposed DCSFF has an excellent advantage compared to that of other ones. Therefore, the proposed DCSFF is suitable for ultra-low power system chips.

Table 1. Performance Comparison Table between DCSFF and Other Ones.

Performance	DCSFF	TGFF [3]	SSCFF [5]	CSFF [6]
Contention-free	**YES**	YES	YES	NO
Number of Transistor	**24**	24	24	24
Single Phase Clock	**YES**	NO	YES	YES
Layout Size (relative size)	**1.04**	1	1.05	1.13
Measured C-Q Delay @1.2 V (ps)	**112.7**	150.6	140.6	128.9
Measured Setup Time @1.2 V (ps)	**216**	165	186	197
Measured Hold Time @1.2 V (ps)	**49**	55	46	34
Measured Power @ 1.2 V, 100 MHz, 20%/100% (μW)	**0.37/1.54**	1.72/2.39	1.49/1.69	0.48/2.09
Measured Power @ 0.5 V, 10 MHz, 20%/100% (μW)	**0.013/0.048**	0.058/0.075	0.051/0.053	0.016/0.066
Measured Leakage@1.2 V (μW)	**0.084**	1.555	1.435	0.079

4. Conclusions

In this paper, the design of a dual change-sensing flip-flop (DCSFF) to reduce dynamic power consumption and short circuit currents was described. Since the DCSFF has minimized the internal transition nodes shown in TGFF and SSCFF, there was no dynamic power consumption when the data activity was 0%. In addition, we proposed a new technique where a node to detect data changes in the CSFF has been separated into DCS-1 node and DCS-2 node, respectively. It reduced the internal transitions to detect the low to high of the data signal. At the same time, the glitch generated from the CSFF has been removed to reduce short circuit currents. Therefore, the dynamic power consumption and short-circuit currents of DCSFF have been drastically reduced. Finally, DCSFF had the lowest power consumption compared to other FFs in all sections of data activity. We expect that the proposed DCSFF could play a significant role in developing future ultra-low-power systems.

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