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Design of a High Performance Phase-Locked Loop With DC Offset Rejection Capability Under Adverse Grid Condition

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ABSTRACT In the new energy grid-connected power generation system, accurately extracting the grid synchronization signals such as the frequency, phase and amplitude of the grid voltage is the basis for effective control. Aiming at the requirements for detecting grid synchronization signals under unbalanced, harmonics and DC offset voltage mixed conditions, a dual second-order complex coefficient filter with DC offset rejection capability (DSOCCF$_{dc}$) is proposed, combining the approach of moving average filter (MAF), a novel hybrid filter in *dq*-frame is designed and on the basis of this design a new synchronous reference frame phase locked loop (SRF-PLL) design approach based on the hybrid filter is proposed. The proposed approach employs moving average filter (MAF) to block the high-frequency harmonics in the grid voltage, and uses DSOCCF$_{dc}$ to separate the fundamental frequency positive and negative sequence and reject DC offset. It can accurately extract the synchronization information of the grid fundamental frequency positive sequence. After simulation and experiment verification, it can be confirmed that the proposed PLL can quickly and accurately lock the properties of the grid voltage under adverse grid condition, and also have high detection accuracy and strong robustness to frequency fluctuations.

INDEX TERMS Dual second-order complex coefficient filter (DSOCCF), harmonic, phase-locked loop (PLL), dc offset, moving average filter (MAF).

I. INTRODUCTION

With the development of new energy technologies, more and more new energy power generation equipment such as wind power and solar power are integrated into the grid to provide power to the grid [1]–[3]. Obtaining the grid synchronization signal such as the frequency, phase and amplitude of the grid voltage is the premise and basis for the grid connection operation. The phase-locked loop (PLL) technology can effectively detect the grid synchronization signal in real time and has been widely used [4]. However, due to the large number of power electronic loads such as uncontrolled rectification and reactive power compensation, the power grid is unbalanced or harmonically distorted [5], [6]. At the same time, the grid-connected generators are changed to have certain fault-crossing ability to keep synchronous connection with the power grid under the unbalanced and distorted conditions. So the higher requirements are required for the acquisition of grid voltage synchronization signals [7]–[9]. Therefore, it has theoretical and practical significance to study the phase-locked loop technology under unbalanced and distorted grid conditions [10], [11].

The synchronous reference frame PLL(SRF-PLL) is widely used in grid-connected applications due to its simple implementation, strong robustness and high phase tracking accuracy. This approach has important value in the three-phase grid phase-locked technology, and many approaches are based on the improvement of this approach. SRF-PLL can achieve good tracking results under the ideal power grid, but under the unbalanced and distorted conditions, the tracking performance of the ideal grid phase-locked loop will be affected due to the existence of fundamental frequency negative sequence voltage and high-frequency harmonics [12]. Therefore, many improved phase-locked loop techniques

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have been proposed [13]–[15]. In [16], the adaptive notch filter (ANF) was used to generate orthogonal signals in the synchronous rotating frame to complete the fundamental frequency positive and negative sequence voltage separation, and the design was suitable for the phase-locked loop under the unbalanced power grid. [17], [18] proposed a frequency adaptive phase-locked loop by designing a quadrature signal generator using double second order generalization integrator (DSOGI). Hamed *et al*. [19] and Golestan *et al*. [20] proposed an improved frequency adaptive DSC-PLL structure to make the PLL adapt to grid voltage frequency variations, but the adaptive process requires a difference calculation, so the number of DSC modules will determine the amount of adaptive difference calculation. However, this method does not solve the problem of reducing the number of cascade modules, so the system calculation amount and implementation complexity are large. In addition, since moving average filter (MAF) is capable of completely blocking all signals at integer multiples ($1/T_\omega$) Hz [21], some MAF-based advanced PLL methods have been proposed [22]–[24].

As a more common approach, the complex coefficient filter based PLL (CCF-PLL) can accurately and quickly extract the fundamental frequency positive sequence component of the PLL input voltage and achieve accurate phase locked. It is usually implemented in a cross-decoupled manner using first-order complex-coefficient filters, but the filtering performance and DC offset elimination capability are insufficient. The multi-CCF-based PLL (MCCF-PLL) uses multiple first-order complex-coefficient filters in parallel to achieve the goal of blocking specific harmonic components. The mathematical model of dual CCF-PLL (DCCF-PLL) was deduced in [25], and the PID controller was used to replace the PI controller in SRF-PLL to improve the transient response speed of DCCF-PLL. In [26], the integral link output signal in the PI controller of SRF-PLL was improved to estimate the grid frequency and the enhanced CCF-PLL (ECCF-PLL) was suggested. This method can be used to improve the performance of the PLL without additional computational burden. In [27], the CCF-PLL was designed based on the second-order complex coefficient filter, which had better harmonic attenuation suppression ability than the first-order complex coefficient filter scheme. Similarly, [28] proposed a generalized multi-order CCF-PLL (GMOCCF-PLL), which further enhances the dynamic characteristics and filtering capabilities of the conventional CCF-PLL.

Rejecting the DC offset in the grid voltage is also a major problem that PLLs need to solve. The existence of DC offset in the PLL input results in fundamental frequency oscillation error in the estimate phase, frequency, and amplitude of the PLL. Because of the low frequency of the oscillation error, it is more difficult to eliminate these oscillations [29], [30]. [31] proposed a novel PLL with DC offset rejection, DC immune PLL (DCI-PLL). The approach employed the $\alpha\beta$-axis component of the input grid voltage minus its respective delayed signal component to extract the fundamental frequency positive sequence component and eliminate the DC offset. This technology can ensure complete and fast rejection of DC offsets. However, using the delay component of the input signal will result in a constant offset error in the estimated phase. In [32], a approach for rejecting DC offset by DSC operator was proposed in the $\alpha\beta$-frame. This approach adopted the characteristics for filtering specific frequency components of the DSC operator to eliminate the frequency component of DC offset.

To improve the filtering performance and DC offset rejection capability of the conventional CCF-PLL based on the first-order complex coefficient filter, this paper proposes a new SRF-PLL based on a hybrid filter composed of a DSOCCF$_{dc}$ with DC offset rejection and MAF. Firstly, the first-order complex coefficient filter and high-order complex coefficient filter are studied and deduced. Then, the DSOCCF$_{dc}$ with DC offset rejection capability is proposed and transformed into dq-Frame to form a new hybrid filter with MAF. Furthermore, incorporating a hybrid filter into the SRF-PLL to propose the hybrid filter based PLL. The mathematical model is derived and the control parameters are presented. Finally, the validity of the proposed PLL is verified by simulation and experiment.

II. OVERVIEW OF COMPLEX COEFFCIENT FILTER

A. FIRST ORDER COMPLEX COEFFCIENT FILTER

The main goal of the three-phase grid PLL in the process of grid synchronization is effectively separating the fundamental frequency positive sequence component and fundamental frequency negative sequence component of the input voltage. Under ideal grid conditions, three-phase grid voltage v_a, v_b, v_c can be expressed as

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} V_m^+ \sin(\omega_0 t + \theta^+) + V_m^- \sin(-\omega_0 t + \theta^-) \\ V_m^+ \sin(\omega_0 t - \frac{2}{3}\pi + \theta^+) + V_m^- \sin(-\omega_0 t - \frac{2}{3}\pi + \theta^-) \\ V_m^+ \sin(\omega_0 t + \frac{2}{3}\pi + \theta^+) + V_m^- \sin(-\omega_0 t + \frac{2}{3}\pi + \theta^-) \end{bmatrix} \tag{1}$$

where, V_m^+ and V_m^- are the voltage amplitudes of fundamental frequency positive and negative sequence respectively; θ^+ and θ^- are the phase angles of fundamental frequency positive and negative sequence respectively; ω_0 is the fundamental voltage frequency.

The three-phase voltage is transformed from abc-frame to $\alpha\beta$-frame by Clark transformation, and v_α and v_β are obtained as follows:

$$\begin{bmatrix} v_\alpha \\ v_\alpha \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} v_\alpha^+ + v_\alpha^- \\ v_\beta^+ + v_\beta^- \end{bmatrix} \tag{2}$$

$$\begin{bmatrix} v_\alpha^+ \\ v_\beta^+ \end{bmatrix} = \begin{bmatrix} V_m^+ \sin(\omega_0 t + \theta^+) \\ -V_m^+ \cos(\omega_0 t + \theta^+) \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} v_\alpha^- \\ v_\beta^- \end{bmatrix} = \begin{bmatrix} V_m^- \sin(-\omega_0 t + \theta^-) \\ -V_m^- \cos(-\omega_0 t + \theta^-) \end{bmatrix} \tag{4}$$

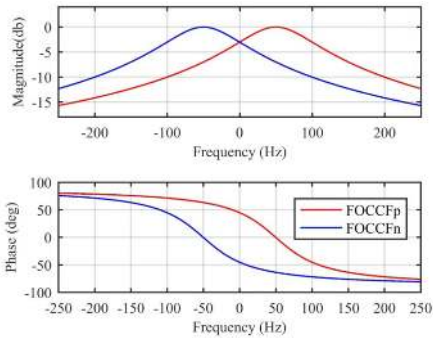

FIGURE 1. Bode diagram of $\mathrm{FOCCF_p(s)}$ and $\mathrm{FOCCF_n(s)}$.

where, the positive sequence component and the negative sequence component of v_α are v_α^+ and v_α^- respectively, and the positive and negative components and negative sequence components of v_β are v_β^+ and v_β^- respectively.

According to (1)-(4), the frequency of the fundamental frequency positive sequence component is ω_0 and the frequency of the fundamental frequency negative sequence component is $-\omega_0$ in the $\alpha\beta$-frame. It can be seen that if the fundamental frequency positive sequence component or the fundamental frequency negative sequence component can be effectively separated, the required filter needs to satisfy the amplitude magnification is 1 and the phase is 0 at the frequency ω_0 or $-\omega_0$, and at other frequencies the amplitude becomes attenuating.

To achieve the decoupling separation between the positive sequence component and the negative sequence component of the grid voltage, the first order complex coefficient filter (FOCCF) is proposed in [33]. The expressions of the positive sequence filter and the negative sequence filter are respectively

$$\mathrm{FOCCF}_p(s) = \frac{\omega_p}{s - j\hat{\omega} + \omega_p} \tag{5}$$

$$\mathrm{FOCCF}_n(s) = \frac{\omega_p}{s + j\hat{\omega} + \omega_p} \tag{6}$$

where, the estimated frequency of the PLL is $\hat{\omega}$, $\omega_p = \xi\hat{\omega}$, ξ is the damping factor, $\hat{\omega} = \omega_0$ when the phase angle is locked.

Fig.1 shows the bode diagram of the positive and negative sequence filters of the FOCCF when $\omega_p = \xi\hat{\omega} = 2\pi 50$rad/s. According to Fig.1, the FOCCF_p and FOCCF_n amplitude magnification is 1 and the phase is 0 at the frequency 50 Hz or -50 Hz, and the amplitude is attenuated at other frequencies, indicating that they can effectively separate the fundamental frequency positive sequence component or the fundamental frequency negative sequence component.

In the PLL grid-connected synchronization application, the dual first-order complex coefficient filter (DFOCCF) is commonly used, that is, the first-order complex positive-negative filters cross-decoupling are employed to completely separate the fundamental frequency positive sequence component, the DFOCCF structure diagram is shown in Fig.2

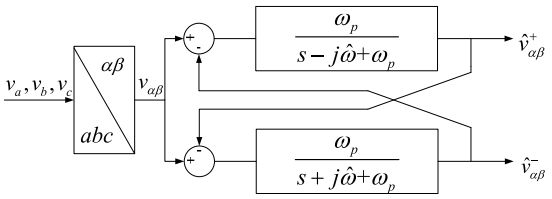

FIGURE 2. Block diagram of DFOCCF.

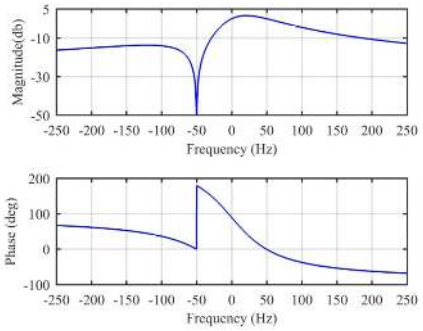

FIGURE 3. Bode diagram of DFOCCF(s).

The mathematical model expression of Fig.2 is

$$\hat{v}^+_{\alpha\beta}(s) = \frac{\omega_p}{s - j\hat{\omega} + \omega_p}[v_{\alpha\beta}(s) - \hat{v}^-_{\alpha\beta}(s)] \tag{7}$$

$$\hat{v}^-_{\alpha\beta}(s) = \frac{\omega_p}{s + j\hat{\omega} + \omega_p}[v_{\alpha\beta}(s) - \hat{v}^+_{\alpha\beta}(s)] \tag{8}$$

Simplify the above equations, we can obtain

$$\hat{v}^+_{\alpha\beta}(s) = \frac{\omega_p(s + j\hat{\omega})}{s^2 + 2\omega_p s + \hat{\omega}^2} v_{\alpha\beta}(s) \tag{9}$$

$$\hat{v}^-_{\alpha\beta}(s) = \frac{\omega_p(s - j\omega_0)}{s^2 + 2\omega_p s + \hat{\omega}^2} v_{\alpha\beta}(s) \tag{10}$$

Then the transfer function of the DFOCCF to extract the fundamental frequency positive sequence component is

$$\mathrm{DFOCCF}(s) = \frac{\hat{v}^+_{\alpha\beta}(s)}{v_{\alpha\beta}(s)} = \frac{\omega_p(s + j\hat{\omega})}{s^2 + 2\omega_p s + \hat{\omega}^2} \tag{11}$$

When $\omega_p = \xi\hat{\omega} = 2\pi 50$rad/s, the bode diagram of DFOCCF is shown in Fig.3. It can be seen from Fig.3 that the amplitude magnitude and the phase of the DFOCCF are 1 and 0, respectively, at 50Hz, so the fundamental frequency positive sequence component of the power grid can be accurately extracted.

B. HIGH ORDER COMPLEX COEFFCIENT FILTER

To effectively extract the fundamental frequency positive sequence component or the fundamental frequency negative sequence component and to achieve higher grid-connected synchronization accuracy and faster dynamic response, the high-order complex coefficient filter (HOCCF) can also be employed, and the expressions of positive sequence filter

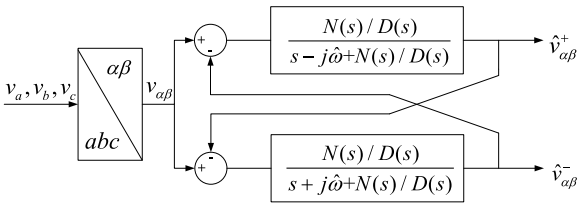

FIGURE 4. Block diagram of DHOCCF.

the negative sequence filter are

$$\mathrm{HOCCF}_p(s) = \frac{N(s)/D(s)}{s - j\hat{\omega} + N(s)/D(s)} \tag{12}$$

$$\mathrm{HOCCF}_n(s) = \frac{N(s)/D(s)}{s + j\hat{\omega} + N(s)/D(s)} \tag{13}$$

where, $N(s)$ and $D(s)$ are polynomials. For the first-order complex filter, $N(s) = \omega_p$, $D(s) = 1$.

Fig.4 shows the structure of dual high-order complex coefficient filter (DHOCCF), and its mathematical model expressions are

$$\hat{v}^+_{\alpha\beta}(s) = \frac{N(s)/D(s)}{s - j\hat{\omega} + N(s)/D(s)}[v_{\alpha\beta}(s) - \hat{v}^-_{\alpha\beta}(s)] \tag{14}$$

$$\hat{v}^-_{\alpha\beta}(s) = \frac{N(s)/D(s)}{s + j\hat{\omega} + N(s)/D(s)}[v_{\alpha\beta}(s) - \hat{v}^+_{\alpha\beta}(s)] \tag{15}$$

Simplify the above equations, we can obtain

$$\hat{v}^+_{\alpha\beta}(s) = \frac{N(s)(s + j\hat{\omega})}{D(s)(s^2 + \hat{\omega}^2) + 2N(s)s} v_{\alpha\beta}(s) \tag{16}$$

$$\hat{v}^-_{\alpha\beta}(s) = \frac{N(s)(s - j\hat{\omega})}{D(s)(s^2 + \hat{\omega}^2) + 2N(s)s} v_{\alpha\beta}(s) \tag{17}$$

Then the transfer function of the DHOCCF for extracting the fundamental frequency positive sequence component is

$$\mathrm{DHOCCF}(s) = \frac{\hat{v}^+_{\alpha\beta}(s)}{v_{\alpha\beta}(s)} = \frac{N(s)(s + j\hat{\omega})}{D(s)(s^2 + \hat{\omega}^2) + 2N(s)s} \tag{18}$$

It can be seen that in order to extract the fundamental frequency positive sequence component and eliminate the fundamental frequency negative sequence component using the high-order complex coefficient filter, it is only necessary to set different $N(s)$ and $D(s)$ [27].

III. DSOCCF WITH DC OFFSET REJECTION CAPABILITY

According to [35], the corresponding relationship between voltage components and frequencies in different frames under the adverse grid condition is shown in Table I, and the grid frequency is 50 Hz.

It can be observed from Table I that the DC offset component of the three-phase grid voltage is located at 0 Hz in $\alpha\beta$-frame, in order to completely reject the DC offset component, we can set the filter transfer function to have a zero at the 0-axis in the s-domain, that is, the amplitude is zero at 0 Hz in the frequency domain.

(12) and (13) can be written as

$$\mathrm{HOCCF}_p(s) = \frac{N(s)}{D(s)(s - j\hat{\omega}) + N(s)} \tag{19}$$

TABLE 1. Dominant components of grid voltage.

Harmonic order	⋯	-11	-5	-1	0	+1	+7	+13	⋯
$\alpha\beta$-frame (Hz)	⋯	-550	-250	-5	0	50	350	650	⋯
Harmonic order	⋯	-12	-6	-2	-1	0	+6	+12	⋯
dq-frame (Hz)	⋯	-600	-300	-100	-50	0	300	600	⋯

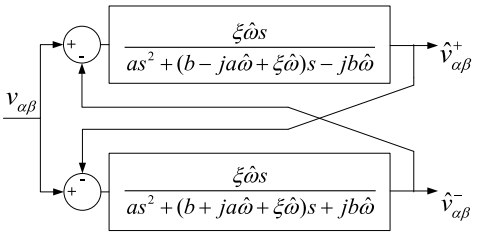

FIGURE 5. Block diagram of DSOCCF_{dc}.

$$\mathrm{HOCCF}_n(s) = \frac{N(s)}{D(s)(s + j\hat{\omega}) + N(s)} \tag{20}$$

According to the above equations, if HOCCF can reject DC offset, the polynomial $N(s)$ needs to satisfy $N(s) = 0$ when $s = 0$.

In this paper, a second-order complex coefficient filter (SOCCF_{dc}) with DC offset rejection capability is proposed by setting $D(s) = as + b$, $N(s) = \xi\hat{\omega}s$.

Taking $D(s) = as + b$, $N(s) = \xi\hat{\omega}s$ into (19) and (20) respectively, we can get the expressions of positive sequence filter and negative sequence filter of SOCCF_{dc} as follows

$$\mathrm{SOCCF}_{dc,p}(s) = \frac{\xi\hat{\omega}s}{as^2 + (b - ja\hat{\omega} + \xi\hat{\omega})s - jb\hat{\omega}} \tag{21}$$

$$\mathrm{SOCCF}_{dc,n}(s) = \frac{\xi\hat{\omega}s}{as^2 + (b + ja\hat{\omega} + \xi\hat{\omega})s + jb\hat{\omega}} \tag{22}$$

The structure diagram of DSOCCF_{dc} with DC offset rejection capability can be obtained as shown in Fig. 5, and the mathematical model expression is

$$\hat{v}^+_{\alpha\beta}(s) = \frac{\xi\hat{\omega}s}{as^2 + (b - ja\hat{\omega} + \xi\hat{\omega})s - jb\hat{\omega}}[v_{\alpha\beta}(s) - \hat{v}^-_{\alpha\beta}(s)] \tag{23}$$

$$\hat{v}^-_{\alpha\beta}(s) = \frac{\xi\hat{\omega}s}{as^2 + (b + ja\hat{\omega} + \xi\hat{\omega})s + jb\hat{\omega}}[v_{\alpha\beta}(s) - \hat{v}^+_{\alpha\beta}(s)] \tag{24}$$

(25) and (26) can be obtained after calculation of (23) and (24) as follow

$$\hat{v}^+_{\alpha\beta}(s) = \frac{\xi\hat{\omega}s(s + j\hat{\omega})}{as^3 + (b + 2\xi\hat{\omega})s^2 + a\hat{\omega}^2 s + b\hat{\omega}^2} v_{\alpha\beta}(s) \tag{25}$$

$$\hat{v}^-_{\alpha\beta}(s) = \frac{\xi\hat{\omega}s(s - j\hat{\omega})}{as^3 + (b + 2\xi\hat{\omega})s^2 + a\hat{\omega}^2 s + b\hat{\omega}^2} v_{\alpha\beta}(s) \tag{26}$$

Then the transfer function of DSOCCF_{dc} which can be employed to extract the fundamental frequency positive

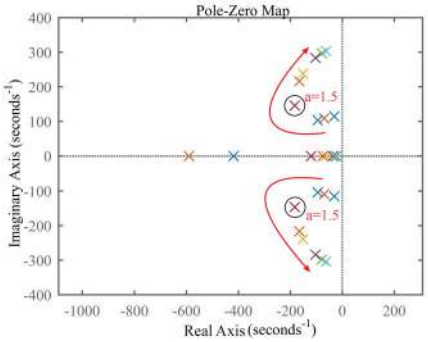

FIGURE 6. Pole-Zero map of the DSOCCF$_{dc}$ with different *a* values.

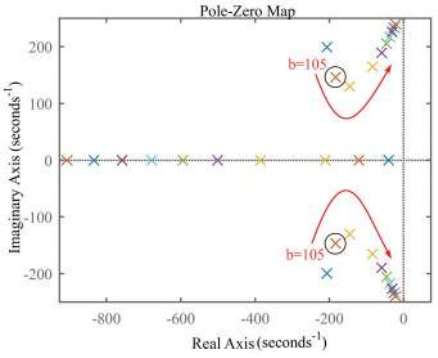

FIGURE 7. Pole-Zero map of the DSOCCF$_{dc}$ with different *b* values.

sequence component and has DC offset rejection capability is

$$DSOCCF_{dc}(s)=\frac{\xi\hat{\omega}s(s+j\hat{\omega})}{as^3+(b+2\xi\hat{\omega})s^2+a\hat{\omega}^2s+b\hat{\omega}^2} \tag{27}$$

It can be observed from the (27) that the proposed DSOCCF$_{dc}$ has three parameters. To ensure good dynamic performance and stability of the PLL in practical applications, it is necessary to select appropriate parameters.

According to the classical control theory, the closer the pole of the system transfer function is to the imaginary axis, the slower the dynamic response of the system; on the contrary, the farther the pole is from the imaginary axis, the faster the dynamic response of the system. First, the parameter ξ is set to 1, the parameter b is set to 100, and the pole change of the system transfer function when the parameter a takes different values is shown in Fig.6. It can be seen from the figure that with the increase of the parameter a, the pole of the system is away from the imaginary axis firstly. After the inflection point, the pole starts to approach the imaginary axis, indicating that there is an optimal value for parameter a, which makes the pole of the system transfer function farthest from the imaginary axis and the system dynamic response is fastest. At this time, $a = 1.5$.

Next, the influence of parameter b on the system performance will be analyzed. It can be known from the above that $a = 1.5$, ξ is set to 1, and the pole change of the system transfer function when parameter b takes different values is shown in Fig.7. As shown in the Fig.7, with the increase of parameter b, the poles of the system gradually approach the imaginary axis, indicating that the dynamic response of the system becomes slower and slower. Therefore, the value of b needs to comprehensively consider the dynamic response and the overshoot system. Here, we take the value of b when the overshoot is minimum, that is, $b = 105$.

From the above, three parameters of the system $a = 1.5$, $b = 105$, $\xi = 1$, then the transfer function of DSOCCF$_{dc}$ can be expressed as

$$DSOCCF_{dc}(s)=\frac{\hat{\omega}s(s+j\hat{\omega})}{1.5s^3+(105+2\hat{\omega})s^2+1.5\hat{\omega}^2s+105\hat{\omega}^2} \tag{28}$$

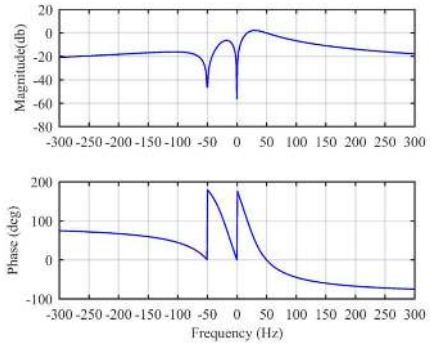

FIGURE 8. Bode diagram of DSOCCF$_{dc}$(s).

It can be found from (28) that there is a zero point at $s = -j\hat{\omega}$ and another zero point at $s = 0$, which shows that the fundamental frequency negative sequence component and DC offset of grid voltage can be completely eliminated at the same time in $\alpha\beta$-frame.

The bode diagram of DSOCCF$_{dc}$ is shown in Fig.8. According to Table I and Fig. 8, the DSOCCF$_{dc}$ can eliminate the frequency component of 0Hz and -50Hz in $\alpha\beta$-frame, it means that fundamental frequency negative sequence component and DC offset will be completely eliminated by using DSOCCF$_{dc}$. And the gain of the fundamental frequency positive sequence component at 50Hz is 0, and the phase is 0. This means that the amplitude and phase of the fundamental frequency positive sequence component is not affected at all.

DSOCCF$_{dc}$ completely eliminates the interference of the fundamental negative sequence component and DC offset by using the complex coefficient filter. However, DSOCCF$_{dc}$ can only suppress high frequency harmonics to a certain extent, but cannot completely block them.

IV. HYBRID FILTER -BASED PLL

A. DESIGN OF HYBRID FILTER BASED ON DSOCCF$_{dc}$ AND MAF

MAF is widely used in SRF-PLL due to its simple digital implementation, low computational burden and effectiveness under harmonic interference conditions. The MAF is capable of completely blocking all signals at integer multiples ($1/T_\omega$) Hz, usually placed in the control inner loop of the SRF-PLL.

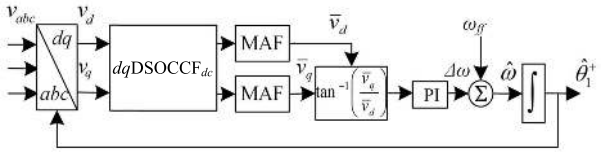

FIGURE 9. Block diagram of the proposed PLL.

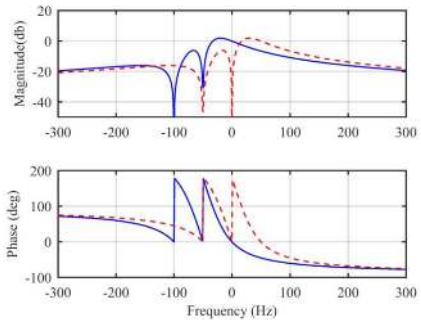

FIGURE 10. Bode diagram of DSOCCF$_{dc}$(s).

The hybrid filter based on DSOCCF$_{dc}$ and MAF proposed in this paper needs to transform DSOCCF$_{dc}$ from $\alpha\beta$-frame to dq-frame to obtain dqDSOCCF$_{dc}$, then dqDSOCCF$_{dc}$ and MAF are cascaded. The structure of SRF-PLL based on the hybrid filter is shown in Fig.9.

According to Table I, dqDSOCCF$_{dc}$ is responsible for eliminating the fundamental frequency negative sequence component and DC offset component corresponding to -100 Hz and -50Hz in the dq-frame. The MAF is responsible for blocking the harmonic components corresponding to $\pm$300Hz, $\pm$600Hz,, $\pm$900Hz.…

The transfer function of dqDSOCCF$_{dc}$ proposed in this paper can be obtained by replacing s in DSOCCF$_{dc}(s)$ with $s + j\hat{\omega}$ [37]. Equation (29), as shown at the bottom of this page.

The bode plots of DSOCCF$_{dc}(s)$ and dqDSOCCF$_{dc}(s)$ are shown in Fig.10, where the red dashed line represents DSOCCF$_{dc}(s)$ and the blue solid line represents dqDSOCCF$_{dc}$(s). It can be observed from the figure that dqDSOCCF$_{dc}$(s) can eliminate the fundamental frequency negative sequence component and DC offset component corresponding to -100Hz and -50Hz in the dq-frame.

Here, the concept of complex variable filter is employed to analyze dqDSOCCF$_{dc}$. The implementation of the complex variable filter is shown in Fig.11. The complex variable filter is actually a transfer function with dual input and dual output complex transformation [34]. The complex transfer function $H(s)$ can be expressed as the following form.

$$H(s) = R(s) + jQ(s) \tag{30}$$

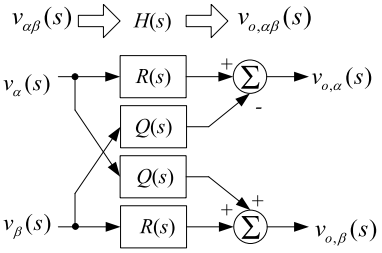

FIGURE 11. The implementation of complex filter.

It is worth mentioning that dqDSOCCF$_{dc}(s)$ has a structure of dual input and dual output, and its transfer function is also a complex transfer function, so it can be analyzed by the method of complex filter.

According to Fig.11 and (30), after mathematical manipulation, the real part $R(s)$ and the imaginary part $Q(s)$ of the dqDSOCCF$_{dc}(s)$ can be obtained as follows:

$$R(s) = \frac{as^5+(b+2\hat{\omega})\hat{\omega}s^4+5a\hat{\omega}^3s^3+4b\hat{\omega}^3s^2+4a\hat{\omega}^5s+4\hat{\omega}^6}{\theta_6 s^6+\theta_5 s^5+\theta_4 s^4+\theta_3 s^3+\theta_2 s^2+\theta_1 s+4\hat{\omega}^6} \tag{31}$$

$$Q(s) = -\frac{3a\hat{\omega}^2s^4+2(b+\hat{\omega})\hat{\omega}^2s^3-6a\hat{\omega}^4s^2-4(b+\hat{\omega})\hat{\omega}^4s}{\theta_6 s^6+\theta_5 s^5+\theta_4 s^4+\theta_3 s^3+\theta_2 s^2+\theta_1 s+4\hat{\omega}^6} \tag{32}$$

where $\theta_6 = a^2, \theta_5 = 2a(b+2\hat{\omega}), \theta_4 = 5a^2\hat{\omega}^2 + (b+2\hat{\omega})^2, \theta_3 = 12a\hat{\omega}^3 + 8ab\hat{\omega}^2,$

$$\theta_2 = 4(2a-1)\hat{\omega}^4 + 4b\hat{\omega}^3 + 4b^2\hat{\omega}^2, \theta_1 = 4a^2\hat{\omega}^5,$$
$$a = 1.5, b = 105.$$

The transfer function of MAF is

$$MAF(s) = \frac{1-e^{-T_\omega s}}{T_\omega s} \tag{33}$$

In this paper, the time window length T_ω is set to $T/6 = 0.0033$s, then the Bode diagram of the MAF is shown in Fig.12.

It can be seen from Fig.12 that when T_ω is set to 0.0033s, the MAF can filter harmonics of frequencies such as $\pm$300 Hz, $\pm$600 Hz, $\pm$900 Hz, etc.

The transfer function of the hybrid filter consisted with dqDSOCCF$_{dc}$ and MAF can be written as (34), as shown at the bottom of the next page.

Fig.13 shows the frequency response curve of the hybrid filter proposed in this paper. It can be observed that the fundamental frequency negative sequence component, DC offset component and other harmonic components in Table I can be rejected completely by the hybrid filter. There is no frequency

$$\begin{aligned} dq\text{DSOCCF}_{dc}(s) &= \text{DSOCCF}_{dc}(s+j\hat{\omega}) \\ &= \frac{\hat{\omega}s^2 - 2\hat{\omega}^3 + j3\hat{\omega}^2 s}{as^3 + (b+2\hat{\omega})s^2 - 2a\hat{\omega}^2 s - v2\hat{\omega}^3 + j[3a\hat{\omega}s^2 + 2(b+2\hat{\omega})\hat{\omega}s]} \end{aligned} \tag{29}$$

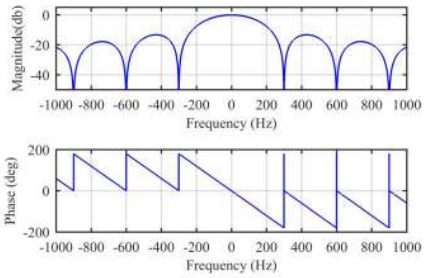

FIGURE 12. Bode diagram of MAF when T_ω =T/6=0.0033s.

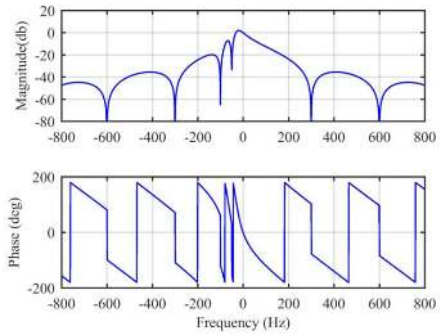

FIGURE 13. Frequency response of the proposed hybrid filter.

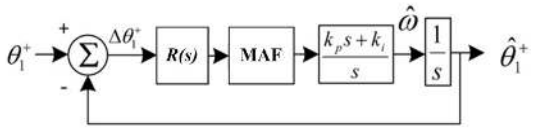

FIGURE 14. Mathematical model of the proposed PLL.

shifted for the fundamental frequency positive sequence component(at 0Hz) in the *dq*-frame, and the amplification factor is 1.

B. PARAMETER DESIGN GUIDELINES

As the structure of the proposed PLL has been shown in Fig.9, the frequency model of the proposed PLL can be simply obtained in Fig.14. According to the modeling method in [35], the dqDSOCCF$_{dc}$. is modeled by R(s) for mathematical modeling. The accuracy will be examined later by simulation.

The open-loop transfer function for the mathematical model is (35), as shown at the bottom of this page.

Because the existence of delay link in MAF in (35), the first-order Pade approximation approach is employed to replace the delay link as follows:

$$e^{-(T/6)s} \approx \frac{1 - sT/12}{1 + sT/12} \tag{36}$$

So

$$MAF(s) = \frac{1 - e^{-Ts/6}}{Ts/6} \approx \frac{1}{1 + sT/12} \tag{37}$$

The presence of the high-order components in (35) complicates the analysis and design PLL. According to the reduced order equivalent method of higher-order PLL system in [36], the Pade approximation reduction approach in [38] is adopted to equivalent R(s)•$MAF(s)$ as the first order transfer function. Equation (38), as shown at the bottom of this page.

So

$$Gol(s) \approx \frac{58.24}{s + 58.24}\frac{k_p s + k_i}{s^2} = \frac{1}{1 + s\underbrace{(1/58.24)}_{T_d}}\frac{k_p s + k_i}{s^2} \tag{39}$$

where, T_d is the delay factor of the system, which determines the bandwidth of the system.

To obtain the PI controller parameters for (39), this paper uses the symmetric optimal design method in [29] to give the two parameters of the PI controller as

$$k_p = 1/(bT_d) \quad k_i = 1/(b^3 T_d^2) \tag{40}$$

where $T_d = 1/58.24$, b is the design parameter for determining the phase margin (PM). In order to ensure the stability of the PLL system, b is set to $b = 1 + \sqrt{2}$, then $k_p = 24.1$ and $k_i = 241.2$. The frequency response curve of the system open-loop transfer function is shown in Fig.15. The PM is 59.9° and the corresponding frequency is 6.71Hz. The gain margin(GM) the PLL is 28.6dB, the corresponding frequency is 76Hz, so the system stability can be ensured.

$$\begin{aligned} H(s &= dqDSOCCF_{dc}(s)MAF(s) \\ &= \frac{\hat{\omega}s^2 - 2\hat{\omega}^3 + j3\hat{\omega}^2 s}{as^3 + (b + 2\hat{\omega})s^2 - 2a\hat{\omega}^2 s - 2\hat{\omega}^3 + j[3a\hat{\omega}s^2 + 2(b + 2\hat{\omega})\hat{\omega}s]}\frac{1 - e^{-T_\omega s}}{T_\omega s} \end{aligned} \tag{34}$$

$$\begin{aligned} Gol(s) &= \frac{\hat{\theta}_1^+}{\Delta\theta_1^+} = R(s)MAF(s)\frac{k_p s + k_i}{s^2} \\ &= \frac{as^5 + (b + 2\hat{\omega})\hat{\omega}s^4 + 5a\hat{\omega}^3 s^3 + 4b\hat{\omega}^3 s^2 + 4a\hat{\omega}^5 s + 4\hat{\omega}^6}{\theta_6 s^6 + \theta_5 s^5 + \theta_4 s^4 + \theta_3 s^3 + \theta_2 s^2 + \theta_1 s + 4\hat{\omega}^6}\frac{1 - e^{-Ts/6}}{Ts/6}\frac{k_p s + k_i}{s^2} \end{aligned} \tag{35}$$

$$\begin{aligned} &R(s)MAF(s) \\ &= \frac{as^5 + (b + 2\hat{\omega})\hat{\omega}s^4 + 5a\hat{\omega}^3 s^3 + 4b\hat{\omega}^3 s^2 + 4a\hat{\omega}^5 s + 4\hat{\omega}^6}{\theta_6 s^6 + \theta_5 s^5 + \theta_4 s^4 + \theta_3 s^3 + \theta_2 s^2 + \theta_1 s + 4\hat{\omega}^6}\frac{1}{1 + 0.02s/12} \approx \frac{58.24}{s + 58.24} \end{aligned} \tag{38}$$

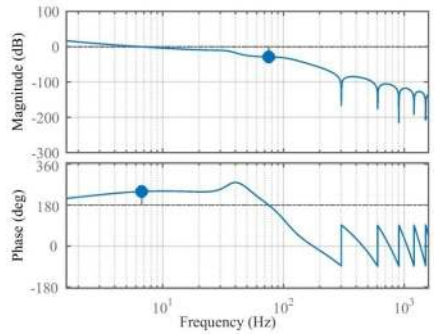

FIGURE 15. Open-loop bode diagram of proposed PLL.

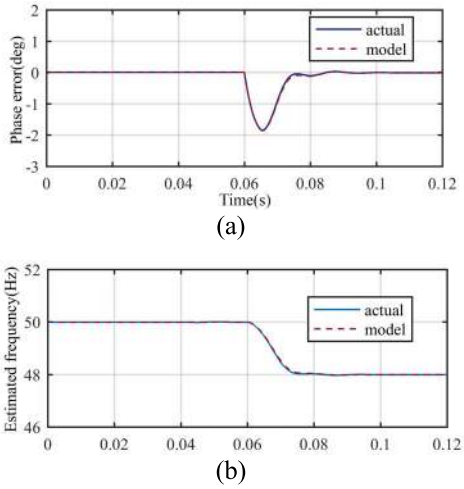

FIGURE 16. Performance comparison between proposed-PLL and its mathematical model. (a) phase error, (b) estimated frequency.

C. ACCURACY OF MATHEMATICL SIGNALMODEL

To verify the accuracy of the mathematical model, this section compares the proposed PLL and its mathematical model results under MATLAB / Simulink. In the simulation, the phase error and estimated frequency under frequency jump of −2Hz are compared respectively, as shown in Fig.16. It can be observed that high accuracy of the mathematical model can be verified.

V. SIMULATION RESULTS

To compare the performance of the proposed PLL with the PLL based on DFOCCF, the simulation of grid voltage unbalance fault and grid voltage distortion. are implemented. The comparison object is DFOCCF$_{\text{pi}}$-PLL, and its parameter design process and parameters are described in [37]. In the simulation, the grid frequency is 50 Hz, the three-phase voltage amplitude is normalized to 1 p.u, and the sampling frequency is 10 kHz.

A. TWO-PHASE VOLTAGE DROP

Fig.17 shows simulation waveforms when the two-phase voltage is dropped. Fig.17(a) is the three-phase grid voltage waveform, Fig.17(b) is the estimated frequency waveform of the three PLLs, and Fig.17(c) is the phase error waveform. It can be seen from Fig.17(a) that the grid fault of the two-phase drop occurs at 0.06s, and the fault returns to normal at 0.1 s after the fault lasts for 40 ms.

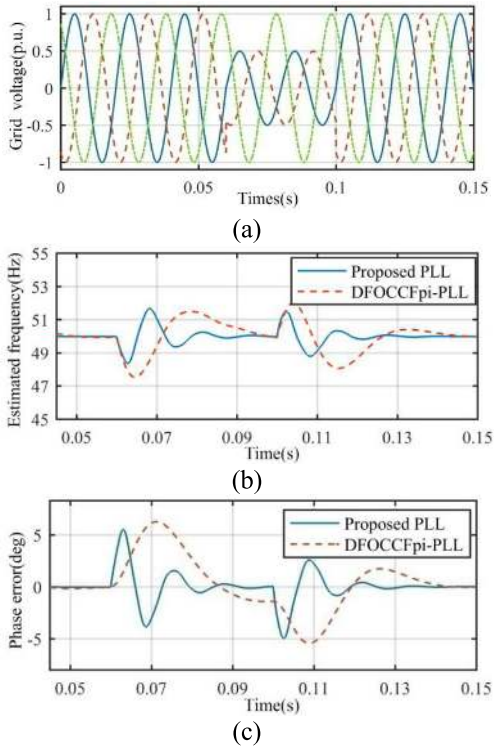

FIGURE 17. Simulation waveforms when grid voltage undergoes two-phase voltage sag. (a) three-phase grid voltages, (b) estimated frequency, (c) phase error.

By observing Fig.17(b) and (c), it can be seen that after the two-phase drop occurs at 0.06s and returns to normal at 0.1s, both PLLs fluctuate in phase error and estimated frequency. The recovery time of the proposed PLL to the stable equilibrium state is significantly shorter than that of the DFOCCF$_{\text{pi}}$-PLL, indicating that the dynamic performance of the proposed PLL is better than DFOCCF$_{\text{pi}}$-PLL.

B. SINGLE-PHASE VOLTAGE DROP AND DISTORTION VOLTAGE

Fig.18 shows the simulated waveforms when the grid voltage undergoes single-phase voltage drop and voltage distortion occur. Fig.18(a) shows the three-phase grid voltage waveforms, Fig.18(b) shows the frequency estimation waveform of the three PLLs, and Fig.18(c) shows the phase estimation waveform. The harmonic voltages are $V_1^+ = 1$p.u., $V_1^- = 0.1$p.u., $V_5^- = 0.1$p.u., $V_7^+ = 0.05$p.u., $V_{11}^- = 0.05$p.u., $V_{13}^- = 0.05$p.u.. It can be seen from Fig.18(a) that the grid fault of single-phase drop and harmonic voltage injection occur at 0.06s, and return to normal at 0.1s after 40ms.

It can be observed that during the 0.06s and 0.1s, the proposed PLL fluctuates in phase error and estimated frequency, but there is no ripple generated by harmonics. Since the

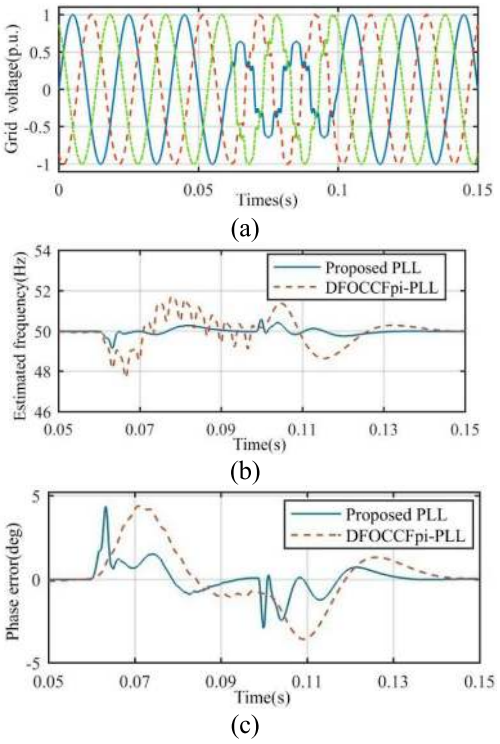

FIGURE 18. Simulation waveforms when grid voltage are distorted and undergoes one-phase voltage sag (a) three-phase grid voltages, (b) estimated frequency, (c) phase error.

DFOCCF$_{pi}$-PLL cannot completely eliminate the harmonic components of the input voltage, the ripple appears between 0.06s and 0.1s. In addition, the settling time of the proposed PLL is also less than that of DFOCCF$_{pi}$-PLL, indicating that disturbance rejection capability and dynamic behavior of the proposed PLL are better than DFOCCF$_{pi}$-PLL.

VI. EXPERIMENTAL RESULTS

To confirm the effectiveness of the proposed PLL, the experiments are implemented in this section and the experimental results are analyzed. The DSP TMS320F28335 is employed in the experiments. The experiments are based on the arbitrary waveform generator to generate three-phase voltage signals. The sampling frequency is set to 10kHz. The nominal frequency is set to $2\pi 50$ rad/s, and the amplitude is normalized to 1p.u.. The third-order Adams-Bashforth method in [33] is used to ensure the accuracy of the discrete system model and avoid algebraic loop. The corresponding relation between the integral link of the continuous domain and the discrete domain is as follows

$$\frac{y(s)}{u(s)} = \frac{1}{s} \Leftrightarrow \frac{y(z)}{u(z)} = \frac{T_s}{12}\frac{23z^{-1} - 16z^{-2} + 5z^{-3}}{1 - z^{-1}} \tag{41}$$

$$y(n) = y(n-1) + \frac{T_s}{12} \times [23u(n-1) - 16u(n-2) + 5u(n-3)] \tag{42}$$

where, T_s is the sampling period and u and y are the inputs and outputs of the integrator, respectively.

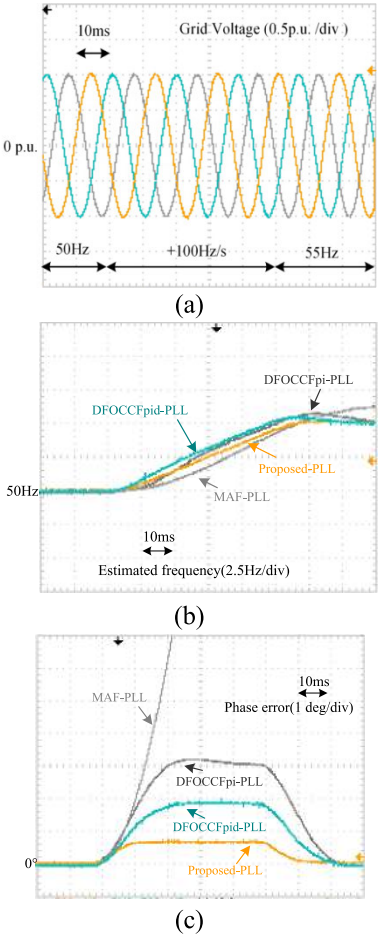

FIGURE 19. Experimental waveforms with ramp changes in the frequency of three-phase voltages. (a) three-phase grid voltages, (b) estimated frequency, (c) phase error.

Since the proposed PLL method in this paper adopts the structure of the complex coefficient filter and the MAF method, the traditional methods based on the first-order complex coefficient filtering such as the DFOCCF$_{pi}$-PL, DFOCCF$_{pid}$-PLL [37] and the MAF-PLL [22] are used in comparative experiments. The parameter design process and parameters of the three methods can be found in [37] and [39].

A. FREQUENCY RAMP CHANGE

Fig.19 shows the experimental waveform of the three-phase grid voltage (Fig.19a), the frequency estimation waveform of the four PLLs (Fig.19b) and the phase estimation error waveform (Fig.19c) when the grid voltage frequency is ramp changed from 50 Hz to 55 Hz. Where, the grid voltage frequency gradual rate is 100Hz/s, and the increasing process lasts for 50ms.

As shown in Fig.19, with the gradual increase of grid frequency, the phase tracking error of the proposed PLL is 0.8 °. which is the smallest compared with the other three PLL errors and can accurately estimate the phase. The phase estimation errors of DFOCCF$_{pi}$-PLL and DFOCCF$_{pid}$-PLL are 1.9 ° and 3.1 ° respectively, and the phase estimation

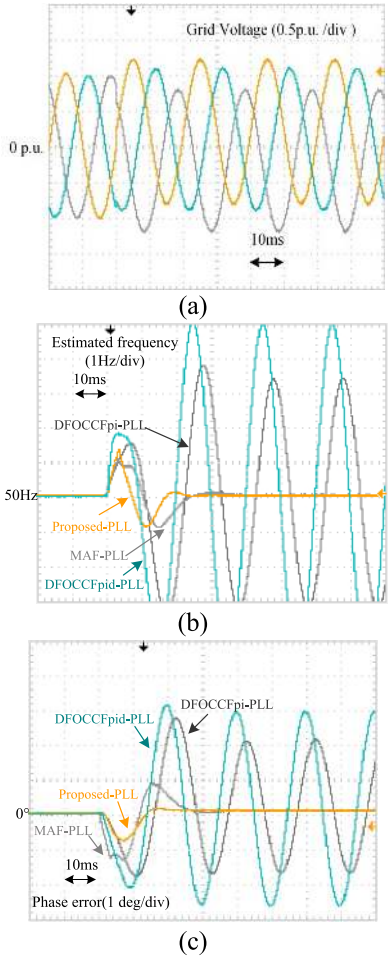

FIGURE 20. Experimental waveforms when three-phase voltages are mixed with DC offset. (a) three-phase grid voltages, (b) estimated frequency, (c) phase error.

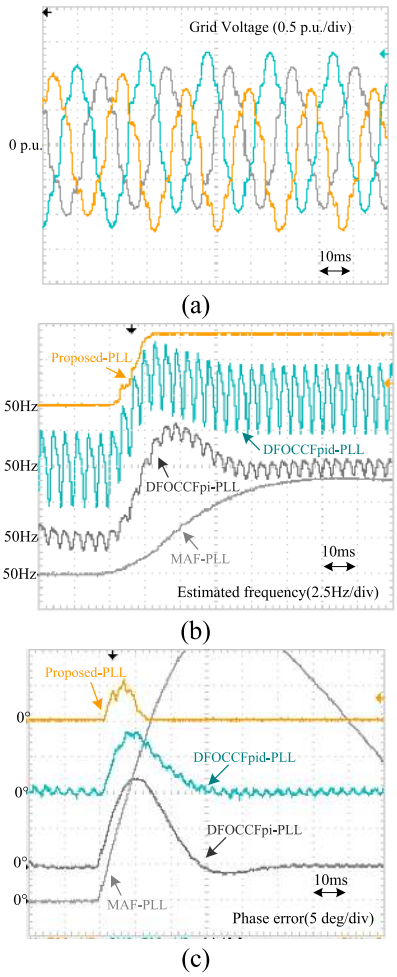

FIGURE 21. Experimental waveforms when three-phase voltages are mixed with harmonic. (a) three-phase grid voltages, (b) estimated frequency, (c) phase error.

errors of MAF-PLL are too large to be accepted. Therefore, when the grid frequency changes continuously, the proposed PLL can track the phase more accurately.

B. DC OFFSET INJECT

In order to verify the DC offset rejection capability, the DC offset injection experiment is carried out. The DC offset injected values of the three-phase voltage are $V_a = 0.2$p.u., $V_b = 0.1$p.u., and $V_c = -0.2$p.u. Fig.20 shows the experimental waveform of the three-phase grid voltage (Fig.20a), the estimated frequency of the four PLLs (Fig. 20b) and the phase error (Fig. 5.20c) when the grid voltage is injected with DC offset.

It can be seen that there are fluctuations in the waveforms of the phase error and the estimated frequency of the proposed PLL and MAF-PLL when the grid voltage undergoes DC offset injection. The dynamic adjustment time of the proposed PLL is shorter than that of MAF-PLL, which is 1.5 grid cycles. Since DFOCCF$_{\text{pi}}$-PLL and DFOCCF$_{\text{pid}}$-PLL do not have the capability to eliminate DC offset, their waveforms have a 50 Hz oscillation.

C. UNBALANCED AND DISTORTED GRID VOLTAGES

Fig.21 shows the experimental waveform when the grid voltage is distorted and the grid frequency of the has a abrupt change of +5Hz, the injected harmonic voltage waveform parameters are consistent with the parameters in previous simulation section. The experimental waveform of the three-phase grid voltage is shown in Fig.21(a). The estimated frequency waveforms of the four PLLs are shown in Fig.21(b), and the phase error waveforms are shown in Fig.21(c).

It can be observed that the proposed PLL and MAF-PLL can completely eliminate the interference of harmonic components when the grid frequency is changed from the initial 50Hz to the 55Hz. But the waveforms of DFOCCF$_{\text{pi}}$-PLL and DFOCCF$_{\text{pid}}$-PLL have oscillation errors caused by harmonics.

D. SIMULATION AND EXPERIMENTAL RESULTS ANALYSIS

The proposed PLL in this paper employs second-order complex-coefficient filter, so its dynamic performance is superior to that of the DFOCCF$_{\text{pi}}$-PLL and DFOCCF$_{\text{pid}}$-PLL using first-order complex-coefficient filter. Its settling time

is the shortest under all experimental conditions. In addition, the proposed PLL can completely eliminate the fundamental frequency negative sequence component, DC offset component and harmonic components in Table I, and the three-phase grid voltage drop will not affect its tracking performance for phase and frequency.

$DFOCCF_{pi}$-PLL and $DFOCCF_{pid}$-PLL are based on first-order complex-coefficient filter, so their dynamic performance is not as good as the proposed PLL. The response speed of $DFOCCF_{pid}$-PLL is slightly faster than $DFOCCF_{pi}$-PLL, because the parameters of $DFOCCF_{pid}$-PLL are optimized by PID. In addition, the $DFOCCF_{pi}$-PLL and $DFOCCF_{pid}$-PLL only can block the fundamental voltage negative sequence component, but cannot reject DC offset component and harmonic components, so their disturbance rejection ability is insufficient.

Compared with the other three PLLs, the dynamic response speed of MAF-PLL is too slow and its dynamic performance is unsatisfactory due to the large time window parameters of the delay link, so it is not suitable for grid connected applications.

VII. CONCLUSION

In this paper, a novel $DSOCCF_{dc}$ structure which can completely reject the fundamental frequency negative sequence component and DC offset component is proposed based on high-order complex filter. And a new hybrid filter composed of $DSOCCF_{dc}$ and MAF is designed, then the mathematical model of the hybrid filter based-PLL is established. The validity of the proposed PLL is verified by simulation and different grid voltage experiments, and the experimental results show that the proposed method has strong filtering ability and DC offset elimination ability, and its dynamic behavior meet the requirements of grid connected application.

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