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Design of a Low Power Dissipation and Low Input Voltage Range Level Shifter in Cedec 0.18-µm Cmos Process

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Abstract: Level shifter (LS) circuits are widely used as an interface for multiple voltage domains in modern ICs and System on Chips (SoCs). Low power dissipation is one of the main design considerations for high performance level shifters. This paper presents the design and performance of a low power dissipation and low input voltage range level shifter in CEDEC 0.18-µm CMOS process. Simulation results shows that the level shifter is able to perform voltage level shifting from low voltage level of 0.4 - 0.7 V into high voltage level of 3 V. The obtained power dissipation is only 1.49 nW for 0.4 V and 1-kHz input pulse. This level shifter fulfills the needs of lower power systems and will be very useful for ICs and SoCs.

Key words: CMOS · Level Shifter · Output Driver · Low Loss · IC · SOC

INTRODUCTION

The most effective and direct way to reduce power dissipation in VLSI and other electronic circuits is to reduce their supply voltage because of their quadratic dependence of the power dissipation on the supply voltage [1-3]. With increase in power consumption, reliability problem also rises and cost of packaging goes high [4]. CMOS technology is being aggressively scaled to meet the increasing demand for low power, low area and high performance ICs [5-6].

Level shifters are circuits used to communicate between the two voltage domains from low voltage level to high voltage level. However, the conventional level shifters have weakness of large power dissipation, delay variation due to different current driving capabilities of transistors and fail to operate at low supply core voltage (V_{DDL}) [7]. In many applications especially in portable devices, the need for low power dissipation has become a necessity. Hence, the use of low power dissipation level shifters with low input voltages is very important.

The level shifters need to be operated correctly when the difference between the two voltages is high. Under such a case, conventional circuit topologies may result in a failure in proper functionality due to low drive current when supply voltage reduces and the conventional LS circuits cannot pull down voltages [8]. Previous researchers have proposed many solutions to address the problem of conventional level shifter [9-16]. However, these circuits still depend on the difference of the voltage supply [9-12], required a complex and large area due to the use of capacitor [13-14] and using algorithms for low supply voltage that is implemented using c++ [15]. Ashouei et. al. has proposed a design with large number of transistors that only capable of converting a small voltage range between 0.31V to 1.32V [16].

Osaki *et al.* proposed an input/output voltage monitoring technique (CMOS technology) for the ultra-low voltage digital in level shifter circuit design that has a feature in a current generation circuit [8]. Their design is capable of converting extremely low voltage signals to high voltage signals but the power dissipation in the circuit is high which can be improved by proper modification of dimensions of the transistors. Therefore, in this paper, we present a level shifter circuit having same design proposed by Osaki et. al. [8] but in 0.18-µm CMOS process with significant improvement in power dissipation.

Conventional Level Shifter: The schematic of a conventional level shifter is shown in Figure 1.

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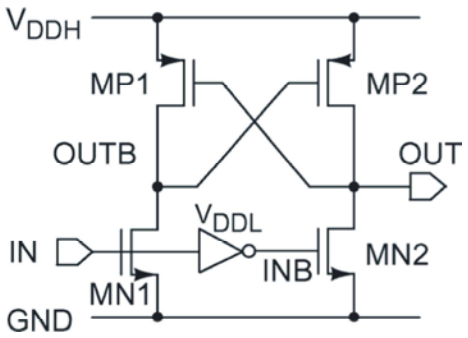

Fig. 1: Schematic of the conventional level shifter [8]

In a level shifter switching is performed when the state of the cross-coupled PMOS latch (MP_1, MP_2) is changed by the NMOS driver transistors (MN_1, MN_2). Both of PMOSs and NMOSs have been driven by complementary inputs signals of IN and INB. The circuit encounters serious problem if there is a big difference between the low voltage supply (V_{DDL}) and high supply voltage (V_{DDH}).

MN_1 and MN_2 are off and on, respectively when the voltages of IN is low and INB is high. MN_2 then pulls down node OUT, causing MP_1 to turn on. Further, the increase value that occurred in OUTB to the V_{DDH} will cause, MP_2 turns off and OUT drops to the GND level. The drive currents of both pull-up transistor MP_2 and pull-down transistor MN_2 will actually determined the voltage of OUT. Therefore, if the drive current of MP_2 is larger than that of MN_2, OUT cannot be discharged.

On the other hand, when IN is high and INB is low, the transistor MN_1 turns on and MN_2 turns off. The node OUT is still low and would start to go up only after node OUTB has dropped one threshold voltage (Vth) below V_{DDH}. Consequently MN_1 has to sink the load discharge current as well as an extra short circuit current that is flowing from MP_1.

Proposed Level Shifter: In the modified level shifter by Osaki *et al.* [8], the circuit consists of two main parts, namely current generation circuit and level conversion circuit. The complementary input signals of IN and INB are applied to both of the circuits and the output signal OUT is applied to the current generation circuit. The current generation circuit feeds the operating current to the level conversion circuit. Figure 2 shows the circuit diagram of proposed level shifter.

Level Conversion Circuit: This part of circuit is based on a conventional two-stage comparator circuit. The comparator generates output voltage signal according to the voltage difference of the inputs, IN and INB. The drive currents of pull-up transistor MP_6 and pull-down transistor MN_8 will determined the voltage of OUT and that the currents flowing in MP_6 and MN_8 depend on the current flowing through MP_2. Therefore, as both the driving current is determined by the same current flowing through the MP_2, the circuit free of constraints discussed in the conventional level shifter.

Current Generation Circuit: The current generation circuit consists of two blocks, transition current generator (IF_{GEN}) and rise transition current generator (IR_{GEN}). The power dissipation of the circuit is able to be minimized due to the operating of the circuit that only supplies an operating current when the input and output logic levels do not correspond to each other. The amount of generated currents depends on lower supply voltage of V_{DDL}.

- IF_{GEN}: The fall transition current generator IF_{GEN} consists of two nMOSFETs (MN_1 and MN_2) connected in series and monitors the voltages of INB and OUT. IF_{GEN} does not operate when the logic level of IN is high (i.e. INB is low) because IF_{GEN} is used to generate a fall-transition current for the level shifter circuit. When the input logic level is low and the output logic level is also low, the current generation circuit does not supply any current for the level conversion circuit because MN_2 is off with the low logic level of OUT. However, when IN and OUT do

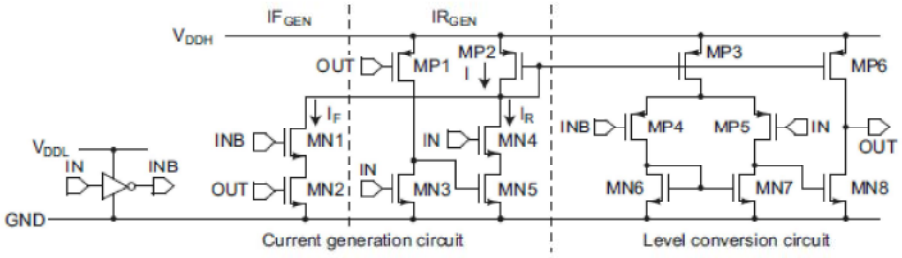

Fig. 2: The circuit diagram of proposed level shifter [6].

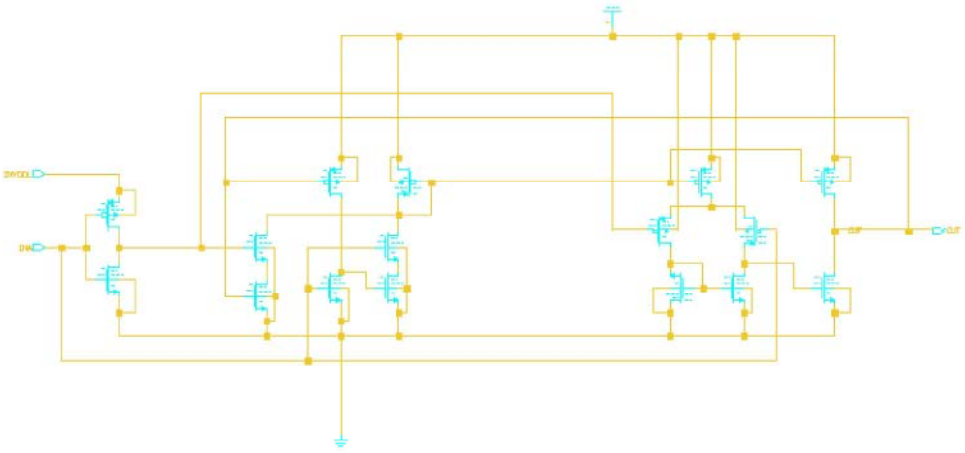

Fig. 3: The circuit diagram of modified proposed level shifter

Table 1 : Transistor Sizes of Modified Proposed Circuit

Transistor	Design 1 (W/L)	Design 2 (W/L)	Design 3 (W/L)	Design 4 (W/L)	Design 5 (W/L)
PMOS	2µ/0.18µ	2µ/0.18µ	1.4µ/0.18µ	1.4µ/0.18µ	1µ/0.18µ
NMOS	2µ/0.18µ	1µ/0.18µ	1.4µ/0.18µ	1µ/0.18µ	1µ/0.18µ

not correspond (i.e. IN, INB and OUT are low, high and high, respectively), the current IF flows because both of the voltages of INB and OUT are high. The current IF pulls OUT down to GND so that the input and output logic levels corresponds each other.

- IR_{GEN}: The rise transition current generator IR_{GEN} consists of three nMOSFETs (MN_3, MN4 and MN_5) and a pMOSFET (MP_1) $_{and}$ monitors the voltages of IN and OUT. IR_{GEN} does not operate when the logic level of IN is low because IR_{GEN} is used to generate a rise-transition current for the level shifter circuit. As is the case in the IF_{GEN}, when the input logic level is high and the output logic level is also high, the current generation circuit does not supply any current because the output voltage of the first stage in the IR_{GEN} becomes low. However, when IN and OUT do not correspond (i.e. IN, INB and OUT are high, low and low, respectively), the IR_{GEN} generates the current of *IR* and operates so that the input and output logic levels correspond each other. When IN and OUT are high and low, respectively, the output voltage of the first stage becomes High level because the overdrive voltage for the MP_1 is larger than that of MN_3. This enables MN_4 and MN_5 to supply the current *IR* for the level conversion circuit. And the current *IR* pulls OUT up to V_{DDH} [8].

$$(I = I_F + I_R) \quad (1)$$

Modified Proposed Level Shifter: In the current work, the main focus is to reduce the power dissipation of the proposed level shifter circuit by doing modifications to the dimensions of the transistors. As the dynamic power dissipation can be reduced by minimizing the size of the gate which in turn reduces both the length and the width of the transistor [12][17]. Figure 3 shows the circuit diagram of proposed level shifter after modification and Table 1 shows the dimensions of the transistors.

Simulation Result: Five designs are simulated with CEDEC 0.18-µm CMOS process. The simulation has been carried out with low supply voltage V_{DDL} within a range of 0.4V-0.7V and high supply voltage V_{DDH} 3V. The frequency f_{IN} was set to 1 kHz.

Waveform: Figure 4 - 6 show the simulated waveforms. As shown in Figure 4, the core voltage 0.4V has successfully shifted into 3V. Figure 5 shows that the low supply voltage of 0.5V significantly converted to 3V. The modified proposed level shifter were also able to perform voltage level shifting from 0.6V and 0.7V into high voltage level of 3 V. These can be seen clearly from Figure 6 and 7.

When there is a transition of input signal IN from low level to high level,there was a period when the logic level of IN did not correspond to that logic of OUT. That period will be detected by IRGEN and current of IR will be generated. The current *IR* ..... was supplied to the level

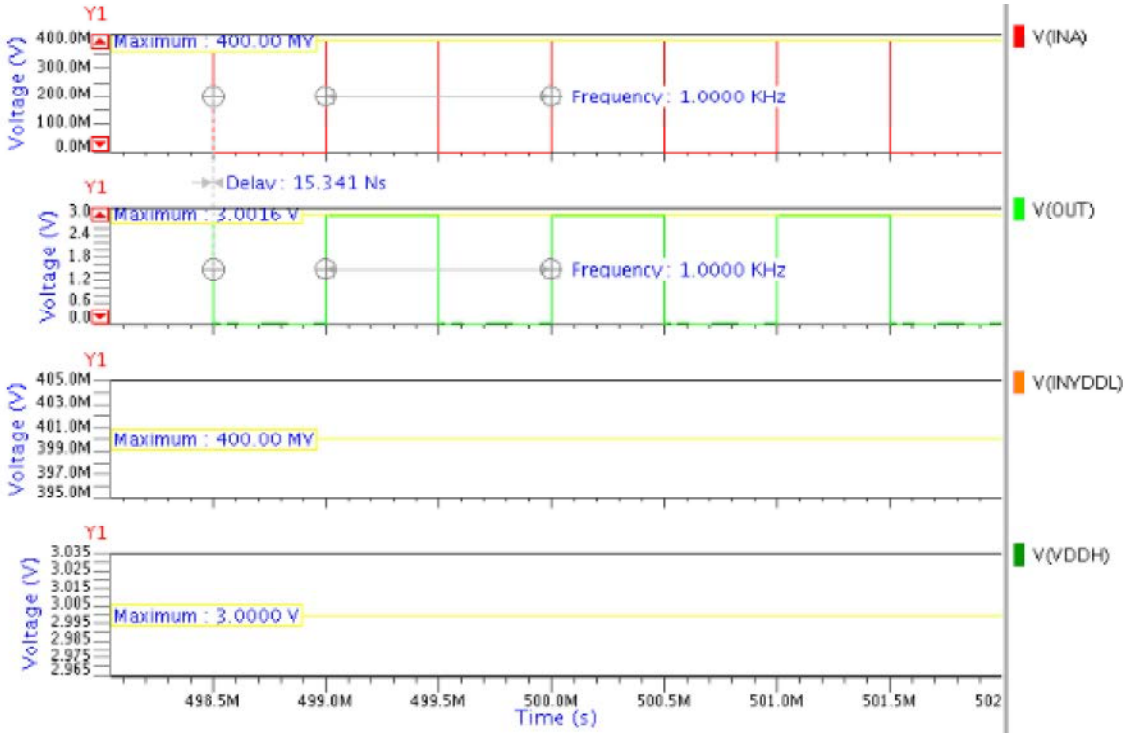

Fig. 4: Simulation results of level shifter for a supply low voltage VddL 0.4V

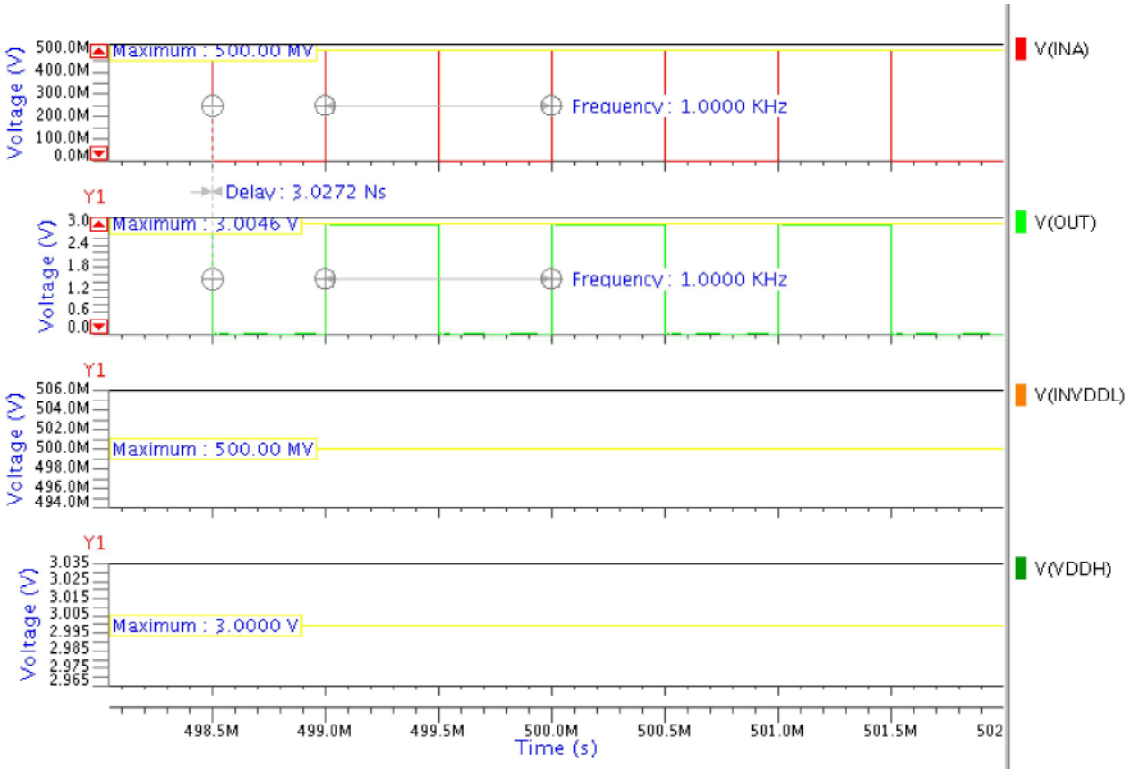

Fig. 5: Simulation results of level shifter for a supply low voltage VddL 0.5V

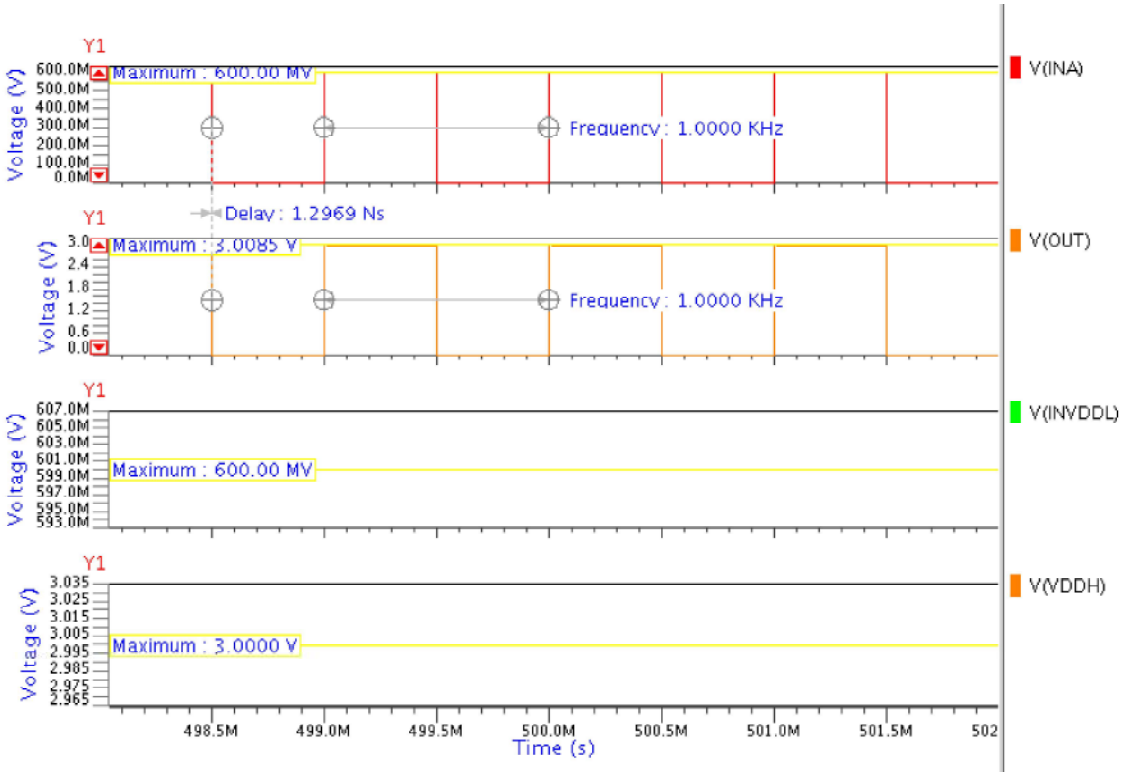

Fig. 6: Simulation results of level shifter for a supply low voltage VddL 0.6V

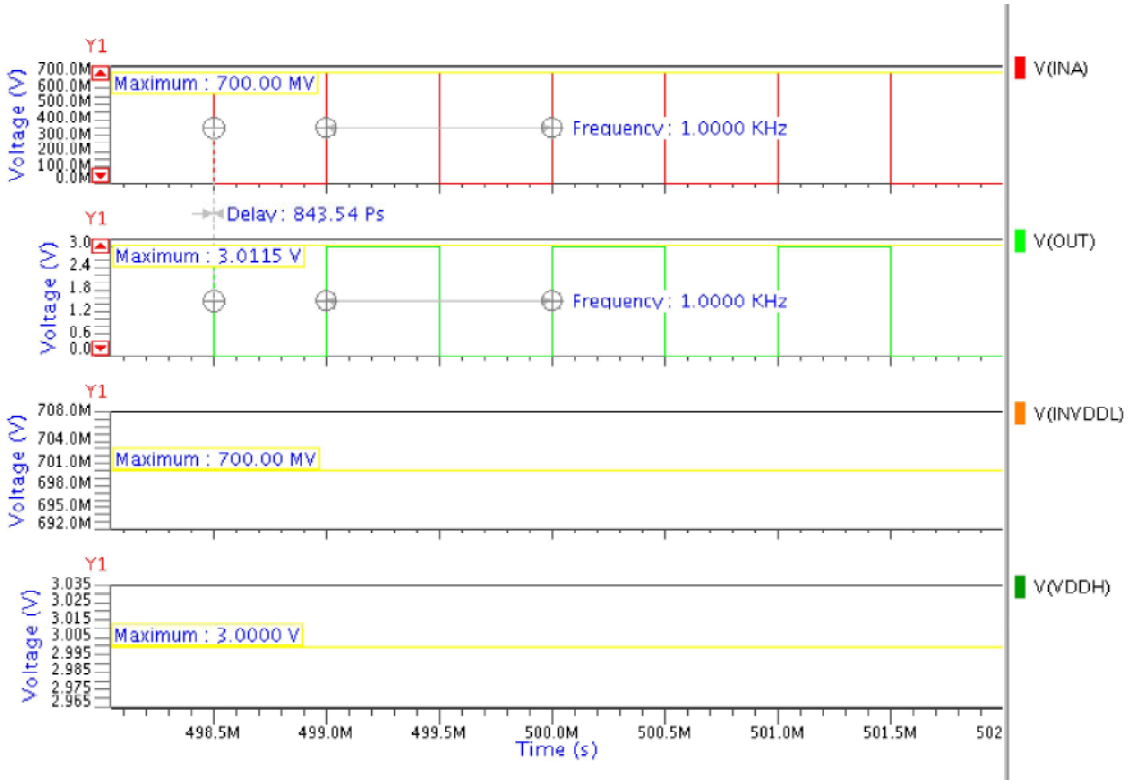

Fig. 7: Simulation results of level shifter for a supply low voltage VddL 0.7V

Table 2: Simulation Results of Power Dissipation and Delay

Design (W/L)	V_{DDL} (V)	Power Dissipation (nW)	Delay (ns)
PMOS 2.0µ/0.18µ	0.4	2.3671	18.851
NMOS 2.0µ/0.18µ	0.5	2.3217	3.4071
	0.6	2.3385	1.261
	0.7	2.3227	0.8576
PMOS 2.0µ/0.18µ	0.4	1.5861	15.213
NMOS 1.0µ/0.18µ	0.5	1.5842	3.0221
	0.6	1.5126	1.2572
	0.7	1.5848	0.8354
PMOS 1.4µ/0.18µ	0.4	1.8233	16.998
NMOS 1.4µ/0.18µ	0.5	1.8234	2.7498
	0.6	1.8233	0.8364
	0.7	1.8248	0.3527
PMOS 1.4µ/0.18µ	0.4	1.533	15.363
NMOS 1.0µ/0.18µ	0.5	1.5317	2.9946
	0.6	1.5325	1.2819
	0.7	1.5339	0.8294
PMOS 1.0µ/0.18µ	0.4	1.4872	15.341
NMOS 1.0µ/0.18µ	0.5	1.489	3.0272
	0.6	1.4918	1.2969
	0.7	1.4957	0.8435

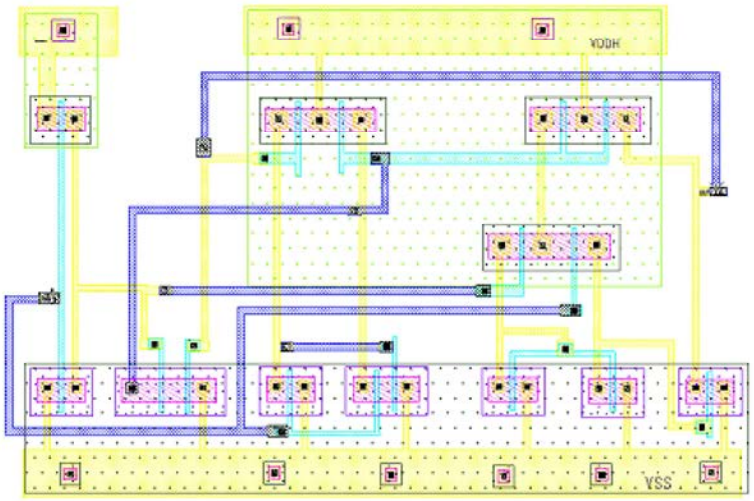

Fig. 8: A layout design of the modified proposed level shifter

conversion circuit and the circuit converted the 0.4-V input signal into the 3-V output signal. At this period, current *IF* will not be generated by the IFGEN. Instead, when the input signal of IN changed to low level of GND, the IFGEN generated current of *IF* ..... while the IRGEN did not generate current of *IR* ..... The proposed level shifter circuit can convert a range of low voltage input into high voltage of 3V because both of drive currents in pull-up and pull-down transistor depend on the generated current by current generation circuit.

Power Dissipation and Delay: Modified proposed level shifters with transistor sizing have been simulated and a better performance is obtained in terms of power dissipation. Table 2 shows the results for the power dissipation and delay of each modified transistor as function of V_{DDL} at V_{DDH}= 3V and f_{IN}=1 kHz. The modified level shifter with both PMOS and NMOS transistors equally size W/L = 1µ/0.18µ gives the lowest power dissipation of 1.49 nW compared to 6 nW with existing proposed level shifter. Result shows the decreasing in power dissipation in modified proposed level shifter with application of transistor sizing.

Figure 8 shows the layout of the modified level shifter. The layout is presented using size for each cell of the PMOS and NMOS, W/L = 1.0µ/0.18µ.

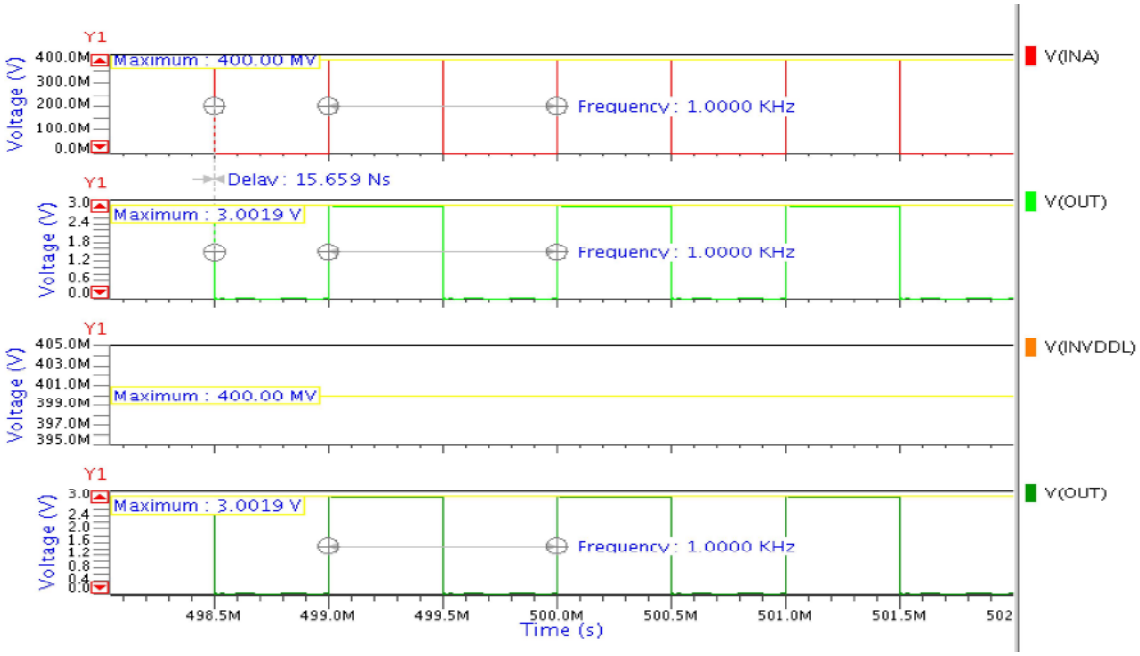

Fig. 9: Simulation result after parasitic extraction at V_{DDL} 0.4V

Table 3: Comparison Result Before and after Pex Simulation

V_{DDL} (V)	Power Dissipation (nW)	Before PEX Delay (ns)	After PEX Delay (ns)	% Difference of the Delay
0.4	1.4872	15.3410	15.6960	2.31
0.5	1.4890	3.0272	3.0485	0.71
0.6	1.4918	1.2969	1.3051	0.63
0.7	1.4957	0.8435	0.8488	0.63

Table 4: Comparison Performance of Level Shifter

Reseach	Technology	Type	VDD Independence	V_{DDL}(V)	V_{DDH}(V)	Frequency	Power Dissipation (nW)
This work	0.18- µm	Comparator	Yes	0.4	3.0	1kHz	1.49
[8]	0.35- µm	Comparator	Yes	0.4	3.0	1kHz	6.0
[9]	0.35- µm	Latch	No	0.1	1.0	1MHz	6.6
[10]	0.35- µm	Current Mirror	Yes	3.3	10.0	500MHz	N/A
[11]	0.18- µm	Latch	No	0.13	1.8	100kHz	N/A

Parasitic Extraction: Parasitic extraction of electronic design automation is an important aspect in the calculation of the effects of parasites found in both the design and wiring devices in electronic circuits. The parasitic can be included as parasitic capacitances, parasitic resistances and parasitic inductances [18, 19]. The major purpose of parasitic extraction is to extracts the parasitic from completed layout in order to ensure an accurate analog model of the circuit can be created. At low frequencies parasitic capacitance is usually negligible, but in high frequency circuits it can be a major problem. The main factor limiting the high frequency performance is the existence of a parasitic capacitance found between the base and collector of transistors and other active devices. The modified circuit has been simulated with parasitic extraction to ensure that the function of this circuit design is within the specifications.

Figure 9 shows the simulation result after parasitic extraction. Simulations have been performed for the Design 5 of the modified circuit within all input voltage range, but only the simulation wave for 0.4V is included here. However, the attached of Table 3 clearly shows the difference before and after extraction of the parasitic.

Delay was defined as the period when the input voltage signal was converted into the high output voltage signal. From simulation, we have found that the delay for the modified proposed level shifter after parasitic extraction is increased with a small percentage between 0.6 to 2.3 percentages only. This is because of the parasitic coupling capacitance between drain and gate terminals in MP_6 can be reduced by adding a bypass capacitor between the gate voltage of MP_2 and V_{DDH} or GND.

Performance Comparison of Level Shifter: A performance comparison of the level shifter in this work with others has been done and it is shown in Table 4. From the comparison, it is proof that the modified proposed level shifter shows better performance in terms of power dissipation and able to work within wide range of low input voltage supply.

CONCLUSION

This paper proposes a level shifter for wide range of low input voltage and has an improved design having the advantage of high power efficiency. The proposed level shifter modifies the circuit design with the use of transistor length and width sizing using CEDEC 0.18-µm CMOS process to achieve a wide operating range with a better performance of low power dissipation. The simulation result shows that the circuit design is able to convert low voltage signals within a range of 0.4V-0.7V to high voltage signals of 3V at 1 kHz and only dissipates 1.49 nW power during operation. The proposed level shifter with extremely low power dissipation will lead the researchers to construct better performance devices.

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