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Design of a Novel Fault Tolerant Reversible Full Adder for Nanotechnology Based Systems

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Abstract: Reversible computation plays an important role in the synthesis of circuits having application in quantum computing, low power CMOS design, bioinformatics and nanotechnology-based systems. Conventional logic circuits are not reversible. A reversible circuit maps each input vector, into a unique output vector and vice versa. We demonstrate how the well-known and very useful, Toffoli gate can be synthesized from only two parity-preserving reversible gates. Parity preserving reversible gates refers to those reversible gates for which the parity of the outputs matches that of the inputs. The proposed parity preserving Toffoli gate renders a wide class of circuit faults readily detectable at the circuit's outputs. It allows any fault that affects no more than a single signal to be detectable at the circuit's primary outputs. We show that our proposed parity-preserving Toffoli gate is much better in terms of number of reversible gates, number of garbage outputs and hardware complexity with compared to the existing counterpart. Then we apply the proposed fault tolerant Toffoli gate to the design of a fault tolerant reversible full adder, which is a versatile and widely used building block in computer arithmetic.

Key words: Quantum computing . nanotechnology based systems . full-adder . fault tolerant . reversible computing

INTRODUCTION

Irreversible hardware computation results in energy dissipation due to information loss. According to R. Landauer's research in the early 1960s, the amount of energy (heat) dissipated for every irreversible bit operation is given by KTln2, where $K = 1.3806505*10^{-23}JK^{-1}$ is the Boltzmann constant and T is the operating temperature [1]. In 1973, Bennett showed that KTln2 energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs [2, 3]. A gate or a circuit is said to be reversible if there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs [4-6]. Thus, reversible logic gates (or circuits) are information-lossless. Furthermore, reversible gates are of major interest in optical computing, low power design, quantum computing and nanotechnology based systems. It is not possible to realize quantum computing without reversible logic.

Neither feedback (loop) nor fan-out is permitted in reversible logic circuits. Thus, synthesis of reversible logic is different from conventional logic synthesis [8]. It is also more difficult to make a fault-tolerant reversible circuit than a conventional logic circuit.

MATERIALS AND METHODS

Reversible Logic Gates: There is a number of commonly used reversible logic gate such as Feynman Gate, FG [7], Toffoli Gate, TG [8], Fredkin Gate, FRG [9], New Gate, NG [10], Feynman Double Gate, F2G [11] and Peres Gate, PG [15].

A 2*2 Feynman Gate, also known as controlled NOT (1-CNOT), is depicted in Fig. 1. It imp lements the logic functions: P = A and Q = A⊕B.

A 3*3 Toffoli Gate has 3 inputs: 2 control inputs, that are copied to the first 2 outputs and one other input that is complemented if all control inputs are 1s and is directly copied to the last output otherwise [11]. A 3-input, 3-output Toffoli Gate is shown in Fig. 2. The inputs 'A' and 'B' are passed as first and second outputs respectively. The third output is controlled by 'A' and 'B' to invert 'C'.

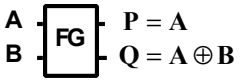

Fig. 1: Feynman gate

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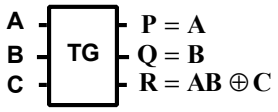

Fig. 2: Toffoli gate

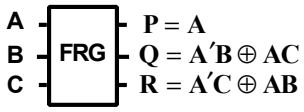

Fig. 3: Fredkin gate

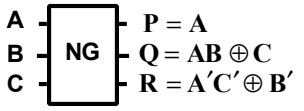

Fig. 4: New gate

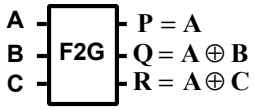

Fig. 5: Feynman double gate

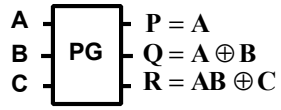

Fig. 6: Peres gate

A 3*3 Fredkin Gate is shown in the Fig. 3. Here the input 'A' is passed as first output. Inputs 'B' and 'C' are swapped to get the second and third outputs, which is controlled by 'A'. If A = 0, then the outputs are simply duplicates of the inputs; otherwise if A = 1, then the two input lines (B and C) are swapped.

A 3*3 New Gate (NG) is depicted in Fig. 4. It can be defined as I_v = (A, B, C) and O_v = (P = A, Q = AB⊕C, R = A′C′⊕B′). Where I_v and O_v are the input and output vectors.

A 3*3 Feynman Double Gate is depicted in Fig. 5. The F2G gate is a Feynman Gate with an additional input and one more output. The extra input and output, along with the control input "A" define a second controlled NOT operation.

A 3*3 Peres Gate (PG), is equivalent to the transformation produced by a Toffoli Gate followed by a Feynman Gate. Fig. 6 shows the block diagram of 3*3 Peres Gate (PG). Several other types of reversible gates have also been used.

Parity preserving reversible gates: Most of arithmetic and other processing functions do not preserve the parity of the data. Parity checking is one of the most widely used methods for error detection in digital logic systems. The author of [12, 13] performed arithmetic operations on specially encoded operands in a way that parity checking becomes applicable. But such methods are not in widespread use. There are some problems using standard methods of error detection in reversible logic circuits, because fan-out is not permitted and it may increase the number of gates. On the other hand, we should care of number of garbage outputs. Garbage output refers to the output that is not used for further computations [14].

Table 1: Truth table of the paity preserving fredkin gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Table 2: Truth table of the paity preserving feynman double gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

A sufficient requirement for parity preservation of a reversible circuit is that each gate be parity preserving. In this case the input and output data can be checked in a manner that is off the computation's critical path. We need parity-preserving reversible gates in order to construct parity-preserving reversible circuits. There exist some parity-preserving reversible gates. It is to be noted that of the gates depicted in Fig. 1-6, only the gates FRG and F2G are parity-preserving. The corresponding truth table of the gates FRG and F2G are shown in the Table 1 and 2 respectively. It can be verified from the truth tables that the input pattern corresponding to a particular output pattern can be uniquely determined. These gates are parity preserving gates. This is readily verified by comparing the input parity A⊕B⊕C to the output parity P⊕Q⊕R. In the other words, these gates satisfy the relation A⊕B⊕C = P⊕Q⊕R.

DESIGN OF PARITY PRESERVING REVERSIBLE CIRCUITS

New Parity Preserving Reversible TG Circuit: In this section, we show how the functionality of the well-known and very useful Toffoli gate can be synthesized by using only two parity preserving reversible gates. Then we apply it to the design of a binary fault tolerant reversible full adder circuit.

A parity preserving reversible TG circuit is presented in [11], which is shown in Fig. 7. The circuit requires three reversible gates (one Fredking gate and two F2G gates) and produces two garbage outputs.

Our proposed design is depicted in Fig. 8 respectively. The circuit shows how one FRG gate and one F2G gate can be used to synthesize a parity-preserving Toffoli gate. It produces one garbage output.

New parity preserving reversible full adder: We next show how the proposed parity preserving reversible Toffoli gate can be used to synthesis a fault tolerant full adder circuit.

Full adder is a versatile and widely used building block in digital arithmetic processing. Several researchers have proposed reversible full adder circuits [14, 16-20]. These designs are not parity preservable. Fig. 9 depicts a relatively simple full-adder circuit containing two Peres gates [11]. Each Peres gate composed of a Toffoli gate and a Feynman gate.

We can state that the proposed fault tolerant TG circuit can be used to synthesis a novel parity preserving reversible full adder via simple substitution. The proposed parity-preserving reversible full adder

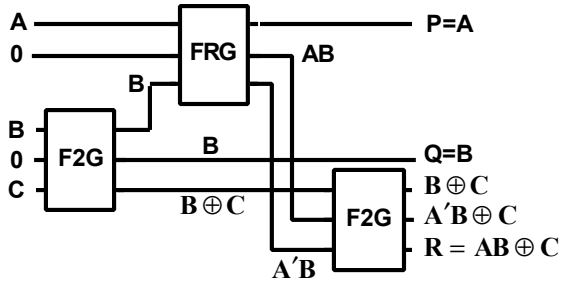

Fig. 7: Existing TG with parity preservation, presented in [11]

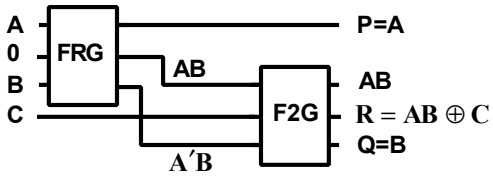

Fig. 8: Proposed parity preserving TG implementation using only two reversible gates

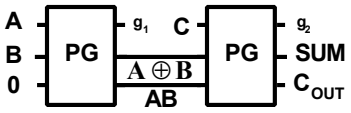

Fig. 9: Existing Reversible Binary Full Adder in [11] without parity preservation

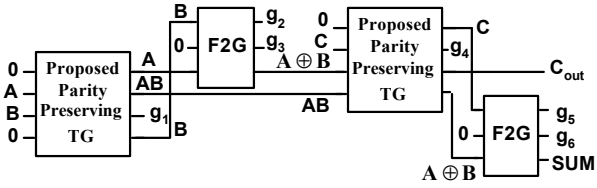

Fig. 10: Proposed parity preserving reversible full adder

using the proposed TG circuit is depicted in Fig. 10. This shows the applicability of our proposed parity-preserving TG circuit.

RESULTS AND DISCUSSION

Evaluation of The Proposed Parity Preserving Reversible TG Circuit: Our proposed parity preserving reversible circuit performs better than the existing circuit presented in [11]. An experimental result will comprehend it clearly. Table 3 compares the proposed reversible circuit with the existing counterpart.

One of the major constraints in reversible logic is to minimize the number of reversible gates used. In our proposed design approach we used only two reversible logic gates (one FRG gate and one F2G). The existing design in [11] requires three reversible gates (one Fredkin Gate and two F2Gs), so we can state that the proposed circuit is better than [11] in term of number of reversible logic gates.

Another significant criterion in designing a reversible circuit is to lessen number of garbage outputs. Every output of the gate that is not used as a primary output or as input to other gate is called garbage output. A heavy price is paid for every garbage bit. The proposed reversible circuit produces one garbage output. The design in [11] produces two

Table 3: Comparative results of different parity preserving reversible Toffoli gate circuits

	This work	Existing circuit [11]
No. of gates	2	3
No. of garbage outputs	1	2
Total clock cycle	2	3
Total logical calculation	$4\alpha+4\beta+2\delta$	$6\alpha+4\beta+2d$

σ = Unit clock cycle, α = A two input EX-OR gate calculation, β = A two input AND gate calculation, d = A NOT calculation

garbage outputs. Thus, we can state that our design is better than [11] in term of number of garbage outputs.

This work requires only two clock cycles, but the design in [11] requires three clock cycles. Thus we can state that our design is better than the existing design in [11] in term of required clock cycles, which is one of the main factors of a circuit.

Our proposed circuit is also better than [11] in term of complexity. Let

α = A two input EX-OR gate calculation
β = A two input AND gate calculation
δ = A NOT calculation
T = Total logical calculation
So, for [11]: $T = 6\alpha+4\beta+2\delta$
For our proposed circuit: $T = 4\alpha+4\beta+2\delta$

Thus, the propounded parity-preserving reversible circuit requires less logical calculations than [11]. So, Our proposed circuit is better than the circuit presented in [11] in all the terms.

Evaluation of the proposed parity preserving reversible full adder: The proposed parity preserving reversible full adder requires six parity preserving reversible gates (four F2G and two Fredkin gates) and produces six garbage outputs (g_1 to g_6 in Fig. 10). It requires six clock cycles (each proposed TG requires two clock cycles). Given that the proposed parity preserving TG in Fig. 8 is better than the existing counterpart in [11], The proposed parity preserving full adder is also better than the existing full adder in [11].

CONCLUSION

In this research, we synthesized a parity preserving reversible TG circuit. Table 3 illustrates that the proposed fault tolerant reversible circuit is better than the existing counterpart. The synthesis methods using Toffoli gates are widely available. Thus, our proposed parity-preserving TG circuit can be used in designing fault tolerant reversible circuits. We applied the proposed parity preserving TG circuit to the design of a parity preserving reversible full adder. Furthermore, the restrictions of reversible circuits were highly avoided.

Synthesis of more parity-preserving reversible circuits are now being studied. We are also trying to minimize reversible circuits as well as full adder.

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