

# Design of a Rail-to-Rail Folded Cascode Amplifier with Transconductance Feedback Circuit

Radu Ciocoveanu, Andreas Bahr, and Wolfgang H. Krautschneider

**Abstract**—In this work a programmable folded cascode rail-to-rail operational amplifier (OpAmp) with small settling time and transconductance feedback circuit is proposed. It employs a 130 nm CMOS technology with 1.2 V power supply. The small settling time is required to charge an ADC within a given time frame. The OpAmp achieves a gain bandwidth of 19.95 MHz with a 70 pF load and a minimum settling time of 144 ns while consuming 0.551 mA quiescent current. It can be shown that with 130 nm technology, high performance amplifiers can be realized on very small area.

**Index Terms**—Small settling time, constant transconductance, rail-to-rail, programmable, operational amplifier.

## I. INTRODUCTION

THE downscaling of the technology has led to lower supply voltages, in order to maintain a constant electric field. With a lower supply voltage, the signal-to-noise ratio has also decreased. To counteract this drawback, it is necessary to make use of the entire signal swing, thus rail-to-rail operation at both the input and output is needed.

Rail-to-rail at the input can be achieved by using complementary n-channel and p-channel differential pair, but the drawback is that the  $g_m$  is varying over the input common mode range, which leads to introduction of distortions, impedes optimal frequency compensation and also leads to a variation of  $GBW$  [1]-[3]. Additional circuitry is needed to maintain the  $g_m$  constant over the input common mode range.

In this work, a programmable rail-to-rail folded cascode amplifier in 130 nm technology with 1.2 V power supply voltage using the topology of [1] is presented, along with the feedback module to maintain the  $g_m$  constant, with the topology shown in [2].

## II. OPAMP AND FEEDBACK MODULE ARCHITECTURE

### A. Overall Architecture

The programmable amplifier is used in a non-inverting configuration. A resistor string and transmission gates are added to allow the selection of different amplification values. The complete schematic of the programmable OpAmp is shown in Fig. 1.

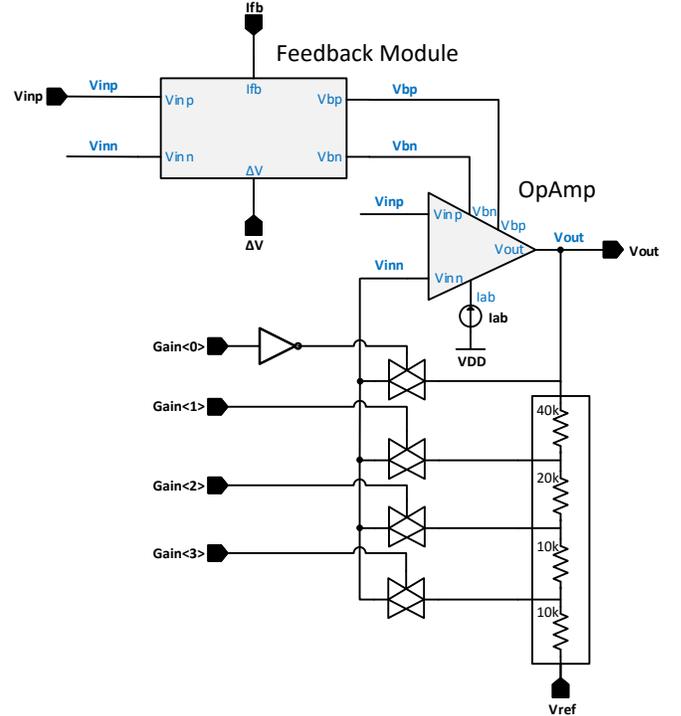


Fig. 1. Complete schematic of the programmable OpAmp.

The inputs of feedback module and folded cascode OpAmp are shared, and the voltages  $V_{bn}$  and  $V_{bp}$  adjust the currents through the input differential pair of the OpAmp, as it is shown in Fig. 1.  $\Delta V$  is a DC voltage that causes an imbalance in the feedback module, which will lead to the generation of the two control voltages  $V_{bn}$  and  $V_{bp}$ .

### B. Folded Cascode OpAmp

The schematic of the OpAmp is shown in Fig. 2. It has complementary p-channel and n-channel differential pairs to achieve rail-to-rail common mode voltage at the input (transistors MN01, MN02, MP01, MP02), and a class AB output stage to obtain rail-to-rail at the output of the amplifier (transistors MNAB, MPAB), as presented in [1].

Transistors MN03, MP03 are biasing the input differential pair, while transistors MP04, MP05, MP06, MP07 and MN04, MN05, MN06, MN07 are used in the cascode current mirrors. Transistors MP11, MP12 and MN11, MN12 represent the floating current source, which biases both the summing circuit and the class-AB control. Transistors MP09, MP10 and MN09, MN10 bias the gates of the transistors from the floating current source. The current source provides power-supply independent

quiescent current [1]. In a folded cascode without a floating current source, the current in the summation stage is varying with the common mode voltage at the input, which will cause a change in the voltage that biases the gates of the output transistors, which in turn contributes to the noise and offset of the amplifier. The floating architecture of the class-AB driver prevents that it contributes to the noise and the offset of the amplifier [1]. Cascoded Miller compensation is used in order to make the operational amplifier stable.

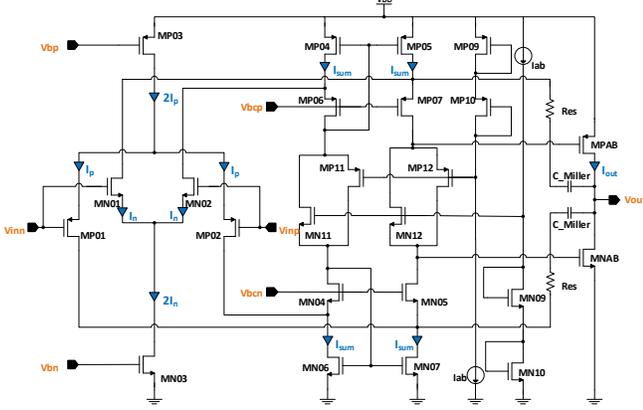


Fig. 2. Proposed rail-to-rail amplifier [1].

The transconductance of the input stage is defined as

$$g_{mT} = g_{MN01} + g_{MP01} \quad (1)$$

and it varies by a factor of two over the input common mode range [3]. The variation can be explained as following: when the input common mode is  $VDD/2$ , both the NMOS and the PMOS transistors operate, therefore the transconductance is at its maximum in that region. At GND, the NMOS will turn off while the PMOS is still conducting. Because only the PMOS is conducting, the transconductance is half of what it is at  $VDD/2$ . At VDD, the PMOS is turned off, while the NMOS is turned on, therefore the transconductance is half of what it is at  $VDD/2$ . To keep the transconductance constant over the input common mode range additional circuitry is needed.

### C. Feedback Module

To maintain a constant  $g_{mT}$ , the circuit schematic in Fig. 5 is used, as presented in [2]. The functioning principle of the feedback module is shown in Fig. 3.

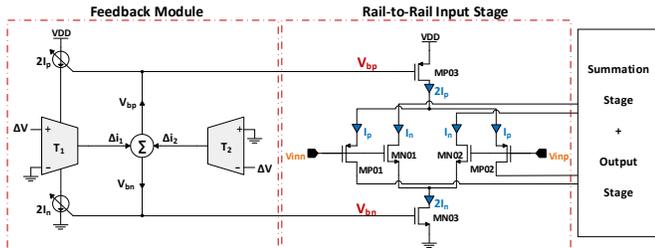


Fig. 3. Feedback module functioning principle [2].

The blocs  $T_1$  and  $T_2$  are transconductance amplifiers and their transconductance values are kept equal by the negative feedback. The outputs of the feedback module are two control voltages  $V_{bn}$  and  $V_{bp}$  that adjust the currents through transistors MN03, MP03 [2]. Depending on the input common-mode, the two control voltages will make the transistors MN03 and MP03 conduct more or less current. The bloc  $T_1$  in Fig. 3 is the  $g_{mT} - R$  converter and the bloc  $T_2$  is the resistive comparator.

The  $g_{mT} - R$  converter is shown in Fig. 4. The transconductance of the input stage  $g_{mT}$  can be expressed as a function of the equivalent small signal resistance  $r_{eq,AB}$  at nodes A and B [2].

$$r_{eq,AB} = \frac{2}{g_{mT} + g_{ds,NMOS} + g_{ds,PMOS}} [2] \quad (2)$$

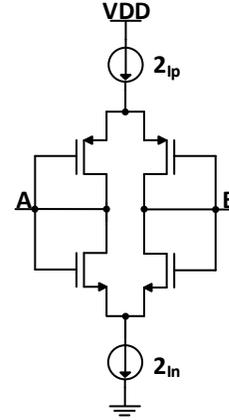


Fig. 4.  $g_{mT} - R$  converter [2].

The complete feedback module in Fig. 5 includes a dynamic bias generator that is used to provide a current  $(I_{bias} + I_n - I_p)$  for the two current sources  $MS1$  and  $MS2$ . It also consists of blocs  $T_1$  ( $g_{mT} - R$  converter),  $T_2$  (resistive comparator) and a folded cascode transimpedance amplifier structure used as current summation stage.  $T_1$  and  $T_2$  are unbalanced by a DC input voltage  $\Delta V$  and generate two output currents. In the current summation stage, the summation of currents from  $T_1$  and  $T_2$  is converted in the two controlling voltages  $V_{bn}$  and  $V_{bp}$  that adjust the tail current sources in both the feedback module and OpAmp [2].

The summation stage in Fig. 5 is a resistive comparator for  $(g_{mT} + g_{ds,NMOS} + g_{ds,PMOS})^{-1}$  and  $R_{ref}$ . The tail currents will be adjusted until  $(g_{mT} + g_{ds,NMOS} + g_{ds,PMOS})^{-1} = R_{ref}$  [2].

Because  $g_{ds,NMOS}$  and  $g_{ds,PMOS}$  are small in comparison to  $g_{mT}$ , they can be ignored, therefore the equation becomes:

$$g_{mT} = R_{ref}^{-1} = R_1^{-1} = R_2^{-1} [2] \quad (3)$$

Two other important conditions have to be met for a good functionality of the feedback module. The minimum value for the reference resistance  $R_{ref}$  is given by eq. 4.

$$R_{ref,min} = \frac{1}{g_{mf}} [2] \quad (4)$$

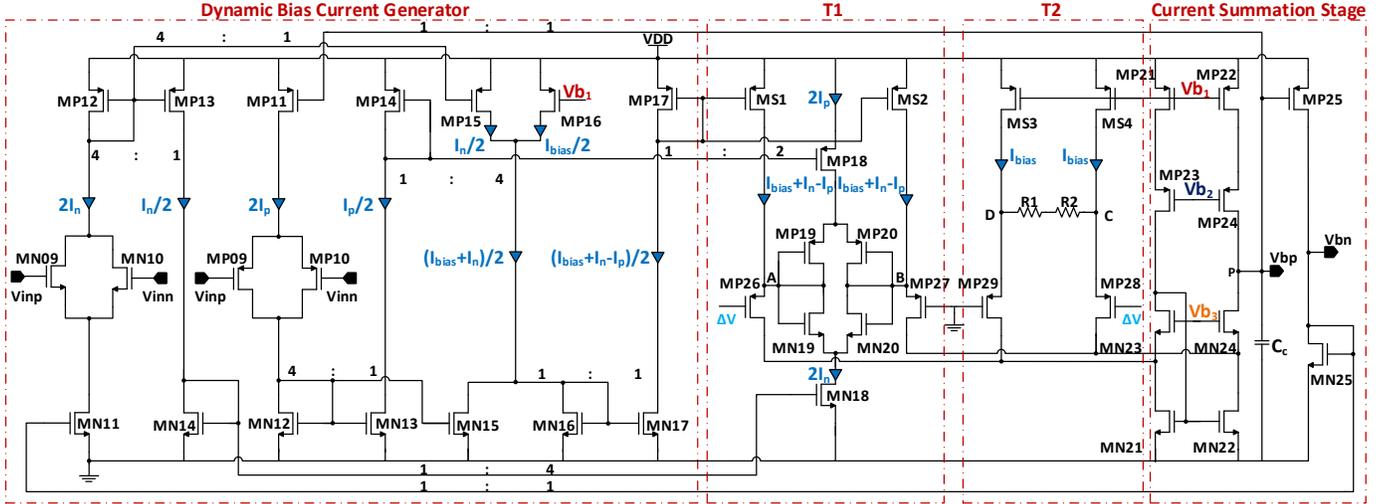


Fig. 5. Circuit schematic of the feedback module [2].

The upper bound of  $g_{mT}$  is showed by eq. 5

$$g_{mT-max} = g_{mf}[2] \quad (5)$$

where  $g_{mf}$  represents the transconductance of transistors MP26-29 from Fig. 5. Therefore, to achieve a constant and accurate  $g_{mT}$ , the maximum  $g_{mT}$  is derived as:

$$g_{mT-max} = R_{ref}^{-1}[2] \quad (6)$$

Large loop gain has to be maintained for a constant and accurate  $g_{mT}$  and therefore  $R_{ref}$  which acts like a degeneration resistor, should not be too large. Moreover, the  $GBW$  of the feedback module has to be as large as the  $GBW$  of the folded cascode amplifier and also enough phase margin is needed to ensure stability of the system [2].

### III. SIMULATION RESULTS AND LAYOUT

In order to assess the performances of the system, two of the most important specifications have been analyzed, namely  $g_{mT}$  variation and settling time for different amplification values. To verify the transconductance variation, the constant  $g_m$  stage had the input common mode voltage swept from 0.1 V to 1.1 V. The normalized  $g_{mT}$  variation is shown in Fig. 6.

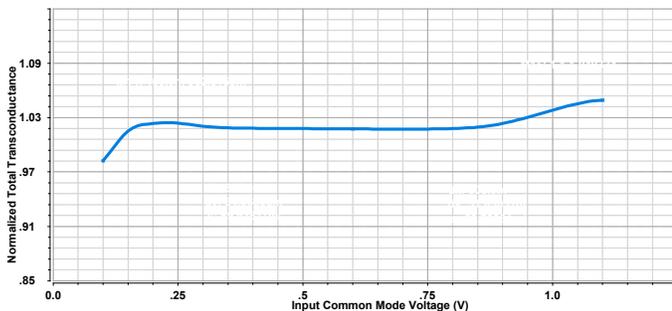


Fig. 6.  $g_{mT}$  variation vs.  $V_{in,cm}$ . The maximum  $g_{mT}$  variation after the post-layout simulation is 3.4%.

The effect of transistor mismatches over  $g_m$  variation was modeled by Monte Carlo analysis with 100 iterations. As shown in Fig. 7, at input common mode voltage of 0.1 V, the probability of having transconductance variations larger than 7 % decreases exponentially.

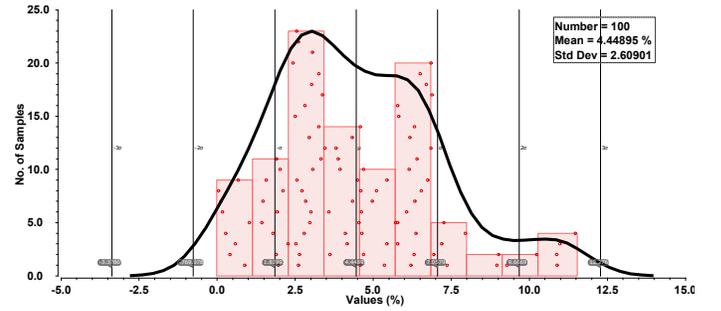


Fig. 7. Monte Carlo histogram for normalized transconductance at input common mode voltage of 0.1 V. The probability of values higher than design specification  $g_{mT} < 9\%$  is very low.

For an input common mode voltage of 1.1 V, the probability of having transconductance variations larger than 6% decreases exponentially, as shown in Fig. 8.

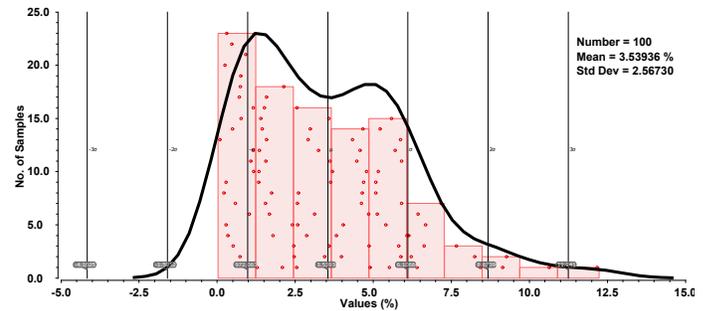


Fig. 8. Monte Carlo histogram for normalized transconductance at input common mode voltage of 1.1 V. The probability of values higher than design specification  $g_{mT} < 9\%$  is very low.

Settling time is a critical specification for this design, because the amplifier has to settle to 1/2 LSB within a given time frame, in order for the ADC to sample the value correctly.

To measure the settling time, a probe was first added at the moment when the pulse is applied at the input, and a second probe, when the output value of the amplifier is within 1/2 LSB of the final value and time difference between the two was measured.

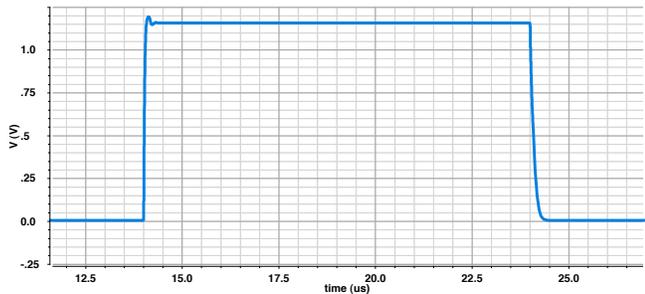


Fig. 9. Settling time simulation.

The values for the settling time for the different amplification factors are given in table I.

Amplification Value	Rise Time	Fall Time
1	144 ns	329 ns
2	490 ns	491 ns
4	308 ns	482.95 ns
8	387 ns	484.13 ns

TABLE I

SIMULATED SETTling TIME FOR DIFFERENT AMPLIFICATION FACTORS.

The area consumption of the layout in Fig. 10 is only  $0.0231 \text{ mm}^2$ .

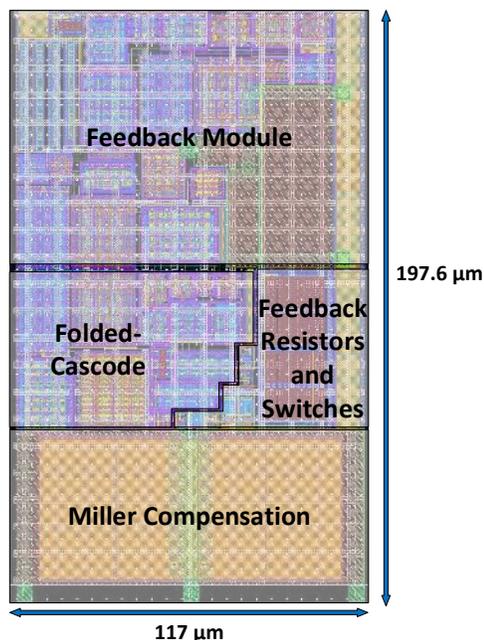


Fig. 10. Layout of the complete rail-to-rail OpAmp with transconductance feedback module.

## IV. CONCLUSION

The performance comparison of the rail-to-rail amplifier is summarized in table II, showing a lower power consumption than in [4] as well as a smaller settling time, larger slew rate and less area consumption.

	[3]	[2]	This paper
Process	0.13 $\mu\text{m}$	0.13 $\mu\text{m}$	0.13 $\mu\text{m}$
Supply Voltage (V)	1.2	1	1.2
Maximum $g_{mT}$ variation	13 %	3.4 %	3.4 %
Load	70 pF	20 k $\Omega$    95 pF	70 pF
DC Gain (dB)	85	60	71.6
Power Consumption (mW)	1.28	0.187*	0.662
GBW (MHz)	4.99	3.7	19.95
Phase Margin	67°	72°	64°
Slew Rate (V/ $\mu\text{s}$ )	0.9	1.74	7.39
Minimum Settling Time ( $\mu\text{s}$ )	$\approx 0.464^{**}$	-	0.144
Occupied area ( $\text{mm}^2$ )	0.109 $\text{mm}^2$	0.0289 $\text{mm}^2$	0.0231 $\text{mm}^2$

\* Only the power-consumption of folded-cascode amplifier is considered.  
 \*\* Minimum settling-time achieved for the specified power consumption. In [4], the power consumption is 1.28 mW .

TABLE II  
PERFORMANCE COMPARISON.

This paper has presented a programmable rail-to-rail amplifier with transconductance feedback technique, with small settling time and good constant transconductance over the input common mode range. The simulated results show good performance of the amplifier, with low power consumption, large slew rate and small occupied area.

## V. ACKNOWLEDGEMENTS

This work was supported by the German Research Foundation, Priority Program SPP1665.

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