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Design of a symmetry-type floating impedance scaling circuits for a fully differential filter

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Abstract Low frequency and low power applications are required for biomedical devices. Thus, a large capacitance is needed for integration of low frequency active filters. To realize a small-size low frequency active filter, impedance scaling techniques have been proposed. In this paper, a symmetry-type floating impedance scaling circuit is proposed. The proposed circuit is composed of voltage followers and current amplifiers. The characteristics of the proposed circuit are confirmed by simulation. The proposed circuit works as a large capacitor which has a capacitance multiplied 50 times. The proposed circuit is applied to a fully differential 3rd-order low-pass filter. Simulation results show validities and availability of the proposed symmetry-type floating impedance scaling circuit.

Keywords Impedance scaling circuit · Analog filters · Analog integrated circuits · Common-mode rejection circuit

1 Introduction

Filters are used to process various signals such as visuals, audios, and communications. Low frequency filter processing biomedical signals [1, 2] from a few Hz to hundreds Hz requires a large time constant. In order to implement a large time constant, a large capacitance and a large resistance are needed. However, large capacitances and large resistances are impracticable in integrated circuits, which are required to be low-powered and downsized.

The large resistance is implemented by a transconductor of low transconductance [3]. The area occupied by a transconductor is much smaller than that of a resistor with the same resistance. In contrast, it is difficult to shrink the area occupied by large capacitances. As a method to realize a large capacitance, an impedance scaling circuit has been proposed [4]. The impedance scaling is a technique to reduce apparent impedance using current feedback.

Several g_m-C filters using impedance scaling circuits have been proposed [5–7]. In those filters, a grounded impedance scaling circuit or a pair of the grounded circuits are employed.

The authors have proposed a floating impedance scaling circuit [8]. Floating impedance scaling circuits are useful for not only low-frequency band-pass and high-pass filters but also fully differential low-pass filters. If the floating impedance scaling circuit is employed in a fully differential low-pass filter, the required capacitance is no more than 1/4 comparing with using a pair of grounded capacitances.

However, the circuit in [8] has a problem that the different level between the DC operating points of two terminals prevents realization of fully differential filters. The problem is due to the asymmetric structure of the current amplification stage.

In this paper, a design of a symmetry-type floating impedance scaling circuit and the improvement method of its operation bandwidth are proposed. The proposed circuit is applied to a fully differential 3rd-order low-pass filter (LPF). The fully differential filter requires introducing of a

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common-mode rejection circuit. The interaction of the common-mode rejection circuit and the proposed floating impedance scaling circuit is confirmed by simulation. The common-mode impedance characteristics of the proposed impedance scaling circuit are verified by small-signal analysis. The effectiveness of the application to the LPF of the proposed circuit is confirmed by simulation.

2 Conventional floating impedance scaling circuit

Figure 1 shows the block diagram of the conventional floating impedance scaling circuit [8].

This circuit is composed of differential unity gain amplifier (DUA) and a differential output current amplifier. The output voltage of the voltage follower is a voltage difference between v_1 and v_2, and applied to the impedance component Z. The output current of the voltage follower is expressed as

$$i_0 = \frac{v_1 - v_2}{Z}. \tag{1}$$

The differential output current amplifier multiplies a signal current i_0 flowing through an impedance Z by N times for current feedback. The relationships among signal current i_0, i_1, and i_2 are given by

$$i_1 = i_2 = Ni_0. \tag{2}$$

The apparent impedance of the conventional circuit is expressed as

$$Z_{sc} = \frac{v_1 - v_2}{Ni_0} = \frac{Z}{N}. \tag{3}$$

The impedance is reduced by current feedback. If the impedance component Z is a capacitor which has capacitance C, Z_{sc} is expressed as

$$Z_{sc} = \frac{1}{sNC}. \tag{4}$$

This means that the circuit performs as floating capacitor having capacitance NC.

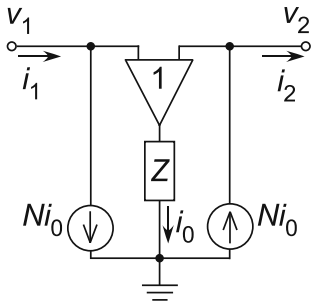


Fig. 1 Block diagram of the conventional floating impedance scaling circuit

Figure 2 shows the circuit diagram of the conventional circuit. This circuit has asymmetric structure at the current amplification stage. The terminal 'i_2/v_2' is set up by adding M25–M31 to the output circuit for 'i_1/v_1'. Even though cascode stages are introduced, the current amplification factors of the current mirrors deviate from the ideal one. Furthermore, the currents flowing M28–M31 are 50 times as much as the currents of M25–M27. Consequently, the degrees of the current mismatches at the 'i_1/v_1' and 'i_2/v_2' terminals tend to be much different. This makes the DC operating points at the terminals different each other. This problem causes serious trouble in operation of fully differential filters, in which a certain node bias voltage is different from one at the counterpart of the opposite node.

In previous authors' study, application to fully differential filters employing the conventional circuit has been examined. However, the filers never worked because of the unbalanced DC bias condition. If both terminals are of the same structure, namely symmetrical topology like an ordinary differential input/output OTA, DC bias deviation from the proper operating point can be about the same level, and the problem can be alleviated.

In the next section, a design of a symmetry-type floating impedance scaling circuit is proposed.

3 Proposed symmetry-type floating impedance scaling circuit

Figure 3 shows the block diagram of the proposed symmetry-type floating impedance scaling circuit. This circuit is composed of two voltage followers and two current amplifiers. The output voltages of the voltage followers are applied to the impedance element Z. The signal current flowing through the impedance element is amplified with the current amplifier for current feedback.

3.1 Basic symmetry-type floating impedance scaling circuit

The circuit diagram of the symmetry-type floating impedance scaling circuit based on the block diagram of Fig. 3 is shown in Fig. 4. Hereinafter, this circuit is called as "Proposed 1". The transistors M_1 and M_2 are source followers. The input voltage signal is applied to the capacitor C through the source followers. The current mirrors of M_4–M_3 and M_5–M_6 perform as the current amplifier of N times. The small signal current flowing through the capacitor is amplified by the current amplifier. Assuming that the drain resistance of the bias current sources M_9 and M_{10} are enough large, the signal current flowing through the capacitor, i_0, is expressed as

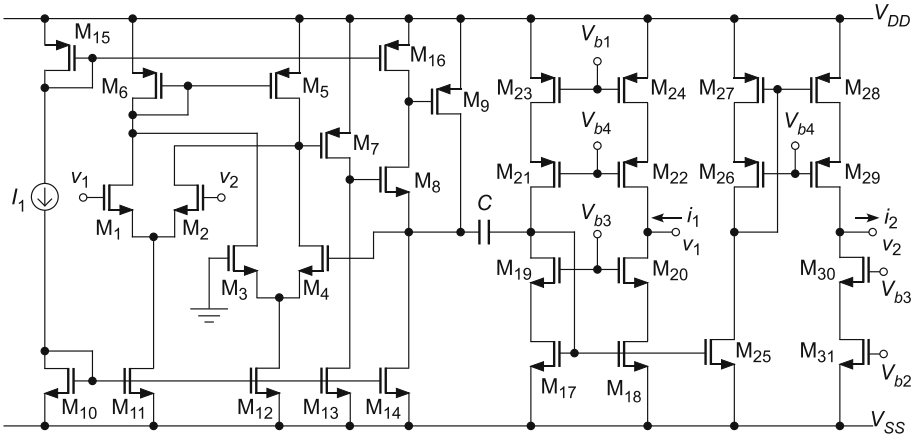


Fig. 2 Circuit diagram of the conventional floating impedance scaling circuit

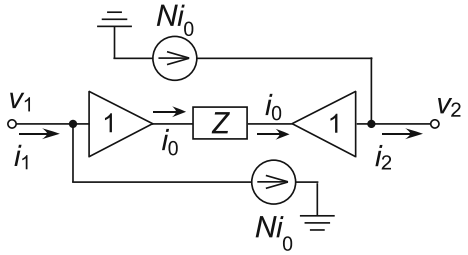


Fig. 3 Block diagram of the proposed symmetry-type floating impedance scaling circuit

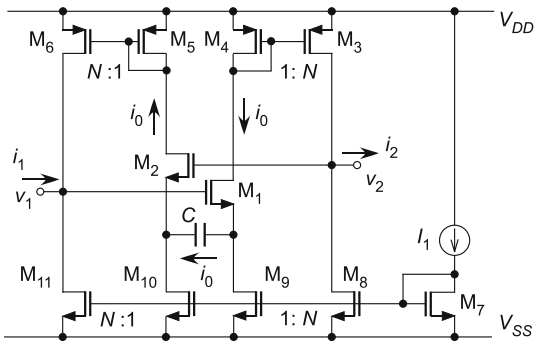


Fig. 4 Circuit diagram of the symmetry-type floating impedance scaling circuit ("Proposed 1")

$$i_0 = (v_1 - v_2)sC. \tag{5}$$

Assuming that the drain resistance of the bias current sources M_8 and M_{11} are enough large, the small signal currents i_1 and i_2 are equal to Ni_0, and expressed as

$$i_1 = i_2 = N(v_1 - v_2)sC. \tag{6}$$

The impedance of "Proposed 1" circuit is given by

$$Z_{sc} = \frac{v_1 - v_2}{N(v_1 - v_2)sC} = \frac{1}{sNC}. \tag{7}$$

Therefore, the apparent capacitance is increased by N times.

To confirm the frequency characteristics of "Proposed 1" shown in Fig. 4, the small-signal characteristics are analyzed. Assuming that the fully differential voltages are applied to the both terminals, the input voltages are expressed as

$$v_1 = \frac{1}{2}v_{in} \tag{8}$$

$$v_2 = -\frac{1}{2}v_{in}. \tag{9}$$

The differential-mode half circuit of "Proposed 1" is shown in Fig. 5. The resistance r_{d10} indicates the drain resistance of the bias current source M_{10}. The resistance R_d indicates the resistance component observed from terminal v_1. The combined resistance R_d is the drain resistances connected in parallel and expressed as $R_d = r_d/(2N)$. Assuming that $g_m r_d \gg 1$, the impedance Z_1 of the half circuit is given by

$$Z_1 = \frac{v_1}{i_1} \simeq \frac{g_{m5}\left(s + \frac{g_{m2}}{2C}\right)}{g_{m2}g_{m6}\left[s + \frac{1}{2C}\left(\frac{1}{r_d} + \frac{g_{m5}}{g_{m6}R_d}\right)\right]}. \tag{10}$$

The pole frequency ω_p and the zero frequency ω_z are given by

$$\omega_p \simeq \frac{1}{2C}\left(\frac{1}{r_d} + \frac{g_{m5}}{g_{m6}R_d}\right) \simeq \frac{1}{2NC}\left(\frac{N}{r_d} + \frac{1}{R_d}\right) \tag{11}$$

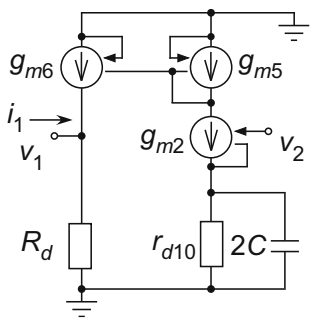


Fig. 5 Small signal equivalent circuit of "Proposed 1"

$$\omega_z \simeq \frac{g_{m2}}{2C} \simeq \frac{g_m}{2C}, \tag{12}$$

where $g_{m5} = g_{m2} = g_m$, and $g_{m6} = Ng_m$. Because of $r_d \gg 1/g_m$, the zero frequency ω_z is much higher than the pole frequency ω_p. The pole ω_p depends on the resistance component R_d in the input terminal, and the zero ω_z depends on the conductance g_m of the input MOS transistors M_1 and M_2 associated with capacitor employed in "Proposed 1".

3.2 Improved symmetry-type floating impedance scaling circuit

From the small signal analysis related to the pole and the zero of "Proposed 1" given by (11) and (12), an improvement technique of the operation bandwidth is provided. The higher the resistance R_d at the terminal v_1 and v_2 are, the lower the pole frequency is, and the higher the conductance components g_{m1} and g_{m2} associated with the capacitor are, the higher the zero frequency is. The circuit diagram of the symmetry-type floating impedance circuit with improved operation bandwidth is shown in Fig. 6. Hereinafter, this is called as "Proposed 2". In order to make the resistance component at the terminals v_1 and v_2 high, the cascode stages configured with the common-gate M_{11}–M_{14} are introduced. In order to make the conductance component g_m high, the negative feedback circuits are composed of M_3–M_8. The small-signal half circuit are analyzed to confirm the frequency characteristics of "Proposed 2". The small-signal half circuit of "Proposed 2" is shown in Fig. 7. Because the drain resistances of M_4 and M_8 are much higher than $1/g_{m8}$, they can be ignored. The drain resistance of M_{10} is included in R_d. The drain resistances of M_2, M_6 and M_{18} are indicated by r_{d2}, r_{d6} and r_{d18}. Assuming that $g_{mx}r_{dy} \gg 1\,(x, y : 2, 8, 16)$, the impedance Z_1 is approximately expressed as

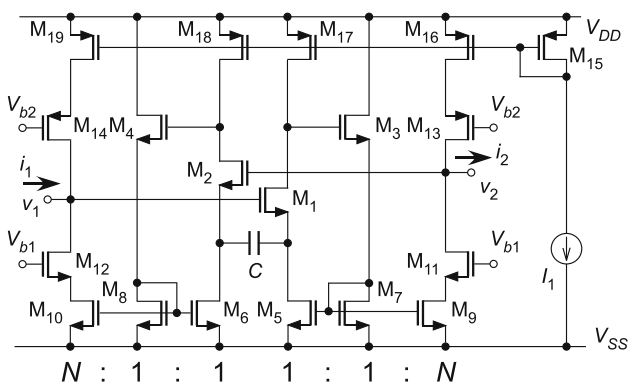


Fig. 6 Circuit diagram of the symmetry-type floating impedance scaling circuit ("Proposed 2")

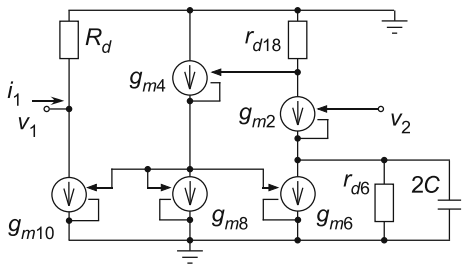


Fig. 7 Small signal equivalent circuit of "Proposed 2"

$$Z_1 \simeq \frac{4}{Ng_m^2 r_{d18}} \cdot \frac{s + \frac{g_m^2 r_{d2} r_{d18}}{4C(r_{d2}+r_{d18})}}{s + \frac{1}{2NC}\left(\frac{1}{R_d} + \frac{N}{r_{d6}}\right)}, \tag{13}$$

where $g_{m2} = g_{m4} = g_{m6} = g_{m8} = g_m$ and $g_{m10} = Ng_m$. The pole frequency ω_p and the zero frequency ω_z are given by

$$\omega_p \simeq \frac{1}{2NC}\left(\frac{N}{r_d} + \frac{1}{R_d}\right) \tag{14}$$

$$\omega_z \simeq \frac{g_m^2 r_{d2} r_{d18}}{4C(r_{d2} + r_{d18})} \simeq \frac{g_m^2 r_d}{8C}. \tag{15}$$

where r_{d2} and r_{d18} are roughly approximated to be equal, and are r_d. Comparing "Proposed 2" with "Proposed 1", R_d becomes $g_m r_d$ times with the cascode stages, the pole moves to lower frequency. Comparing (15) with (12), the zero frequency is multiplied by $g_m r_d/4$ times and moves to higher frequency. The impedance Z_1 in the range between the pole and the zero frequencies, $\omega_z \gg \omega \gg \omega_p$, is given by

$$Z_{sc} = 2Z_1 \simeq 2 \cdot \frac{4}{Ng_m^2 r_{d18}} \cdot \frac{\omega_z\left(\frac{s}{\omega_z} + 1\right)}{s\left(1 + \frac{\omega_p}{s}\right)} \tag{16}$$

$$\simeq \frac{8}{Ng_m^2 r_d} \cdot \frac{\frac{g_m^2 r_d}{8C}}{s} \tag{17}$$

$$\simeq \frac{1}{sNC}. \tag{18}$$

The "Proposed 2" performs as an N-times capacitance in wider range than "Proposed 1".

3.3 Simulation results

The validity of the proposed circuits is confirmed using simulation software LTspice (Linear Technology). The transistor model used in the simulation is BISIM3 0.18 μm process model. The supply voltage is 1.8 V. The reference current I_1 is 30 nA. In order to realize the scaled capacitance of 500 pF, $N = 50$ and the base capacitance is set to 10 pF. The tables of transistor size are shown in Tables 1 and 2.

The simulation results of impedance and phase frequency characteristics are shown in Fig. 8. The solid line

Table 1 Transistor size of proposed circuit (Proposed 1)

Transistors	W (μm)/L (μm)
M_3, M_6, M_8, M_{11}	90.0/1.8
The others	1.8/1.8

Table 2 Transistor size of proposed circuit (Proposed 2)

Transistors	W (μm)/L (μm)
M_9–M_{14}, M_{16}, M_{19}	90.0/1.8
the others	1.8/1.8

indicates the proposed circuit of "Proposed 2", the broken line indicates the proposed circuit of "Proposed 1", the dash-dotted line indicates the conventional impedance scaling circuit [8], and the dotted line indicates the ideal capacitor of 500 pF. From the impedance characteristic of "Proposed 1", it is seen that the pole and the zero frequencies are near each other.

Table 3 shows the comparison of the power consumption, the occupied area, and the frequency range. The definition of the frequency range is one in which the phase is between −80° and −90°.

The power consumption and area of "Proposed 2" are reduced by 5.5 and 3.9% compared to "Conventional", respectively. Although the operation frequency range of the proposed circuit is narrower than the conventional one, the proposed circuit has an advantage that the problem of DC operating points can be improved. In the next section,

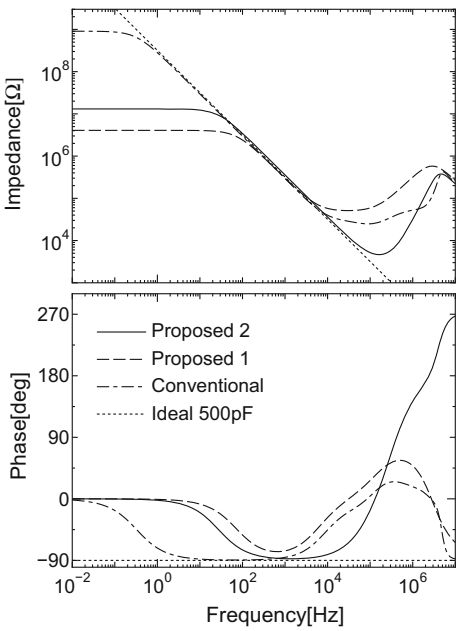


Fig. 8 Frequency characteristics

Table 3 Power consumption and area

	Power (μW)	Area (μm^2)	Range (Hz)
Conventional	6.05	2310	1.86–2.09 k
Proposed 1	5.94	1120	N/A
Proposed 2	5.72	2220	158–11.5 k

application of the proposed circuit to a 3rd-order fully differential filter is shown. While the conventional circuit can be applied to a 2nd-order bandpass filter [8], even a 1st-order fully differential filter can not work. This is because a node bias voltage is different from one at the counterpart of the opposite node.

The phase characteristic of "Proposed 1" do not reach −90° in the range of 100–10 kHz, in which the minimum value of phase is −77.2°. The impedance characteristic of "Proposed 2" shows the capacitor characteristics in the range from 158 Hz to 11.5 kHz. In summary, comparing "Proposed 2" with "Proposed 1", the pole frequency is lower and the zero frequency is higher.

4 Application to fully differential filter

4.1 Configuration of fully differential LPF

Employing the proposed circuits, a fully differential 3rd-order butterworth LPF shown in Fig. 9 designed in this study. The capacitors C_1, C_2, and C_L are implemented employing the floating impedance scaling circuit. The low-g_m linear OTA [9] shown in Fig. 10 is used as G_{m1}–G_{m7}. Table 4 shows the bias currents in the OTA. All transconductances of the OTAs are 606.7 nS by simulation. The fully differential filter requires introducing of a common-mode rejection (CMR) circuit. The CMR circuit employed in the LPF is shown in Fig. 11. The reference current I_1 in the CMR circuit is 300 nA. In order to realize the 3rd-order butterworth LPF of f_c = 100Hz, C_1 = C_2 = 965 pF, and C_L = 1.93 nF. By setting N = 50, the capacitances in the floating impedance scaling circuit are $C_1/50$ = $C_2/50$ = 19.3 pF, and $C_L/50$ = 38.6 pF.

As is mentioned previously, the conventional circuit is not suitable for fully differential filters. For comparison,

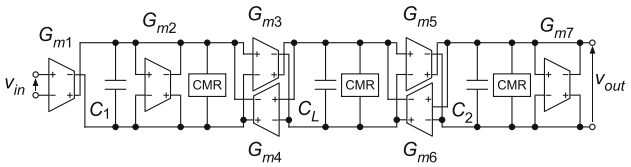


Fig. 9 3rd-order LPF employing symmetry-type floating impedance scaling circuit ("Proposed LPF")

Table 4 The bias current source

Current source	Current (nA)
$I_1 = I_8$	50
$I_2 = I_5 = I_7 = I_9$	100
$I_3 = I_4$	68.3
I_6	36.6

the conventional floating circuit is used as a grounded circuit. The terminal 'i_2/v_2' shown in Fig. 2, which is difficult to be proper operating condition, is grounded. A scaled capacitance $C_x\,(x : 1, 2, \mathrm{L})$ realized by the proposed circuit is replaced with two grounded conventional circuits with 4 times capacitance as shown in Fig. 12.

4.2 Frequency characteristics

The frequency characteristics of the LPF are shown in Fig. 13. The solid line indicates the characteristics of the LPF employing "Proposed 2", the dashed line indicates the characteristics of the LPF employing "Proposed 1", the dash-dotted line indicates the characteristics of the LPF employing the conventional circuit as a grounded circuit, and the dotted line of "Ideal" indicates the ideal LPF. The passband gain and the cutoff frequency are listed in Table 5.

From the simulation results in Fig. 13, the proposed circuits show the characteristics of floating capacitors in stop band. The reduction of passband gain from ideal response are 0.66 dB (Conventional), 5.70 dB (Proposed 1) and 2.27 dB (Proposed 2). It is seen that the stopband characteristic of "Proposed 2" is superior to the conventional one and "Proposed 1".

The parasitic resistances of the conventional one, "Proposed 1", "Proposed 2", and CMR are 4.07, 13.1, 908, and 42.6 MΩ, respectively. Thus, it can be considered that the passband gain are reduced by the parasitic resistance component of the CMR circuit and the proposed impedance scaling circuits.

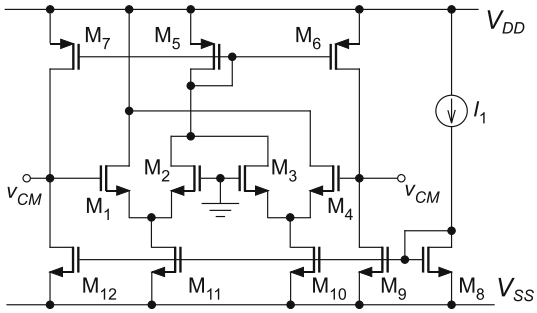


Fig. 11 Common-mode rejection circuit

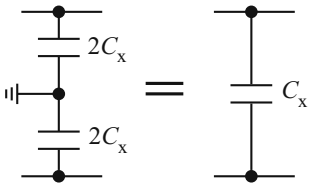
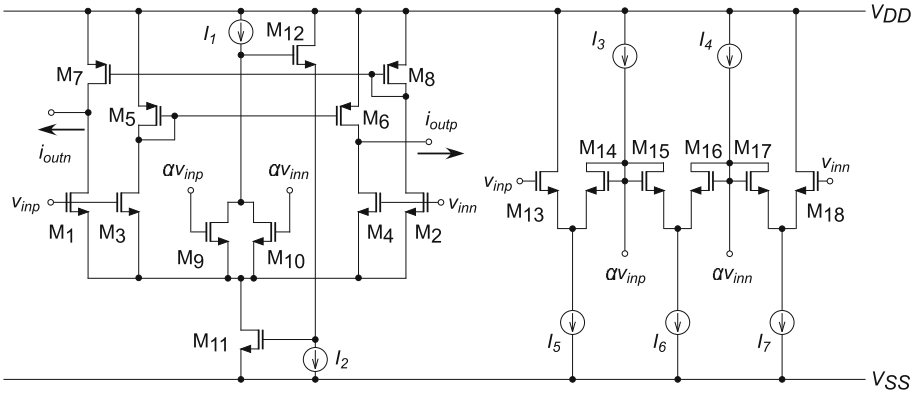


Fig. 12 Replacement of capacitance

4.3 Common-mode impedance characteristics

The current never flows when the same voltages are applied to the both terminals of passive elements, and the impedance is obviously infinite. However, because the impedance scaling circuit is synthesized with transistors, the impedance to the same voltage at the both terminals is finite, practically. Although it may not be correct expression, such an impedance is called "common-mode impedance" in this paper. Appling the common-mode voltage v_{CM} to the both terminals of "Proposed 2", the output voltages of the source followers M_1 and M_2 are equal, currents do not flow in the capacitor C associated with the source followers. Thus, the capacitor C can be considered as an open element. The common-mode half circuit is shown in Fig. 14. The resistances r_{d6}, r_{d18}, and R_d indicate the drain resistances of the transistor M_6, the bias current source M_{18}, and the resistance component at the terminal

Fig. 10 Low-g_m linear OTA



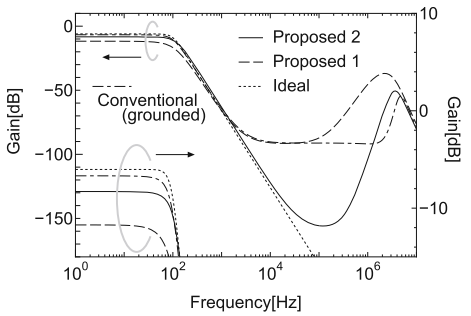


Fig. 13 Frequency characteristics of LPF

Table 5 Passband gain and cutoff frequency of LPF

	Gain (dB)	Frequency (Hz)
Ideal	−6.02	100
Conventional	−6.68	92.0
Proposed 1	−11.72	79.4
Proposed 2	−8.29	105.0

v_1, respectively. Assuming that $g_m r_d \gg 1$, the impedance Z_{CM} of the half circuit is given by

$$Z_{CM} \simeq \frac{R_d r_{d6} g_{m6}}{g_{m6} r_{d6} - g_{m10} R_d} \tag{19}$$

$$\simeq \frac{R_d \cdot \left(-\frac{r_{d6}}{N}\right)}{R_d - \frac{r_{d6}}{N}} \tag{20}$$

$$= R_d \parallel \left(-\frac{r_{d6}}{N}\right), \tag{21}$$

where $g_{m6} = g_m$, $g_{m10} = N g_m$. Moreover, we have $R_d = (g_m r_d^2)/N$ and $R_d \gg r_{d6}/N$,

$$Z_{CM} \simeq -\frac{r_{d6}}{N}, \tag{22}$$

For the common-mode signal, the "Proposed 2" symmetry-type impedance scaling circuit performs as a negative resistance $-r_{d6}/N$ due to positive current feedback.

The common-mode impedance of the CMR circuit Z_{cmr} is expressed as

$$Z_{cmr} = \frac{1}{g_m} \tag{23}$$

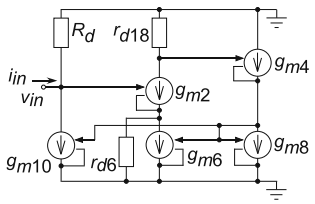


Fig. 14 Small signal equivalent circuit of the floating type scaling capacitor circuit for common-mode signal ("Proposed 2")

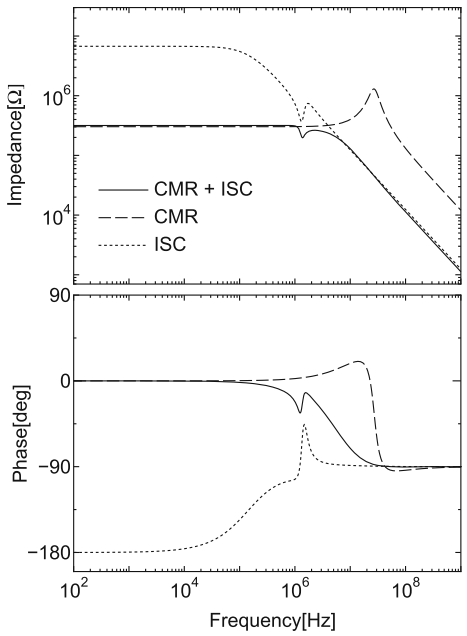


Fig. 15 Common-mode impedance

where $g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_{m6} = g_{5m}/2 = g_m$. The synthetic admittance Y is expressed as

$$Y = \frac{1}{Z_{cmr}} + \frac{1}{Z_{CM}} = g_m - \frac{N}{r_{d6}} \tag{24}$$

The reason why I_1 in the CMR circuit is set to be 300 nA, which is 10 times as much as I_1 in "Proposed 2", is not only to obtain high common-mode rejection but also to hold $Y > 0$.

The simulation results of the common-mode impedance and the phase characteristics are shown in Fig. 15. The solid line of "CMR + ISC" indicates the result of the parallel of the common-mode rejection circuit and "Proposed 2" circuit, the dashed line of "CMR" indicates the common-mode rejection circuit, the dotted line of "ISC" indicates "Proposed 2" circuit. From the phase characteristic of "ISC", it is shown that the symmetry-type floating impedance scaling circuit performs as the negative resistance in lower frequency range. The phase characteristic of "ISC + CMR" performs as the positive resistance. Consequently, because of the combined impedance of "CMR" and "ISC" is positive from the characteristics of "CMR + ISC", the operation of the LPF is stable.

5 Conclusion

In this paper, to implement large capacitance for the application of the biomedical signal processing such a LPF, a design of a symmetry-type floating impedance scaling

circuit and the improvement methods of those operation bandwidth had been proposed. Floating impedance scaling circuits are useful for not only low-frequency band-pass and high-pass filters but also fully differential low-pass filters. The conventional floating impedance scaling circuit has a problem that the different level between the DC operating points of two terminals prevents realization of fully differential filters.

The proposed circuit is composed of two source followers and two current amplifiers. From the small signal analysis, the improvement methods of the operating bandwidth are found. In order to lower the pole frequency, the resistance component in the parts of input terminals has been increased by introducing the common gate, and to enhance the zero frequency, the conductance component associated to the capacitor has been enhanced by negative feedback. To realize the scaled capacitance of 500 pF, N and the capacitance are set to 50 and 10 pF, respectively. The impedance characteristic of the synthesized impedance scaling circuit had shown the capacitor characteristics in the range from 158 Hz to 11.5 kHz. The power consumption and area are reduced comparing the conventional circuit. The fully differential 3rd-order butterworth LPF with the $fc = 100$ Hz has been designed employing the proposed circuit. The appropriate operation of the scaling capacitor composed of the proposed circuit and the LPF employing the proposed circuit has been confirmed by the simulation results. By the small signal analysis, it has been shown that the improved proposed circuit becomes the negative conductance when the same voltages are applied to both terminals. This negative resistance can be ignored due to the small common-mode resistance of the common-mode rejection circuit. The future work is the analysis of the characteristics under PVT variation, the improvement of the pass band gain of the filter, the application for the higher-order filters, and the prototype of the proposed circuit.

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Conflict of interest The authors declare that they have no conflict of interest.

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