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PHYSICAL AND TECHNICAL ENERGY PROBLEMS

DESIGN OF A THREE-PHASE BIDIRECTIONAL PWM RECTIFIER WITH SIMPLE CONTROL ALGORITHM

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The paper covers the main aspects of designing a low voltage three-phase PWM rectifier for bidirectional AC/DC power flow with unity power factor. A model in Matlab/Simulink environment has been built for a 10kW active rectifier with an LCL filter connected to grid side of the rectifier. The primary goal of the model is to achieve low grid current harmonic content for frequency ranges described in worldwide applicable standards and above. LCL filter parameter design procedure is described in the paper and implemented in the rectifier model to achieve a better power quality with limitations in passive element size. A simple ‘’p-q” theory-based voltage oriented control algorithm is used in the model and described in the present paper. Model performance is characterised by dynamic response, stability and grid parameters during simulation. The simulation results demonstrate that the modelled rectifier system is stable and the grid current harmonic content is low both in the low- and high-frequency ranges.

Keywords: *bi-directional AC/DC rectifier, LCL filter*

1. INTRODUCTION

Bidirectional AC/DC power flow converter or three-phase pulse-width-modulation (PWM) rectifier is a rapidly developing research field since different applications of various kinds of DC micro-grids evolve considerably. Interfacing DC systems to AC distribution grids by means of uncontrolled rectifiers often creates unacceptable voltage and current distortion in the AC grid. Moreover, many DC micro-grid systems incorporate DC power sources (e.g., renewables, regenerative braking of electrical machines), which in some cases require passing electrical energy back to the AC grid [1]–[3].

The goal of the paper is to design a three-phase bidirectional rectifier model with input current in the limits of regulated standards, such as IEEE 519-1992. A

third-order low-pass LCL filter will be designed as the current ripple attenuation is very effective for limited inductor sizes with the capacitor impedance inversely proportional to the frequency of the grid current. LCL filter will be designed to attenuate low and high (around switching frequency) order harmonics [4], [5]. Rectifier control will be implemented with synchronously rotating *dq* frame to control load current d and q axis components and active/reactive power separately and maintain a constant DC link voltage during dynamic load changes. Matlab/Simulink environment will be used to design the rectifier and simulate the behaviour during different operation modes. The model is built such that afterword an experimental setup using dSpace platform is possible.

2. SIMULATION STUDY

The designed rectifier model is shown in Fig. 1. Apart from the main full-bridge circuit, this topology also includes a 3-phase grid network with accordant grid impedance parameters L_{source}, LCL parameters L_{filter}, L, C_f, R_d and DC link capacitor C_{dc}. Load is changed with DC side resistance $R_{dc1,}$ external DC source is used to test the model in inverter mode.

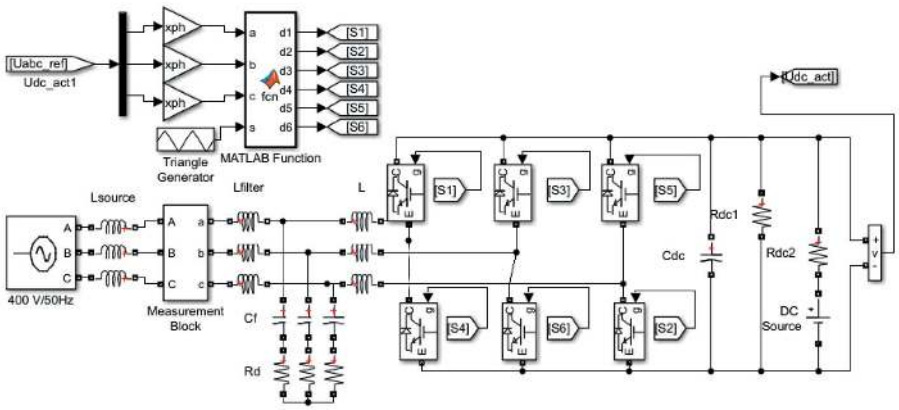

Fig. 1. Basic structure of designed PWM rectifier.

Inductors connected between the input of the rectifier and line bring the current source character of the input circuit and provide boost feature of the rectifier. The line current i_L is controlled by the voltage drop across the inductance L interconnecting line and rectifier voltage sources. By controlling the phase angle and amplitude of rectifier voltage, phase and amplitude of line current are indirectly controlled [3].

With a larger DC side capacitor, smaller LCL filter inductance and smaller voltage loop proportional gain k_{vp}, the rectifier will be more stable. A larger capacitance will lead to a slower dynamic response of the converter, so a tradeoff between system stability and other performances must be made [6].

LCL filter configuration produces better attenuation of switching harmonics than L and LC filters [4]. With an LCL filter, it is possible to use relatively low switching frequency for a given harmonic attenuation. The gained attenuation of LCL filter is 60dB/decade in excess of the resonance frequency according to [7].

The resonant frequency of the LCL filter is given by:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{\left(L_{filter} + L\right)}{L_{filter} \cdot L \cdot C_f}}. \quad (1)$$

LCL filter may cause both dynamic and steady state input current distortion due to resonance [7]. If a third-order LCL filter is proper designed – resonant frequency is far away from both fundamental AC frequency and switching frequency, it is possible to eliminate the line current ripple and the switching noise at low switching frequencies with smaller inductor than with L or LC filters. Generally, all LCL filter design approaches, which are introduced in papers [8], [9], [4] are similar. The mentioned papers show great results in simulation and experimental tests.

The procedure for choosing the LCL filter parameters uses the power rating of the converter, the line frequency, and the switching frequency as input. Filter must be properly damped. LCL filter capacitor value is limited by a decrease in the power factor at rated power (less than 5 %). The total value of LCL filter inductance is limited to 0.1 pu [8].

After calculation described in [8], LCL filter parameters are shown in Table 1. The LCL filter is connected to a grid of inductance according to a 75 MVA three-phase transformer. Capacitor on the DC side of the converter is chosen to ensure that DC voltage fluctuations do not exceed 1 %.

Table 1

LCL Filter Parameters for the Designed Model

Source inductance, L_{source}, mH	0.135
Grid side inductance, L_{filter}, mH	1
Converter side inductance, L, mH	1
Filter capacitor, C_f, μF	2.2
Damping resistor, Rd, Ω	15.55
DC capacitor capacitance, Cdc, μF	6500
Switching frequency, fs, Hz	15000
Sampling frequency, fsampling, Hz	30000
Rectifier nominal power, Pn, W	10000
Grid voltage, Vl, V	400

Resonant frequency is kept in the range between ten times the line frequency and one half of the switching frequency to avoid resonance problems in lower and upper parts of harmonic spectrum. The network frequency f_n is 50Hz, switching frequency f_{sw} is 15 kHz. The resonant frequency f_0 of 4603 Hz satisfies this requirement.

The Matlab/Simulink model control (Fig. 3) uses a closed loop current control in a rotating reference frame – voltage oriented control (VOC) topology described in [3]. Current feedback is managed from the rectifier side. As a model in *abc*-frame cannot realise a zero steady state error for PI controller with time variant variables, three-phase stationary frame is transformed into the synchronously rotating *dq* frame [6].

Coordinate transformation of current and voltage to rotating *dq*-coordinates (Park transformation) is done by a Simulink block that transforms a three-phase signal to rotating *dq*-coordinates with the grid angular frequency *w*, and *d* axis aligned with grid voltage vector (Fig. 2). The variables in *dq*-coordinates are DC quantities and PI controller can provide zero steady state error control.

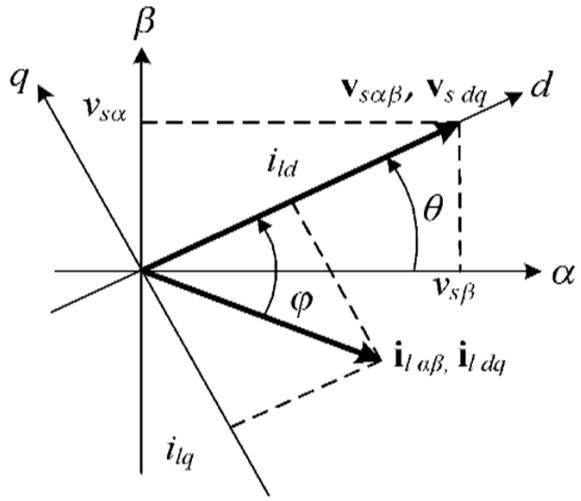

Fig. 2. Load current and grid voltage phasors in Clark's and Park's reference frames.

The PWM rectifier model in *dq*-frame can be obtained as follows, according to [3], [6]:

$$V_{Ld} = L\frac{di_{Ld}}{dt} - w \cdot L \cdot i_{Lq} + e_d \tag{2}$$

$$V_{Lq} = L\frac{dil_{Lq}}{dt} + w \cdot L \cdot i_{Ld} + e_q \tag{3}$$

$$C\frac{dV_{dc}}{dt} = \left(i_{Ld} \cdot S_d + i_{Lq} \cdot S_q\right) - i_{DC}\,, \tag{4}$$

where e_d, e_q, i_{Ld} and i_{Lq} are grid voltage and current, V_{Ld}, V_{Lq} are voltages at the rectifier terminals in *dq*-frame. $V_{Ld}=S_d \cdot V_{dc}$, $V_{Lq}=S_q \cdot V_{dc,}$ S_d and S_q are components of the switching function and i_{DC} is the DC link current [6].

Rectifier control consists of double-loop control (Fig. 3). The outer loop is DC voltage loop and the inner are current loops. Task of current loops is to perform regulation of converter's currents along *d* and *q* axis to control active and reactive power independently as i_{Lq} determines the reactive power, i_{Ld} determines the active power flow [10]. Task of the voltage loop is to keep the DC link voltage constant and at a value to keep the diodes of the converter blocked and maintain the controller stability – 700V. The voltage control loop controls the active energy flow and compensates the active losses of the converter.

For the DC voltage loop, the command DC voltage V_{DC_ref} is compared with the measurement of actual DC voltage V_{DC_act}, the error is delivered to PI controller UDC_PI, which stabilises DC voltage and generates an output signal or command active current i_d^*, therefore regulating the active power of the converter. Reactive current command i_q^* is set to 0 in order to achieve a unity power factor. Command currents can be expressed as follows:

$$\begin{cases} i_d^* = k_{vp}\left(V_{DC\_ref} - V_{DC\_act}\right) + k_{vi}\int \left(V_{DC\_ref} - V_{DC\_act}\right)dt \\ i_q^* = 0, \end{cases} \tag{5}$$

where k_{vp}, k_{vi} represent proportional and integral factors of voltage loop.

Command active and reactive currents are compared with their measured values from Clark transformation block I_d and I_q and errors are delivered to the respective PI controller. To generate V_d^* and V_q^* references, output of the PI controller is compared with the actual values of measured V_d, V_q voltages and the voltage drop on filter, source and converter side inductances in order to decouple d and q axis. A first-order low-pass filter set to passband edge frequency 628 rad/s eliminates high frequency noise from V_d^* and V_q^*, expressed as follows [3],[6]:

$$\begin{cases} V_d^* = V_d + w \cdot L \cdot i_q - k_{ip}(i_d^* - i_d) - k_{ii}\int (i_d^* - i_d)dt \\ V_q^* = V_q - w \cdot L \cdot i_d - k_{ip}\left(i_q^* - i_q\right) - k_{ii}\int \left(i_q^* - i_q\right)dt \end{cases} \tag{6}$$

where k_{ip}, k_{ii} represent proportional and integral factors of current loop.

Commands V_d^* and V_q^* are transformed to *abc*-frame to generate switching signals of IGBTs locked to the grid voltage vector by phase angle of line voltage determined by PLL block in Simulink. Control signals of upper and lower power switch in the same bridge arm are turned on complementarily to avoid short circuit on the DC side [3],[6],[11].

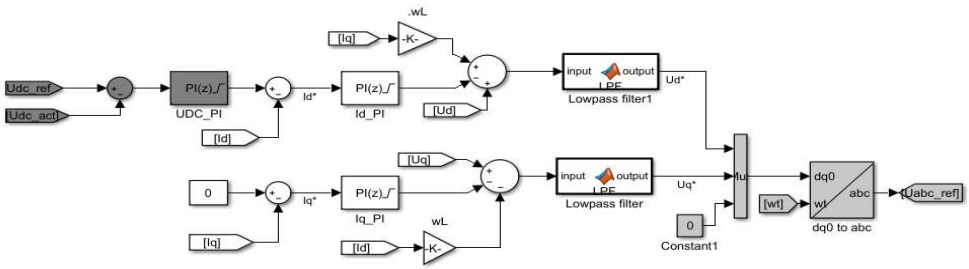

Fig. 3. Control system in Simulink environment.

3. RESULTS

In order to validate the selected control approach and developed topology, a simulation in MATLAB/Simulink environment is carried out with parameters shown in Table 1. Simulation for rectifier input current distortion is carried out with the power consumption in rectifier and inverter mode set to 10kVA. Grid (at point of common coupling) and converter (between LCL filter and rectifier) current waveforms in rectifier mode are illustrated in Fig. 4.

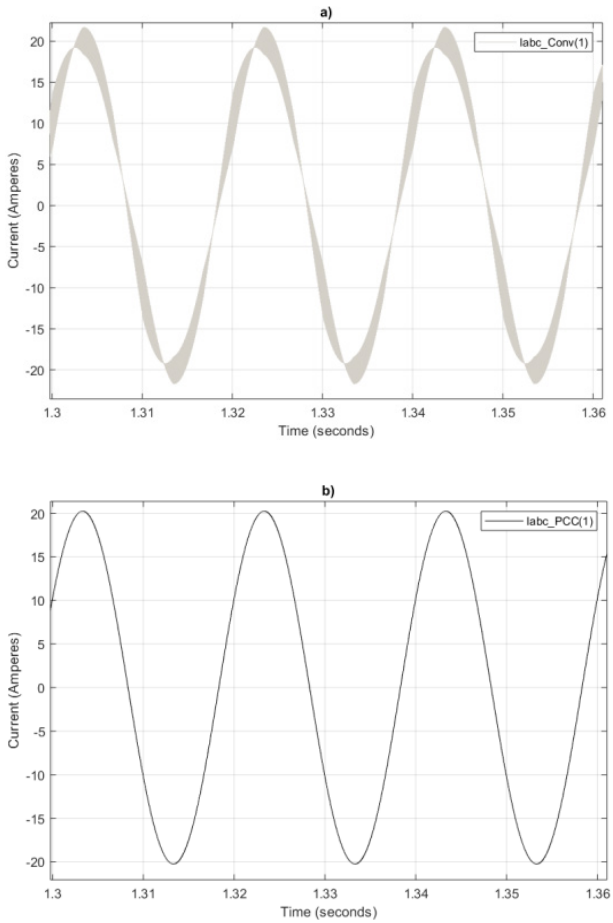

Fig. 4. Converter – a, Grid – b, current waveforms for phase A with load set to 10kVA, during rectifier mode.

The current is purely sinusoidal and in phase with the grid voltage as can be seen in Fig. 5 during rectifier mode and in phase but negative during inverter mode.

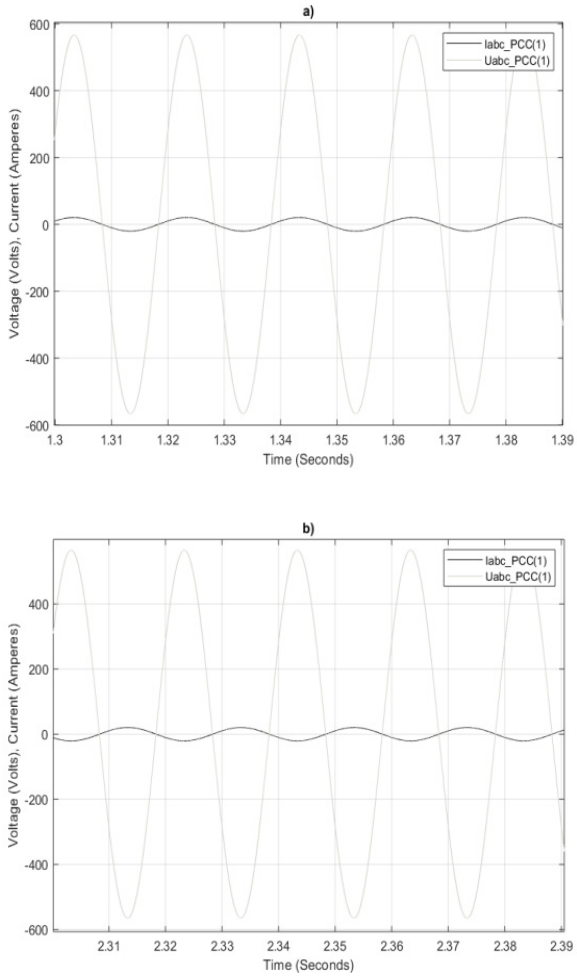

Fig. 5. Grid current and voltage waveforms for phase A with load set to 10kVA during a – rectifier mode, b – inverter mode.

Grid and converter current harmonic spectrum with the dominating harmonic orders is illustrated in Table 2. The THD of the grid current in rectifier mode with nominal load is 0.37 % and 0.34 % in inverter mode, and complies with IEEE-519 (THD<5 %). As can be seen from Fig. 4 and Table 2, the LCL filter is effective in attenuating harmonics around switching frequency *h*=296, 298.

Table 2

Grid and Converter Current Harmonic Spectrum

	THD, %	h=5	h=7	h=296	h=298
I_{grid} rectifier mode	0.37	0.01	0.01	0.02	0.37
$I_{converter}$ rectifier mode	12.43	0.07	0.04	2.38	12.18
I_{grid} inverter mode	0.34	0.01	0.01	0.02	0.34
$I_{converter}$ inverter mode	11.48	0.07	0.03	2.19	11.25

To ensure the dynamic response of PWM rectifiers, load is changed during simulation and rectifier is set to work as an inverter since an external voltage is connected to the DC side.

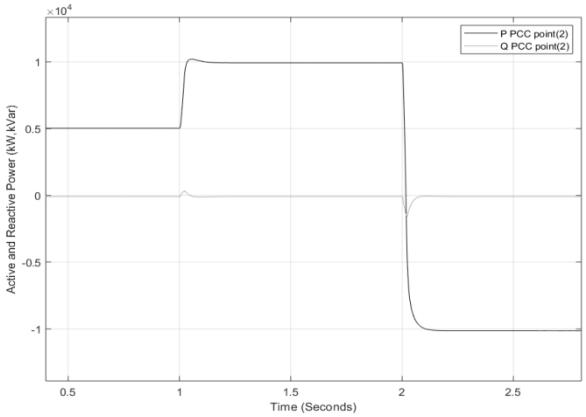

Fig. 6. Active and reactive power consumption at point of common coupling.

As can be seen from Fig. 6, the converter is able to compensate reactive power in rectifier and inverter modes. After an external voltage source is connected, the converter operates as inverter and power is delivered to grid, hence, the negative value of active power after 2 seconds.

Control of the converter effectively regulates the DC link voltage and stabilizes it after load changes as can be seen in Fig. 7.

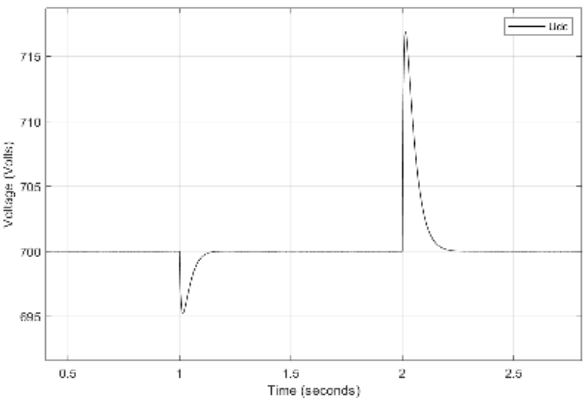

Fig. 7. DC link voltage during load change.

4. CONCLUSIONS

Model of a bidirectional PWM rectifier has been implemented in Matlab/ Simulink environment in order to validate the power circuit design considerations as well as the proposed simple control method. The PWM rectifier can operate as a rectifier or inverter with grid current distortion lower than the applicable standards (THD=0.4 % in rectifier mode and THD=0.3 % in inverter mode). The designed LCL filter effectively attenuates high switching frequency harmonics. The control method

is capable of compensating reactive power and maintaining the DC link voltage even during rapid load variations. Since the simulation results confirm effectiveness of the proposed control method, the algorithm in Matlab/Simulink environment will further be used for experimental validation with a dSpace real time interface control platform and a 10kVA laboratory prototype of a PWM rectifier.

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TRĪSFĀZU AKTĪVĀ TAISNGRIEŽA AR VIENKĀRŠOTU VADĪBAS ALGORITMU IZPĒTE UN IZSTRĀDE

K.Frišfelds, O.Krievs

K o p s a v i l k u m s

Raksts veltīts trīsfāzu aktīvā IPM taisngrieža izstrādei, kas spētu nodrošināt divvirzienu elektroenerģijas plūsmu ar pilnībā aktīvu ieejas jaudas koeficientu. Rakstā piedāvāta vienkāršota aktīvā IPM taisngrieža sprieguma vadības metode un izstrādāts tā datormodelis Matlab/Simulink vidē. Iegūtie modelēšanas rezultāti apliecina, ka piedāvātā vadības metode nodrošina stabilu taisngrieža darbību pat pie dinamiskām slodzes pārmaiņām un efektīvu darbu gan taisngrieža, gan invertora režīmos. Taisngrieža ieejas strāvas harmonisko kropļojumu koeficients (THD) pie pārveidotāja nominālās slodzes ir 0.4 % taisngrieža režīmā un 0.3 % invertora režīmā, kas atbilst IEEE-519 standarta prasībām. Ar piedāvāto vadības algoritmu turklāt iespējama maiņsprieguma puses aktīvās un reaktīvās jaudas regulēšana. Ieejā pieslēgtais LCL filtrs efektīvi vājina ieejas strāvas augstākās harmoniskās komponentes IPM komutācijas frekvences apgabalā. Turpmākais darbs paredz Matlab/Simulink vidē izstrādātā vadības algoritmu pielietošanu 10kVA aktīvā taisngrieža eksperimentālā prototipa vadībai, izmantojot dSpace reālā laika vadības platformu.

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