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Design of Adaptive Highly Efficient GaN Power Amplifier for Octave-Bandwidth Application and Dynamic Load Modulation

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***Abstract*—This paper presents a novel adaptive power amplifier (PA) architecture for performing dynamic-load-modulation. For the first time, a dynamically-load-modulated PA design that achieves octave bandwidth, high power and high efficiency simultaneously is experimentally demonstrated. This PA design is based on a commercial GaN HEMT. The output matching scheme incorporates a broadband static matching for high-efficiency at the maximum power level and a wideband dynamic matching for efficiency enhancement at power back-offs. The impedance and frequency tunability is realized using silicon diode varactors with a very high breakdown voltage of 90 V. Experimental results show that a dynamic-load-modulation from maximum power to 10-dB back-off is achieved from 1 to 1.9 GHz, with a measured performance of ≈10-W peak power, ≈10-dB gain, 64%–79% peak-power efficiency, and 30%–45% efficiency at 10-dB power back-off throughout this band.**

***Index Terms*—Adaptive, broadband matching, diode varactor, dynamic load modulation, GaN, high efficiency, high power, power amplifier (PA), tunable matching network.**

I. Introduction

POWER amplifiers (PAs) are the most energy-consuming component in wireless transceivers. Modern wireless communication systems require high PA efficiency to achieve reduced energy consumption and better device reliability. Such PAs are usually designed and implemented based on switch-mode (Classes D and E) and harmonic-tuned topologies (Classes J, F, and F^{-1}) [1], [2], which, however, operate efficiently only at high saturation levels. Nevertheless, modern bandwidth-efficient communication signals usually have high peak-to-average ratios (PARs), e.g., around 8-dB PAR for a typical 3GPP long-term-evolution (LTE) signal [3]. Thus, in these systems, PAs tend to work in significant power back-offs, leading to degradations of average efficiencies.

Several techniques have been proposed and demonstrated to improve the efficiency at power back-offs, such as dynamic power supply [6], [7], Doherty PAs [4], [5], and outphasing method [5]. However, extra amplifiers are required in those methods, leading to extra loss, size issues and increased circuit complexity. Comparatively, dynamic load modulation (DLM) has been proposed and demonstrated as an effective substitution [9]–[13]. It utilizes tunable output matching networks (OMNs) with passive tuning components that consume negligible dc power and can be designed as a part of the OMN. Moreover, the DLM technique has also been demonstrated at transmitter-level [14], [15], where the varactor-based matching network is controlled by the baseband signal, generated and predistorted by the DSP module.

Furthermore, traditional high-efficiency PAs require precise harmonic terminations, resulting in bandwidth restrictions of those PAs. However, in some future wireless systems, more and more frequency bands and spectrum allocations will be involved. Also, the effective bandwidth of the communication signals, such as WCDMA, LTE and WiMax, can be as wide as 20 MHz. Therefore, there is a pressing need to extend the frequency performance of traditional high-efficiency PAs. Recently, several static design methodologies [16]–[19] have been proposed to address this problem, achieving high efficiencies (>60%) across octave-level bandwidths. Nevertheless, such high efficiencies are only achieved at maximum power levels, which drop significantly at the power back-offs, e.g. around 20% at 10-dB back-off in [18] and [19].

It is also important to note that most of the current DLM-PAs/transmitters are designed for single-band operation [11], [12], [15], due to the complication of the varactor-based DLM matching. A multiband design has been demonstrated using the approach [10], but the peak efficiency and power are fairly low (50%, 28 dBm). In this research, we perform DLM over an octave bandwidth while maintaining the same level of peak efficiency and power as those achieved in static designs [16], [18], [19]. This adaptive PA design is based on a commercial GaN HEMT and diode varactors with a high breakdown voltage are used as the tuning element. The tunable output matching network is designed using a combination of a tunable series LC resonator and a fixed multistage low-pass filter-transformer. This tunable matching network provides not only the optimal fundamental impedance according to various power levels and frequencies, but also very favorable harmonic impedances. Moreover, only one tuning element is used in this DLM-PA topology, yielding simpler controlling scheme and lower insertion loss, compared to those which use multiple varactors/switches [10], [11], [13]. Using the proposed topology, the DLM-PA in this paper presents the optimized performance over a bandwidth of

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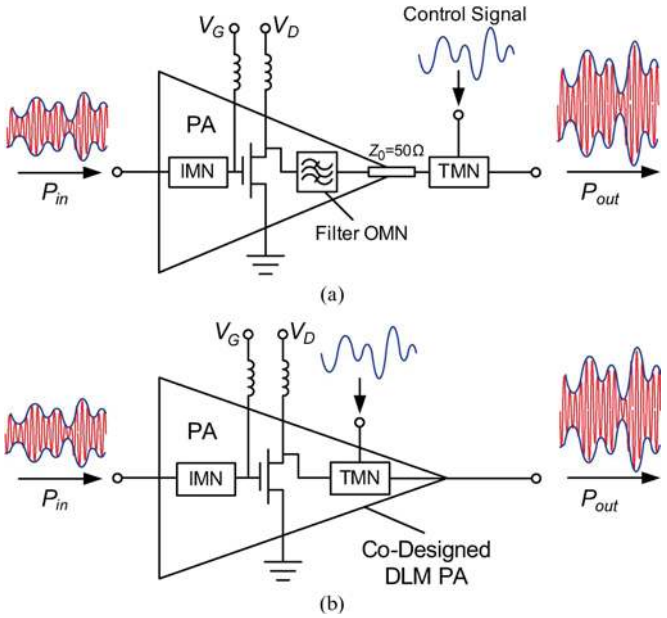

Fig. 1. Schematics of DLM-PA. (a) Separate design [12]. (b) Codesign [10], [15].

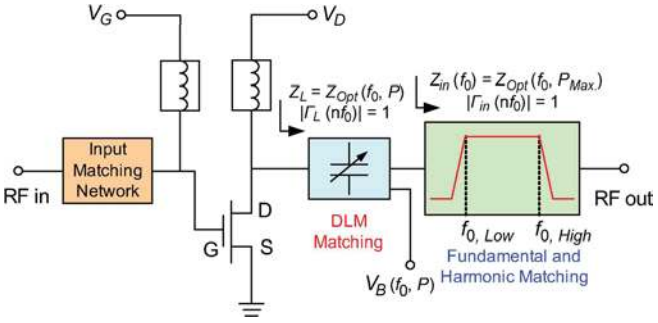

Fig. 2. DLM-PA schematic for achieving a continous broad bandwidth.

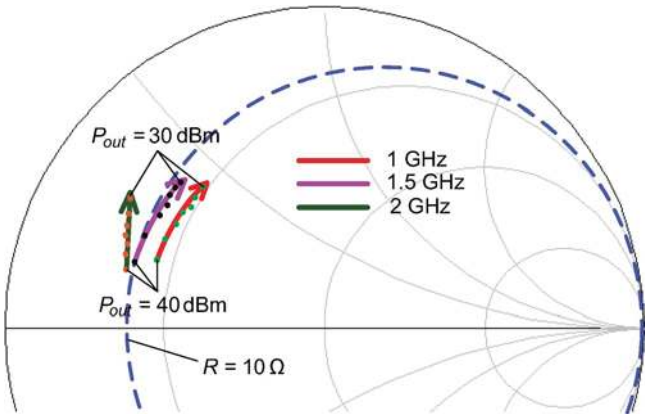

Fig. 3. Efficiency-optimized load impedance at various output power from 10 to 1 W within L-band, extracted from the loadpull simulation using ADS.

1–1.9 GHz (62%) with a peak power of around 10 W, efficiency of 64%–79% at the peak power level, and 30%–45% efficiency at 10-dB power back-off.

II. Broadband Dynamically-Load-Modulated PA

A. Extending the Bandwidth of DLM-PA

Fig. 1(a) schematically illustrates a typical DLM transmitter [12], [14], which consists of a static PA and a tunable matching network (TMN). The PA and TMN are designed and implemented independently. This method enables measurement-based characterizations of the PA and tunable matching network, leading to a better design accuracy. However, this independently designed DLM-PA contains more elements than a stand-alone PA, resulting in additional insertion loss and mismatch, as well as an efficiency-decrease (from 70% in [2] to 57% in [12]). Also, as mentioned in [15] the bandwidth is limited to <5 MHz, due to the interconnecting 50-Ω transmission line between the PA and TMN. Thus, this independent design methodology is not optimal for implementing a broadband DLM-PA.

Alternatively, as shown in Fig. 1(b), the design of PA output matching network and TMN is integrated, achieving a reduced circuit complexity and potential for broadband application. A multiband design is presented in [10] using this codesign method, which is based on a classical ladder-based tunable matching network topology. It is noted that this design gives priority to the fundamental-impedance matching rather than the harmonics, leading to a relatively low peak-power efficiency (40%–50%). In [15], another codesign method is proposed, in which harmonic matching is performed in parallel with fundamental matching, leading to a high efficiency at P_{Max}, which is comparable to those of the static PAs. However, this approach dose not address the multiband design.

To extend the bandwidth of the DLM-PA to an octave-level, a novel dynamically load modulated PA topology is proposed in this investigation as shown in Fig. 2. Two steps are involved in this DLM matching scheme. First, a fixed filter-matching network is designed to transform the 50-Ω load to the optimal impedance at maximum power level ($Z_{\mathrm{Opt}}(f_0, P_{\mathrm{Max}})$) within the passband of the filter, while providing a stopband reflection coefficient of $|\Gamma_{\mathrm{in}}(nf_0)| = 1$, as required for high efficiencies. Second, a varactor-based tunable circuit is connected between the filter and transistor, to provide the optimal fundamental impedance for the transistor with respect to various power levels and frequencies. While the tunable matching circuit also affects the harmonic impedances, it does not change the magnitude of $|\Gamma_{\mathrm{in}}(nf_0)|$, due to its zero-resistance (ideally). Thus, harmonics are still rejected. In turn, a continuous broad bandwidth can be achieved using this DLM-PA topology, while a high efficiency can be maintained.

B. Transistor Characterization for Dynamic-Load-Modulation

To demonstrate the proposed design methodology, a Cree GaN HEMT (CGH40025, 25 W, dc-6 GHz) is selected as the RF power device. As mentioned in [10] and [15], the co-design method relies heavily on the accuracy of the transistor model. In [19], the manufacturer's model is demonstrated to be very trustable for the broadband high-efficiency PA design, and it is thus utilized for this broadband DLM-PA design.

The transistor is characterized using load-pull simulation setup in Agilent's Advanced Design System (ADS) [20]. The initial target bandwidth is the entire L-band from 1 to 2 GHz. Fig. 3 shows the simulated dynamic load locus at 1, 1.5, and 2 GHz, respectively. The desired output impedance varies with both power and frequency. When the power level

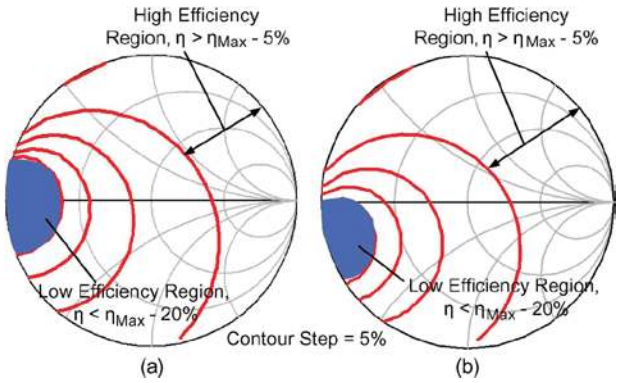

Fig. 4. Simulated load-pull contours of the second harmonic impedance. (a) At $2f_0 = 2$ GHz. (b) At $2f_0 = 4$ GHz [19].

drops (from 10 to 1 W), the desired impedance becomes more inductive. Specifically, it approximately moves along the 10-Ω constant-resistance circle on the Smith chart, as indicated by the arrows in Fig. 3. Having such a trajectory with a nearly constant real part is a key enable for the proposed design. Another GaN transistor used in [15] shows similar DLM impedance trajectory. It is also observed from Fig. 3 that the DLM locus at 2 GHz deviates slightly from the constant-resistance circle, because the parasitic effects of the transistor becomes more significant at higher frequencies.

Harmonic-impedance matching is also critical for high-efficiency PAs. Only the second harmonic is considered in this research as it plays the most important role in affecting the PA efficiency. Fig. 4 shows the simulated load-pull contours of the second harmonic at 1 and 2 GHz, indicating the tolerable region of the second harmonic impedance in which the high efficiency can be achieved.

On the PA designer's side, there are three challenging requirements for the tunable output matching network:

1) to over the dynamic load modulation locus within a broad bandwidth;
2) to be capable of handling the PA output power (10 W at maximum);
3) to provide appropriate harmonic impedance avoiding the low-efficiency region.

In the following section, the design of the tunable output matching network will be presented in detail, including topology selection, varactor selection, bandwidth–power tradeoff, and characterizations.

III. Tunable Output Matching Network Design

A. Broadband DLM Matching Scheme for the GaN Transistor

As shown in Fig. 3, the desired DLM trajectory within 1–2 GHz is nearly located on the 10-Ω constant-resistance circle. To match this particular locus within the target bandwidth, the matching scheme in Fig. 2 is modified slightly. The output matching network is constructed with a tunable series "resonator" and a fixed low-pass matching network, as shown in Fig. 5. Instead of matching 50-Ω load to $Z_{\rm Opt}(P_{\rm Max})$, the fixed matching network is designed to transform 50 Ω load to 10 Ω within the desired bandwidth. Then, a fixed inductor and a tunable capacitor are connected in series with the fixed

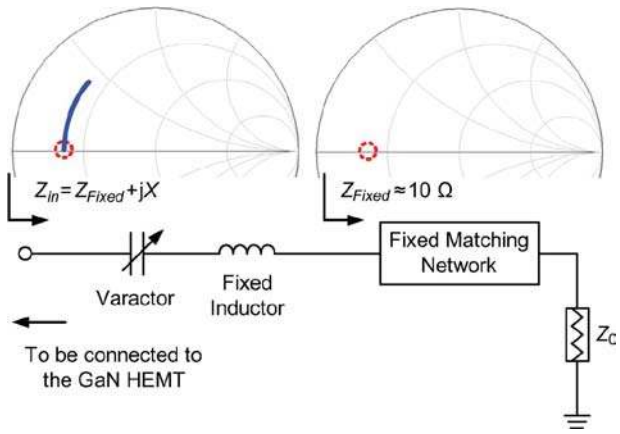

Fig. 5. Output matching network topology for performing broadband DLM on the Cree GaN transistor.

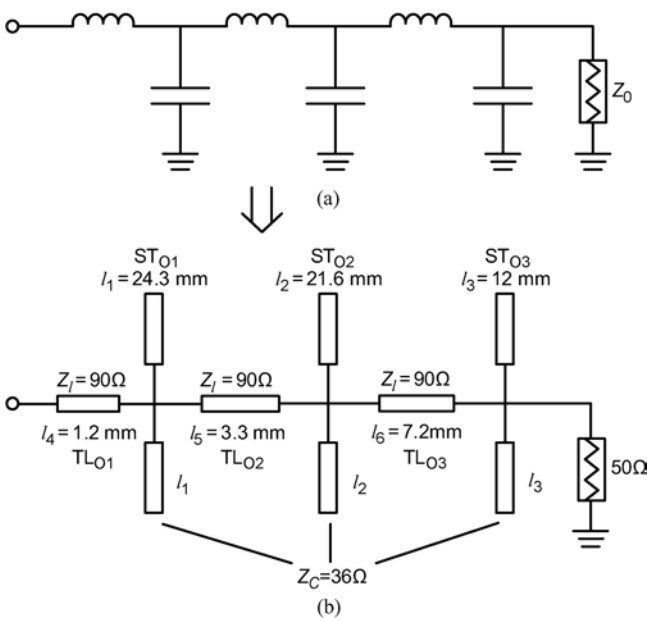

Fig. 6. Fixed output matching network design. (a) Ideal low-pass topology. (b) Implemented circuit using all-distributed elements on Rogers Duroid 5880LZ substrate.

matching network to provide a variable imaginary part. Thus, the input impedance of this entire matching network is given by

$$Z_{\rm in} = Z_{\rm Fixed} + jX \approx 10 + j\left(\omega L - \frac{1}{\omega C_{\rm Var}}\right) \qquad (1)$$

within the desired bandwidth. By changing the value of $C_{\rm Var}$, the frequency-induced impedance variation is compensated and $Z_{\rm in}$ can be brought to any point of the blue region in Fig. 5, which covers the desired DLM trajectory. In turn, only one tuning element is required for this topology. This matching network topology is actually equivalent to that shown in Fig. 3, because a part of the fixed inductor can be absorbed in the fixed matching network to provide the inductive $Z_{\rm Opt}(f_0, P_{\rm Max})$.

B. Fixed Matching Network

The fixed matching network is aimed to transform 50 Ω to 10 Ω within the bandwidth of interest (a 67%-bandwidth 5:1 impedance transformer). Recently, a high-order

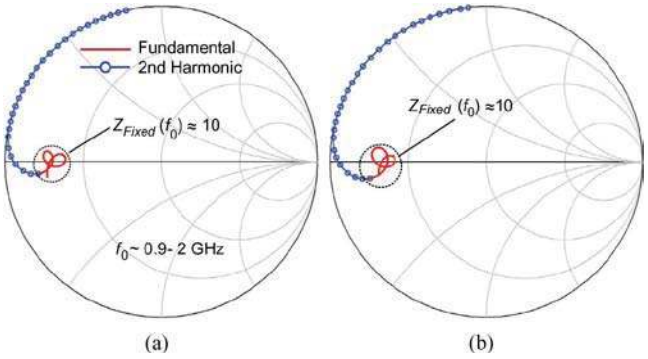

Fig. 7. Input impedance of the implemented fixed matching network extracted from (a) schematic simulation and (b) full-wave simulation.

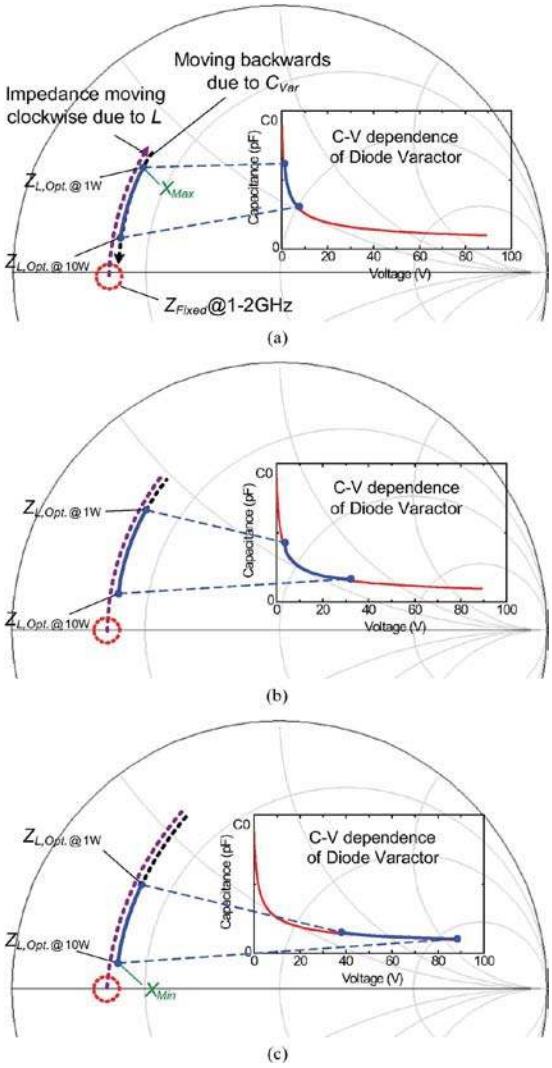

Fig. 8. Broadband DLM matching scheme using diode-varactor-based tunable matching network. (a) At 1 GHz. (b) At 1.5 GHz. (c) At 2 GHz.

low-pass filter has been successfully applied in designing octave-bandwidth high-efficiency PAs [19]. This low-pass-filter matching topology is also utilized in this design. A 3-stage low-pass matching network is designed to achieve the 5:1 impedance transformer across the 1–2 GHz bandwidth, as shown in Fig. 6(a). Using the similar synthesis and implementation method as presented in [19], the fixed low-pass matching network is implemented using transmission lines, shown in Fig. 6(b). The inductors and capacitors are replaced by high-impedance (high-Z) transmission line sections and low-impedance open-circuit stubs, respectively. The parameters of the implemented low-pass matching network are also shown in Fig. 6(b).

Fig. 7(a) and (b) plots the simulated fundamental and second-harmonic impedances of the implemented low-pass matching network within the target frequency band. A good agreement between schematic and full-wave simulations is observed. The input impedance enclosed in the black circle (within 1–2 GHz) has a real part of approximately 10 Ω.

C. Tunable Series LC Resonator

The tunable capacitor is the most critical component in the output matching network. To date, various varactor techniques have been utilized to implement the tunable PA, such as diodes [10]–[12], MEMS varactors/switches [13], and LDMOS [15]. Considering the tuning range and commercial availability, diode varactors are chosen in this design. For a diode varactor, quality factor, power handling, tuning range, and linearity are the most important parameters taken into account for microwave applications. The GaAs varactor diodes, used in [11], has a high quality factor of up to 3000 at 50 MHz, but its low break down voltage, typically 20 V, hinders its application to high power circuits. The hyperabrupt-doping silicon diodes yield a very high tuning range, but they also lead to a low quality factor [23], [24] and poor linearity [25]. Considering these four parameters, the abrupt-junction silicon diode varactors from Micrometrics (MTV4090 series) are utilized for implementing this tunable PA. They have a high break down voltage of 90 V, high tuning range of $C_{\rm Max}/C_{\rm Min} > 8$, and fairly high quality factors of 750–1000 at 50 MHz [23]. A similar Micrometrics varactor (MTV4060-12-20) has been successfully applied in high power designs [12], [14]. The voltage-dependent junction capacitance (C_j) of this uniformly doped diode is theoretically expressed as

$$C_j(V_B) = \frac{C_0}{\left(1+\frac{V_B}{B}\right)^M} \tag{2}$$

where C_0 denotes the initial capacitance value, $B = 0.5$ V, and $M = 0.45$. Thus, the imaginary part of (1) becomes

$$X = \omega L - \frac{(1+2V_B)^{0.45}}{\omega C_{\rm Var,0}} \tag{3}$$

where $C_{\rm Var,0}$ does not have to be C_0 in (2) as a combination of varactors (series or/and parallel) can be used in the actual circuit, which allows a better design flexibility.

Fig. 8 depicts how the DLM locus is matched using the tunable OMN within 1–2 GHz, where $Z_{L,\rm Opt}(f_0, P)$ stands for the optimized input impedance of the tunable OMN for different frequencies and power levels. As the fixed matching network has already transformed the 50-Ω load to the region enclosed in the red circle, the impedance moves clockwise due to the series inductor and is brought back by the varactor. As the frequency increases, the fixed inductor makes the impedance travel farther and a smaller capacitance is needed to compensate it. Therefore, at different frequencies, different fragments of the diode tuning range are used to cover the DLM locus, as shown in Fig. 8(a)–(c). The blue lines represent the covered DLM locus

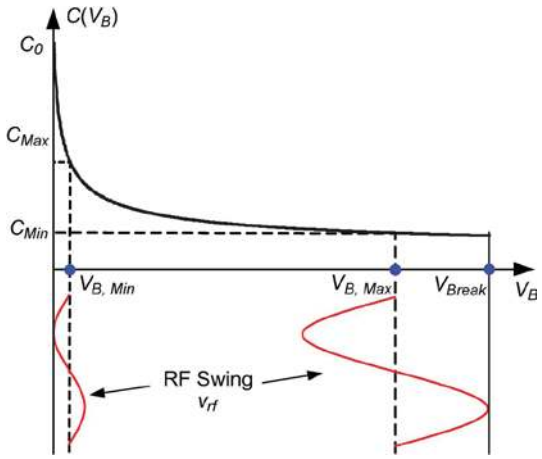

Fig. 9. Turn-on and breakdown limits of diode varactors in presence of RF swings [12].

corresponding to the capacitance value of the varactor. It is also observed that $C_{\mathrm{Var,Max}}(V_{B,\mathrm{Min}})$ denotes $Z_{L,\mathrm{Opt}}$ of 1 W output power at 1 GHz, $C_{\mathrm{Var,Min}}(V_{B,\mathrm{Max}})$ denotes $Z_{L,\mathrm{Opt}}$ of 10 W output power at 2 GHz. Therefore, as depicted in Fig. 8(a)–(c), the dynamic load modulation locus can be covered at every frequency point within the 1–2 GHz band, and the nearly entire tuning range of the varactor is applied.

To optimize this tunable LC resonator, firstly, the values of L and $C_{\mathrm{Var},0}$ can be estimated analytically by

$$\begin{aligned} X_{\mathrm{Max}} &= \omega_{\mathrm{Min}} L - \frac{(1+2V_{B,\mathrm{Min}})^{0.45}}{\omega_{\mathrm{Min}} C_{\mathrm{Var},0}} \\ X_{\mathrm{Min}} &= \omega_{\mathrm{Max}} L - \frac{(1+2V_{B,\mathrm{Max}})^{0.45}}{\omega_{\mathrm{Max}} C_{\mathrm{Var},0}} \end{aligned} \tag{4}$$

where $X_{\mathrm{Max}} \approx 16$ and $X_{\mathrm{Min}} \approx 6$ denote the imaginary parts of $Z_{L,\mathrm{Opt}}$ at 1 W, 1 GHz [Fig. 8(a)] and $Z_{L,\mathrm{Opt}}$ at 10 W, 2 GHz [Fig. 8(c)], respectively. According to (4), $V_{B,\mathrm{Min}}$ and $V_{B,\mathrm{Max}}$ need to be determined in order to find the proper values of L and $C_{\mathrm{Var},0}$. Due to the RF swing across the varactor, which should be carefully considered in the high power design, the entire tuning range is usually not achievable. The final design will be further optimized using ADS simulation together with a compromise between bandwidth and power-handling capability.

D. Power Handling Issues and Enhancement

For the adaptive high power amplifier application, the RF voltage swing (v_{rf}) on a tuning element is usually very large, e.g., 26.6 V when an output power of 7 W is delivered [12]. To avoid turn-on and breakdown of the diode, as illustrated in Fig. 9, the dc-bias voltage and the RF voltage swing should satisfy the following relation:

$$|v_{\mathrm{rf}}| \le V_B \le V_{\mathrm{Break}} - |v_{\mathrm{rf}}|. \tag{5}$$

Therefore, as illustrated in Fig. 9, V_B should be sufficiently far away from the turn-on point (0 V) and the breakdown point (90 V), which actually reduces the tuning range of the varactor $(C_{\mathrm{Max}}/C_{\mathrm{Min}})$. To enhance the power handling of the varactor diodes and to increase the tuning range, a diodes-stack with $M \times N$ elements in parallel and series can be utilized [25].

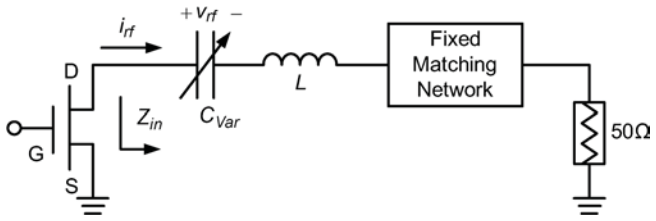

Fig. 10. Prediction of the voltage swing on the tuning element.

Therefore, the RF swing of each varactor diode is divided by a factor of N. Practically, this method introduces extra parasitics that should be considered carefully for GHz-level applications. In this design, $N = 2$ is considered, serving as the anti-series (or back-to-back) diodes pair [26]. On the other hand, to further reduce the series resistance, five pairs of anti-series diodes are stacked in parallel $(M = 5)$ as a single tuning element. This anti-series topology also enhances the linearity of the varactor, which has been demonstrated in [25] and [26].

The RF voltage swing is also dependent on the matching network topology and the location of the tuning element. In [12], the varactors are connected in parallel with the load, so the voltage swing across the varactor is the same as the load voltage amplitude. In our design, the varactor is connected in series with the transistor drain (Fig. 10). Therefore, the voltage swing across it is dependent on the output RF current of the drain, which can be approximately calculated by

$$|i_{\mathrm{rf}}| = \sqrt{\frac{2P_{\mathrm{out}}}{R_{\mathrm{in}}}} \tag{6}$$

where R_{in} is around 10 Ω and maximum P_{out} is 10 W. In turn, the voltage swing across the varactor can be estimated by

$$|v_{\mathrm{rf}}| = |i_{\mathrm{rf}}| \times \frac{1}{\omega C_{\mathrm{Var}}}. \tag{7}$$

The above (7) underlines that a larger capacitance value (C_{Var}) results in a smaller voltage swing. However, (3) also implies that a smaller $C_{\mathrm{Var},0}$ is needed to achieve a larger impedance tuning range. Therefore, a compromise between the tuning range and the voltage swing is necessarily made here to select the value of $C_{\mathrm{Var},0}$.

Herein, a simplified ADS model of the output matching network is utilized to investigate the proper value of $C_{\mathrm{Var},0}$, which is shown in Fig. 11(a). A 5×2 varactor stack is used here, leading to $C_{\mathrm{Var},0} = 2.5C_0$. In this topology, the voltage swing across each diode is an half of the total voltage swing across the diode-stack.

For any given value $C_{\mathrm{Var},0}$, a harmonic-balance (HB) ADS simulation provides the expected maximum voltage swing at 1 GHz [red line in online version in Fig. 11(b)]. Based on Fig. 8 under the restriction outlined in (5), the maximum frequency (f_{Max}) that a perfect match can be achieved will depend on this voltage swing. This maximum frequency can be calculated by HB simulation by varying the bias voltage (V_B) in Fig. 11(a). The maximum frequency versus $C_{\mathrm{Var},0}$ is plotted in Fig. 11(b). It can be seen that, as the value of $C_{\mathrm{Var},0}$ increases, the voltage swing drops significantly from 70 V to around 10 V, while f_{Max} increases sharply and reaches a local maximum when $C_{\mathrm{Var},0} \approx$

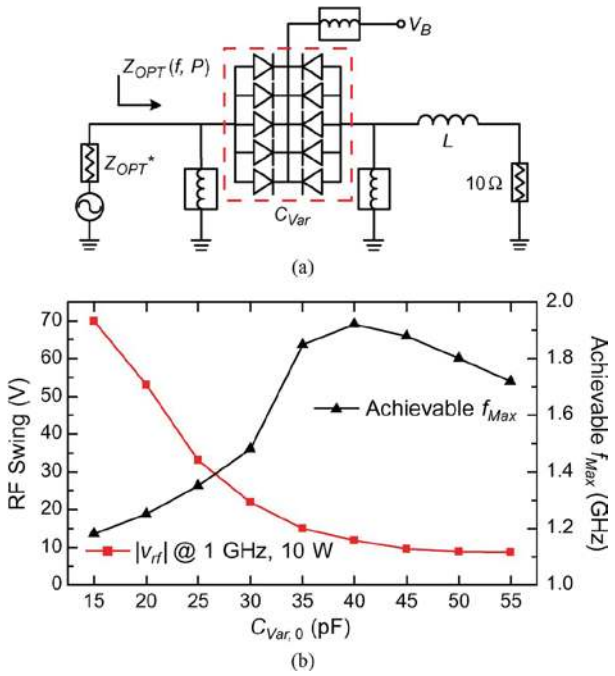

Fig. 11. Determining the optimal value of $C_{\mathrm{Var},0}$. (a) Simplified ADS model. (b) Voltage swing and tuning range versus $C_{\mathrm{Var},0}$.

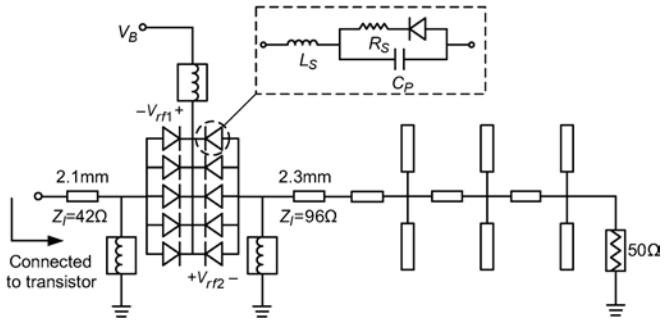

Fig. 12. Circuit topology of the output matching network.

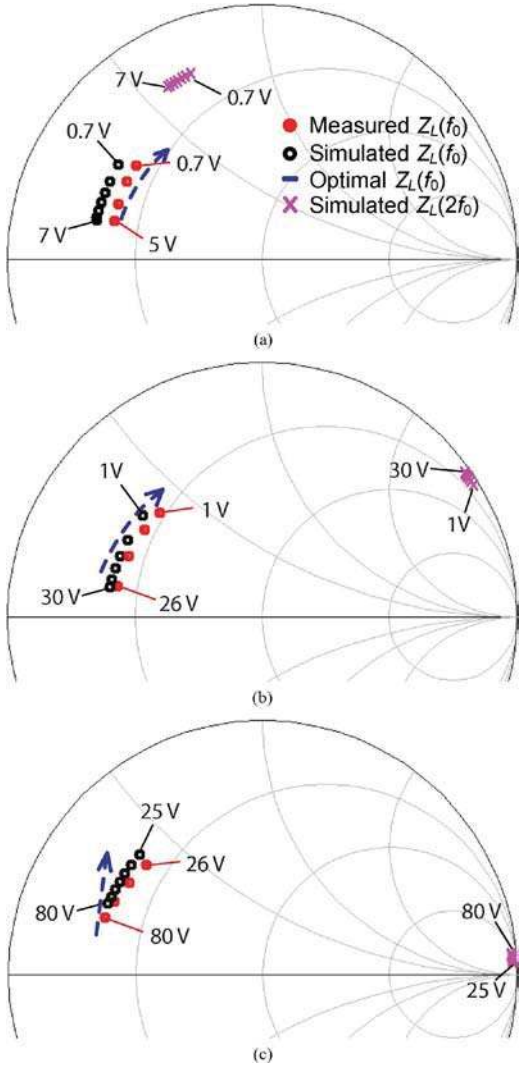

Fig. 13. Measured and simulated input impedances and simulated second-harmonic impedance of the output matching network. (a) At 1 GHz. (b) At 1.5 GHz. (c) At 1.9 GHz.

40 pF. For $C_{\mathrm{Var},0} > 40$ pF, the tuning range decreases gradually, because a larger initial capacitance value leads to a smaller reactance variation range as indicated in (3). Therefore, the optimal value of $C_{\mathrm{Var},0}$ is around 40 pF for achieving a maximum frequency tuning range.

However, according to [23], a larger capacitance value leads to a lower quality factor. As a result, the Micrometrics diode varactor with $C_0 = 14.8$ pF and $Q = 800$ at 50 MHz (MTV4090-12-1) is selected, leading to $C_{\mathrm{Var},0} = 37$ pF for the 5×2 diodes stack. To achieve a wider frequency tuning range, a compromise needs to be made with lower output power and/or smaller dynamic range, e.g., 5–1 W.

The output matching network is eventually optimized together with the transistor using ADS, in order to perfect the PA performance in frequency and efficiency. The finalized design is schematically shown in Fig. 12. The diode model used in this design is shown in the dotted rectangle of Fig. 12, same as that presented in [12]. The parasitics involve a series inductance L_S of 1.5 nH, a series resistance R_S of 1.2 Ω, and a parallel capacitance C_p of 0.2 pF. The inductive parasitic (due to both the package and connection) and detuning effect of the diode-stack layout can result in a fairly significant mismatch, as mentioned in [12]. It is important to note that these two effects can be compensated by the series inductor L in this particular topology, leading to no adverse impact on the matching accuracy. This series inductor is implemented using a 96-Ω transmission line with an electrical length of 5.8° at 1.5 GHz (2.3 mm), which is approximately equivalent to a 2.1-nH inductor. Another 2.1-mm 42-Ω transmission line is placed on the left-hand side of the varactor to fit the leading pad of the packaged GaN transistor.

E. Evaluation of the Entire Tunable Output Matching Network

The varactor-based tunable OMN is implemented and characterized in advance of the PA. Fig. 13 shows the measured and simulated small-signal DLM impedance locus of the tunable OMN at 1, 1.5, and 1.9 GHz, respectively. The simulation and measurement agree well with each other. They show a good coverage of the optimal DLM locus (Fig. 3). Fig. 13 also plots the simulated second-harmonic impedance corresponding the fundamental one with the same V_B, indicating that $Z_L(2f_0)$ of this

TABLE I
SUMMARY OF LARGE-SIGNAL SIMULATION RESULTS

Freq. (GHz)	P_{out} (W)	$\lvert v_{rf}\rvert$ (V)	V_B (V)	Loss (dB)
1	1	1.4	0.7	0.35
1	10	12	6	0.36
1.5	10	14	22	0.25
1.9	10	20	80	0.26

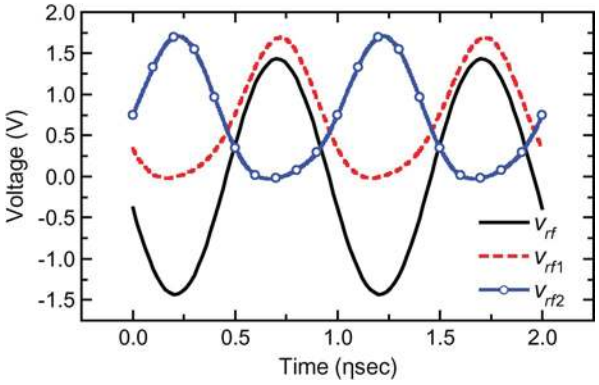

Fig. 14. Simulated voltage waveforms on the varactors for 1-W output power at 1 GHz.

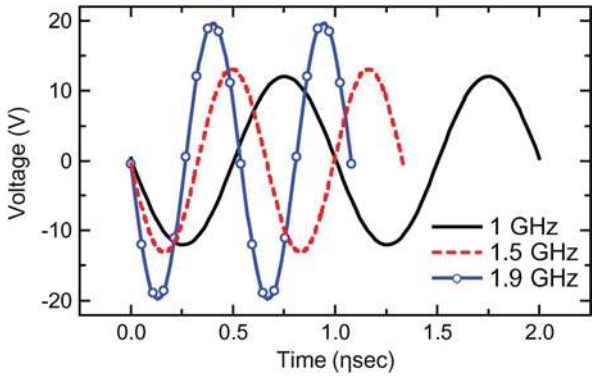

Fig. 15. Simulated voltage waveforms on the stack of varactors for 10-W output power at 1, 1.5, and 1.9 GHz.

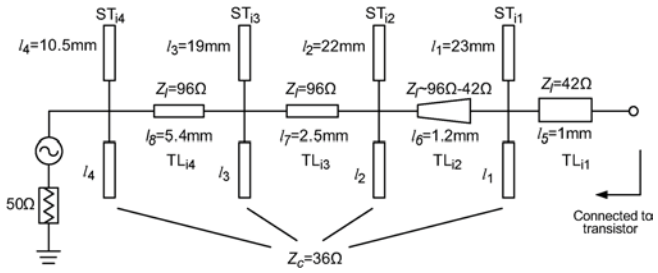

Fig. 16. Schematic of the input matching network [19].

output matching network locates in the high-efficiency region compared to Fig. 4.

Furthermore, the large-signal characterization of the tunable OMN is performed using the HB simulator in ADS. Table I lists the simulation results at different power levels and different frequencies, indicating a low insertion loss of <0.4 dB and 10-W power handling capability. Fig. 14 shows the simulated voltage waveforms of the matching network for $V_B = 0.7$ V ($V_{B,\mathrm{Min}}$) and $P_{\mathrm{out}} = 1$ W. v_{rf1} and v_{rf2} are the voltage swings across two varactors in series in Fig. 12. It is observed from Fig. 14 that the

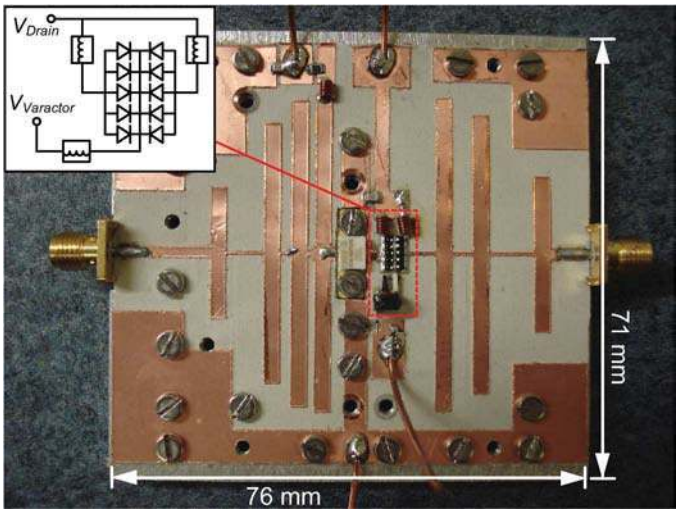

Fig. 17. Fabricated circuit of the adaptive power amplifier.

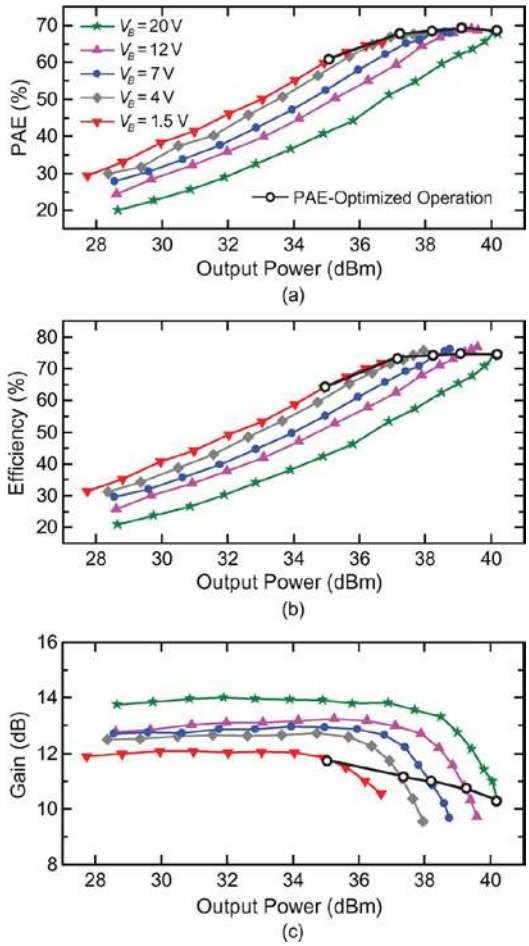

Fig. 18. Measured PA performance at 1.3 GHz versus output power for various varactor bias voltages. (a) PAE. (b) Efficiency. (c) Gain.

varactor voltages do not cross 0 V, thus avoiding the turn-on effect. It is also noted that although the voltage waveforms on each of the varactors are distorted, the total voltage of anti-series varactors is almost a perfect sinusoidal wave. Fig. 15 shows the simulated v_{rf} at 1, 1.5, and 2 GHz when 10-W power is delivered. As the total voltage swing is equally shared by these two series varactors, i.e., $v_{\mathrm{rf1}} = v_{\mathrm{rf2}} = v_{\mathrm{rf}}/2$, the turn-on or

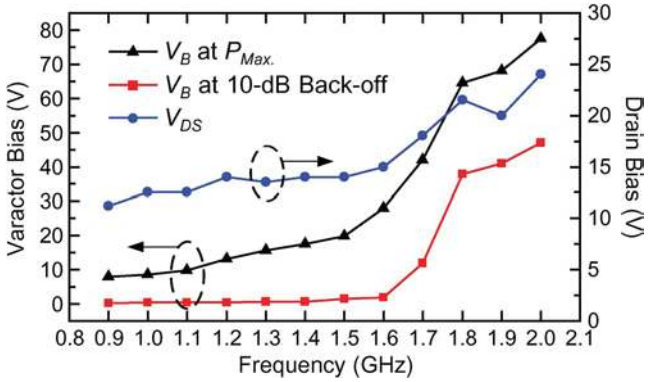

Fig. 19. Optimal bias voltage of varactor diode at the maximum power level and 10-dB back-off within 0.9–2 GHz.

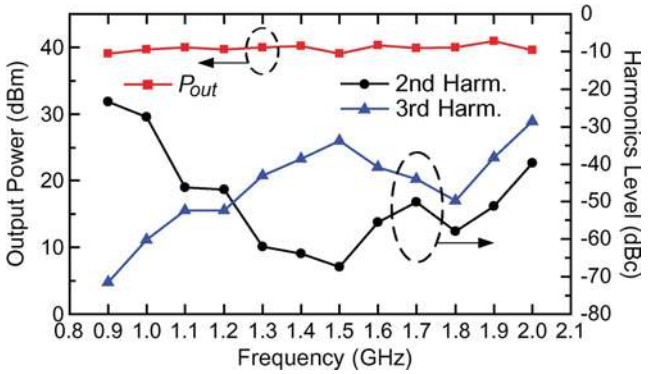

Fig. 20. Measured maximum output power and harmonics level.

breakdown limits expressed in (5) are not exceeded, according to the bias voltages listed in Table I.

IV. PA Design and Implementation

The broadband input matching network in this design is the same as that in [19], which has been optimized for L-band input matching of the CGH40025 transistor. The schematic of the input matching network is shown in Fig. 16. The entire PA circuit is fabricated on a Rogers Duroid 5880LZ substrate with a thickness of 20 mil, as shown in Fig. 17. The circuit board is mounted on an aluminum plate which serves as a heat sink and common ground. The gate bias network is realized using a 27–nH Coilcraft air-coil inductor in series with a 250-Ω resistor. The same inductor is also used for the drain biasing network. A Coilcraft conical inductor of 0.57 μH, which is ultra broadband and high-Q, is utilized to bias the varactors. It is important to note that the actual bias voltage on the varactor is the electrical potential difference between the varactor voltage and the drain voltage, as shown in the insert of Fig. 17, which is given by

$$V_B = V_{\text{Varactor}} - V_{\text{Drain}}. \tag{8}$$

The dc blocks are not included in this circuit board, and two external dc blocks are connected at the input and output in the PA testing.

V. Experimental Results of the Broadband Load-Modulated PA

In previous sections, the optimum bias voltage of the varactor has been found from the independent characterizations of the transistor and the tunable OMN, as shown in Fig. 3 and Fig. 13, respectively. Combining them together as the adaptive PA, the actual optimum-bias-voltage is obtained eventually in the PA testing, by perfecting the PA efficiency with respect to different frequencies and different power levels. Two cases are compared

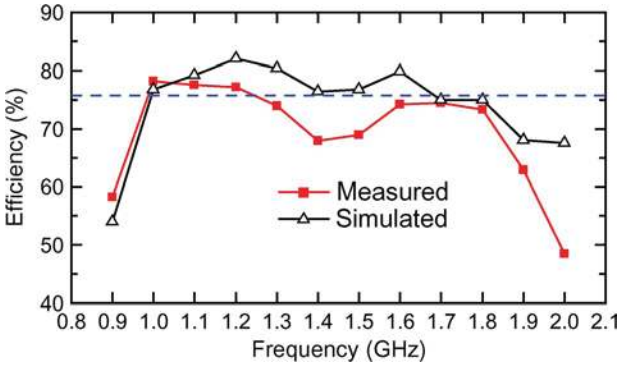

Fig. 21. Measured and simulated efficiency at the maximum power level.

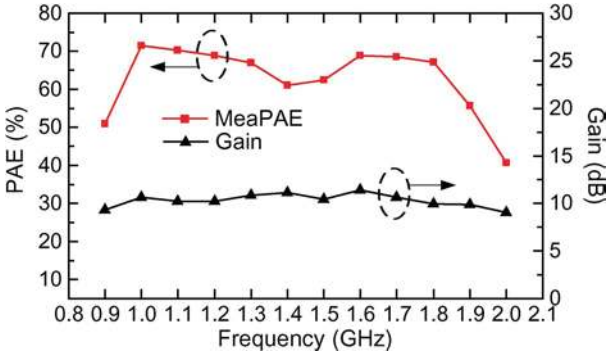

Fig. 22. Measured PAE and gain at the maximum power level.

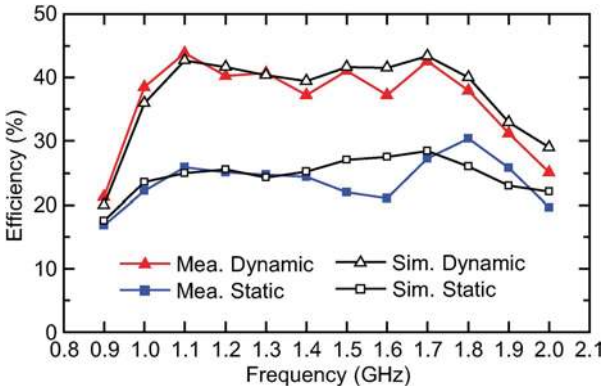

Fig. 23. Measured and simulated drain efficiency at 10-dB power back-off.

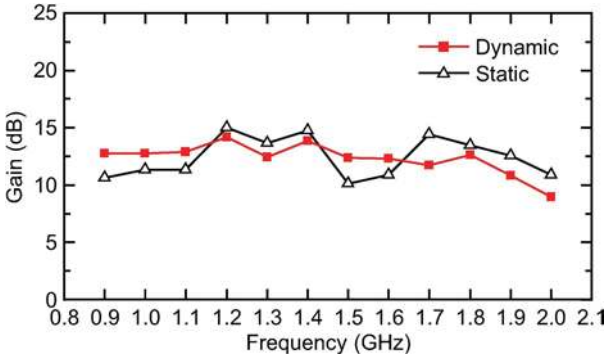

Fig. 24. PA gain at 10-dB back-off under static operation and DLM operation.

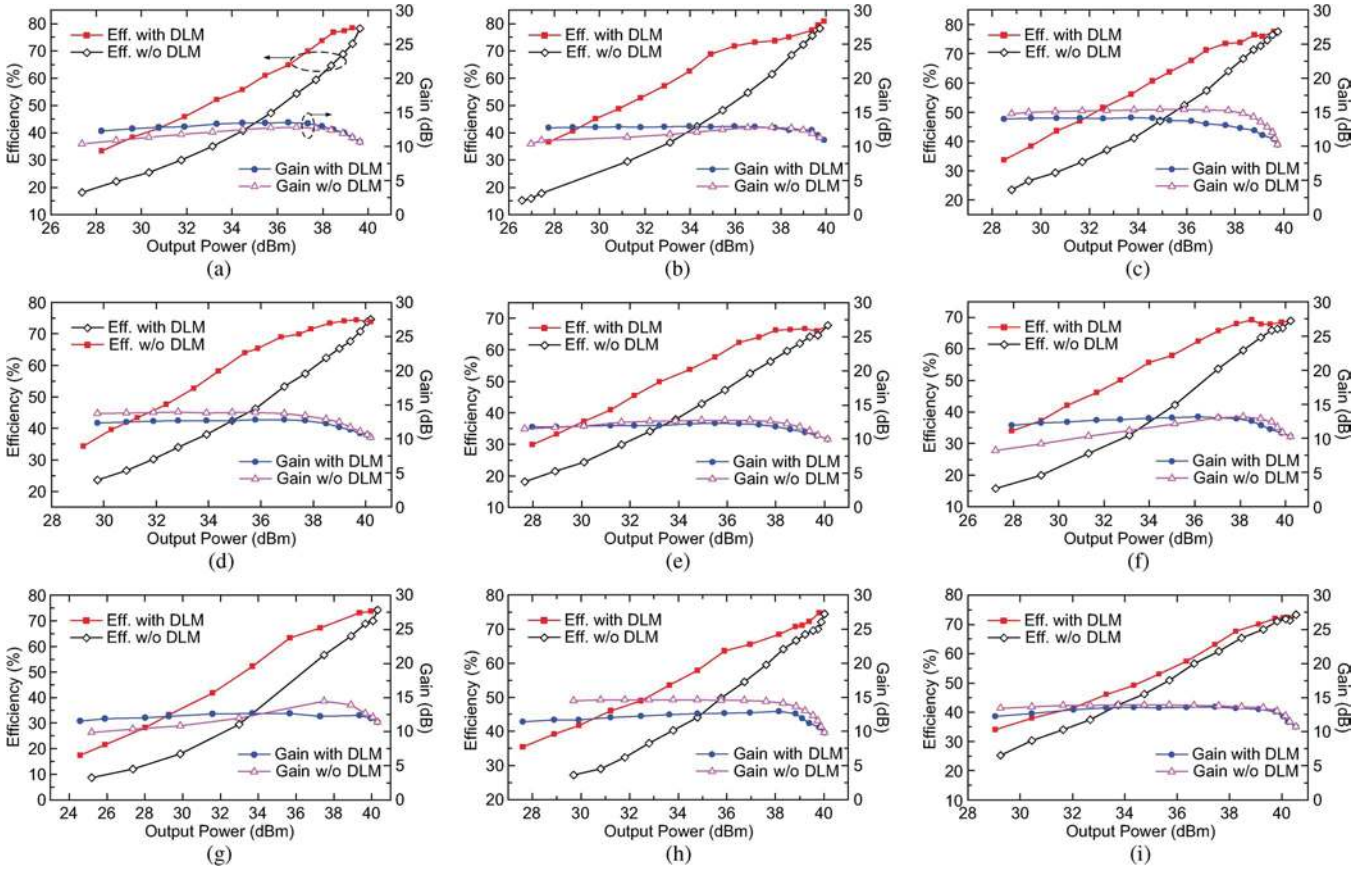

Fig. 25. Measured PA gain and efficiency under the DLM operation and static operation. (a) 1 GHz. (b) 1.1 GHz. (c) 1.2 GHz. (d) 1.3 GHz. (e) 1.4 GHz. (f) 1.5 GHz. (g) 1.6 GHz. (h) 1.7 GHz. (i) 1.8 GHz.

here: 1) the classical high-efficiency PA with the TMN statically tuned for only the maximum power level at each frequency point; 2) the dynamic PA with OMN dynamically modulated for different power level.

The transistor gate is biased at the pinch-off point of -3.3 V. The DLM-PA is excited with a continuous-wave input signal, which is generated by an Agilent signal generator and boosted by a driver PA. The output power is measured by a spectrum analyzer, and the losses in the connecting cables has been calibrated beforehand. A power-sweep experiment is first performed with the realized PA at 1.3 GHz for various varactor bias voltages to validate its operation. Fig. 18 shows the measured PAE, efficiency and gain versus $P_{\rm out}$ for five different V_B values, indicating that a significant enhancement at power back-offs can be achieved by decreasing V_B. It is also seen from Fig. 18(c) that a flatter gain versus $P_{\rm out}$, compared to the static case, is achieved under the efficiency-optimized controlling scheme, implying a good potential for performing linearization on this PA using digital-predistortion-based techniques, such as [14] and [15].

The same experiment is conducted over the entire band from 0.9 to 2 GHz with steps of 0.1 GHz. Fig. 19 shows the optimized V_B at maximum power level and 10-dB back-off, as well as the drain bias voltage, versus frequency. Fig. 20 plots the measured maximum power and corresponding harmonics level at each frequency point. This is the highest power level demonstrated for the adaptive PA design compared to the state-of-the-art results [10], [12], [15]. It is also seen from Fig. 20 that the second and third harmonics are very low (less than -30 dBc for most of the frequency points), due to the combined filter behavior of the low-pass matching network and the LC resonator tank. Moreover, the high-linearity antiseries topology of varactors leads to an insignificant contribution to the harmonic generation [12]. Fig. 21 plots the measured efficiency at the maximum power level within the entire band, which agrees with the predicted efficiency from ADS simulation. The measured efficiency of 64%–79% is achieved from 1 to 1.9 GHz. Fig. 22 shows the measured PAE and gain at the maximum power level, which shows that 55%–72% PAE and $\cong$10-dB gain are achieved from 1 to 1.9 GHz. The drop of PA performance above 1.9 GHz is primarily due to the connection parasitics and the dispersive effect of the varactor-stack. The maximum-power performance of this tunable PA compares favorably to the state-of-the-art static broadband PAs [16]–[18]. Compared to the static low-pass-filter-based PA in [19], the efficiency-degradation of this adaptive PA is mainly owing to the lossy diode varactors. The PA performance can be further improved, if using varactors with higher quality factors, e.g. MEMS, ferroelectric or LDMOS transistor [15].

The measured and simulated PA efficiencies at 10-dB power back-off are shown in Fig. 23, indicating a good agreement between measurement and simulation. The comparison is made between the static operation (fixed V_B for $P_{\rm Max}$) and DLM operation (efficiency-optimized V_B). From 1 to 1.7 GHz, the efficiency improvement at 10-dB back-off is typically greater than 15%, resulting in an effective doubling of the efficiency when

compared to the PA with a static load. The efficiency improvement degrades when operating above 1.8 GHz, because the optimal DLM locus deviates from the constant-resistance circle [see Fig. 3(c)] due to the transistor's package parasitics. For higher frequency applications, i.e., >2 GHz, the same design methodology can be conducted on an unpackaged transistor, e.g. the one used in a 2.65 GHz load-modulated PA in [15]. Moreover, the DLM operation results in a minimal effect on the PA gain at the 10-dB back-off, which can be observed from Fig. 24.

Fig. 25 plots the measured efficiency and gain of this load-modulated PA under the efficiency-optimized and static operations from 1 to 1.8 GHz. It is indicated that an optimized DLM operation can be conducted over a broad power range (>10 dB) within the entire L-band. The reduction of dc power consumption using this DLM optimization can be calculated by

$$\Delta P_{\rm dc} = \frac{P_{\rm out}}{\eta_{\rm Static}} - \frac{P_{\rm out}}{\eta_{\rm Dynamic}}. \quad (9)$$

For example, the increase of efficiency from 25% to 40% at 1-W power level, shown in Fig. 25 (operating at 1.3 GHz), indicates a 1.8-W reduction of the dc power consumption. For amplification of an actual communication signal, V_B is dynamically tuned by the base-band processor according to the instantaneous envelop of the signal. Using the dynamic-controlling and linearization techniques for single-band DLM-PAs [14], [15], which has the same load-adaption range, a multiband DLM transmitter can be created with this PA.

VI. Conclusion

A novel methodology for designing and implementing adaptive power amplifier with continuous tunability for broadband dynamic-load-modulation has been proposed in this paper. The tunable output matching network is composed of a combination of a tunable series resonator in cascade with a sixth-order low-pass filter. Commercial available diode varactors with high breakdown voltage and high tuning range are used to realize the tunability. The implemented PA achieves a substantial operating frequency band from 1–1.9 GHz, in which an optimal dynamic-loadline-modulation is performed. A PA performance of ≈10-W peak power, ≈10-dB gain, 64%–79% peak-power efficiency, and 30%–45% 10-dB back-off efficiency has been measured throughout this band. This is the first experimental demonstration of a high-power, high-efficiency, broadband and dynamically-load-modulated PA suitable for next-generation wireless communication systems.

Acknowledgment

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References

[1] P. Saad, H. M. Nemati, M. Thorsell, K. Andersson, and C. Fager, "An inverse class-F GaN HEMT power amplifier with 78% PAE at 3.5 GHz," in *39rd Eur. Microw. Conf.*, Oct. 2009, vol. 1, pp. 496–499.

[2] A. Adahl and H. Zirath, "A 1 GHz class E LDMOS power amplifier," in *33rd Eur. Microw. Conf.*, Oct. 2003, vol. 1, pp. 285–288.

[3] D. Kang, D. Kim, J. Choi, J. Kim, Y. Cho, and B. Kim, "A multimode/multiband power amplifier with a boosted suply modulator," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 10, pp. 2598–2608, Oct. 2010.

[4] J. Kang, D. Yu, K. Min, and B. Kim, "A ultra-high PAE Doherty amplifier based on 0.13-mm CMOS process," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 9, pp. 505–507, Sep. 2006.

[5] M. Pelk, W. Neo, J. Gajadharsing, R. Pengelly, and L. de Vreede, "A high-efficiency 100-W GaN three-way Doherty amplifier for base-station applications," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 7, pp. 1582–1591, Jul. 2008.

[6] G. Hanington, P.-F. Chen, P. M. Asbeck, and L. E. Larson, "High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 8, pp. 1471–1476, Aug. 1999.

[7] J. Jeong, D. Kimball, M. Kwak, P. Draxler, C. Hsia, C. Steinbeiser, T. Landon, O. Krutko, L. Larson, and P. Asbeck, "High-efficiency WCDMA envelope tracking base-station amplifier implemented with GaAs HVHBTs," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2629–2639, Oct. 2009.

[8] J. Qureshi, M. Pelk, M. Marchetti, W. Neo, J. Gajadharsing, M. van der Heijden, and L. de Vreede, "90-W peak power GaN outphasing amplifier with optimum input signal conditioning," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 8, pp. 1925–1935, Aug. 2009.

[9] F. H. Raab, "High-efficiency linear amplification by dynamic load modulation," in *Proc. IEEE MTTS Int. Microw. Symp.*, 2003, pp. 1717–1720.

[10] W. E. Neo, J. Lin, X. Liu, L. C. N. de Vreede, L. E. Larson, M. Spirito, M. Pelk, K. Buisman, A. Akhnoukh, A. de Graauw, and L. Nanver, "Adaptive multi-band multi-mode power amplifier using integrated varactor-based tunable matching network," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2166–2177, Sep. 2006.

[11] J. Fu and A. Mortazawi, "Improving power amplifier efficiency and linearity using a dynamically controlled tunable matching network," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 12, pp. 3239–3244, Dec. 2008.

[12] H. M. Nemati, C. Fager, U. Gustavsson, R. Jos, and H. Zirath, "Design of varactor-based tunable matching networks for dynamic load modulation of high power amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 5, pp. 1110–1118, May 2009.

[13] A. M. M. Mohamed, S. Boumaiza, and R. R. Mansour, "Novel reconfigurable fundamental/harmonic matching network for enhancing the efficiency of power amplifiers," in *Proc. Eur. Microw. Conf. Tech.*, Sep. 2009, pp. 1122–1125.

[14] H. Cao, H. M. Nemati, A. S. Tehrani, T. Eriksson, J. Grahn, and C. Fager, "Linearization of efficiency-optimized dynamic load modulation transmitter architectures," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 4, pp. 873–881, Apr. 2010.

[15] H. M. Nemati, H. Cao, B. Almgren, T. Eriksson, and C. Fager, "Design of highly efficient load modulation transmitter for wideband cellular applications," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 11, pp. 2820–2828, Nov. 2010.

[16] P. Wright, J. Lees, J. Benedikt, P. J. Tasker, and S. C. Cripps, "A methodology for realizing high efficiency class-J in a linear and broadband PA," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 12, pp. 3196–3204, Dec. 2009.

[17] D. Wu, F. Mkadem, and S. Boumaiza, "Design of a broadband and highly efficient 45 W GaN power amplifier via simplified real frequency technique," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2010, pp. 1090–1093.

[18] P. Saad, C. Fager, H. Cao, H. Zirath, and K. Andersson, "Design of a highly efficient 2–4-GHz octave bandwidth GaN-HEMT power amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 7, pp. 1677–1685, Jul. 2010.

[19] K. Chen and D. Peroulis, "Design of highly efficient broadband class-E power amplifier using synthesized low-pass matching networks," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 12, pp. 3162–3173, Dec. 2011.

[20] "Agilent Technologies Inc.," Santa Clara, CA [Online]. Available: http://www.agilent.com

[21] F. H. Raab, "Electronically tunable class-E power amplifier," in *Proc. IEEE MTTS Int. Microw. Symp.*, 2001, pp. 1513–1516.

[22] S. C. Cripps, *RF Power Amplifier for Wireless Communications*, 2nd ed. Boston, MA: Artech, 2006.

[23] "Aeroflex/Metelics," Londonderry, NH [Online]. Available: http://www.aeroflex.com/ams/metelics
[24] "Skyworks Solution Inc.," Woburn, MA [Online]. Available: http://www.skyworksinc.com/
[25] R. G. Meyer and M. L. Stephens, "Distortion in variable-capacitance diodes," *IEEE J. Solid-State Circuits*, vol. 10, no. SSC-1, pp. 47–54, Feb. 1975.
[26] K. Buisman, L. C. N. de Vreede, L. E. Larson, M. Spirito, A. Akhnoukh, T. L. M. Scholtes, and L. Nanver, "Distortion-free varactor diode topologies for RF adaptivity," in *Proc. IEEE MTTS Int. Microw. Symp.*, 2005, pp. 157–160

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Mr. Chen was the recipient of the Third-Place Award of the Student High Efficiency Power Amplifier Design Competition in 2011 IEEE MTT-S International Microwave Symposium (IMS).

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He has been with Purdue University, West Lafayette, IN, since August 2003, where he leads the Adaptive Radio Electronics and Sensors (ARES) Team that focuses on reconfigurable analog/RF electronics for adaptive communications, signal intelligence, and harsh-environment sensors. He has been a PI/co-PI in over 40 projects funded by government agencies and industry in these areas. Since 2007, he has been a key contributor to the DARPA Analog Spectral Processors (ASP, Phases I–III) project resulting in the first widely tunable (tuning range $>$3:1) preselect radio filters with unprecedented quality factors ($Q > 1000$) and power handling ($>$10 W) for high frequency applications (1–30 GHz). A wide variety of reconfigurable filters with simultaneously adaptable features including frequency, bandwidth, rejection level, filter order, and group delay have been demonstrated over the past four years. His group recently codeveloped a ground-breaking concept of field programmable filter arrays (FPFAs). Inspired by FPGAs in digital systems, FPFAs are based on a sea of coupled resonators and multiple ports in order to enable reutilization of the same adaptive resonators to support diverse needs for dissimilar systems. Arbitrary operational modes and multiple operational channels may be created and reconfigured at will. He has made significant advances in high-power high-efficient power amplifiers and RF CMOS ICs with high-efficiency antennas. In the areas of sensors, he has also demonstrated the first wireless battery-free high-temperature MEMS sensors for health monitoring of sensitive bearings in aircraft engines. These sensors continuously monitor (RFID-type) the true temperature of the bearing to over 300 °C or 550 °C (depending on the design) and wirelessly transmit it to a base station. These sensors are based on well-established silicon processing for low-cost high-yield manufacturing. They have demonstrated extremely robust operation for over 1-B cycles and continuous loading for over three months without failure.

Prof. Peroulis' team won third place in the student PA design competition at the 2011 International Microwave Symposium (IMS). He was assistant team leader to a student design team at Purdue University that won the first place awards in Phases I and II of the 2007–2008 SRC/SIA IC Design Challenge by demonstrating high-efficiency chip-to-chip wireless links with U-band transceivers. Further advances led to bondwire Yagi antenna arrays with efficiencies exceeding $>$80%.