Design of an Advanced PLL for Accurate Phase Angle Extraction Under Grid Voltage Harmonics/Interharmonics and DC Offset

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Abstract: The presence of dc offset and harmonics/interharmonics in grid voltage input signal of phase-locked loop (PLL) results in inaccurate controller response. The inaccuracies are due to the low and high frequency oscillations that appear in the PLL estimated phase, amplitude and frequency. The importance of DC offset and harmonic/interharmonic rejection capability for PLLs can be appreciated by international standards that impose strict limitations for grid-tied converters. The suppression of fundamental frequency oscillations caused by DC offset in the input signal must be carried out without compromising the dynamic response of the system. The use of low pass filters for example results in undesirable, slow response. This paper proposes an accurate and fast decoupling of fundamental frequency oscillations using a mathematic cancellation decoupling cell. Higher frequency oscillations generated by harmonics/interharmonics are eliminated by a different compensation network (HCN) that is also proposed in this paper. The performance of conventional techniques is limited because they eliminate only specifically selected harmonics. The proposed HCN module, however, eliminates any number of harmonics/interharmonics present in the grid with the least computational complexity and without any prior knowledge. Furthermore, its advanced features provide accurate synchronization under any abnormal grid condition at the lowest computational complexity when compared to existing state-of-the-art PLLs. The advanced performance of the proposed Harmonic-Interharmonic-DC-Offset (HIHDO) PLL is verified through simulation and experimental results.

1. Introduction

The continuous large scale integration of renewable energy sources (RES) require the development of appropriate control techniques that can work accurately in order to meet the ever-changing grid regulations. The main controllable system component that offers design flexibility and adjustability is the grid side converter (GSC) [1-3]. The control system of GSC can be designed in two control frames, that is, the stationary $\alpha\beta$ reference frame using a Proportional Resonant (PR) controller and/or the synchronous reference frame (SRF) by employing a conventional PI controller [4]. The control of GSC in $\alpha\beta$ frame requires a frequency lock loop (FLL) for acquiring the accurate value of grid frequency [4, 5]. In contrast, the latter case uses the phase angle information of grid voltage for transforming the three phase measured current/voltage variables into corresponding two phase dq-variables. The control in SRF domain mainly depends on the fast and accurate estimation of grid voltage phase angle, which is usually extracted at Point of Common Coupling (PCC) using Phase-Locked Loop (PLL) algorithm [6-10]. This paper considers the second category, in which a PLL is used as a main component for enabling the implementation of control scheme. The phase angle extraction of PLL is, however, affected by various abnormal grid scenarios, such as, unbalanced grid faults, harmonic distortion, frequency variations, phase jumps, direct current (DC) offset and interharmonics in the grid voltage. Therefore, there is a need to develop more advanced and suitable PLL techniques that can work efficiently under these off-nominal grid situations. The work presented in this paper mainly focuses on the mitigation of harmonics/interharmonics and DC offset problems. Recognizing however that computational complexity is of a major concern since the real time Digital Signal Processors (DSP) employed in GSC have limited storage in performing large number of computations [11, 12], the design of the proposed PLL gave particular attention to this respect as well.

PLL algorithms have undergone many advancements in the past few years and many new PLLs have been proposed. The very basic PLLs developed, based on the two reference frames, are the SRF frame based dqPLL and the stationary αβ frame based αβPLL. The dqPLL [13] utilizes the q-component of fundamental positive SRF and force it to zero by the PI controller. The dqPLL is very simple in structure and performs accurately under balanced grid conditions. However, when an unbalance grid fault occurs (negative voltage sequence), its performance is jeopardized due to the presence of unwanted double frequency oscillations on the q-component of transformed SRF^{+1}. Furthermore, the dqPLL is also not immune to grid voltage harmonic/interharmonic distortion. The αβPLL [14-16] has similar behavior like dqPLL, it cannot perform accurately under unbalanced faults and grid harmonic distortion. However, the frequency overshoot of αβPLL at the instant of fault is less compared to dqPLL. The performance of dqPLL was enhanced by enabling the accurate operation under unbalanced condition in [17], referred to as ddsrfPLL (or equivalent DSOGIPLL [18]). The ddsrfPLL performs accurately due to significant addition of decoupling cells (D.C), which are used to eliminate the unwanted double frequency oscillations from dq^{+1} components. The ddsrfPLL however suffers from slight high frequency overshoot at the time of fault, due to the presence of dqPLL in the phase

detector (PD) part. To reduce the high frequency overshoot of ddsrfPLL, a hybrid dαβPLL is proposed in [8], which replaces the phase detector part of existing ddsrfPLL by αβPLL. The new dαβPLL achieves accurate response, but the only drawback is that it cannot perform satisfactorily under grid voltage harmonics, inter-harmonics and DC offset, similar to that of ddsrfPLL. For mitigating the undesired effect of unbalance and harmonics, some moving average filter (MAF) based techniques are proposed in the literature [19-22]. The MAF versions of dqPLL and ddsrfPLL are proposed in [21], as MAFPLL and MRFPLL. In MAFPLL, the q-component of positively rotated SRF is passed through an MAF and is then provided to PI controller. In MRFPLL, the Low Pass Filters (LPF) of ddsrfPLL are modified by adding MAFs. However, the main drawback of using filters in the control path is the slow dynamic response [7]. Furthermore, the MAFPLL cannot perform adequately under off-nominal grid frequencies and suffers from offset error in the extracted phase angle [6, 21, 23]. The offset error can be reduced by selecting the number of samples according to operating grid frequency but it cannot eliminate the offset error completely [21]. For complete mitigation of inaccurate phase, a possible way is to adapt the MAF window length by enabling the variable sampling rate of PLL [23, 24]. The variable sampling rate is, however, not possible for the accurate operation of GSC controller, since it is not always possible to operate GSC controller at variable sampling period [7]. For instance, if the problem of offset error is solved, still the slow dynamic response due to filter is the main disadvantage of MAF filter. Furthermore, the tuning procedure of MAFPLL is not straightforward [6]. Recently, a novel EPMAFPLL is proposed for eliminating the problem of offset error under off-nominal frequencies [6]. The EPMAFPLL employed the MAF in the pre-filtering stage of PLL, which reduces the problems related to tuning parameters. In addition, an effective modification is proposed to Phase Detector (PD) for compensating the offset error under off-nominal grid frequency. However, the EPMAFPLL suffers from high frequency overshoot at the time of fault and may violate the assigned grid frequency codes. Furthermore, the EPMAFPLL cannot mitigate harmonics accurately under off-nominal grid frequencies [25]. The PLL design presented in [26] results in higher order compensators, ultimately leading to higher implementation complexity. For example, to mitigate the negative sequence fundamental and 5^{th} harmonic component, the resulting PLL compensator is of 5^{th} order. Consequently, extending for more harmonics will further increase the order and complexity. Furthermore, this PLL design presents high startup transients (13 Hz overshoot in the startup) and high frequency/phase overshoot under faults (for a voltage sag of 40%, 4 Hz frequency overshoot is observed).

For improving the dynamic response of PLL, a multi sequences harmonic decoupling network based PLL is proposed in [27], referred as MSHDCPLL. This PLL extended the decoupling network of existing ddsrfPLL [17] and dαβPLL [8] by including the decoupling of undesired oscillation caused due to the presence of harmonic frequencies. The MSHDCPLL is more computational complex due to significant number of Park's transformations required for frame conversion. Consequently, the DNαβPLL [7] introduces a novel decoupling network implemented in αβ frame for reducing the need of large computational resources. Even after the reduction in complexity by DNαβPLL, the computational resources required by DNαβPLL remain significant in number and challenging for real time implementation. The DNαβPLL is tuned to some specific known grid harmonics and in order to incorporate more harmonics, it requires additional decoupling cells increasing further the computational cost. Furthermore, it is worth mentioning that MSHDCPLL and DNαβPLL cannot work for DC offset and interharmonics if present in the grid voltage. The interharmonics can result in voltage flicker at the PCC due to an intertwined relationship [28], thereby affecting the estimation of phase angle. After July 2014 the problem of interharmonics received considerable attention due to limits imposed for interharmonics in [29]. Thus, there is a need to develop an advanced PLL algorithm fully equipped with interharmonic compensation, for accurate estimation of phase angle.

The harmonic distortion and grid voltage unbalance are not the only problems that a PLL should deal with. It must also provide rejection capability against interharmonics and DC offset. The presence of non-linear power electronic and DC loads together with the grid source impedance is the primary reason for their existence in the grid voltage. None of the PLLs discussed above consider the mitigation of DC offset and interharmonics expect MAF PLLs (which however suffer from slower dynamic response and inaccurate phase estimation under off-nominal frequencies). The DC offset may exists in the grid voltage and results in fundamental frequency oscillations in the PLL estimated phase, amplitude and frequency. The suppression of these oscillations is a challenging task due to their low frequency.

There are several reasons for the presence DC offset in the grid voltage, including grid faults [30], analog to digital conversions [31], measurement device limitations, half wave rectification (generating DC component), geomagnetic phenomena, injection of DC from RES systems, saturation of current transformer [32], sine wave asymmetries because of non-uniform characteristics of semiconductor devices, etc. [33-35]. The removal of these oscillations is therefore necessary in order to eliminate inaccuracies, especially in the case of grid tied converters which will subsequently result in DC current injection. The importance of DC offset rejection capability for PLLs can be realized from international standards IEC61727 [36] and IEEE 1547-2003 [37], where strict limitations are imposed on grid-tied converters with DC current injection no more than 1% and 0.5% of their rated capacity, respectively.

As discussed, DC offset appears as fundamental frequency in the estimated PLL quantities. The use of low-pass filter for attenuation of such low frequency oscillation reduces the system's bandwidth and dynamic response becomes slower. This result in undesirable time delays, especially when fast controller response is required (such as during fault ride through operation of GSC) [15, 38]. In addition to the PLLs addressed above, even the well-known enhanced-PLL (EPLL) causes error at fundamental frequency in the control loop due to the presence of dc offset and it is quite hard to filter. Furthermore, the quadrature signal and estimated PLL quantities of the second-order Generalized Integrator (SOGI) PLL suffer from large oscillations due to the presence of DC offset. A cross-feedback network (CFN) and complex coefficient network (CNN) based PLLs involving multiple use of low pass filters are discussed in [39]

for removing the DC offset. The transformed dq+1 components are passed through LPF for removing oscillations. The resulting filtered components are subsequently subtracted form grid voltage for removing DC offset. The CNFPLL (or CCNPLL), however, has slow dynamic response due to LPF and depending on the selection of cutoff frequency it may lower the harmonic filtering performance. In [40], the DC offset is compensated by quantifying the bandwidth of conventional SRFPLL as a function of DC offset. For mitigating a DC offset of around 2% for example, the PLL bandwidth is set at 20 Hz. For higher magnitudes up to 8%, the bandwidth of SRFPLL is further reduced to 5 Hz. The selection of SRFPLL bandwidth according to this procedure results in slower dynamic response. Two methods based on integration module are discussed in [38] for incorporating the mitigation of DC offset in the conventional three-phase PLL of [41]. The integration module based DC offset mitigation involves complexity in terms of implementation and design procedure. Furthermore, it has slower dynamic response due to inherent requirement to integrate the input grid voltage and requires a longer response time greater by about 30 ms [42]. A Notch filter (NF) PLL presented in [39] mitigates the oscillations caused by DC offset, but results in the slower dynamic response. A recent technique discussed in [42] mitigates the effect of DC offset using a delayed signal subtraction approach. The fact that this approach uses a delayed version of input signal for estimation, results in a constant offset error on the estimated phase. Furthermore, the performance of this PLL is heavily dependent on the hit and trial selection of delay variable t_o, and results in large errors if very low value is selected. The work presented in this paper enables an accurate and faster DC offset compensation due to effective decoupling of fundamental frequency oscillation using a novel mathematic-based decoupling cell cancellation.

The new PLL proposed in this paper can work under unbalanced faults, harmonics, interharmonics, and DC offset in the grid voltage with reduced computational complexity when compared to existing state-of-the-art PLL algorithms. The main novelty of this paper is the introduction of a mathematic-based decoupling cell for effective mitigation of DC offset in the grid voltage and of a more straightforward yet effective modification for enabling the accurate estimation of phase angle under harmonics and/or interharmonics. The new PLL is referred to as Harmonic Interharmonics DC-offset (HIHDO) PLL. In addition to the extra advanced features of interharmonics and DC offset mitigation, the proposed HIHDO-PLL enables an accurate and fast operation with reduced computational complexity and low processing time compared to existing state-of-the-art PLLs. The computational complexity is an important factor when implementing the designed algorithm in limited sized digital microprocessors such as the ones employed by GSC manufacturers [11, 12, 22]. The advanced performance of proposed HIHDO-PLL is verified through simulations and experiments.

Details of the proposed PLL for the mitigation of harmonics/interharmonics and DC offset are discussed in sections II. Section III briefly presents computational complexity analysis of proposed PLL. The design and tuning procedure of proposed PLL is discussed in section IV. Simulation results and experimental verification of the proposed PLL are presented and discussed in section V.

2. Details of Proposed HIHDO-PLL

Most of the listed techniques do not consider the effect of interharmonics and DC offset in the grid voltage while estimating the grid voltage. In this paper, in addition to unbalanced compensation (which is already addressed by many), a novel DC offset compensation cell and harmonic/interharmonic compensation network is proposed for the effective mitigation of DC offset and the undesired effect of harmonics and/or interharmonics on the estimated PLL quantities. The new HIHDO-PLL provides accurate synchronization with lower computational cost compared to existing state-of-the-art PLL algorithms. The HIHDO-PLL is developed by introducing two innovative compensations, one for the mitigation of DC offset in the grid voltage and the second one for compensation against the effect of harmonics and interharmonics.

As the aim of the proposed HIHDO-PLL is to work accurately under unbalanced, DC shifted and harmonically distorted grid conditions, voltage vector analysis under such abnormal conditions is presented. Consequently, grid voltage can be expressed as the sum of the positive sequence (v_{dq}^{+1}), negative sequence (v_{dq}^{-1}), DC offset component (v_{dq}^{0}) as well as all the harmonic/interharmonic components ($\sum \mathrm{v}_{dq}^{h}$), given in (1).

$$\mathrm{v}_{dq} = \mathrm{v}_{dq}^{+1} + \mathrm{v}_{dq}^{-1} + \mathrm{v}_{dq}^{0} + \sum \mathrm{v}_{dq}^{h} \qquad (1)$$

The transformation of three phase v_{abc} to corresponding dq frame is accomplished using (2). When dealing with normal grid conditions, the grid voltage transformation with $n = 1$ results in only positive sequence DC components, that is v_{dq}^{+1}. However, under abnormal grid conditions, the DC terms of positive SRF $\left(\mathrm{v}_{dq}^{n}\big|_{n=+1}\right)$ are accompanied by undesired coupling oscillations because of the unbalance sequence ($n = -1$), DC offset ($n = 0$) and all the existing harmonics/interharmonics. The oscillations on voltage vectors appear because of coupling effect between these vectors rotating at different angular speeds. The coupling of voltage vectors in SRF can be realized by (5).

$$\mathrm{v}_{dq}^{n} = \mathrm{T}_{dq}^{n}\left([T_{\alpha\beta}]v_{abc}\right) \quad (2)$$

where, $[T_{\alpha\beta}] = \frac{2}{3}\begin{bmatrix}\cos(\theta) & \cos(\theta-120°) & \cos(\theta+120°)\\ \sin(\theta) & -\sin(\theta-120°) & -\sin(\theta+120°)\end{bmatrix}$ (3)

$$\mathrm{T}_{dq}^{n} = \begin{bmatrix}\cos(nwt) & \sin(nwt)\\ -\sin(nwt) & \cos(nwt)\end{bmatrix} \qquad (4)$$

$$\mathrm{v}_{dq}^{n} = \underbrace{V^{n}\begin{bmatrix}\cos(\theta_n)\\ \sin(\theta_n)\end{bmatrix}}_{DC\ Term} + \underbrace{\sum_{m\neq n}\left\{V^{m}\left[\mathrm{T}_{dq}^{n-m}\right]\begin{bmatrix}\cos(\theta_m)\\ \sin(\theta_m)\end{bmatrix}\right\}}_{Oscillation\ Term} \quad (5)$$

These oscillations caused under abnormal situation are consequently transferred to synchronization signals causing serious problems in control of GSC. Therefore, such oscillations must be removed by the development of appropriate control algorithm.

2.1. DC offset Compensation Cell (DOCC)

In this modification, the DC offset appearing as fundamental frequency oscillation on the other rotating

vectors is effectively decoupled by proposing a mathematic-cancellation Decoupling Network (DN) incorporated with a DC offset compensation cell (DOCC). The structure of decoupling network with DOCC is shown in Fig. 1. This modification concerns the DC offset without considering the harmonics/interharmonics (that is, $v_{dq}^{h} = 0$). The multiple use of (5) for $n = +1, -1$, and 0 results in voltage vector of containing speeds corresponding to each reference frame, that is, positive sequence, negative sequence and DC component, as shown in (6). An important thing to notice in (6) is that the same amplitude of DC term of n^{th} rotating vector also appears as the magnitude of coupling oscillations. This serves as a way to decouple the undesired oscillations and thereby enable the oscillation free phase estimation.

$$\begin{bmatrix} v_{dq}^{+1} \\ v_{dq}^{-1} \\ v_{dq}^{0} \end{bmatrix} = \underbrace{\begin{bmatrix} V_{dq}^{+1} \\ V_{dq}^{-1} \\ V_{dq}^{0} \end{bmatrix}}_{DC\ terms} + \underbrace{\begin{bmatrix} [0] & T_{dq}^{+1-(-1)} & T_{dq}^{+1-(0)} \\ T_{dq}^{-1-(+1)} & [0] & T_{dq}^{-1-(0)} \\ T_{dq}^{0-(+1)} & T_{dq}^{0-(-1)} & [0] \end{bmatrix} \begin{bmatrix} V_{dq}^{+1} \\ V_{dq}^{-1} \\ V_{dq}^{0} \end{bmatrix}}_{Oscillation\ part} \quad (6)$$

The unknown oscillation free DC terms (V_{dq}^{n}) are calculated by shifting the oscillation part of (6) to the left side and subtracting it from the known voltage vectors (v_{dq}^{n}), as shown in (7). This estimation, however, is carried out by replacing the unknown vectors (V_{dq}^{n}) of the left hand side of (7) with the estimated vector (V_{dq}^{*n}). Furthermore, the unknown vector of the right hand side of equation (7) is replaced with the filter estimated vector ($\bar{V}_{dq}^{*n}$). The decoupled estimated vectors in (8) lead to the development of a new decoupling network equipped with DOCC as shown in Fig. 1. The main novelty of the new DN is the addition of the extra DOCC which emerges because of the last row of (8).

$$\begin{bmatrix} V_{dq}^{+1} \\ V_{dq}^{-1} \\ V_{dq}^{0} \end{bmatrix} = \left(\begin{bmatrix} v_{dq}^{+1} \\ v_{dq}^{-1} \\ v_{dq}^{0} \end{bmatrix} - \begin{bmatrix} [0] & T_{dq}^{+1-(-1)} & T_{dq}^{+1-(0)} \\ T_{dq}^{-1-(+1)} & [0] & T_{dq}^{-1-(0)} \\ T_{dq}^{0-(+1)} & T_{dq}^{0-(-1)} & [0] \end{bmatrix} \begin{bmatrix} V_{dq}^{+1} \\ V_{dq}^{-1} \\ V_{dq}^{0} \end{bmatrix} \right) \quad (7)$$

$$\begin{bmatrix} V_{dq}^{*+1} \\ V_{dq}^{*-1} \\ V_{dq}^{*0} \end{bmatrix} = \left(\begin{bmatrix} v_{dq}^{+1} \\ v_{dq}^{-1} \\ v_{dq}^{0} \end{bmatrix} - \begin{bmatrix} [0] & T_{dq}^{+1-(-1)} & T_{dq}^{+1-(0)} \\ T_{dq}^{-1-(+1)} & [0] & T_{dq}^{-1-(0)} \\ T_{dq}^{0-(+1)} & T_{dq}^{0-(-1)} & [0] \end{bmatrix} \begin{bmatrix} \bar{V}_{dq}^{*+1} \\ \bar{V}_{dq}^{*-1} \\ \bar{V}_{dq}^{*0} \end{bmatrix} \right) \quad (8)$$

The generation of filtered estimated vector ($\bar{V}_{dq}^{*n}$) for the proper operation of (8) requires a low pass filter (LPF), given in (9). The LPF is used to remove any other residual

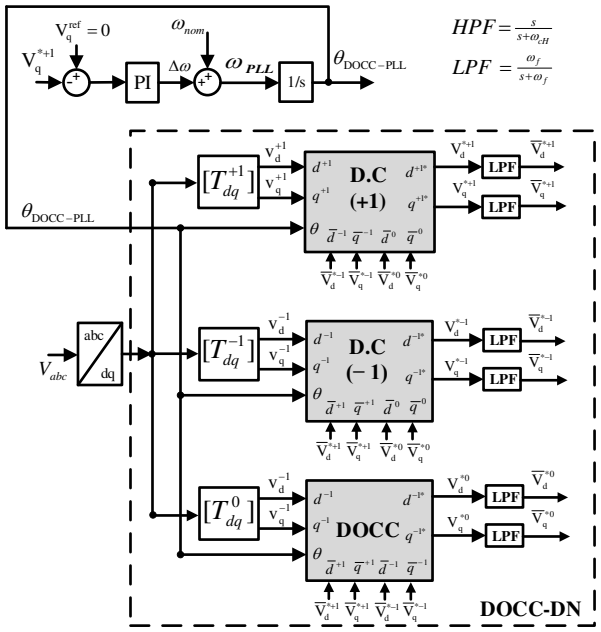


Fig. 1: The block diagram of DOCC-DN based DOCC-PLL

oscillations in estimated vector (V_{dq}^{*n}) and allows the proper operation of cross-feedback terms.

$$\bar{V}_{dq}^{*n} = [F(s)]V_{dq}^{*n} \quad (9)$$

$$where, \quad [F(s)] = LPF = \frac{\omega_f}{s+\omega_f}[I] \ and \ [0] = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \quad (10)$$

In generic form equation (9) can be expressed by:

$$V_{dq}^{*n} = v_{dq}^{n} - \sum_{m \neq n} [T_{dq}^{(n-m)}]\bar{V}_{dq}^{*m} \quad (11)$$

After the vectors are decoupled, the positive sequence V_{dq}^{*+1}(not affected by filter) is transferred to phase detection algorithm based on *dqPLL*. The resulting DOCC-PLL estimates the phase angle accurately under unbalanced grid faults and DC offset in grid voltage. The overall structure of DOCC-PLL is shown in Fig. 1.

2.1.1 Theoretical Response of DOCCPLL: The theoretical analysis of proposed new DOCC based decoupling network is developed by calculating the transfer function $(V_{\alpha\beta}^{+1*}/v_{\alpha\beta})$, where $v_{\alpha\beta} = [T_{\alpha\beta}]v_{abc}$ is the stationary frame voltage (containing DC offset, fundamental positive and negative components) and $V_{\alpha\beta}^{+1*}$ is the pure fundamental positive sequence component. The reason for selecting $\alpha\beta$ is to clearly analyze the response of DOCC for each frequency component, that is, $+f, 0, -f$. For obtaining the transfer function in $\alpha\beta$ frame, (11) is mathematically manipulated by applying space vector transformations to acquire its equivalent $\alpha\beta$ version. When both sides of equation (11) are multiplied with $[T_{dq}^{-n}]$, equation (11) can be re-written as:

$$\left[\mathrm{T}_{dq}^{-n}\right]\mathrm{V}_{dq}^{*n} = \left[\mathrm{T}_{dq}^{-n}\right]\left(\mathrm{v}_{dq}^{n} - \sum_{m\neq n}\left[T_{dq}^{(n-m)}\right]\bar{\mathrm{V}}_{dq}^{*m}\right) \quad (12)$$

Equation (12) can further be modified by using the transformation $\mathrm{V}_{\alpha\beta}^{*n} = \mathrm{T}_{dq}^{-n}\,\mathrm{V}_{dq}^{*n}$, shown in (13)

$$\mathrm{V}_{\alpha\beta}^{*n} = \mathrm{v}_{\alpha\beta} - \left[\mathrm{T}_{dq}^{-n}\right]\cdot\sum_{m\neq n}\left[T_{dq}^{(n-m)}\right]\bar{\mathrm{V}}_{dq}^{*m} \quad (13)$$

The non-filtered version (V_{dq}^{*m}) of filtered estimated vector of ($\bar{\mathrm{V}}_{dq}^{*m}$), given by according to $\bar{\mathrm{V}}_{dq}^{*m} = [F(s)]\mathrm{V}_{dq}^{*m}$, can be substituted in (13), and re-written as:

$$\mathrm{V}_{\alpha\beta}^{*n} = \mathrm{v}_{\alpha\beta} - \left[\mathrm{T}_{dq}^{-n}\right]\cdot\sum_{m\neq n}\left[T_{dq}^{(n-m)}\right][F(s)]\mathrm{V}_{dq}^{*m} \quad (14)$$

The estimated vectors of m-SRF can also be transformed back to αβ-frame according to $\mathrm{V}_{dq}^{*m} = \left[\mathrm{T}_{dq}^{m}\right]\mathrm{V}_{\alpha\beta}^{*m}$ and when the two transformation matrices are used, the final αβ-version of DOCC based decoupling network is obtained and given by (15).

$$\mathrm{V}_{\alpha\beta}^{*n} = \mathrm{v}_{\alpha\beta} - \sum_{m\neq n}\left[T_{dq}^{-m}\right][F(s)]\left[\mathrm{T}_{dq}^{m}\right]\mathrm{V}_{\alpha\beta}^{*m} \quad (15)$$

The transfer function of proposed DOCC-PLL can be found by analyzing (15) in detail. Thus, (15) can be written for $n = +1$ in terms of $m = -1$ and 0, as shown in (16).

$$\mathrm{V}_{\alpha\beta}^{*+1} = \mathrm{v}_{\alpha\beta} - \sum_{m\neq 1}\left[T_{dq}^{-m}\right][F(s)]\left[\mathrm{T}_{dq}^{m}\right]\mathrm{V}_{\alpha\beta}^{*m}$$
$$\Leftrightarrow \mathrm{V}_{\alpha\beta}^{*+1} = \mathrm{v}_{\alpha\beta} - \begin{pmatrix}\left[T_{dq}^{+1}\right][F(s)]\left[\mathrm{T}_{dq}^{-1}\right]\mathrm{V}_{\alpha\beta}^{*-1} + \\ \left[T_{dq}^{0}\right][F(s)]\left[\mathrm{T}_{dq}^{0}\right]\mathrm{V}_{\alpha\beta}^{*0}\end{pmatrix} \quad (16)$$

For extracting the transfer function of proposed DOCC-DN $\left(\mathrm{V}_{\alpha\beta}^{+1*}/\mathrm{v}_{\alpha\beta}\right)$, there is a need to express (16) only in terms of $\mathrm{V}_{\alpha\beta}^{+1*}$ and $\mathrm{v}_{\alpha\beta}$. Consequently, the voltage vectors $\mathrm{V}_{\alpha\beta}^{*m}$ of (16) are expressed in terms of required vectors $\mathrm{V}_{\alpha\beta}^{+1*}$ and $\mathrm{v}_{\alpha\beta}$ by the recursive use of (15). Hence (16) can be expressed as:

$$\mathrm{V}_{\alpha\beta}^{*+1} = \mathrm{v}_{\alpha\beta} - \begin{pmatrix}\left[T_{dq}^{+1}\right][F(s)]\left[\mathrm{T}_{dq}^{-1}\right]\begin{pmatrix}\mathrm{v}_{\alpha\beta} - \left[T_{dq}^{-1}\right][F(s)]\left[\mathrm{T}_{dq}^{+1}\right]\mathrm{V}_{\alpha\beta}^{*+1} \\ -\left[T_{dq}^{0}\right][F(s)]\left[\mathrm{T}_{dq}^{0}\right]\mathrm{V}_{\alpha\beta}^{*0}\end{pmatrix} \\ +\left[T_{dq}^{0}\right][F(s)]\left[\mathrm{T}_{dq}^{0}\right]\begin{pmatrix}\mathrm{v}_{\alpha\beta} - \left[T_{dq}^{-1}\right][F(s)]\left[\mathrm{T}_{dq}^{+1}\right]\mathrm{V}_{\alpha\beta}^{*+1} \\ -\left[T_{dq}^{+1}\right][F(s)]\left[\mathrm{T}_{dq}^{-1}\right]\mathrm{V}_{\alpha\beta}^{*-1}\end{pmatrix}\end{pmatrix} \quad (17)$$

The transfer function can only be extracted by expressing all the remaining $\mathrm{V}_{\alpha\beta}^{*m}$ vectors in terms of desired vectors $\mathrm{V}_{\alpha\beta}^{+1*}$ and $\mathrm{v}_{\alpha\beta}$. The process of representing vectors is repeated recursively and it becomes almost impossible to represent (17) in terms of vectors $\mathrm{V}_{\alpha\beta}^{+1*}$ and $\mathrm{v}_{\alpha\beta}$. Hence, the extraction of transfer function is enabled by ignoring the voltage vectors that undergo filtering through $[F(s)]$ for three or more times. The reason for ignoring these multi-time filtered vectors is their slow dynamic response. By analyzing (17) for vectors which are filtered out more than three or more times, the resulting simplified version of (17) is shown in (18).

$$\mathrm{V}_{\alpha\beta}^{*+1} = \mathrm{v}_{\alpha\beta} - \begin{pmatrix}\left[T_{dq}^{+1}\right][F(s)]\left[\mathrm{T}_{dq}^{-1}\right] + \\ \left[T_{dq}^{0}\right][F(s)]\left[\mathrm{T}_{dq}^{0}\right]\end{pmatrix}\left(\mathrm{v}_{\alpha\beta} - \left[T_{dq}^{-1}\right][F(s)]\left[\mathrm{T}_{dq}^{+1}\right]\mathrm{V}_{\alpha\beta}^{*+1}\right) \quad (18)$$

The transfer function corresponding to $\left[T_{dq}^{-k}\right][F(s)]\left[\mathrm{T}_{dq}^{k}\right]$ is derived by converting the Park's transformation matrices in complex-frequency domain by using Euler formula [7, 18]. Where k can be 0, +1, or -1, respectively for DC offset, positive or negative sequence. The resulting transfer function for $\left[T_{dq}^{-k}\right][F(s)]\left[\mathrm{T}_{dq}^{k}\right]$ referred as TFT^{k} is shown in (19).

$$TFT^{k} = \left[T_{dq}^{-k}\right][F(s)]\left[\mathrm{T}_{dq}^{k}\right] = \frac{\omega_f}{s+(\omega_f - j\cdot k\cdot\omega)} \quad (19)$$

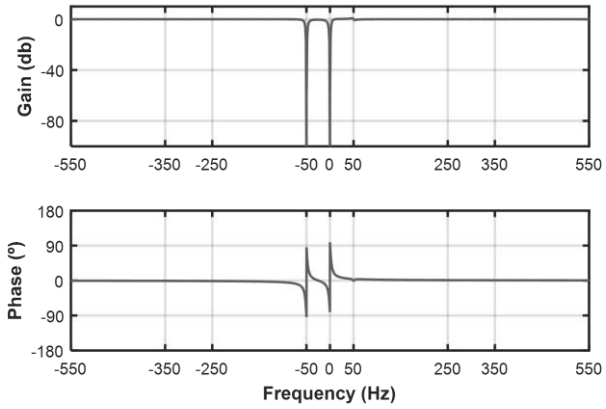
where, $\omega = 2\pi 50$ rad/s is grid nominal frequency and ω_f is the cutoff frequency of LPF.
Consequently, (18) can be re-written using (19),

$$\mathrm{V}_{\alpha\beta}^{*+1} = \mathrm{v}_{\alpha\beta} - \begin{pmatrix}TFT^{-1} + \\ TFT^{0}\end{pmatrix}\left(\mathrm{v}_{\alpha\beta} - TFT^{+1}\,\mathrm{V}_{\alpha\beta}^{*+1}\right) \quad (20)$$

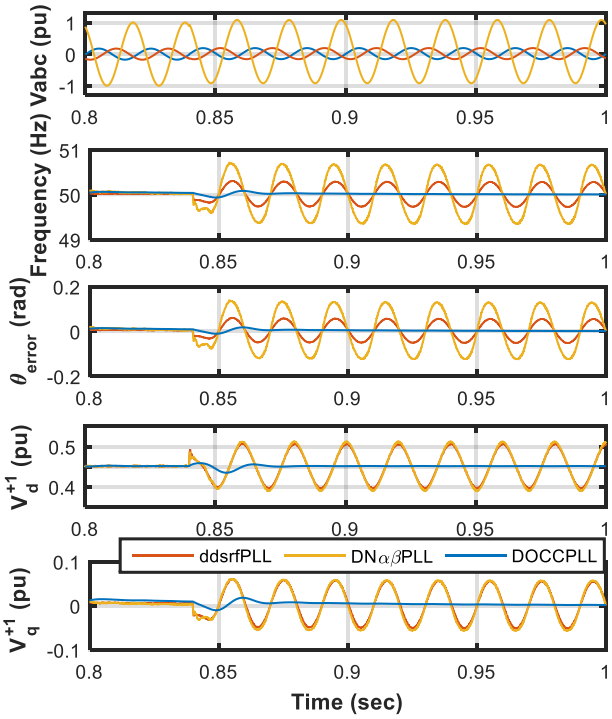
Finally, the transfer function for proposed DOCC-DN is given in (21).

$$H_{DOCC} = \frac{\mathrm{V}_{\alpha\beta}^{*+1}}{\mathrm{v}_{\alpha\beta}} = \frac{1 - [TFT^{-1} + TFT^{0}]}{1 - [TFT^{-1} + TFT^{0}]TFT^{+1}} \quad (21)$$

The transfer function in (21) is a cornerstone for investigating the response of proposed DOCC-DN and the selection of appropriate design parameter ω_f. It is obvious from the Bode plot of Fig. 2 (a), that the DOCC-DN completely blocks the negative sequence component and DC offset by providing negative gain. On the other hand, the positive sequence component is passed accurately with unity gain and zero phase shift without affecting the dynamic response. Therefore, the proposed DOCC-DN provides efficient estimation of fundamental positive sequence, while blocking the undesired negative sequence and DC offset, without compromising the dynamics of estimation. Further investigation of design parameter ω_f according to (21) shows that selection of ω_f is a tradeoff between the speed of dynamic response and estimation accuracy. The analysis shows that the value of $\omega_f = \omega/\sqrt{2}$ is optimal for LPF of fundamental positive and negative sequence decoupling cells, whereas for LPF of DC offset compensation cell, $\omega_f = \omega/4.5$ results in accurate response. The even lower cutoff frequency for DC offset compensation cell makes sense because the frequency of oscillations on dq^{+1} frame produced by DC offset is very small and equal to fundamental grid frequency ω. However, as discussed earlier, the DOCC-DN based PLL cannot mitigate the effect of harmonics and interharmonics, as can be seen from Fig. 2 (a), where harmonics/interharmonics are passed with unity gain and zero phase shift.



(a)



(b)

Fig. 2: (a) Bode diagram of proposed DOCC-DN (b) Simulation results comparing the DC offset mitigation of proposed DOCCPLL.

The DOCC-PLL enables accurate phase estimation with a faster dynamic response as compared to the existing state-of-the-art PLLs. A sample simulation is presented in Fig. 2 (b) for verifying the performance of DOCCPLL under unbalance and DC offset. The initial input voltage of PLL is unbalanced to which all the three PLLs respond accurately. However, at t=0.84 sec a DC offset with a magnitude of 0.08 pu is superimposed on the unbalanced grid voltage. The DOCCPLL is responding accurately with almost no error, whereas the estimated quantities of ddsrfPLL and DNαβPLL suffer from fundamental frequency oscillatory error. The peak-peak value of frequency error ddsrfPLL and DNαβPLL is about 0.60 Hz and 1.4 Hz, respectively.

2.2. Harmonic/Interharmonic Compensation Network (HCN)

The DOCC-PLL cannot work for grid voltage harmonics and interharmonics, hence the angle estimation may deviate from any grid codes imposed. A possible way is to extend the existing ddsrfPLL and DSOGIPLL for harmonics and inter-harmonics, as long as the frequencies of harmonics/interharmonics to be compensated are known. The extension of DSOGI and DDSRF for interharmonics is practically not possible because the exact interharmonics frequencies are not know and also there exists infinite number of interharmonics between two integer harmonics. By extending DDSRF for some arbitrary number of selected harmonics/interharmonics the complexity will be too high and also the performance capability for other existing uncompensated/unselected harmonics/interharmonics will be poor. A possible extension of ddsrfPLL for some low order harmonics is done by [27], but the resulting PLL has higher complexity and it requires prior knowledge of which harmonic to compensate. It is worth mentioning that the harmonic compensation proposed in this paper is able to compensate any harmonic and/or inter-harmonics present in the grid. Prior knowledge of what harmonics/interharmonics are present in the gird voltage is not needed for the proposed case and all the harmonics are eliminated with lower computational complexity. The proposed technique distinctively differentiates in this respect and is also superior in performance to any other PLL investigated.

The HCN is a more straightforward yet effective solution for the mitigation of undesired oscillations appearing in the V_{dq}^{*+1} signal because of harmonics and interharmonics. The combined version of DOCC and HCN is referred as HIHDO-DN. The DOCC-DN effectively estimates the positive sequence vector V_{dq}^{*+1} by decoupling the oscillations caused by negative sequence and DC offset. Consequently, the V_{dq}^{*+1} voltage vectors contain oscillations only because of the presence of harmonics and interharmonics. These oscillations need to be removed in order to obtain pure positive sequence fundamental component. The HCN extracts the oscillation free $V_{dq}^{*+1\prime}$ voltage vector in two steps. The V_{dq}^{*+1} resulting from DOCC-DN is first passed through a high pass filter (HPF), allows through all high frequencies oscillations while blocking the DC terms of positive SRF $\left(V_{dq}^{n}\big|_{n=+1}\right)$. The output of HPF is then subtracted from the voltage vector V_{dq}^{*+1} (which contained the DC terms of positive SRF and also the oscillations because of harmonics). The high frequency oscillations extracted by HPF are effectively decoupled from the voltage vector V_{dq}^{*+1} and the oscillation free positive sequence voltage vector $V_{dq}^{*+1\prime}$ is estimated. The estimated voltage vector $V_{dq}^{*+1\prime}$ is then transferred to dqPLL for the extraction of grid voltage phase angle. The resulting PLL is called HIHDO-PLL and is shown in Fig. 3. Thus, the proposed HIHDO-PLL is able to extract the phase angle of positive sequence of grid voltage accurately under unbalance grid faults, presence of DC offset, harmonics and interharmonics in the grid voltage. Hence, HIHDO-PLL is the most suitable and complete PLL for the accurate synchronization of grid connected RES.

2.2.1 Theoretical Response of HIHDO-PLL: The HIHDO-DN is theoretically analyzed by deriving its transfer function. The HIHDO-DN is basically the combination of DOCC-DN and HCN. Hence, the transfer function of HCN is first calculated and is then multiplied with (21) to extract the overall transfer function $\left(V_{dq}^{*+1\prime}/V_{dq}^{*+1}\right)$. The transfer function for the HPF of HCN is given by (22).

$$HPF = \frac{s}{s + \omega_{cH}} \quad (22)$$

where, ω_{cH} is the cutoff frequency for high pass filter and is the main design parameter for the accurate operation of proposed HIHDO-DN.

The transfer function F_{HCN} of HCN as whole is given by (23), which however is in dq-reference frame. In order to get the equivalent of HCN transfer function in *αβ-frame*, (21) is applied by considering filter transfer function F_{HCN} of (23) with $k = +1$ and resulting αβ version of transfer function is shown in (24). The transfer function of (24) is obtained by transforming $V_{\alpha\beta}^{*+1}$ (which is the output of DOCC-DN in αβ-frame) to V_{dq}^{*+1} by utilizing $\left[T_{dq}^{+1}\right]V_{\alpha\beta}^{*+1}$ and is then passed through F_{HCN}, that is, $\underbrace{F_{HCN}\left[T_{dq}^{+1}\right]V_{\alpha\beta}^{*+1}}_{V_{dq}^{*+1\prime}}$. Finally the filtered output $V_{dq}^{*+1\prime}$ is re-transformed back to αβ frame for the purpose of analysis, that is $\underbrace{\left[T_{dq}^{-1}\right]F_{HCN}\left[T_{dq}^{+1}\right]V_{\alpha\beta}^{*+1}}_{V_{\alpha\beta}^{*+1\prime}}$.

$$F_{HCN} = \left(V_{dq}^{*+1\prime}/V_{dq}^{*+1}\right) = 1 - \frac{s}{s + \omega_{cH}} \quad (23)$$

$$T_{HCN} = \left(V_{\alpha\beta}^{*+1\prime}/V_{\alpha\beta}^{*+1}\right) = 1 - \frac{s - j\cdot\omega}{s + (\omega_{cH} - j\cdot\omega)} \quad (24)$$

The overall transfer function $\left(V_{\alpha\beta}^{*+1\prime}/v_{\alpha\beta}\right)$ of HIHDO-DN is calculated by multiplying the transfer function of HCN with (21) and is given by (25).

$$H_{HIHDO} = \frac{V_{\alpha\beta}^{*+1\prime}}{v_{\alpha\beta}} = T_{HCN}\cdot H_{DOCC}$$
$$\Leftrightarrow H_{HIHDO} = \left(1 - \frac{s - j\cdot\omega}{s + (\omega_{cH} - j\cdot\omega)}\right)\left(\frac{1 - [TFT^{-1} + TFT^{0}]}{1 - [TFT^{-1} + TFT^{0}]TFT^{+1}}\right) \quad (25)$$

The Bode diagram of proposed HIHDO-DN is presented in Fig. 4 (a). The result verifies the accurate and improved performance of proposed HIHDO-DN that can extract the positive sequence fundamental component without compromising the dynamic response, since the gain in dB and phase shift in degree at desired 50Hz frequency is respectively unity and zero. However, the negative sequence fundamental component (-50Hz), the DC offset (0Hz), and all other harmonics and interharmonics are eliminated efficiently. A performance capability comparison of DOCC-DN, HIHDO-DN and DNαβ is presented in Fig. 4 (b). The inaccurate estimation of DOCC-DN under harmonics is obvious due to its unity gain and zero phase. However, as opposed to DNαβ, DOCC-DN can compensate for DC offset.

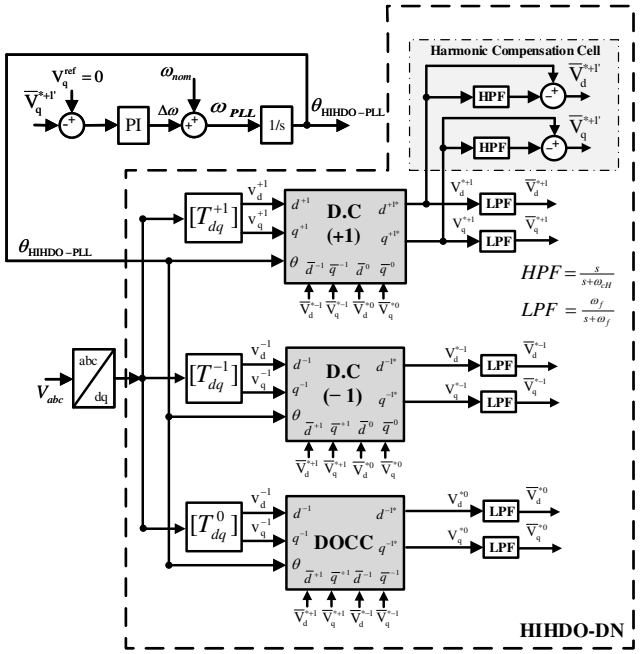


Fig. 3: Block diagram of proposed HIHDO-PLL.

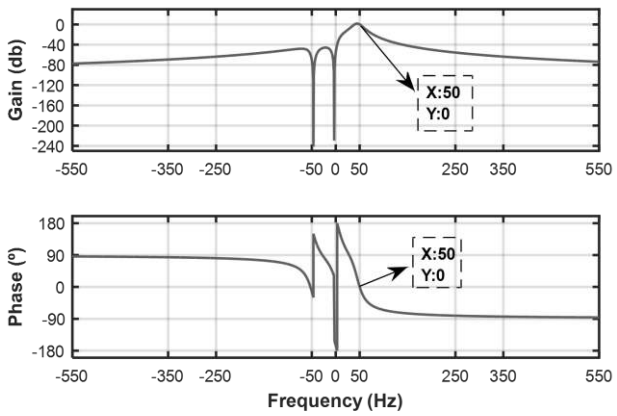
The proposed HIHDO-DN can work for DC offset, harmonics and interharmonics of any order as compared to DNαβ. The DNαβ can compensate only for specific low-order harmonics and in addition it allows interharmonics with unity gain. The above mentioned characteristics constitute the proposed HIHDO-DN superior in terms of advanced features and performance.

The step response of proposed HIHDO-DN for estimating the input voltage is shown Fig. 4 (c). In Fig. 4 (c) subplot 1, the positive sequence of voltage is estimated when the decoupling network is supplied with a step input of unity positive sequence. The proposed HIHDO-DN enables very fast and accurate estimation of the positive sequence component within a response time of 18 ms. The accurate estimation of positive sequence under negative sequence with a step amplitude of 0.5 pu and 5.2th interharmonic with a step input of 0.3 pu is shown in Fig. 4 (c) subplot 2 and subplot 3, respectively. It is obvious from the results that HIHDO-DN performs fast and accurate decoupling of negative sequence and interharmonic component from that of positive sequence and results in oscillation free estimation of positive sequence voltage.

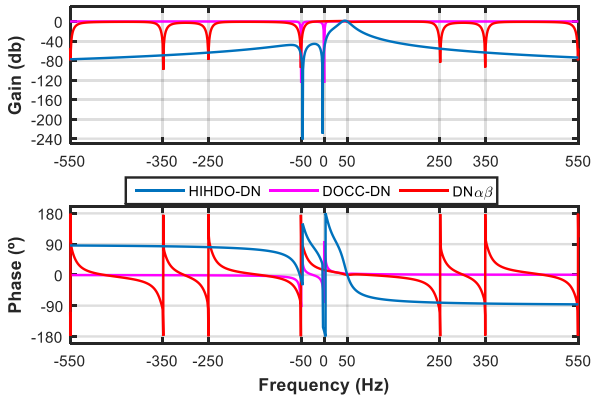
The theoretical analysis of proposed PLL validates that the new HIHDO-PLL is able to perform accurately under unbalance, harmonics, interharmonics and DC shifted gird conditions, without compromising the dynamic response of phase angle estimation. The outstanding performance will be further verified through simulations and experiments in the subsequent sections.

3. Computational Complexity Analysis

The computational complexity of proposed HIHDO-DN is lower compared to existing techniques in the literature for mitigating the unbalances and harmonics together. The computational complexity analysis together with the performance capabilities of proposed PLL compared to existing PLL algorithms is presented in Table 1. The proposed HIHDO-PLL is 377% less computational complex than the DNαβPLL in spite the fact that it is equipped with



(a)



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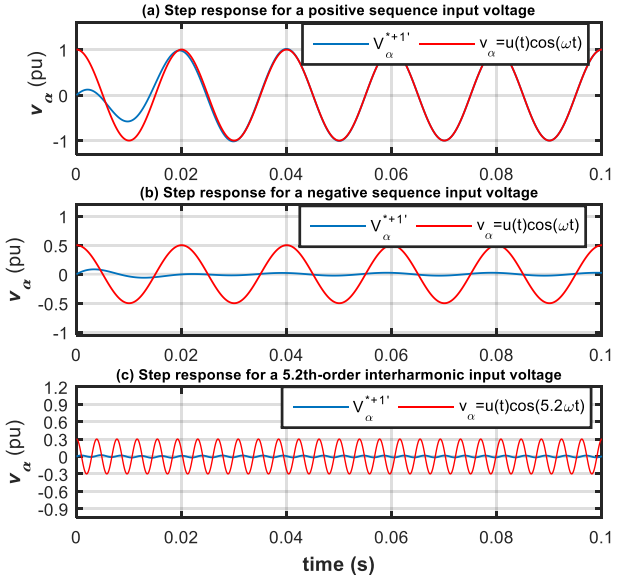


(c)

Fig. 4: (a) Bode diagram of proposed HIHDO-DN (b) Bode diagram comparison for HIHDO-DN, DOCC-DN and DNαβ (c) The time domain response of HIHDO-DN for positive sequence, negative sequence, and Interharmonic (5.2^{th}) step input.

additional advanced features. Furthermore, the performance of HIHDO-PLL is compared against ten existing state-of-the-art PLLs. This comparison is summarized in Table 2. The proposed PLL shows accurate performance under all the abnormal grid conditions investigated without the processing time being compromised.

4. Tuning and Design Procedure of Proposed HIHDO-PLL

The optimal tuning of proposed HIHDO-PLL is very critical for the fast and accurate estimation of phase angle, and is developed using the small signal linearized model of PLL [8, 18, 43]. The small signal model consists of PI controller $\left(k_p + \frac{k_i}{s}\right)$ and an integrator. The resulting closed loop transfer function of PLL is presented in (26).

$$G(s) = \frac{\theta_{HIHDO-PLL}}{\theta_{grid}} = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} = \frac{k_p s + k_i}{s^2 + \underbrace{k_p}_{2\xi\omega_n}\, s + \underbrace{k_i}_{\omega_n^2}} \qquad (26)$$

The $\theta_{HIHDO-PLL}$ corresponds to the estimated PLL angle and θ_{grid} is the actual phase angle. The transfer function of proposed HIHDO-PLL in (26) is of second order and can be easily tuned according to desired settling time T_s and damping coefficient ξ [18, 44]. For optimally damped response of PLL, the selected value of $\xi = 1/\sqrt{2}$. The resulting tuning parameters k_p and k_i in terms of desired settling time T_s, is given by (27) and valid for per unit grid voltage. The stability of tuned PLL verified through Routh Hurwitz (RH) criterion applied to denominator of (26). The RH condition for stability of (26) is $k_p > 0$.

$$k_p = \frac{9.2}{T_s} \text{ and } k_i = (4.6/\xi T_s)^2 \qquad (27)$$

The values of tuning parameters used in this work are $k_p = 32.7$ and $k_i = 66.67$. The response of PLL can be made faster or slower by substituting the appropriate value of T_s in (27).

The cutoff frequency of HPF (ω_{cH}) in HCN is an important factor and needs further investigation. The selection of appropriate value of ω_{cH} is very important for fast and accurate estimation of positive sequence voltage component under harmonics and interharmonics. An investigation is carried out by measuring the Integral Absolute Error (IAE) for estimated phase error, peak value of oscillations magnitude under harmonic distortion, overshoot in estimated phase error at the time of fault and settling time to observe the dynamic response for different values of ω_{cH}. The harmonic conditions are set to $|V_5| = 5\%$ and $|V_7| = 2.5\%$, and fault type is single phase to ground fault. The results of this investigation are listed in Table 3. The optimal range of ω_{cH} comes out as $2\pi 10 \leq \omega_{cH} \leq 2\pi 22$ (where nominal grid frequency is $2\pi 50$).

5. Results and Discussion

The outstanding performance of HIHDO-PLL is also verified through simulation and experimental results. The novel HIHDO-PLL proves to be beneficial for accurate synchronization of grid connected RES systems.

5.1. Simulation Results

The simulation study is carried out using MATLAB SimPowerSystem. The performance of proposed HIHDO-PLL is compared to ddsrfPLL and DNαβPLL under various

Table 1: Comparison of computational complexity and performance capabilities of HIHDO-PLL, DOCC-PLL, MSHDCPLL, DNαβPLL and DDSRFPLL.

PLL Algorithms	HIHDO-PLL	DOCCPLL	MSHDCPLL	DNαβPLL	DDSRFPLL
Mathematical Operations in each loop	×: 70 +: 19 −: 17 Total:106	×: 66 +: 15 −: 15 Total:96	×: 640 +: 120 −: 280 Total:1040	×: 160 +: 40 −: 200 Total:400	×: 32 +: 8 −: 8 Total:48
Computational Complexity	Low (220%)	Low (200%)	High (2166%)	Medium (833%)	Normal (100%)
Performance Capabilities (accurate estimation under)	1.Unbalance 2.Harmonics 3.Interharmonics 4.DC Offset	1.Unbalance 2.DC Offset	1.Unbalance 2.Harmonics	1.Unbalance 2.Harmonics	1.Unbalance

Note: Each: $[T_{dq}]$ requires 6 Multiplications (×), 1 Addition (+) and 1 Subtraction (−); Each: $[F(s)]$ requires 4 (×), 2 (+)
Each: Decoupling Cell has $2N(n-1)$ subtractions, N^2: $[T_{dq}]$ blocks, and N: $F(s)$ blocks.

Table 2: Response and processing time comparison of ten different PLLs.

PLL Algorithms	Processing Time (ms) (MPR)	Dynamic Response under faults	Accurate Estimation under				
			Unbalanced Voltage	Harmonics	Inter-Harmonics	DC-offset	Off-nominal frequency
dqPLL/αβPLL	3.168	Faster	No	No	No	No	Yes
ddsrfPLL	8.878	Faster	Yes	No	No	No	Yes
dαβPLL	9.694	Faster	Yes	No	No	No	Yes
MAFPLL*°	2.981	Slow	Yes	Yes	Partial	Yes	No
EPMAFPLL*°	4.573	Slow	Yes	Yes	Partial	Yes	Partial
MRF PLL*°	9.100	Slow	Yes	Yes	Partial	Yes	No
MSHDC PLL**	91.04	Faster	Yes	Yes	No	No	Yes
DNαβPLL**	29.41	Faster	Yes	Yes	No	No	Yes
DOCC-PLL	18.20	Fast	Yes	No	No	Yes	Yes
HIHDO-PLL	19.77	Fast	Yes	Yes	Yes	Yes	Yes

*Cannot compensate harmonics/Interharmonics accurately under off-nominal grid frequency and lower attenuation capability for Interharmonics.
°Compensate DC offset only if MAF window length $T_\omega = 0.02\ s$. **Eliminate selected harmonics

Table 3: Selection of appropriate design parameter ω_{cH} for proposed HIHDO-PLL

ω_{cH} (rad/sec)	Peak Value of Phase Oscillations (rad)	IAE for Δθ (rad)	Error $T_{settling}$ (ms)	Estimated Phase Error Overshoot (rad)
$\mathbf{2\cdot\pi\cdot 30}$	0.01016	0.006093	27	0.125
$\mathbf{2\cdot\pi\cdot 27}$	0.009305	0.005743	28	0.123
$\mathbf{2\cdot\pi\cdot 25}$	0.008735	0.0055	27	0.120
$\mathbf{2\cdot\pi\cdot 22}$	0.007567	0.005118	27	0.116
$\mathbf{2\cdot\pi\cdot 20}$	0.007276	0.004848	27	0.113
$\mathbf{2\cdot\pi\cdot 18}$	0.006668	0.004568	27	0.109
$\mathbf{2\cdot\pi\cdot 15}$	0.005706	0.004119	23	0.102
$\mathbf{2\cdot\pi\cdot 13}$	0.005007	0.003792	19	0.095
$\mathbf{2\cdot\pi\cdot 10}$	0.003807	0.003408	20	0.0835
$\mathbf{2\cdot\pi\cdot 8}$	0.002903	0.003223	40	0.0732
$\mathbf{2\cdot\pi\cdot 5}$	0.002466	0.003305	53	0.0539

grid conditions, shown in Fig. 5. It can be verified from results that the HIHDO-PLL is performing accurate under various grid conditions, especially in the case of interharmonics and DC-offset. The various harmonic and fault conditions are listed in Table 4 and all the PLLs are compared for same tuning parameters. Initially, the grid voltage contains harmonics (HC-1). At t=0.64 s the harmonic conditions are changed to HC-2, where -5^{th} and $+7^{th}$ harmonics are injected. In both the cases, the performance of DNαβPLL and HIHDO-PLL is identical. However, at t=0.68 s and t=0.72 s the injection of interharmonics (referred as IHC-1 and IHC-2) are enabled whereby the estimated frequency and phase error response of DNαβPLL suffer from oscillations. In contrast, the HIHDO-PLL performs accurately due to the interharmonics compensation features. The response of PLL is also evaluated under two-phase-to-ground fault (applied at t=0.76s). The DNαβPLL and ddsrfPLL suffer from high phase and frequency overshoot as compared to HIHDO-PLL. At t=0.84 s DC offset occurs, both ddsrfPLL and DNαβPLL are unable to accurately estimate desired phase angle due to 50 Hz oscillations. In contrast, the proposed HIHDO-PLL estimates the phase angle fast and accurately by mitigating the effect of DC offset. The DC offset is mitigated within a response time of 7 ms, which is less than the response time (30 ms) of PLL method discussed in [38].

The performance of HIHDO-PLL is further investigated under a new set of disturbances as shown in Fig. 6 (a). The three PLLs perform equivalently under normal condition, however at t=0.64 s the interharmonics (IHC-2) are injected whereby HIHDO-PLL is responding accurately to this disturbance. At t=0.72 s a two phase to ground fault is applied with IHC-2 still activated. The DNαβPLL and ddsrfPLL suffer from high frequency/phase overshoot and oscillations as opposed to HIHDOPLL. Furthermore, the PLLs are compared under DC-offset together with HC-2 condition and one phase to ground fault, thereby verifying the superior performance of HIHDOPLL. Under phase fault and frequency variation the proposed HIHDO-PLL performs accurately with fast and improved dynamic response.

The new HIHDOPLL is also tested for severe harmonics and interharmonics distortion, as shown in Fig. 6 (b). The response of ddsrfPLL is inaccurate for both harmonics and interharmonics, whereas, DNαβPLL cannot tolerate interharmonics only. HIHDOPLL however presents accurate and robust response to these disturbances and results in accurate estimation of phase angle. The DNαβPLL requires 20 ms to fully mitigate the effect of harmonics (at t= 0.55 sec), whereas the proposed PLL mitigates immediately as the disturbance occurs. The integral absolute error (IAE) for various abnormal grid conditions is summarized in Table 4. The IAE is used to analyze the estimation error of algorithm. The HIHDOPLL has lower IAE value under all the cases of

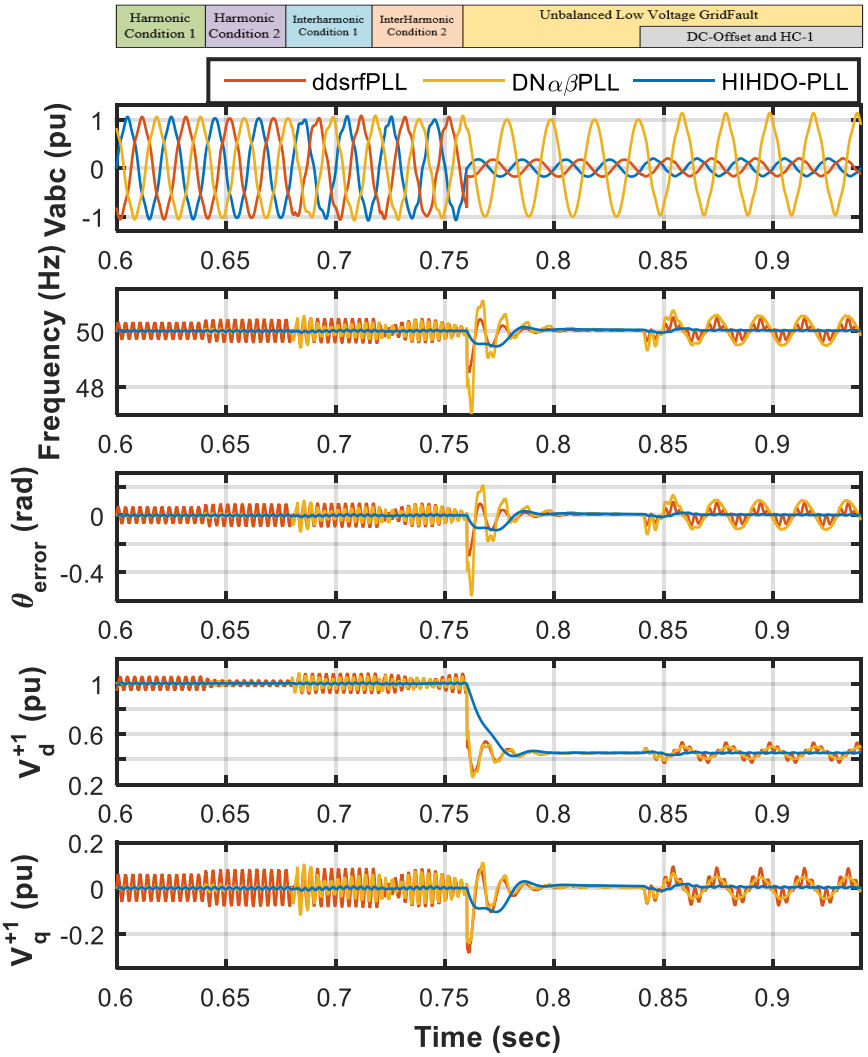


Fig. 5: Simulation results comparison among HIHDO-PLL, ddsrfPLL and DNαβ-PLL responses under various abnormal

grid disturbances, verifying its outstanding performance. A recent EPMAFPLL cannot perform accurately under grid voltage interharmonics, as observed from the high value of IAE for EPMAFPLL. Under IHC-2 condition, IAE of proposed HIHDO-PLL and EPMAFPLL is 0.02966 and 0.09424, respectively. The performance of the proposed PLL was also evaluated for the interharmonics near the fundamental such as positive sequence 1.2th interharmonic but also for negative sequence 1.2th interharmonic. Experimental results were taken for both of these interharmonic cases, Fig. 9, and are discussed in section 5.2 under case study 4. The simulation results shown in Fig. 6 (c) are for the negative sequence 1.2th interharmonic with a magnitude of 8 % injected in to the grid voltage at 0.4 sec. The proposed PLL estimates the phase angle more accurately when compared to the other two PLLs. The ddsrfPLL and DNαβPLL suffer from oscillations in the estimated phase and frequency as they are not immune to interharmonics.

The proposed PLL is further tested under a case with several grid harmonics. The harmonic order and corresponding maximum magnitude limits are obtained from EN 51060 standard, listed in Table 4 as harmonic condition 3 (HC-3). The DNαβPLL if extended for eliminating this set of harmonics requires higher real-time computational burden, that is, it requires 832 mathematical operations (908 % more complexity compared to proposed case). During the first 0.55 s the grid voltage is harmonic free after which, HC-3 is activated, as shown in Fig. 6 (d). The proposed PLL responds accurately to these harmonics without any initial oscillations. However, the DNαβPLL suffers from spikes and oscillations in the start and takes slightly more time to settle. The accurate estimation of proposed PLL under worst case harmonics is validated in this case.

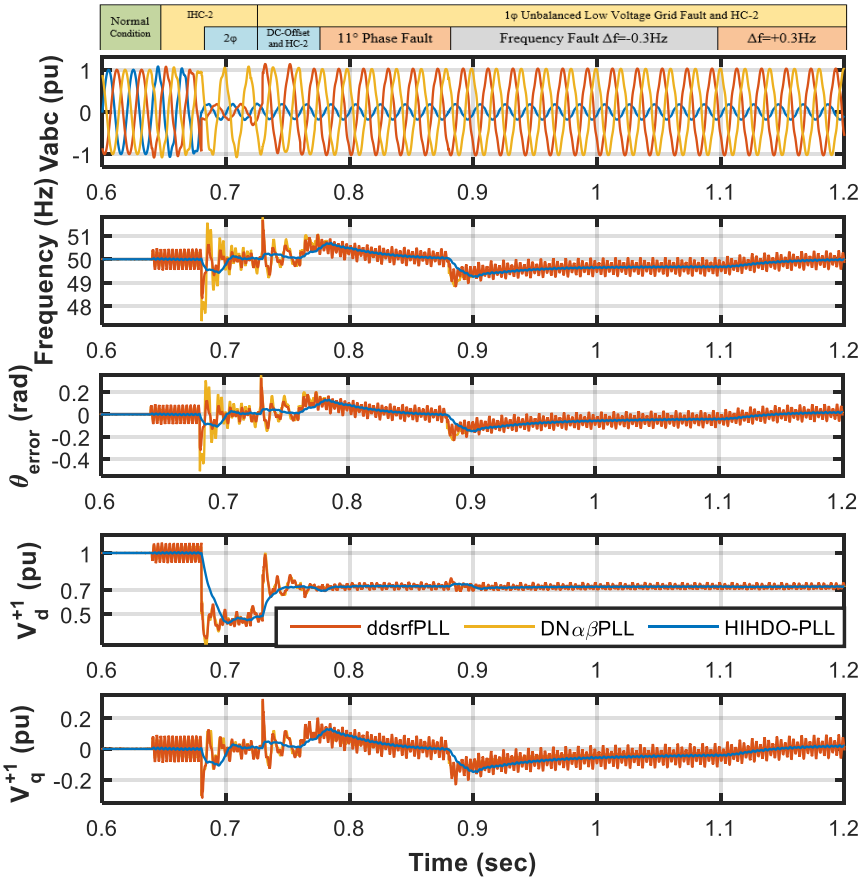
A performance comparison of HIHDO-PLL, ddsrfPLL, DNαβPLL and EPMAFPLL under unbalanced fault is shown in Fig. 7 (a) and is summarized in Table 5. Referring to Fig. 7 (a), the PLLs are initially operated under normal grid conditions, however, at t=0.75 sec a two-phase to ground fault is applied with a phase change of -10° to observe the dynamic response of PLLs. The frequency overshoot for the proposed HIHDO-PLL is lower among all the PLLs, hence it can be used for the synchronization of grid connected RES without violating the grid frequency limits. Furthermore, the frequency settling time for HIHDO-PLL is lower compared to DNαβPLL and EPMAFPLL.

Furthermore, a test case is presented in Fig. 7 (b), where the grid voltage is subjected to a three-phase to ground fault with 99.99 % voltage sag. This allows the proposed PLL performance to be examined under zero grid voltage condition (for instance, in the case of a three-phase to ground fault or blackout). Under such a case, the input to the PLL becomes zero. This means that the resulting q^{+1}-component of the grid voltage will also be zero. As a result, the PI controller's output i.e. $\Delta\omega$, will also be zero. Consequently, the nominal grid frequency ω_{nom} is translated to the estimated phase angle. The proposed PLL and ddsrfPLL perform accurately with fast dynamics, as can be seen from Fig. 7 (b). However, DNαβPLL suffers from large oscillations at the time of the fault and also a constant offset

Table 4: Integral Absolute Error (IAE) comparison of HIHDO-PLL, ddsrfPLL, DNαβ-PLL and EPMAFPLL under various abnormal grid conditions

Grid Operating Conditions		HIHDO-PLL	DDSRFPLL	DNαβPLL
HC-1	IAE Δω	**0.03541**	0.5288	0.05463
	IAE Δθ	**0.001183**	0.01627	0.001785
HC-2	IAE Δω	**0.05318**	0.7952	0.0590
	IAE Δθ	**0.001726**	0.02442	0.00191
IHC-1	IAE Δω	**0.04043**	0.6326	0.245
	IAE Δθ	**0.001336**	0.01945	0.007596
IHC-2	IAE Δω	**0.02966**	0.4644	0.181
	IAE Δθ	**0.001007**	0.0143	0.00564
Fault (2φ)	IAE Δω	**0.05047**	0.7866	0.1542
	IAE Δθ	**0.00189**	0.002843	0.00506
DC Offset and HC-1	IAE Δω	**0.02833**	0.467	1.07
	IAE Δθ	**0.001035**	0.01439	0.03282
HC-1 and 1φ Fault	IAE Δω	**0.07402**	0.4796	0.1633
	IAE Δθ	**0.002499**	0.0148	0.005313

Harmonic Condition 1 (HC-1): $|V_5| = 5.5\%$
Harmonic Condition 2 (HC-2): $|V_5| = 5\%$ and $|V_7| = 2.5\%$
Harmonic Condition 3 (HC-3): $|V_5| = 6\%$, $|V_7| = 5\%$, $|V_{11}| = 3.5\%$, $|V_{13}| = 3\%$, $|V_{17}| = 2\%$, $|V_{19}| = 1.5\%$, $|V_{23}| = 1.5\%$, $|V_{25}| = 1.5\%$
Interharmonic Condition 1: (IHC-1): $|V_{5.28}| = 6\%$
Interharmonic Condition 2: (IHC-2): $|V_{5.28}| = 4.4\%$ and $|V_{7.20}| = 3.5\%$
DC Offset: $|V_{DC}| = 8\%$
Harmonic/Interharmonic/DC Condition (HIDC): $|V_5| = 6\%$, $|V_7| = 5\%$, $|V_{3.2}| = 3\%$, $|V_{4.6}| = 3.5\%$ and $|V_{DC-abc}| = [8\% \quad -6.1\% \quad 3.6\%]$
Fault (2φ): Low Voltage Two Phase to Ground Fault
1φ Fault: Low Voltage Phase to Ground Fault



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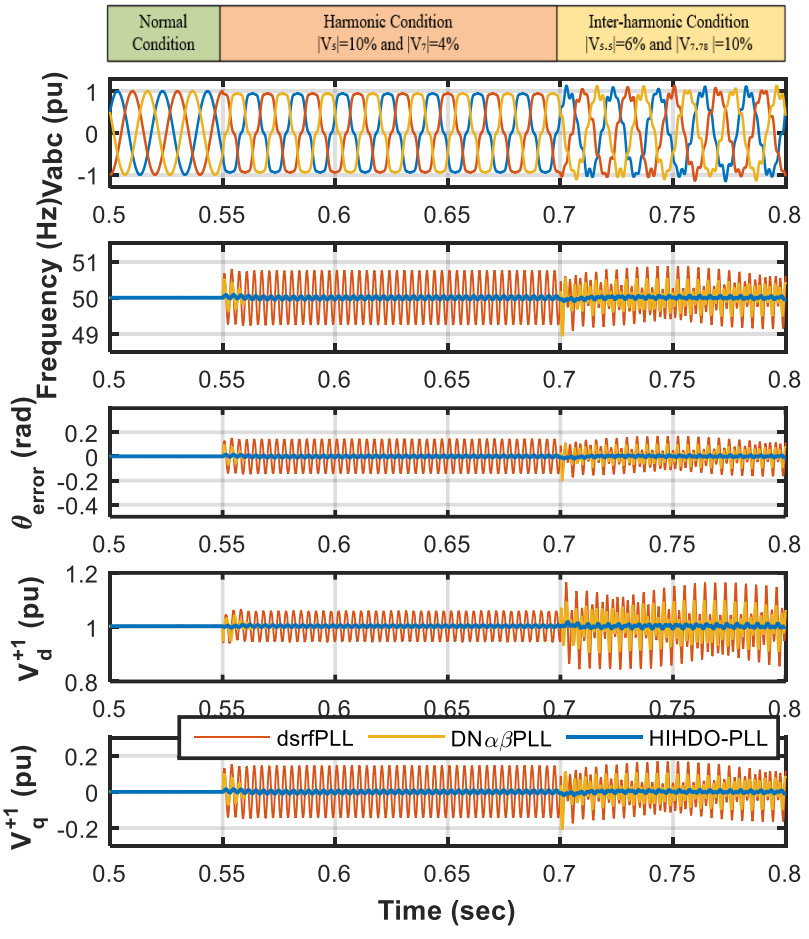

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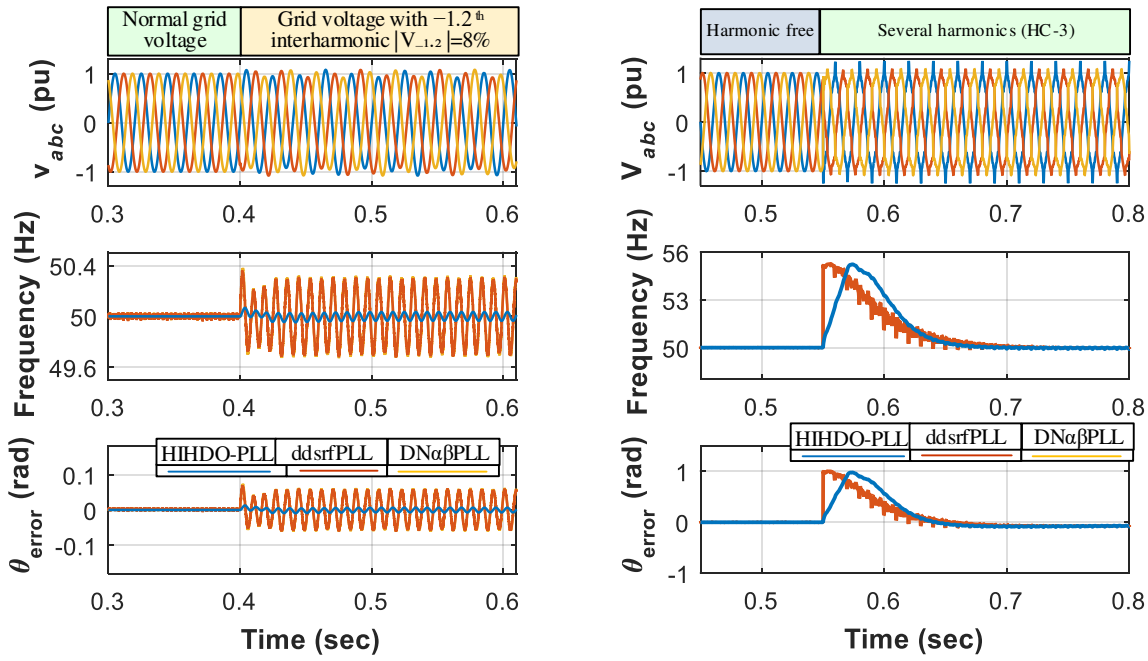

Fig. 6: Simulation results comparison among HIHDO-PLL, ddsrfPLL and DNαβ-PLL responses: (a) under normal and various abnormal grid conditions (b) under severe harmonic/interharmonic conditions (c) under -1.2th interharmonic in the grid voltage, (d) under severe harmonic condition (HC-3).

appears in the estimated phase error. This is due to the presence of αβPLL in the phase detector part of this PLL.

The proposed PLL is also compared to ddsrfPLL and DNαβPLL for a frequency change event under balanced and harmonic free grid conditions (with $\omega_{cH} = 2\pi 20$ rad/s). The grid frequency is varied from 50 Hz to 47 Hz at 0.4 s and then reverted back to 52 Hz at 0.6 s. The corresponding frequency estimation responses of PLLs are shown in Fig. 7 (c). The proposed PLL is observed to respond slightly faster when compared to ddsrfPLL and DNαβPLL (DNαβPLL and ddsrfPLL have same responses) despite the fact that they do not employ HPF. The optimal selection of ω_{cH} according to Table 3 enabled the fast dynamic response of the proposed PLL.

Lastly, the proposed PLL is verified for the frequency variations under the condition when the grid voltage is injected with 5th and 7th harmonics, 3.2th and 4.6th interharmonics and DC offset (HIDC condition listed in Table 4). The grid frequency is varied from 50 Hz to 47 Hz at 0.3 s and is then changed to 52 Hz at 0.6 s, presented in Fig. 7 (d). The ddsrfPLL cannot compensate for harmonics, DC offset and interharmonic, whereas DNαβPLL cannot compensate for DC offset and interharmonic. The proposed PLL accurately mitigates the undesired effects of interharmonics, harmonics and DC offset both under nominal (50 Hz) frequency and off-nominal frequencies (47 Hz and 52 Hz). This validates the effectiveness of proposed PLL for the elimination of interharmonics under off-nominal grid frequencies.

5.2. Experimental Results

The performance of HIHDO-PLL is further verified through experimental results in the laboratory. The HIHDO-PLL algorithm has been designed using a dSPACE-DS1104-DSP board in combination with dSPACE Control Desk and *Matlab/Simulink* Real-Time-Workshop. A California Instrument 2253iX programmable AC source with an isolation transformer is installed for emulating electrical grid. The schematic of experimental setup is presented in Fig. 8 (a). An equivalent setup has been developed in *Matlab* for simulation purposes, before testing proposed PLL practically through experiments. Various experimental case studies are presented to validate the proposed PLL under different working conditions.

5.1.1 *Case Study 1 - Steady state response of HIHDO-PLL:* The working conditions for case study 1 are listed in Table 6 and corresponding result is shown in Fig. 8 (b). It is noted that a very accurate response can be achieved by the proposed HIHDO-PLL with phase error less than 0.01 rad under unbalanced voltage sag, DC offset, harmonic and inter-harmonic distortion.

Table 5: Summary of results presented in Fig. 7 (a).

PLL	Frequency Overshoot (Hz)	Frequency Settling Time (ms)	Phase Error Peak Value (Degree)	Phase Settling Time (ms)
ddsrfPLL	1.42	19.6	14.73	26.5
EPMAFPLL	2.37	39.2	1.158	20.1
DNαβPLL	2.54	43.7	27.20	35.3
HIHDOPLL	0.53	19.6	4.12	20.1

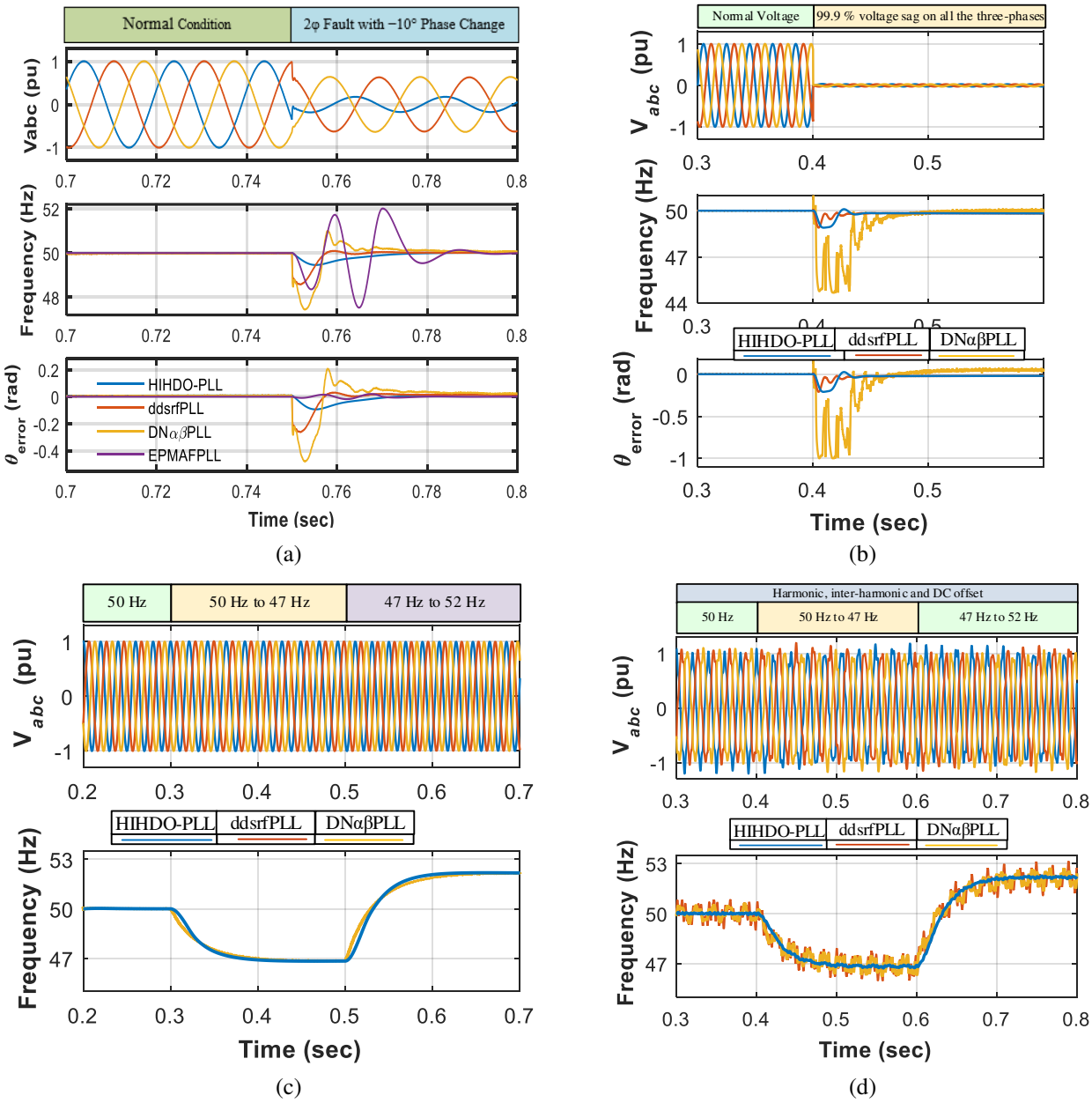

Fig. 7: Simulation results comparison among (a) HIHDO-PLL, ddsrfPLL, DNαβ-PLL and EPMAFPLL responses under unbalanced grid condition (b) HIHDO-PLL, ddsrfPLL, and DNαβ-PLL under loss of grid voltage (c) HIHDO-PLL, ddsrfPLL, and DNαβ-PLL under frequency variation (d) HIHDO-PLL, ddsrfPLL, and DNαβ-PLL under frequency variation and grid voltage harmonic, interharmonic and DC offset grid conditions.

5.1.2 *Case Study 2 – Transient response of HIHDO-PLL vs ddsrfPLL when harmonic/interharmonic distortion occurs:* The second case study observes the transient behavior of proposed HIHDO-PLL in comparison to ddsrf-PLL. In this case, the voltage conditions are balanced and DC offset is removed. However, at $t = 7.67\ s$, harmonic distortion occurs on the grid voltage (with a 10% amplitude on 5th harmonic and a 5% amplitude 7.2th inter-harmonic). The results for acquiring phase angle under these operating conditions are shown in Fig. 8 (c). It is noted that HIHDO-PLL can achieve fast and accurate estimation of the phase angle with a θ_{error} < 0.01 rad. In contrast, ddsrf-PLL present an error of 0.16 rad. The corresponding error in V_{dq}^{+1} and estimated frequency is clearly depicting the outstanding performance of proposed HIHDO-PLL.

Case Study 3 – Transient response of HIHDO-PLL vs ddsrfPLL under DC offset and unbalanced voltage sag: The third case study analyzes the behavior of HIHDOPLL under DC offset, harmonic/interharmonic distortion and unbalanced grid fault. Initially, all the three phases of grid voltage are balanced. The initial values of 5th harmonic and 7.2th inter-harmonic are respectively set to 10% and 5% of fundamental voltage component. The DC-offset is initially set to a value of $+24.6\ V_{dc}$. However, an unbalanced voltage drop event occur at $t = 0.278\ s$, where the voltage at phase-a drops by 50%. Fig. 8 (d) shows the transient response of the both HIHDOPLL and ddsrfPLL. The proposed HIHDO-PLL estimates the grid angle accurately with θ_{error} < 0.01 and also the estimated frequency is close to 50 Hz (actual grid frequency). However, the ddsrf-PLL results in inaccurate

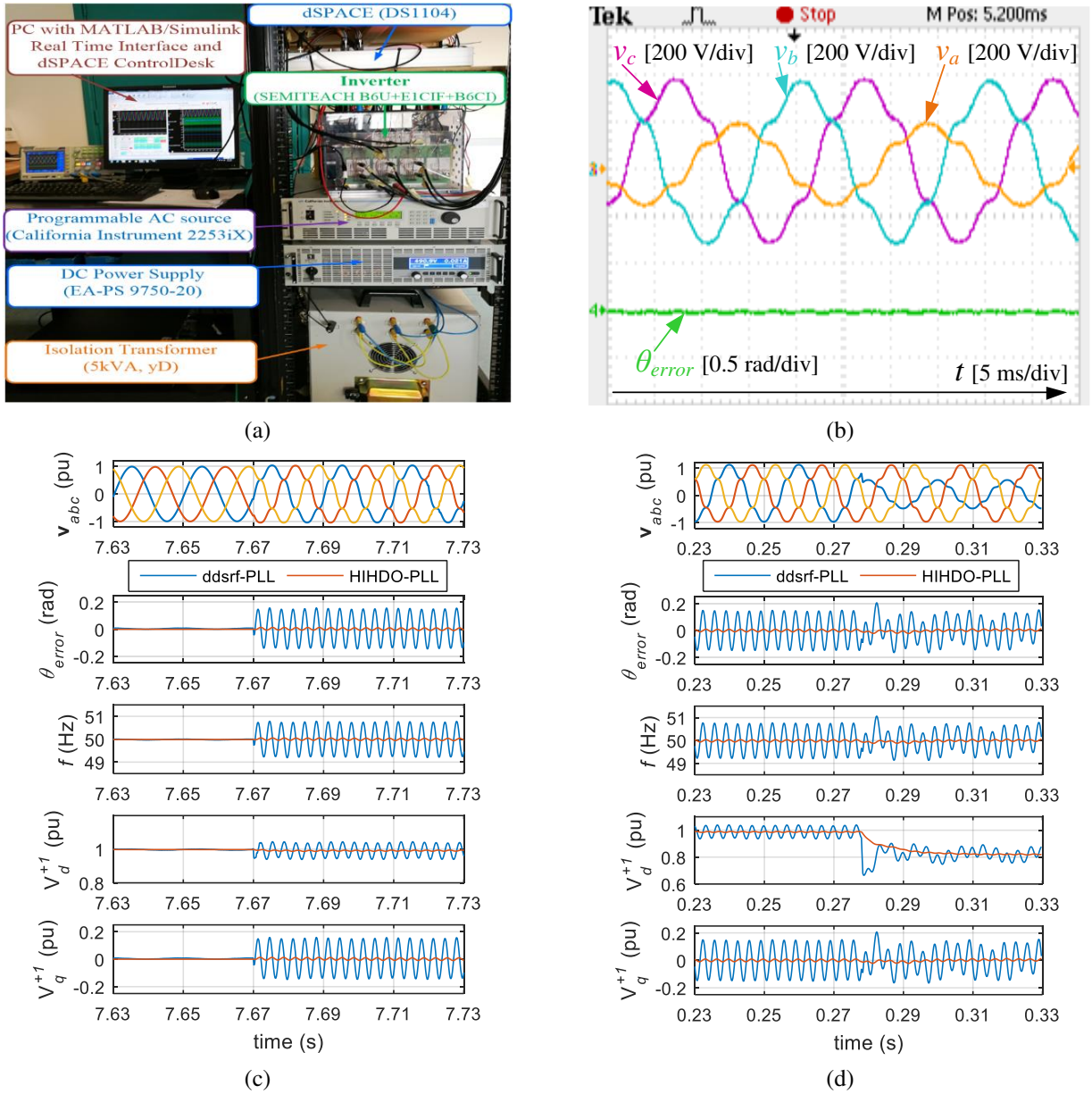

Fig. 8: Experimental validation:
(a) Schematic of experimental setup (b) Steady state response of proposed HIHDO-PLL (case study 1),
(c) Experimental results showing transient response of HIHDO-PLL vs ddsrf-PLL for case study 2,
(d) Experimental results showing transient response of HIHDO-PLL vs ddsrf-PLL for case study 3.

estimation under harmonics and DC offset, and the value of error in estimated angle for ddsrf-PLL is approximately 0.2 rad.

Table 6: Case study 1 operating conditions.

Voltage Conditions:	$V_a = 115\ V, V_b = 230\ V,$ $V_c = 230\ V$ (Type B – 50% unbalanced fault)
Harmonic/Interharmonic	5th Harmonic = 10%; 7.2^{th} interharmonic = 5%
DC offset	+ 24.6 V_{dc}

Case Study 4 – Response of HIHDO-PLL for the mitigation of low order Interharmonics: The experimental case studies for the mitigation of both positive and negative sequences of 1.2^{th} interharmonic are presented in Fig. 9 (a) and Fig. 9 (b). The results show that the proposed HIHDOPLL performs accurately under these interharmonic conditions giving the desired phase estimation. The magnitude of both $+1.2^{th}$ and -1.2^{th} interharmonics is set to 5 % of the fundamental positive sequence voltage component. As per *SRF* transformation, the $+1.2^{th}$ and -1.2^{th} interharmonics generate 110 Hz and -10 Hz oscillations on the estimated phase, which however, are accurately mitigated by the proposed PLL. The peak value of phase error (θ_{error}) for $+1.2^{th}$ and -1.2^{th} interharmonics is 0.018 rad and 0.01 rad respectively, evincing the accurate response of the proposed PLL.

Case Study 5 – Mitigation of harmonics/Interharmonics and DC offset under grid frequency variations (47Hz–52 Hz): This experimental study investigates the performance of proposed PLL when eliminating the interharmonics under grid frequency variations in the

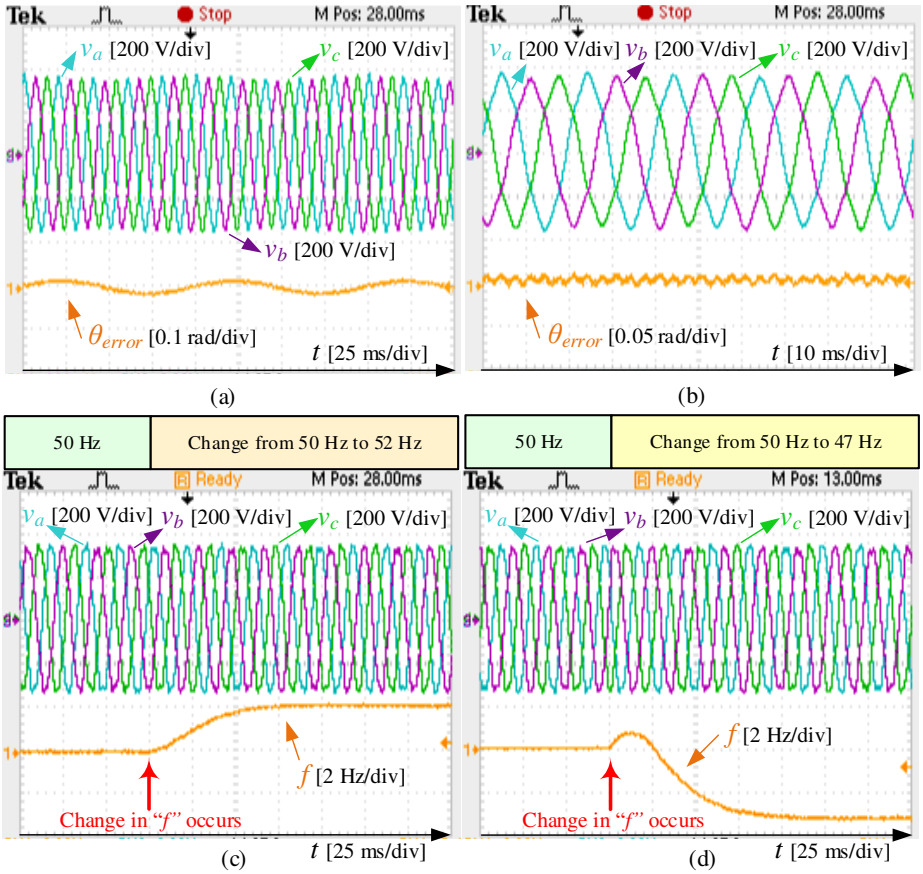

Fig. 9: Experimental validation: (a) Experimental results showing response of HIHDOPLL for the mitigation of +1.2th interharmonic, (b) Experimental results showing response of HIHDOPLL for the mitigation -1.2th interharmonic, (c) Experimental results showing transient response of HIHDOPLL to +2 Hz frequency change under harmonic, interharmonic and DC offset, (d) Experimental results showing transient response of HIHDOPLL to -3 Hz frequency change under harmonic, interharmonic and DC offset.

presence of DC offset and harmonics. The magnitude of DC offset is initially set to a value of $+24.6\ V_{dc}$. The magnitudes of 4.6th and 3.2nd interharmonics are set to 4 % and 3.5 %, respectively. The 5th and 7th order harmonic magnitudes are 4 % each. Under these conditions, the rise and decrease in grid frequency with respect to the nominal (50 Hz) is investigated. The result shown in Fig. 9 (c) is obtained by changing the grid frequency from 50 Hz to 52 Hz, and similarly, the response to change in frequency from 50 Hz to 47 Hz is presented in Fig. 9(d). For both cases, the proposed PLL mitigates for the abnormal grid conditions and accurately tracks the desired grid frequency. As also shown by the simulation results, the frequency settling time required to track the 52 Hz frequency change is 62 ms, whereas, 75 ms settling time is required for the 47 Hz case.

6. Conclusion

The HIHDO-PLL successfully addresses all the off-nominal/abnormal grid conditions in tandem while estimating the grid phase angle. The proposed PLL, equipped with all the aforementioned features including the compensation for interharmonics and DC offset, constitute it more advanced and complete than any other PLL that exist. In addition to the extra advanced features, the proposed HIHDO-PLL enables an accurate and fast operation with reduced computational complexity and low processing time, a critical characteristic necessary for real time implementation of such advanced algorithms. The advanced performance of proposed HIHDO-PLL is verified through simulations and experiments.

7. Acknowledgement

The authors Zunaib Ali and Nicholas Christofides are highly grateful to the Erasmus Mundus Leaders (EM-Leaders) mobility program for providing PhD fellowship. The authors Lenos Hadjidemetriou and Elias Kyriakides are supported by the Research Promotion Foundation (RPF, Cyprus, Project KOINA/SOLAR-ERA.NET/1215/06), by the Ministry of National Infrastructure Energy and Water (Israel) and the SOLAR-ERA.NET (European Union's Seventh Framework Programme).

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