

NASA Technical Memorandum 103147

## Design of an Optically Controlled Ka-Band GaAs MMIC Phased-Array Antenna

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CONTROLLED KA-BAND GaAs MMIC PHASED-ARRAY  
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**Richard R. Kunath**  
*Lewis Research Center*  
*Cleveland, Ohio*

**Paul C. Claspy and Mark A. Richard**  
*Case Western Reserve University*  
*Cleveland, Ohio*

**Kul B. Bhasin**  
*Lewis Research Center*  
*Cleveland, Ohio*

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**NASA**

## **Design of an Optically Controlled K<sub>a</sub>-band GaAs MMIC Phased-Array Antenna**

**Richard R. Kunath, Paul C. Claspy\*, Mark A. Richard\* and  
Kul B. Bhasin**

**NASA Lewis Research Center, Space Electronics Division  
Cleveland, Ohio 44135**

**\* Case Western Reserve University, Department of Electrical  
Engineering, Cleveland, Ohio 44106**

### **1. INTRODUCTION**

Phased-array antennas long have been investigated to support the agile, multibeam radiating apertures with rapid reconfigurability needs of radar and communications. With the development of the Monolithic Microwave Integrated Circuit (MMIC), phased array antennas having the stated characteristics are becoming realizable. However, at K-band frequencies (20-40 GHz) and higher, the problem of controlling the MMICs using conventional techniques either severely limits the array size or becomes insurmountable due to the close spacing of the radiating elements necessary to achieve the desired antenna performance.

Investigations have been made that indicate using fiber optics as a transmission line for control information for the MMICs provides a potential solution [ref. 1]. By adding an optical interface circuit to pre-existing MMIC designs, it is possible to take advantage of the small size, lightweight, mechanical flexibility and RFI/EMI resistant characteristics of fiber optics to distribute MMIC control signals. This paper will describe the architecture, circuit development, testing and integration of optically controlled K-band MMIC phased-array antennas.

### **2. PHASED-ARRAY ANTENNA ARCHITECTURE**

NASA Lewis Research Center's Space Electronics Division has been investigating using MMICs in K-band phased-array antennas. Due to the  $0.6\lambda$  radiating element spacing required to eliminate grating lobes in the front radiating hemisphere (+, - 90°), the distance between elements is 5mm (200 mils) at 30 GHz. The previous MMIC development at NASA-Lewis [ref. 2] has yielded devices at this frequency. The device of greatest importance, the phase shifter, is approximately 250x125 mils in dimension. This size rivals that of the radiating element and consequently forces equally close spacing of the MMICs. Spacings this close do not allow for conventional interconnects to be used. Therefore, a decision to exploit fiber optics was made and a contract to develop a low power, high speed OptoElectronic Interface Circuit (OEIC) was begun by Honeywell's Science Center in 1986 [ref. 3].

### **3. HYBRID OEIC DEVELOPMENT**

A hybrid OEIC was delivered for verification in 1989. The circuit features an optical receiver comprised of an interdigitated (2um finger width, 5um finger spacing) PIN photodiode and a three-stage (~10dB/stage), capacitively-coupled, differential Low Noise Amplifier (LNA) with approximately 100mW of power consumption [fig. 1]. The hybrid OEIC design used a second circuit design under a second NASA contract [ref. 4] to provide 1:16 demultiplexing and GaAs to TTL logic level level shifting. The hybrid design requires external clocking, synchronization and level shifting to complete the interface to the 30GHz MMIC phase shifter. As configured,

the hybrid OEIC takes a serial optical input and demultiplexes it into 16 TTL level outputs. The maximum data rate that the optical receiver can support is 1Gbps; however, the demultiplexer limits the data rate to only 300Mbps.

#### 4. HYBRID OEIC TESTING AND EVALUATION

As detailed in reference 3, the hybrid OEIC performance was tested and verified. The inherent delay between the optical and electrical interface signals is accommodated for using adjustable time-delay pulse generators. The MMIC phase shifters require 0 and -6 volt switching levels which are provided for by external CMOS analog multiplexers. Two different characterization/verification tests were made as described below.

The first test evaluated the hybrid OEIC characteristics and functionality [fig. 2]. A 64-bit NRZ-format word was cycled, and after external clock and synchronization signal timing was adjusted, the corresponding TTL level output bit signals were measured. The optical power required to obtain repeatable performance was  $>200\mu\text{W}$ , and the overall power consumption (dependant on termination impedance and demultiplexer output magnitude) was measured to be as low as 120mW.

The second test used the hybrid OEIC together with a 30GHz MMIC phase shifter. Employing an interferometric technique, the switching of the phase shifter by the hybrid OEIC could be measured by monitoring the constructive and destructive interference effects at the interferometer output with a crystal detector [fig. 3]. The external level shifter limited the test switching frequency to 2MHz; however, the use of this technique verified the hybrid OEIC's abilities to control the  $45^\circ$ ,  $90^\circ$  and  $180^\circ$  bits of the phase shifter.

#### 5. MONOLITHIC OEIC

While a fully monolithic OEIC was the anticipated deliverable from the OEIC contract, a materials processing problem prevented the successful development of the low power demultiplexer which inevitably led to a hybrid approach using a known, working demultiplexer (slower in speed and higher in power consumption). Further investigation by Honeywell into the processing problem finally led to the fabrication of usable fully monolithic devices [fig. 4]. The new devices feature the integrated optical receiver as before but require only an external clock signal. Synchronization is generated internally on the OEIC.

Future generations of fully monolithic OEIC designs will be augmented to provide enhanced performance and functionality. The current fully monolithic OEIC still requires a delay adjustable external clocking signal and when used in a phased-array of an appreciable size, will require adjustable delays for each MMIC in the array to account for the signal delay to the distributed MMIC elements. This can partly be corrected for by encoding the clock signal into the data stream and adding the necessary decoding circuits to the OEIC. Also, the OEIC is not a "smart" device. As it is currently configured, it relies upon the circuit sending it data to sort out its data from the data being sent to other OEIC/MMIC modules.

Distributed intelligence architectures as mentioned above are a relatively new concept for phased-array antennas, which heretofore relied upon single point array control. However, the OEIC circuitry is perfectly suited to combine all of these functions together. The design techniques to allow for independent address decoding, on-chip "look-up tables" and autonomous control are well-known and could be implemented in future OEIC/MMIC generations. NASA plans to investigate distributed intelligence architectures in future designs.

#### 6. PLANNED INTEGRATION AND TESTING

The critical issue to address in utilizing the OEIC in phased-array antennas is how to integrate the OEIC into

the overall array architecture. NASA is designing and planning to evaluate techniques to address the integration issues. Leveraging off a NASA-Lewis program to develop MMIC packaging and characterization techniques above 20GHz [ref. 5], a package to house a new generation of 32GHz MMIC phase shifters will be designed and fabricated.

Because the OEIC requires no ground plane for operation, it can be isolated from the ground plane necessary for both the MMIC and the radiating patch antenna. A carrier has been designed to mount the fully monolithic OEIC on, which minimizes the number of bias and external control signals [fig. 5]. The OEIC carrier is then epoxied onto the lid of the MMIC phase shifter package. This "piggy-back" approach results in two levels of wire bonds from the OEIC carrier [figs. 6 & 8]. One set of bonds connect the OEIC carrier to the top surface bias/clock distribution board, while a second set of bonds connect the OEIC data output lines to the MMIC package. Although it is not desirable to have two-level wire bonding, it is believed that "flip-chip" and via hole connection techniques could be used to eliminate these problems, and stable, reliable connections would be realized.

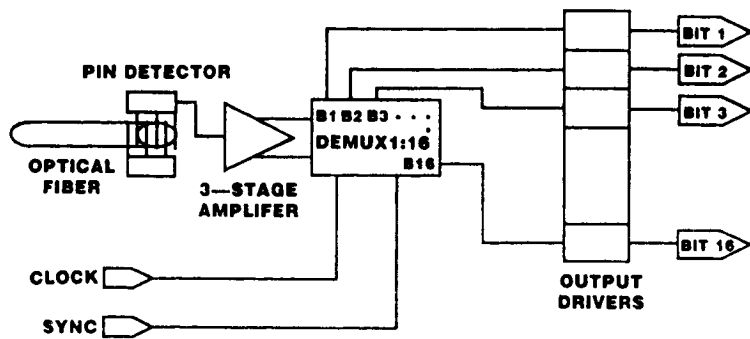
In order to test the integrated OEIC, NASA will design and build (in-house) an optical transmitter/controller suitable to control up to a 16 element optically controlled MMIC phased-array antenna. The transmitter/controller will use LEDs as channel signal sources and will provide for external clocking signal delays. When complete, the phased-array will be tested by measuring the antenna beam performance as the antenna is optically/electronically steered.

## 7. CONCLUSIONS

This paper has presented and discussed the use of fiber optic distribution of control signals in  $K_a$ -band MMIC phased-array antennas. Through the development of OEICs and their subsequent combination with previously developed MMICs, it has been shown that a potential solution to distributing control information to MMICs in closely-spaced arrays is possible. Further, a plan to integrate OEICs into MMIC phased-array antennas has been outlined, and future modifications to the OEIC have been discussed.

## 8. REFERENCES

1. Richard R. Kunath and Kul B. Bhasin, "Optically Controlled Phased-Array Antenna Technology for Space Communication Systems", Proceedings of the SPIE Optoelectronics and Laser Applications in Science and Engineering Symposium (O/E LASE '88), January 1988.
2. K. B. Bhasin and D. J. Connolly, "Advances in Monolithic Microwave Integrated Circuit Technology for Space Communications Systems," IEEE Transactions on Microwave Theory Techniques, Volume MTT-34, pp. 994-1001, 1986.
3. Kul B. Bhasin, et al, "A High Speed  $G_A$ , Optoelectronic Integrated Circuit for Control of a  $G_A$ , Monolithic  $K_a$ -band Phase Shifter", IEEE Photonics Technology Letters, Volume 1, No. 11, November 1989.
4. NASA Contract #NAS3-24676, "Development of Gallium Arsenide High-Speed, Low-Power Serial Parallel Interface Modules", Executive Summary and Final Report, May 1988.
5. Robert R. Romanofsky and Kurt A. Shalkhauser, "Universal Test Fixture for Monolithic mm-Wave Integrated Circuits Calibrated With an Augmented TRD Algorithm", NASA Technical Paper 2875, March 1989.



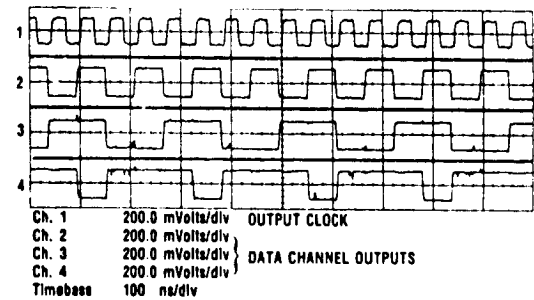
APPLICATIONS:

- PHASED ARRAY ANTENNAS
- HIGH SPEED COMPUTER INTERCONNECTS
- LOW POWER RECEIVER ARRAYS
- NEURAL NETWORKS



CHARACTERISTICS:

- INPUT DATA RATE  
~300 MBIT/S
- PROVIDES 16 PARALLEL OUTPUTS FOR  
SINGLE SERIAL INPUT
- INPUT OPTICAL POWER < 200  $\mu$ W
- GaAs E/D MODE MESFET TECHNOLOGY
- LOW ELECTRICAL POWER CONSUMPTION  
~277 mW

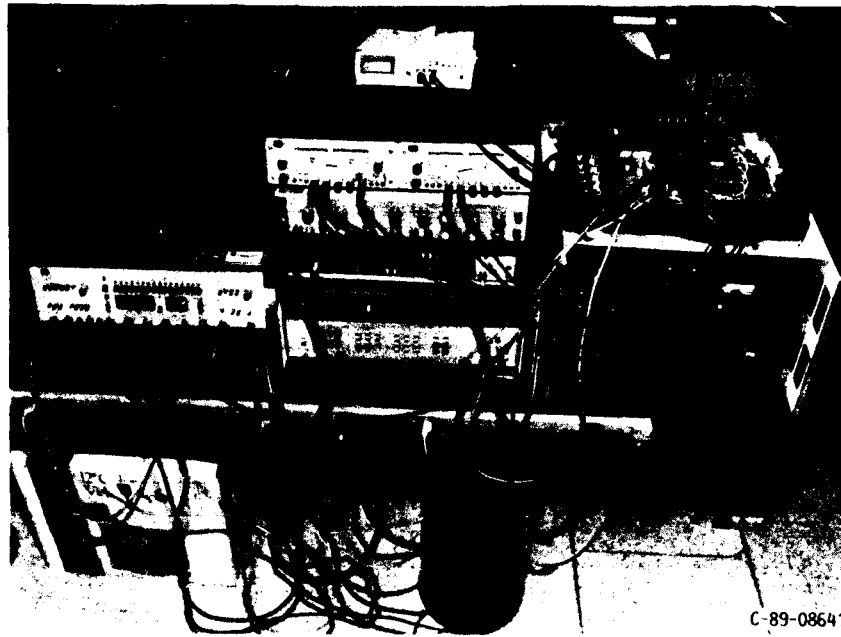


INPUT DATA RATE: 280 Mb/sec

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FIGURE 1. - HYBRID OPTOELECTRONIC INTERFACE CIRCUIT.

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FIGURE 2. - OEIC TEST SET UP TO MEASURE OEIC CHARACTERISTICS.

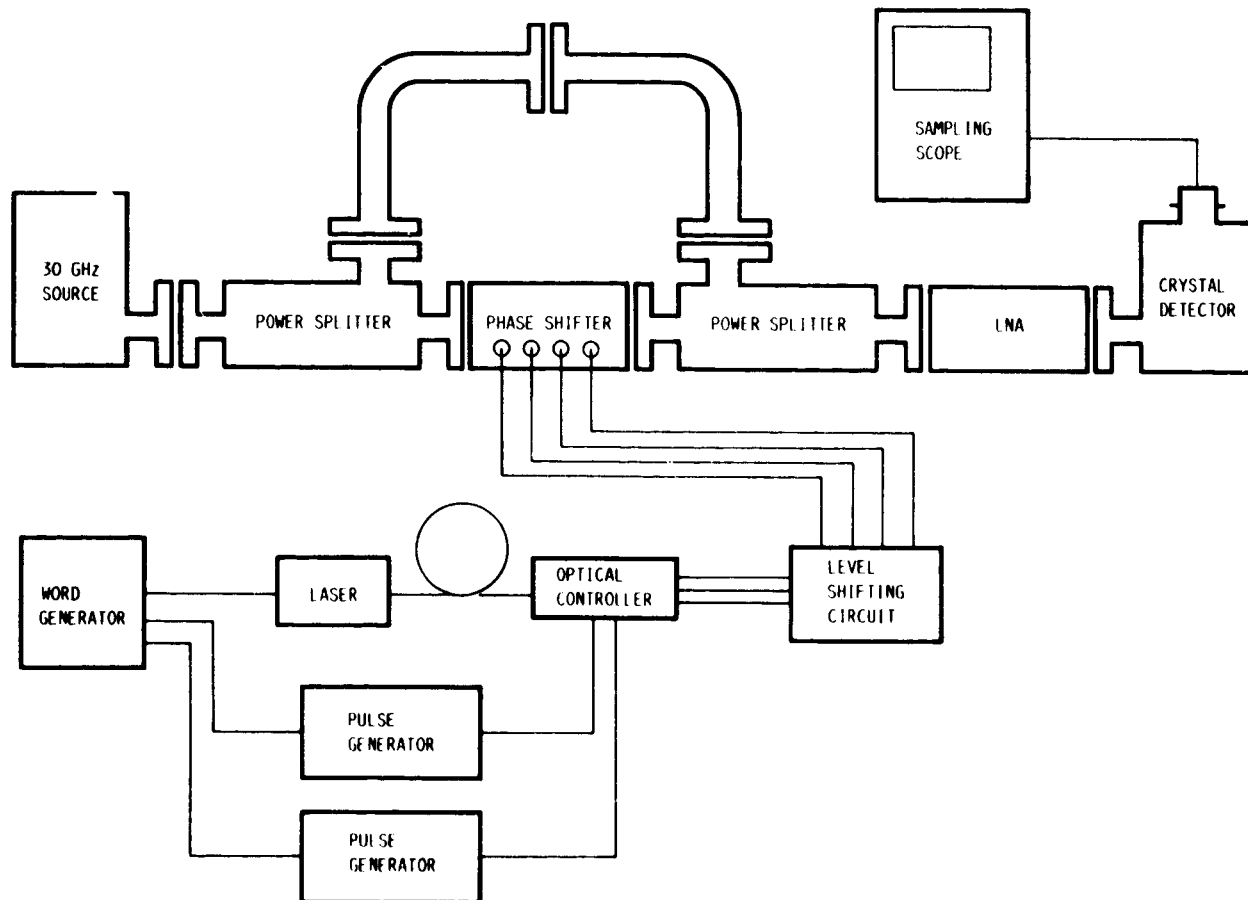
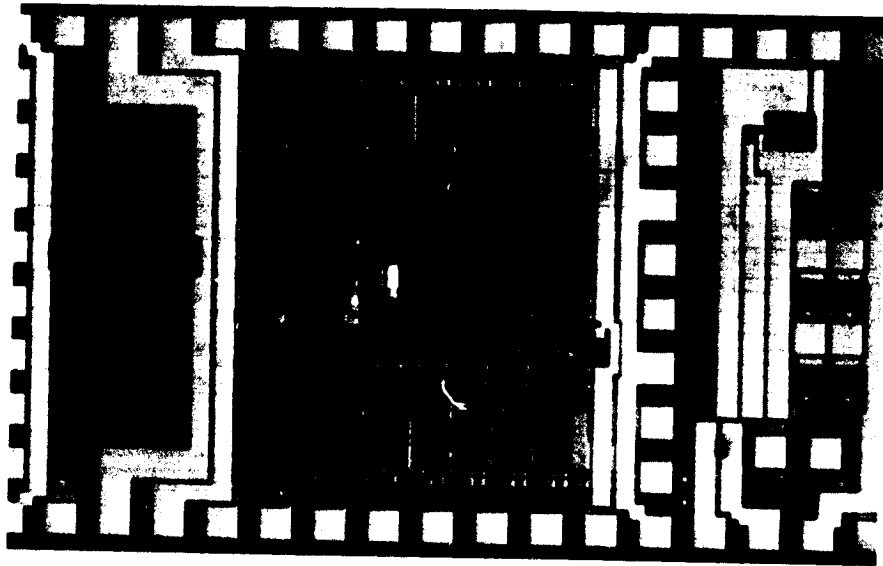


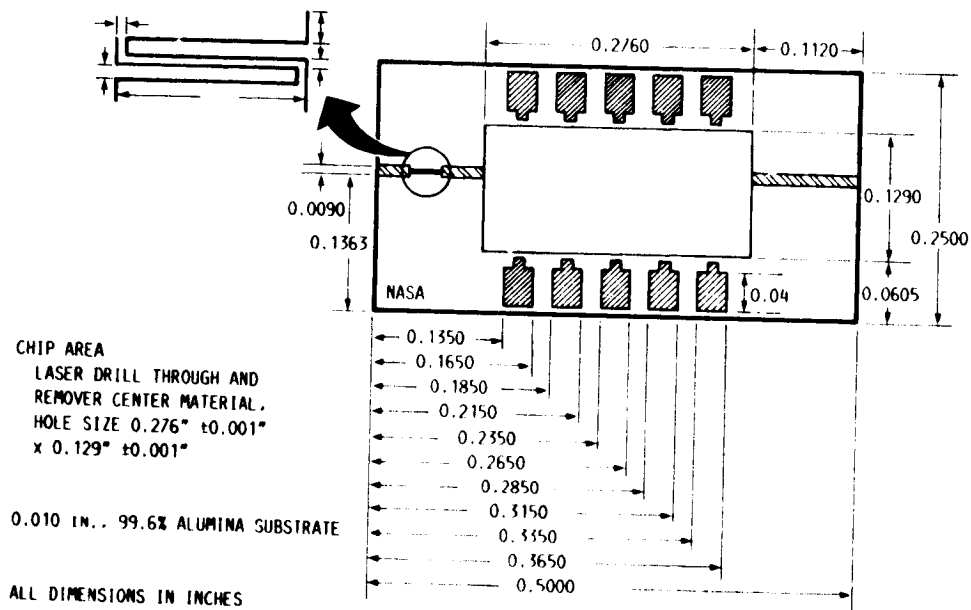
FIGURE 3. - OEIC TEST SET UP TO CONTROL A 50 GHz MMIC PHASE SHIFTER.

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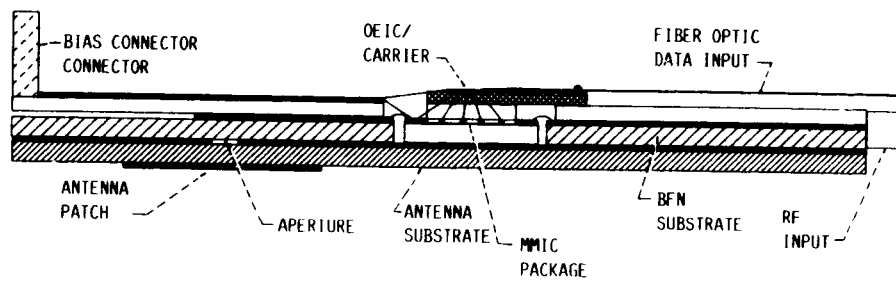
FIGURE 4. - MONOLITHIC OPTOELECTRONIC INTERFACE CIRCUIT.



NASA PHASE SHIFTER CARRIER TYPE 1

FIGURE 5. - MMIC PHASE SHIFTER SHOWING MMIC DIMENSIONS.

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OPTICALLY CONTROLLED MMIC PHASED-ARRAY CONFIGURATION  
 FIGURE 6. - PROPOSED OEIC INTEGRATION SCHEME FOR A PHASED-ARRAY ANTENNA.

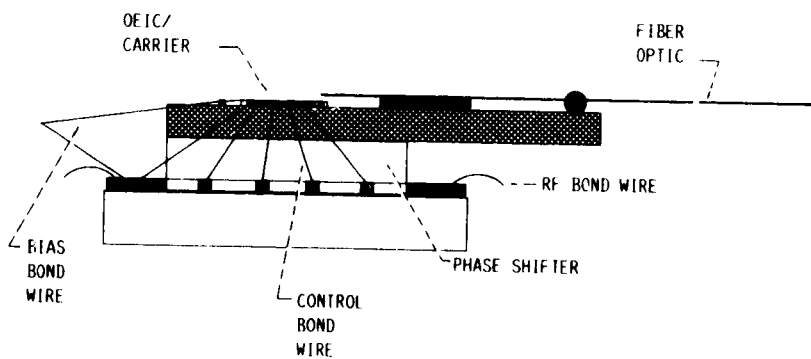


FIGURE 7. - CLOSEUP VIEW OF PROPOSED "PIGGY-BACK" OEIC INTEGRATION.





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