Design of an Ultra-Low Power SA-ADC with Medium/High Resolution and Speed

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***Abstract* — Design strategies for power effective medium/high resolution Successive-Approximation ADC are discussed. The study considers reducing the power of the capacitive array with suitable capacitive attenuators that do not need using non-unity capacitors. The design of minimum power comparators is analyzed and a novel comparator scheme, named time-domain comparator, is described. The proposed methodologies, verified with a test design, is capable to provide 12-bit with 50-kHz signal band and 1-V supply. The achieved FoM is 14 fJ/conv-level, which is well below the state-of-the-art.**

I. INTRODUCTION

In energy-limited applications, such as wireless sensor networks and portable instruments, the use of ultra-low power ADCs extends the battery life and, possibly, allows autonomous operations. The successive approximation (SA) algorithm is a suitable low-power solution, [1 - 4], when the signal band is in up to about 1 MHz and the resolution ranges between 10 and 12 bit. The SA architecture uses a comparator, a subtracting DAC together with its logic, and the successive approximation register (SAR) implementing the SA algorithm. The conversion starts with the sampling of the input signal and uses a clock period per bit. Therefore, the sampling rate is lower than the clock by a (N+1) factor. Since a capacitive array of equal unity capacitors achieves the subtraction DAC and the sampling function, the required power is related to the capacitances charge and discharge. With relatively low clock frequencies, the power consumption is in the μW range. A conventional scheme of voltage comparator consists in the cascade of a preamplifier and a latch. With submicron technologies, the capacitances to be charged and discharged are few ten of fF. Therefore, even for the comparator, the required power is very low. Finally, the limited complexity of the SAR logic and the low clock frequency enable very low power consumption. As a result, the figure of merit (FoM) defined by

$$FoM = \frac{P}{2^{ENOB} \cdot 2 \cdot f_B} \qquad (1)$$

where ENOB is the effective number of bits and f_B is the bandwidth, can be as low as various tens of fJ/conv-level.

This paper discusses various design strategies to obtain a very low FoM, well below the state-of-the-art. The proposed methods and the use of a new comparator scheme are used in a test-design, obtaining a simulated FoM of 14 fJ/conv-level almost verified on silicon, as synthetically described in [5].

II. CAPACITIVE ARRAY

The array of binary weighted capacitors of Fig. 1 realizes the sampling of the input signal and the charge redistribution by means of switches, controlled by the SAR logic, which connect the capacitors bottom plates to $V_{cm} \pm V_R/2$. The power consumed by the capacitors affects the input terminal and the references. For the former contribution, notice that the SA algorithm gives rise to a redistribution of charges and leaves the array charged at the previous input sample at the end of the conversion. Therefore, for each sample, the input terminal must provide a charge to the total capacitance C_T of the array given by

$$Q(nT_s) = C_T\left[V_{in}(nT_s) - V_{in}(nT_s - T_s)\right] \qquad (2)$$

that increases with the input frequency and becomes maximum at Nyquist. Therefore, a full-scale sine wave at the Nyquist frequency drains a maximum current $I_{in} = C_T V_R/T_s$.

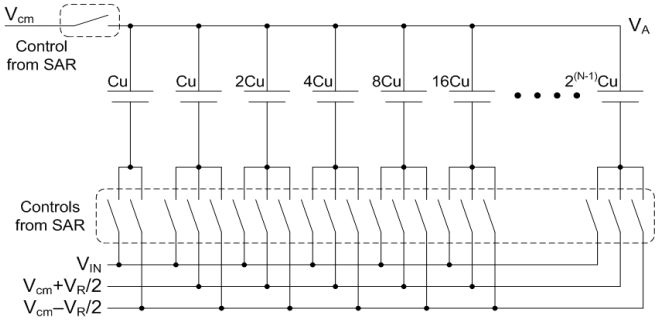

Figure 1. Binary weighted capacitors array.

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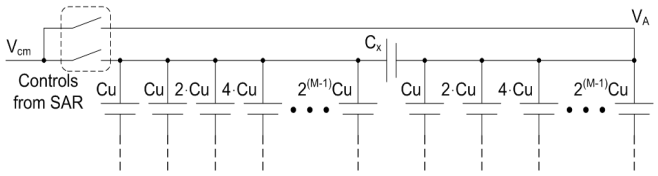

Figure 2. Binary capacitors arrays with attenuation capacitor.

The minimum total capacitance of the array is limited by the $2kT/C$ noise associated to the array charging and discharging. Since the power of the quantization noise is $V_R^2/2^{2N}/12$, it is necessary to verify the condition

$$C_T > \frac{24 \cdot kT \cdot 2^{2 \cdot N}}{V_R^2} \qquad (3)$$

For $V_R = 1$ V and $N = 12$, the minimum value of C_T is 1.64 pF and the corresponding current I_{in} is equal to 0.164 µA. The figure is very low, but it is also necessary to account for the minimum unity capacitance that gives rise to a suitable mismatch error. As known, the capacitance accuracy is inversely proportional to the plate area, A_C: $\Delta C^2/C^2 = K_C/A_C$. Moreover, it is necessary to account for the mismatch caused by the parasitic metal connections and switches. Modern technologies obtain very low values for K_C. However, overall limitations and a suitable margin suggest using $C_U > 40$ fF. Therefore, the use of a plain 12-bit binary array gives rise to $C_T = 2^{12} C_U > 164$ pF, a limit much larger that what established by the $2kT/C$ limit. Accordingly, I_{in} becomes about 16.4 µA.

The power drawn from the reference generator depends on the input amplitude and the resulting SA cycle. In average, the charge flowing from the reference generators to sustain the charge redistribution is about $\frac{1}{2} C_T V_R$. Therefore, the average current is $I_R = \frac{1}{2} C_T V_R / T_s$, half of the current drawn from the input terminal, considering a full scale sine wave at Nyquist.

The above study shows that if the minimum value of C_U constrains C_T, an array of 2^N binary array consumes significant power, making convenient the use of an attenuation capacitance as shown in Fig. 2. Since the value of C_2 is scaled by a factor $k = 2^M$, than the series of C_1 and C_x must become C_1/k

$$\frac{C_1 C_x}{C_1 + C_x} = \frac{C_1}{k} \qquad (3)$$

resulting in $C_x = C_1/(k - 1)$. If $C_1 = 2^m C_U$, as normally chosen, C_x is a fractional value that is difficult to realize (and this is the main limit to the use of the method). Instead, if $C_1 = (2^M\text{-}1)C_U$, $C_x = C_U$ and this is positive. Moreover, having C_1 made by $(2^m\text{-}1)$ unity elements is not a big limit because there is a unity capacitance always connected to the lower reference. Its role is to have equivalent DAC full scale at 1 LSB below $V_{cm}+V_R/2$. If that capacitor is removed, the full scale becomes $V_{cm}+V_R/2$ with a negligible gain error α. This result is an improvement of the technique proposed in [6].

It is also possible to extend the method to two attenuating capacitors, but having unity scaling capacitances is more problematic. The method described above with two scaled sections is not effective because the gain error α is inessential

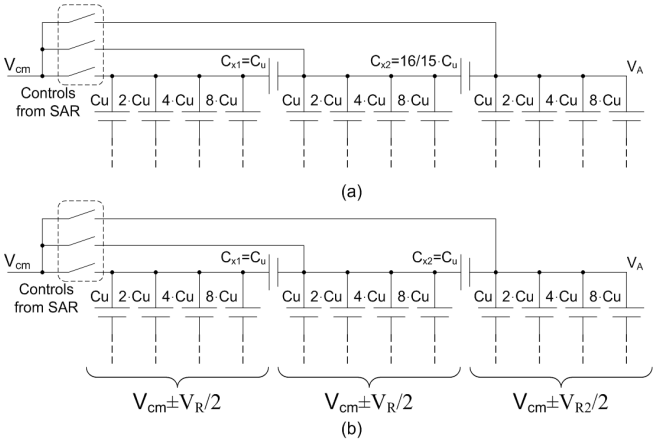

Figure 3. Binary capacitors arrays with two attenuation capacitors.

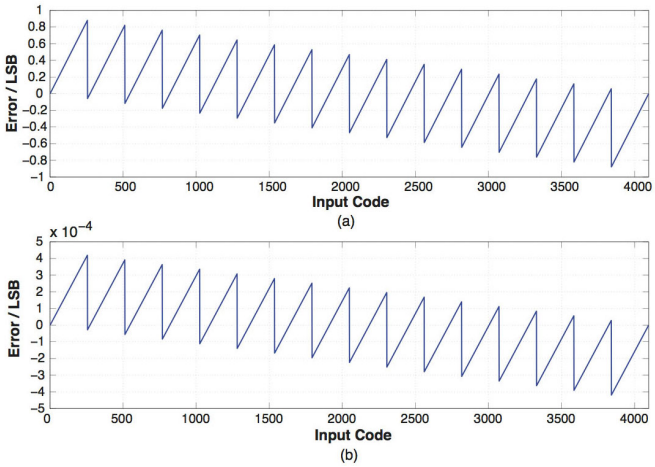

Figure 4. (a): INL of Fig. 3(a) scheme; (b): INL of Fig. 3(b) scheme.

when caused at the output, but it is responsible of a periodic 1-LSB INL if the architecture uses another attenuating section. Fig. 3(a) shows a 4+4+4 binary arrays with one unity scaling capacitance, C_{x1}, and the other, C_{x2}, equal to $16/15 C_U$. Fig. 4 (a) shows the INL determined by this scheme. The INL worsens if even the second scaling element equals C_U. However, the gain error caused by the LSB scaling and the one produced by changing C_{x2} from $16/15 C_U$ to C_U (Fig. 3 (b)) can be corrected by scaling the reference voltage in the MSB array. The use of $V_{cm}\pm V_{R2}/2$ with $V_{R2} = 1.0586 V_R$ allows obtaining the INL of Fig. 4 (b), that is lower than ±0.0005LSB. The MSB references, V_{R2}, can be possibly obtained by an off-line calibration at the converter turn-on.

III. Comparator

The second element that consumes power is the comparator. Since the input differential signal of a latch should be at least 20 mV to avoid latching errors, it is necessary to use a preamplifier. The LSB of a 10-12-bit ADC is a fraction of mV; therefore, the differential dynamic gain of the preamplifier should be in the 30-60 dB range. The transconductance of the input pair used in the preamplifier

with input voltage V_{in} determines a signal current, $g_m V_{in}$, that charges a parasitic capacitance, C_p, for the preamplification time, T_p. The output voltage at the latch time becomes

$$V_{out} = V_{in}\frac{g_m T_p}{C_p} = V_{in}\frac{I_B T_p}{m V_T C_p} \quad (4)$$

where I_B is the bias current of the input pair. Moreover, it is assumed that the MOS transistors of the input pair are in weak inversion ($m \approx 2.2$). Equation (4) determines the minimum current for a given clock frequency, dynamic gain, V_{LSB} and parasitic capacitance loading the preamplifier output. C_p is given by the parasitic of the preamplifier output and the input parasitic of the latch. Assuming a preamplifier made by a cascode structure, C_p for 0.13-0.18 μm CMOS technology is estimated to be 40 fF. With $V_{LSB} = 0.2$ mV, $T_p = 380$ ns, and $V_{out} = 20$ mV, the bias current I_B equals 0.76 μA.

Even if this current consumption is already very low, the figure can be improved by using a new proposed time-domain comparator structure that, instead of operating in the voltage domain, transforms the input voltage into a pulse whose duration is compared with half period of the master clock. Fig. 5 shows the circuit schematic of the voltage-to-time (*V2T*) cell, used to generate the pulse. The input voltage V_A establishes a current through R_D that charges capacitor C_L.

When the signal Φ_C is low, transistors M_1 discharges the capacitor C_L. In the meantime, transistor M_4 discharges the parasitic capacitor C_P to cancel out any memory of the previous conversion. When Φ_C rises, transistors M_2 turns on and the current generator made by M_3 and R_D charge C_L at constant rate. If the input voltage is constant and produces V_R across R_D, then

$$I_D = \frac{V_R}{R_D} \quad (5)$$

When, after a given time T_d, the voltage across C_L, V_C, crosses the threshold of M_5, Out_{V2T} rises up, driven by the tapered inverter chain. Out_{V2T} drives also the logic which turns off M_2 for saving power, as the operation avoids to complete discharge C_L. Fig. 6 conceptually shows the V2T cell operation. For the used configuration T_d increases when the input voltage is reduced and vice-versa. Moreover, since the parasitic capacitor C_P is discharged by M_4, its series connection with C_L gives an initial charging of C_L itself. Therefore, voltage V_C immediately falls to

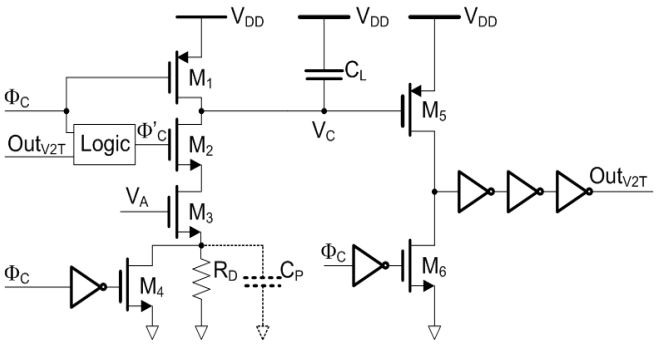

Figure 5. V2T cell schematic diagram.

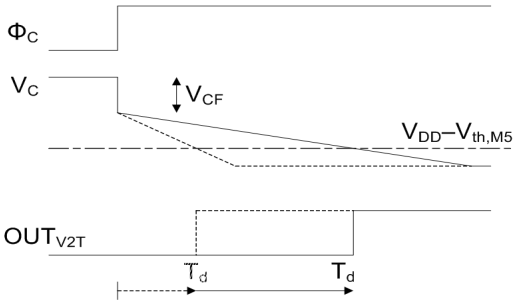

Figure 6. V2T main signal waveforms.

$$V_{CF} = V_{DD}\frac{C_P}{C_L + C_P} \quad (2)$$

Then, the constant rate discharge of C_L starts. The initial drop of V_C has positive effects because it reduces T_d without increasing the discharge current. Splitting C_L in two parts, C_{L1} and C_{L2}, enhances the drop. C_{L1} is connected to V_{DD} as in the scheme, C_{L2} is connected between V_{DD} and the source of M_2 and pre-charged to V_{DD} by a switch that ties the source of M_2 to ground during Φ_C. Neglecting C_P, the drop of V_C becomes $V_{DD}(C_{L2}/C_{L1}+C_{L2})$.

Fig. 7 shows the block diagram of the comparator together with its timing. It consists of a *V2T* cell and a flip-flop delay (*FFD*). The phase Φ_C used to pre-charge C_L is on for a quarter of the clock. A delay of the Out_{V2T} pulse larger than $3/4T_{CK}$ is revealed by the *FFD* clocked by the master clock, *CK*. The time-domain comparator output voltage, Out_{comp}, is then used as input of the *SAR*. Slightly after the crossing of the threshold, the logic opens M_2 and stops the flow of current through R_D. Therefore, if ΔV_C is the drop of the voltage V_C giving rise to the bit detection, the energy per clock period consumed by C_L is $C_L \cdot \Delta V_C^2$.

The design parameters of the *V2T* are determined by the required accuracy that, by turn, is controlled by three main factors: the *kT/C* noise, the input referred noise of M_5, $v_{n,5}$, and the minimum distance between clock and *D* input in the *FFD*.

Since the time for discharging C_L by ΔV_C is $T_0 = 3/4T_{CK}$, the bias value of V_A must produce across R_L a drop voltage ΔV_R such that $\Delta V_C/\Delta V_R = T_0/R_L C_L$. Therefore, an *LSB* added to the bias of V_A determine a $\delta V_C = LSB \cdot T_0/R_L C_L = LSB \cdot \Delta V_C/\Delta V_R$ variation at $t=T_0$.

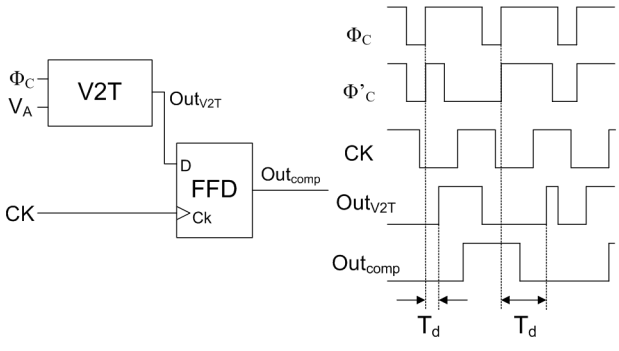

Figure 7. Time-domain block diagram.

Therefore, the amplification of the LSB by $A_0 = \Delta V_C/\Delta V_R$ must be lower than the equivalent noise across C_L; i.e. the quadratic superposition of sqrt($2kT/C_L$) with $v_{n,5}$. If C_L = 0.8 pF, $v_{n,5}$ = 130µV and A_0 = 2, the LSB, that equals the noise, is as low as 83 µV.

The nominal slope of the discharge of V_{CL} is $\Delta V_C/T_0$; accordingly, a time uncertainty δt in the operation of the *FFD* corresponds to an input referred noise $\delta V_A = \delta t \Delta V_C/T_0/A_0$. With ΔV_C = 0.2 V, T_0 = 0.5 µs and δt = 250 ps, δV_A = 43 µV. The value of R_L is 312 kΩ and the average consumed power is 0.26 µW.

IV. Design Example

The proposed design methods and the use of a time-domain comparator have been verified with transistor level simulations using a 0.18-µm CMOS technology.

Two 31-C_U elements and a C_U attenuating capacitor make the capacitive array. The nominal value of C_U is 100 fF. The switches used in the subtracting DAC are made by complementary devices, except the one connected to V_{cm} that is an *n*-channel transistor with clock boost, [7].

The minimum supply voltage that achieves a good comparator response is as low as 0.7 V, because the only limit to reduce the supply voltage is given by the drop across R_D and the threshold of M_3. The nominal used supply voltage is 1 V, V_{cm} and V_R are 0.5 V and 1 V, respectively. Notice that the scheme allows using a V_R higher than the rail-to-rail provided that the switches are only *n*-channel with clock boost, [6]. The values of discharging capacitances C_{L1} and C_{L2} are 0.6 pF and 0.2 pF, respectively, thus achieving an initial drop of 250 mV.

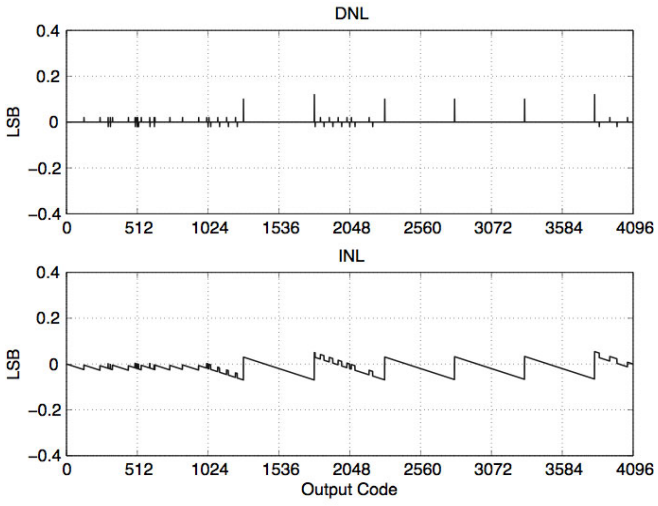

Figure 8. Simulated DNL and INL.

The simulations use a random error on unity capacitances with variance σ = 0.003, value that is higher than what modern technologies obtain with C_U = 100 fF. Nevertheless, the obtained simulated results show typical DNL and INL plots like the one depicted in Fig. 8. It can be noted that both DNL and INL are less than ±0.2 LSB.

The spectra with f_{CK}=1.3 MHz, 12-bit and a full-scale sine-wave at 2.6 kHz and 44.3 kHz are shown in Fig. 9. The simulation results show SNRs of 70.8 dB and 68.6 dB respectively (11.8 and 11.1 ENOB) with a third harmonic below 90 dB.

The total simulated power consumption is 3.1 µW that allows obtaining a 14-fJ/conv-step of FoM. A similar circuit with a less sophisticated architecture of the time-domain comparator has been experimentally evaluated. The obtained ENOB is 9.4-bit which demonstrates the effectiveness of the approach providing a FoM of 56 fJ/conv-level, [5].

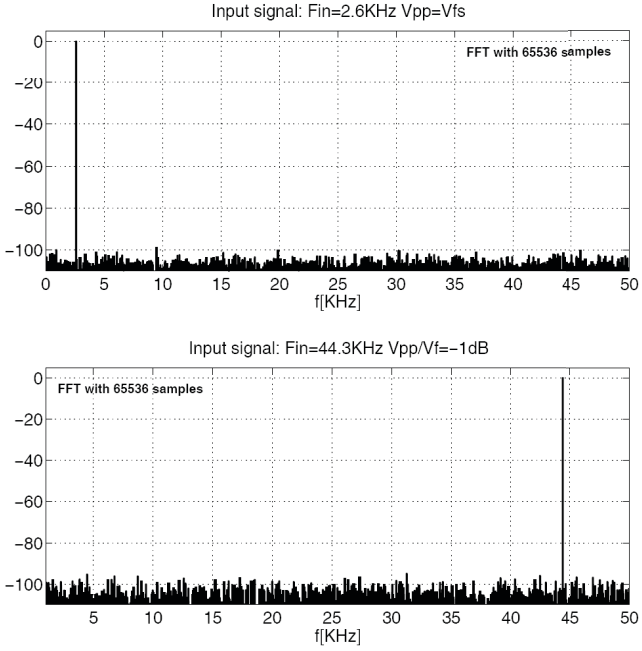

Figure 9. Output Spectrums with input sine wave @ 2.6 kHz and 44.3 kHz.

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