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Research Article

Design of Analog Signal Processing Applications Using Carbon Nanotube Field Effect Transistor-Based Low-Power Folded Cascode Operational Amplifier

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Carbon nanotube (CNT) is one of the embryonic technologies within recent inventions towards miniaturization of semiconductor devices and is gaining much attention due to very high throughput and very extensive series of applications in various analog/mixed signal applications of today's high-speed era. The carbon nanotube field effect transistors (CNFETs) have been reconnoitred as the stimulating aspirant for the future generations of integrated circuit (IC) devices. CNFETs are being widely deliberated as probable replacement to silicon MOSFETs also. In this paper, different analog signal processing applications such as inverting amplifier, noninverting amplifier, summer, subtractor, differentiator, integrator, half-wave and full-wave rectifiers, clipper, clamper, inverting and noninverting comparators, peak detector, and zero crossing detector are implemented using low-power folded cascode operational amplifier (op-amp) implemented using CNFET. The proposed CNFET-based analog signal processing applications are instigated at 32 nm technology node. Simulation results show that the proposed applications are properly implemented using novel folded cascode operational amplifier (FCOA) implemented using CNFET.

1. Introduction

Over the last few decades, the electronics industries have seen remarkable growth in integrated circuits applications. There is substantial increase in integration density, speed, and performance, which results in high-speed portable devices and such demands are still raising in day-to-day life. Power dissipation and heating constraints are also increasing with every new technology, as emerging silicon technologies continues to scale unfathomable into the ultra-nanometer regime. Through the last few decades, significant efforts are made to reduce the power budget ensuring high performance. But, the aggressive scaling of MOS transistors now approached to the fact that the channel and gate oxide becomes very thin and diffusion regions of transistors are in such vicinity that the charge carriers can easily cross the channel in vertical direction leading to unwanted currents through it and hence further horizontal scaling is not possible. As anticipated by the International Technology Roadmap for Semiconductors [1], rigorous exploration is desirable in order to endure this process and, undeniably, to encourage novel devices and methods that will move the technology developments in other directions [2, 3]. Carbon nanotube field-effect transistor (CNFET) is the competitor transistor which will permit for both the scaling process to sustain and for the progress of novel devices [4]. The details of CNFET and its properties are explained in Section 2.

Operational amplifiers (op-amps) are indispensable blocks in almost all analog/mixed signal applications [5]. Design and development of maximum throughput analog

integrated circuits is fetching progressive constraining due to the persistent tendency towards scaling in very deep submicron regime. There is a significant degradation in the performance of op-amp in nanometer regime and there is a stringent requirement to reconnoitre new circuit design strategies for new upcoming devices like CNFET for their speedy merchandise to prolong Moore's law in deep nanometer regime [6]. Explanation of finest design of CMOS-based folded cascode op-amp is extensively discussed by us in [7] and will not be covered here. Brief about CNFET and its performance comparison with CMOS is explained in section 2. Design of CNFET-based FCOA and the effect of pitch and diameter on the performance parameters are explained in Section 3. Section 4 explains different analog signal processing applications implemented using CNFET-FCOA at 32 nm technology node. Concluding remarks towards the achievement of various performance metrics using CNFET are stated in Section 5.

2. Carbon Nanotube Field Effect Transistor

CNFETs are the transistors in which number of carbon nanotubes (CNTs) acts as a physical channel between source and drain unlike virtual channel in case of metal oxide semiconductor field effect transistor (MOSFET) [8]. CNTs are thin sheets of graphene. Graphene is an allotrope of carbon made up of tightly packed thin layer of pure carbon atoms. This thin single-layered sheet is then rolled into tubes along different directions to form either metallic or semiconducting single-walled CNTs (SWCNTs). This direction of rotation is termed as the chirality and represented in the form of sum of two vectors (n, m), as shown in Equation (1), representing two different directions. Out of these two types of SWCNTs, metallic nanotubes are widely used as interconnect and semiconducting nanotubes have captivated prevalent attention as an alternative solution for high-performance transistors in nanometer regime [9, 10]. An SWCNT is a conductor if $n - m = 3k$ ($k \in Z$); otherwise it is a semiconductor [11], where n, m are positive integers that specify the chirality of the tube [7–13]. The magnitude of the chirality depends on the diameter of the CNT and is determined by using Equation (2):

$$\mathrm{Ch} = a\sqrt{n^2 + m^2 + nm}, \tag{1}$$

$$D = \frac{a\sqrt{n^2 + m^2 + nm}}{\pi} \approx 0.0783\sqrt{n^2 + m^2 + nm}, \tag{2}$$

where a is the carbon-to-carbon atomic distance, which is ~2.49 Å.

A distinctive construction of a CNFET device is demonstrated in Figure 1. All regions in this device are heavily doped except the CNT channel region, which is completely undoped. Analogous to the MOSFET, a CNFET also has a threshold voltage which needs to turn on the device. An inimitable feature of the CNFET device is the adjustability of its threshold voltage by changing the diameter of the CNTs. This is due to the fact that the CNT band gap, which is the function of the threshold voltage, depends inversely on the diameter as shown in the following equation [11, 14, 15]:

$$V_{\mathrm{th}} \approx \frac{Eg}{2e} = 0.557a\frac{V\pi}{\mathrm{DCNT}} \approx \frac{0.43}{\mathrm{DCNT}}, \tag{3}$$

where "e" is the unit electron charge and $V\pi$ (~3.033 eV) is the carbon p-p bond energy in the tight bonding model. This pertinent property makes the CNFET very useful for voltage mode analog and digital circuits [7, 11].

2.1. Performance Comparison of CMOS and CNFET with Respect to Electrical Characteristics. CNFETs are better than bulk complementary metal oxide semiconductor (CMOS) transistors in case of contact resistance, subthreshold slope, and current drive capability. The contact resistance and the subthreshold slope of a CNFET are analogous to those of CMOS transistors. The CNFET current is measured in current per tube and can be increased by increasing the number of tubes, while a CMOS current drive is characteristically represented in current per unit device width (e.g., μA/μm) [12]. The ON current of CNFET can be approximately given by Equation (4) and it has little dependency on the channel length in case of near-ballistic transportation:

$$I_{\mathrm{cnt}} \approx \frac{Ng_{\mathrm{cnt}}\left(V_{\mathrm{DD}} - V_{\mathrm{th}}\right)}{1 + g_{\mathrm{cnt}}L_{\mathrm{s}}\rho_{\mathrm{s}}}, \tag{4}$$

where L_{s} is the length of the doped CNT source region, ρ_s is the source resistance per unit length of doped CNT, and g_{cnt} is the transconductance per CNT and is given by the following equation:

$$g_{\mathrm{cnt}} = \frac{\mu_{\mathrm{cnt}}C_{\mathrm{gc\_u}}\left|V_{\mathrm{gs}} - V_{\mathrm{th}}\right|}{L} = \frac{\mu_{\mathrm{cnt}}C_{\mathrm{gc_u}}\left|V_{\mathrm{gs}} - 0.43/D_{\mathrm{cnt}}\right|}{L}, \tag{5}$$

where μ_{cnt} and $C_{\mathrm{gc\_u}}$ are the carrier mobility in CNT and gate to channel capacitance per unit length, respectively.

I-V characteristics of a typical 32 nm MOSFET-like N-CNFET and P-CNFET are shown in Figure 2(a). According to Figure 2(b), a 32 nm CNFET has proper I_{d}-V_{ds} characteristics without short channel effects, whereas the 32 nm MOSFET suffers from higher channel resistance in the triode region, degraded r_0, and velocity saturation. Furthermore, as illustrated in Figure 2(b), besides the considerable higher ION/IOFF of the CNFET, it has a quadratic I_{d}-V_{gs} curve in the saturation region while the MOSFET device has a linear I_{d}-V_{gs} curve, mostly due to velocity saturation. Hence, it can be concluded that the MOSFET-like CNFET can be a promising device for designing some nanoscale analog circuits such as precise comparators and high-gain amplifiers [11].

Additionally, compared to bulk CMOS, the effective gate capacitance of one CNT per gate of CNFETs is about 4% and the current drive capability of each CNT is about 50% in contrast to bulk n-type MOSFET [12]. This is due to the ballistic transport of carriers along the CNT in specific direction. This results into 13 times better CV/I performance of CNFET over that of bulk n-type MOSFET. Enhancement in performance of p-CNFET is more than that in n-CNFET as compared to PMOS and NMOS, respectively. This is due

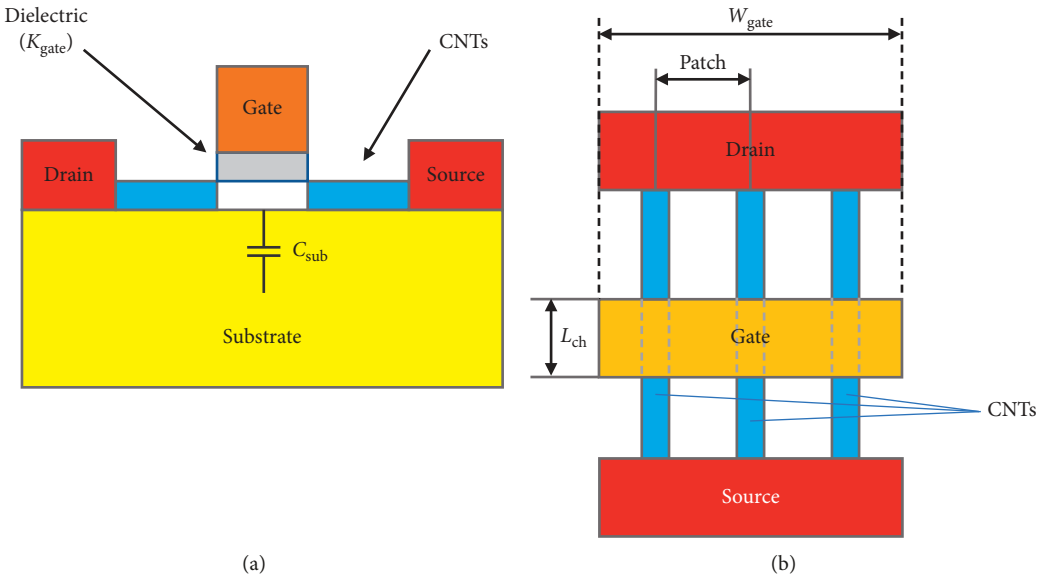


Figure 1: Structure of CNFET [23].

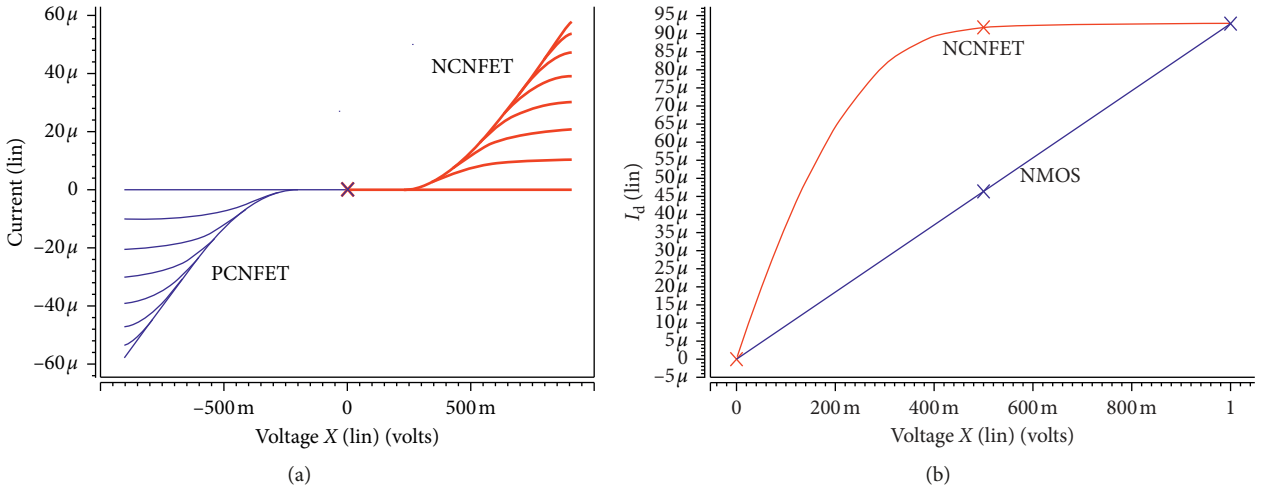


Figure 2: I-V characteristics of 32 nm CNFET and CMOS. (a) I_d-V_{ds} of NCNFET and PCNFET for various values of V_{gs}. (b) I_d-V_{ds} of NCNFET and NMOS.

to the similar behaviour and the current driving capability of a p-CNFET compared to those of an n-CNFET. The major problem associated with CNFET is the significant amount of leakage current in the off state, but it can be rectified by controlling the band to band tunneling and the full band gap of the CNTs which is less than for a MOSFET [13–17].

Moreover, the motion of the electrons in the nanotubes is sternly confined along the direction of tube axis, due to the quasi-1D structure of CNT. Hence, only forward and backward scatterings are possible for the carriers in nanotubes, and all other scatterings are prohibited. The experimentally observed mean free path (MFP) is ~1 μm [18, 19], which implies near-ballistic carrier transport. Typical range of mobility is very high, up to 10^3~10^4 cm^2/V·s observed during conductance experiments in transistors and as has been proved by a diversity of studies [20, 21]. Hypothetical study too forecasts a mobility of ~10^4 cm^2/V·s for semiconducting CNTs [22]. The current carrying capability of multiwalled CNTs are confirmed to be more than 10^9 A/cm^2, about 3 orders greater than the extreme current carrying capacity of copper and also able to sustain the same performance well above the room temperature [19]. In nutshell, the superior carrier transport and conduction characteristic makes CNFETs a promising candidate for nanoelectronics applications [13].

With these tremendous features of CNTs and CNFETs, circuit design using CNFET is on the top choices of circuit designers. However, more emphasis and hence extensive research is done in digital circuit implementation, and analog circuit design is still a challenge. As on today, very few, only one or two, topologies of op-amps are implemented using CNFET. In this paper, first attempt is made, to

the best of our knowledge, to design CNFET-based folded cascode op-amp (CNFET-FCOA) and successfully calculate almost all parameters associated with an op-amp. Further different signal processing applications are implemented using novel folded cascode op-amp (FCOA) designed using CNFET at 32 nm CNFET technologies. Next section explains about the design of CNFET-FCOA.

3. Design of Folded Cascode op-Amp Using Carbon Nanotube Field Effect Transistor

A CNFET works on the fundamental concept of applying gate voltage to modulate the current between drain and source and exhibits unipolar behaviour. In back-gated structures, due to different junction and overlap capacitances, high-frequency operation is limited but the top-gate edifice of CNFET permits high-speed operation. Also, due to inbuilt channel of nanotubes and its structure, leakage current is no longer the problem with CNFET and it shows enhanced current handling competency [24–26]. CNFET endeavours remarkable carrier transport and conduction characteristics predominantly due to the high mobility and high current density [25–27]. The width of the CNFET transistor (W), the diameter of CNT (D_{cnt}), number of CNTs in the channel (N), the spacing between two adjacent nanotubes, and pitch (S) [13, 19, 22–26] are related by the following equation:

$$W = (N-1)S + D_{\text{cnt}}. \tag{6}$$

In CNFET-based implementation, number of tubes, pitch, and diameter are the parameters that are designed to achieve optimum result unlike aspect ratios in case of CMOS [2, 3, 28–30]. Figure 3(a) shows the schematic of proposed CNFET-FCOA, and Figure 3(b) shows the symbolic representation of proposed CNFET-FCOA.

In this analysis, unlike conventional op-amp, it is presumed that the current from $Q1$ directly flows through the drain of $Q6$ and thus to the load capacitance and the current from $Q2$ goes indirectly through $Q5$ and the current mirror consisting of $Q7$ to $Q10$. Also, it is assumed that maximum amount of current flows through $Q1$ and hence these two paths have slightly different transfer functions. The high-frequency poles and zeros are nondominant and can be ignored because they are located at high frequency compared to unity gain frequency [7].

An approximate small-signal transfer function for the folded-cascode op-amp in CMOS technology is given by

$$\text{Av} = \frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = g_{\text{m1}} \cdot Z_{\text{L}}(s), \tag{7}$$

where g_{m1} is the amplifier's transconductance gain and $Z_{\text{L}}(\text{s})$ is the output impedance.

The open loop gain of op-amp is further calculated as

$$\text{Av} = \frac{g_{\text{m1}} \cdot r_{\text{out}}}{1 + s \cdot r_{\text{out}} \cdot \text{C}_{\text{L}}}, \tag{8}$$

where r_{out} is the output impedance of the op-amp and C_{L} is the load capacitance.

For high frequencies, the load capacitance dominates, and hence

$$\text{Av} = \frac{g_{\text{m1}}}{s \cdot C_{\text{L}}}. \tag{9}$$

The input transconductance can be increased by using long-channel transistors and ensuring that the input transistor pair's bias current is significantly larger than the cascode transistor's bias current. This will also result in improvement of bandwidth. To maximize the dc gain of the designed op-amp, it is considered that the current flowing through all the transistors connected to output node is at small levels. This will not only maximize the input transconductance but also output impedance. Maximum amount of bias current through the input differential pair results in large transconductance of the input devices and hence in the improvement of thermal noise performance of OpAmp [7, 31].

In this work, MOSFET-like CNFETs are used for designing the FCOA circuit and due to the similarities between the MOSFET and MOSFET-like CNFET devices in terms of I-V characteristics and the other inherent attributes, design procedure of CNFET-based circuits is similar to CMOS [13, 30–37]. Furthermore, as in CNFET device μn = μp and all of the characteristics of the used CNFETs such as gate length (L = 32 nm), CNT diameters (DCNT = 1.49 nm), and pitch (8 nm), except the width of the CNFETs, are set to be identical, the only parameter here that could affect the gain of the FCOA is the width of CNFETs. In addition, because of the direct relation between the width of a CNFET and the number of its nanotubes [38], the desired widths can be set by adopting proper number of CNTs for each transistor [37].

For simulation purposes, CNFET, SPICE compatible Stanford University 32 nm CNFET model is used [30]. In this study, top-gated undoped semiconducting MOSs like CNFETs with 4 nm thick HfO2, high-k dielectric (k = 16), chirality (19, 0), and fixed diameter at 1.49 nm are used. The number of tubes is calculated using Equation (1) for pitch equals to 8 nm, keeping the diameter constant, and is itemized in Table 1. The designed folded cascode op-amp configuration is further simulated using HSPICE to achieve satisfactory DC performance and further used to calculate various performance metrics such as DC gain (Av0), phase margin (PM), unity gain bandwidth (UGB), common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), slew rate (SR), output swing (OS), and power consumption [6].

3.1. Optimum Choice for Pitch and Diameter of CNFET. The simulations are performed for three different values of pitch 8 nm, 12 nm, and 20 nm for CNFET-based FCOA. Table 2 shows the comparative results at different values of pitch with respect to specifications. The comparative examination of the important parameters of CNFET-FCOA architectures affirms that a noteworthy improvement in performance is achieved in the CNFET-based FCOAs and the gain is highest amongst three for pitch equals to 8 nm. The similar kind of performance is not possible at such

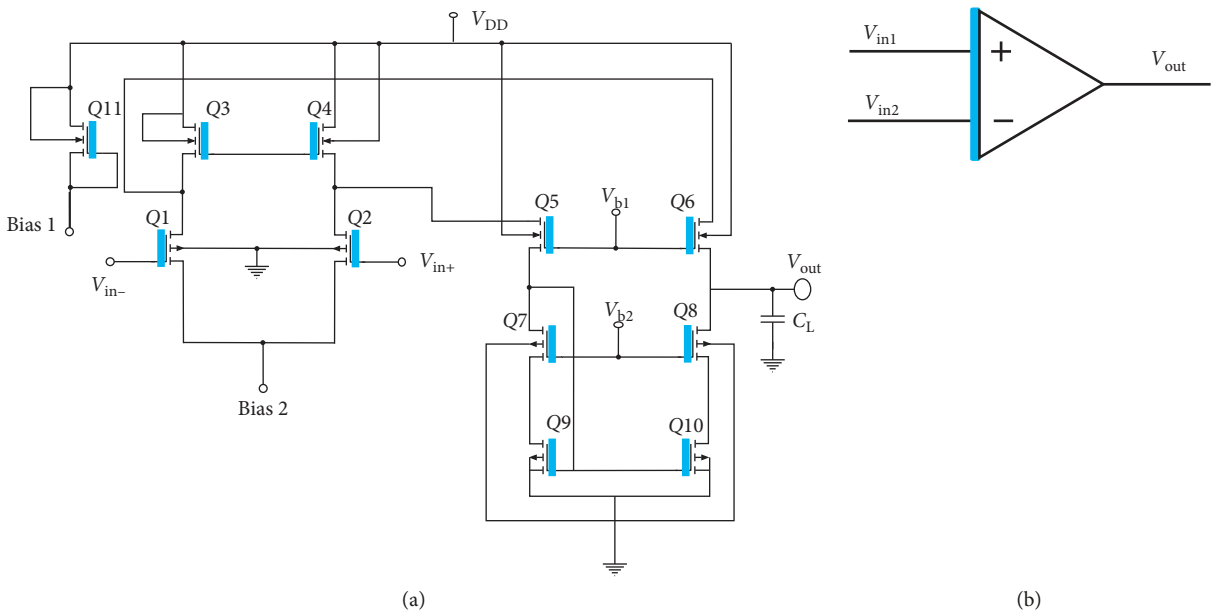


Figure 3: Proposed folded cascode operational amplifier using CNFET. (a) Schematic and (b) symbol.

Table 1: Number of tubes for pitch = 8 nm.

Transistors	Number of tubes
M1	600
M2	600
M3	200
M4	200
M5	100
M6	100
M7	20
M8	20
M9	100
M10	100
M11	200

very deep submicron levels using CMOS due to extreme short-channel effects, lithographic limitations, process variations, leakage current, and source-to-drain tunneling [25, 37–41]. Further CNFET technology can also be easily clubbed with the bulk CMOS technology on a single chip and utilizes the same infrastructure [23, 30, 42].

An investigative result demonstrates that the frequency response of the designed OTA improves with the increase in diameter of the nanotube as shown in Figures 4(a) to 4(c). This is due to the fact that the transconductance goes up with the increase in diameter of the nanotubes. The DC gain decreases with the diameter because the reduction in the output resistance with diameter is more than the rise in its transconductance. This trend is observed because CNFET circuit performance and electrical behaviour directly depend on the CNT diameter. Diameter is the main parameter that affects the on current proportionally in a CNFET apart from barrier height at the S/D contact (or RS/D), chirality, and oxide thickness, but for larger diameters, current tends to saturate due to large screening and scattering effects [14, 24, 25, 33]. Also, the power consumption of an amplifier goes up due to the smaller band gap and higher current drive.

4. CNFET-FCOA-Based Analog Signal Processing Applications

Operational amplifier was formerly aimed to execute different operations on signals such as addition, subtraction, differentiation, integration, and comparison. In the proposed work, the functionality of the CNTFET-FCOA is tested for all such signal processing applications to check the practical usefulness of the proposed CNFET-FCOA at very deep submicron node. All the signal processing circuits are designed and implemented at 32 nm, a nanometer regime where there are certain constraints with CMOS technology due to sternness of nonideal effects.

4.1. CNFET-FCOA-Based Noninverting Amplifier. The op-amp circuitry, comprising voltage divider at inverting node, is called a noninverting amplifier because its voltage gain is positive [30]. This means that the output voltage will follow the input voltage. The period of input and output voltage is same as the phase, only amplitude of output waveforms depends on gain of the op-amp. CNFET-FCOA-based noninverting amplifier is shown in Figure 5(a). The input voltage V_{in} is applied to the noninverting terminal of op-amp. Partial output, i.e., feedback, is given to the inverting input through the feedback resistor R_F, which forms voltage divider network with R_{in1}. For the designed noninverting amplifier, voltage gain is 14. The expression for output voltage is given by using Equation (10) and its waveform is shown in Figure 6(a):

$$V_{out} = V_{in}\left(1 + \left(\frac{R_F}{R_{in1}}\right)\right). \quad (10)$$

Table 2: Comparative results at different values of pitch.

Performance parameter	Design specification	Simulation results		
		Pitch 8 nm	Pitch 12 nm	Pitch 20 nm
Open loop gain (dB)	60	75.2	66.2	60.4
Phase margin (°)	45°	86.6°	86.9°	87.2
Unity gain bandwidth (MHz)	255	530	523	510
Power dissipation (mW)	<0.3	0.323	0.321	0.319
Slew rate (V/μsec)	20	25.05	24.77	24.87
Output swing (V)	1	0.969	0.969	0.969
CMRR (dB)	≥60	106.1	62.63	57.21
PSRR (dB)	≥60	165.2	155.6	149.6
Settling time (ns)	—	5.41	5.33	5.25
Input referred noise voltage (nV/$\sqrt{\text{Hz}}$)	—	0.657	0.659	0.666

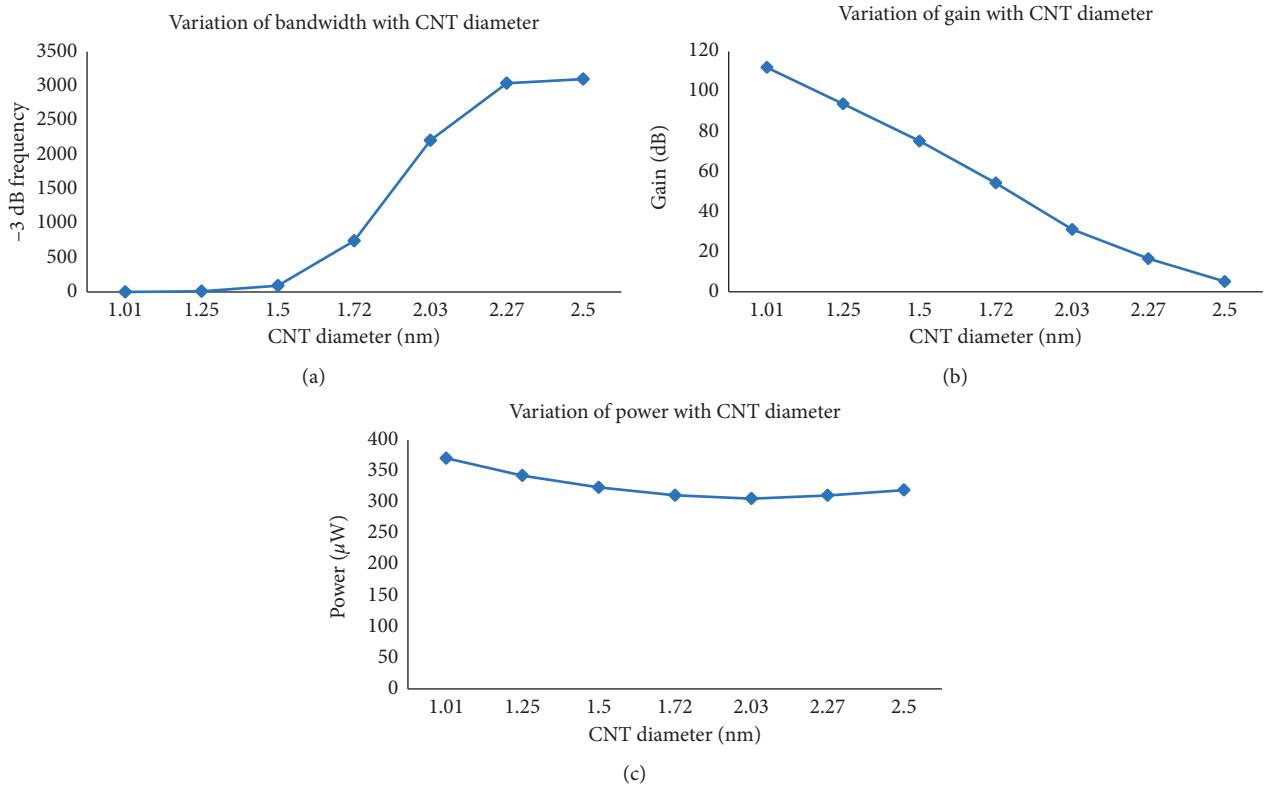
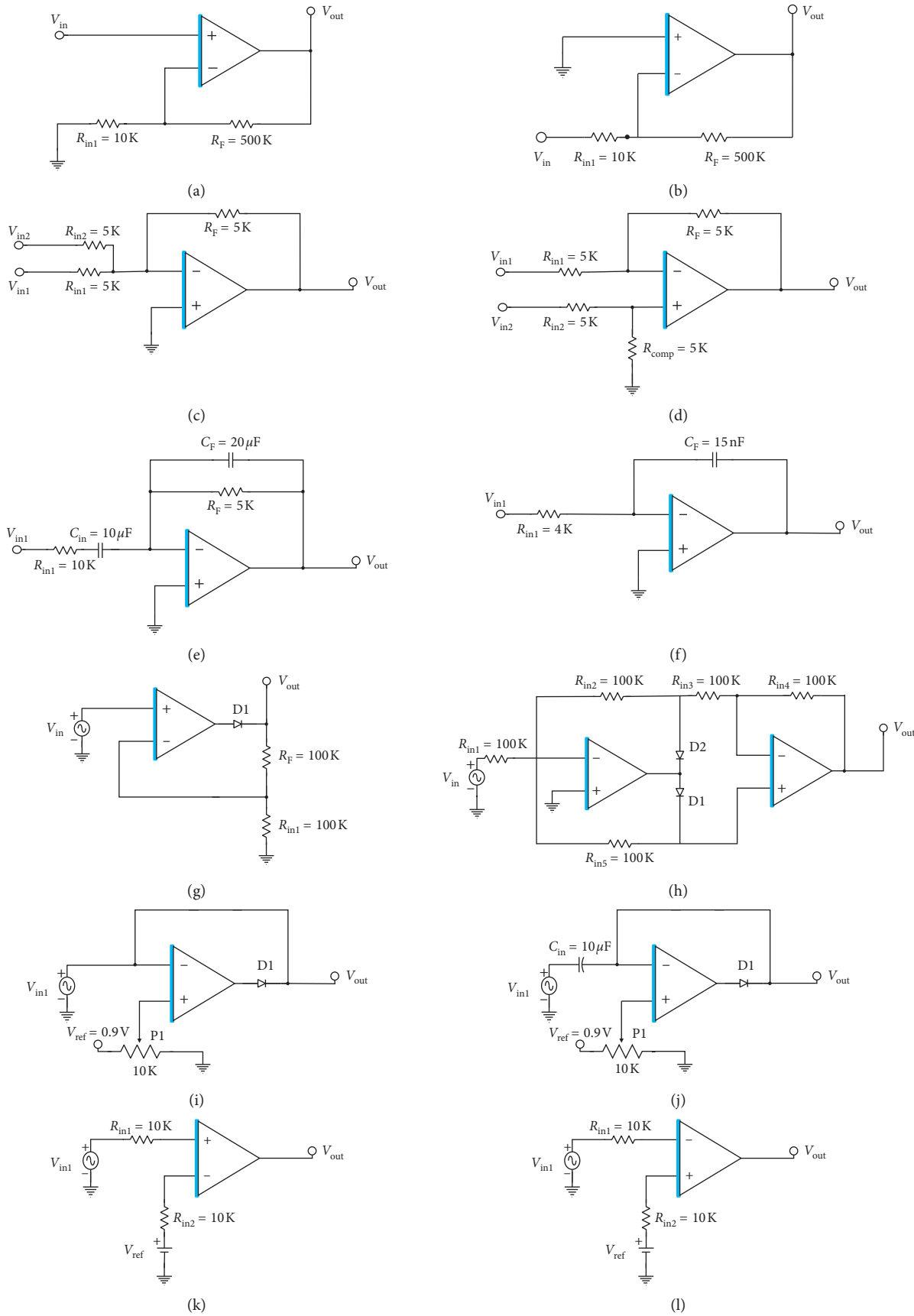


Figure 4: Effect of diameter variation on frequency response and power. (a) Frequency response (bandwidth). (b) Frequency response (open loop gain). (c) Power.

4.2. CNFET-FCOA-Based Inverting Amplifier. As the name suggests, input and output waveforms are out of phase or are having 180° phase shift, i.e., whenever input voltage increases, output voltage decreases and vice-a-versa. The circuit diagram of a CNFET-FCOA-based inverting amplifier is shown in Figure 5(b). The input signal, V_{in}, is applied through resistor R_{in1} to the inverting terminal of the op-amp. Feedback resistor R_F connects the partial output to the noninverting input. Second input of the op-amp is connected to fixed potential, say ground. For the designed inverting amplifier, voltage gain is 14 and the expression for output voltage of the inverting amplifier is as shown by Equation (11) and the resulting waveform is shown in Figure 6(b):

$$V_{out} = -V_{in}\left(\frac{R_F}{R_{in1}}\right). \tag{11}$$

4.3. CNFET-FCOA-Based Summer. As the name suggests, summer means the circuit which adds two signals [30]. Figure 5(c) shows the basic inverting summer which is used to sum two or more signal voltages and at the output produces amplified sum of the two input signal. For the designed non inverting summer, the expression for output voltage is given by Equation (12), and the waveform is as displayed in Figure 6(c):



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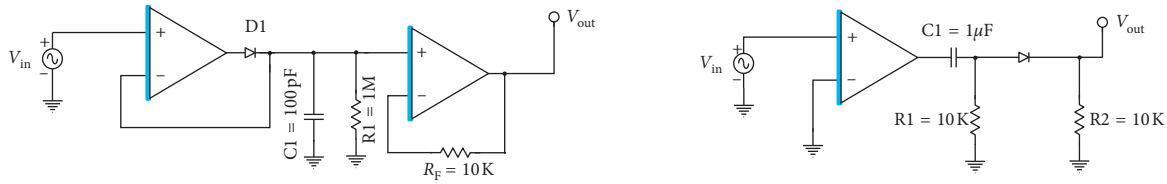
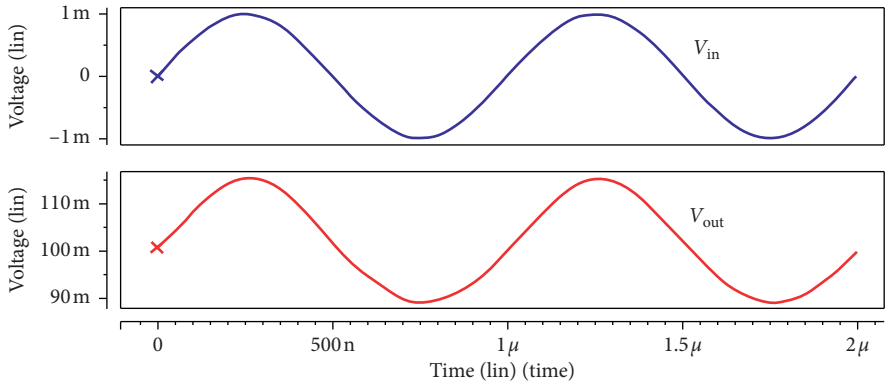
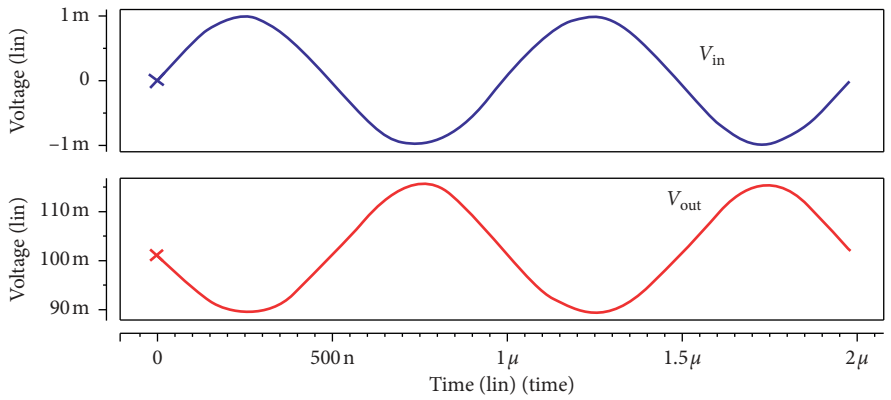


(m) (n)

Figure 5: Analog signal processing applications. (a) Noninverting amplifier. (b) Inverting amplifier. (c) Summer. (d) Subtractor. (e) Differentiator. (f) Integrator. (g) Half-wave rectifier. (h) Full-wave rectifier. (i) Clipper. (j) Clamper. (k) Noninverting comparator. (l) Inverting comparator. (m) Peak detector. (n) Zero crossing detector.



(a)



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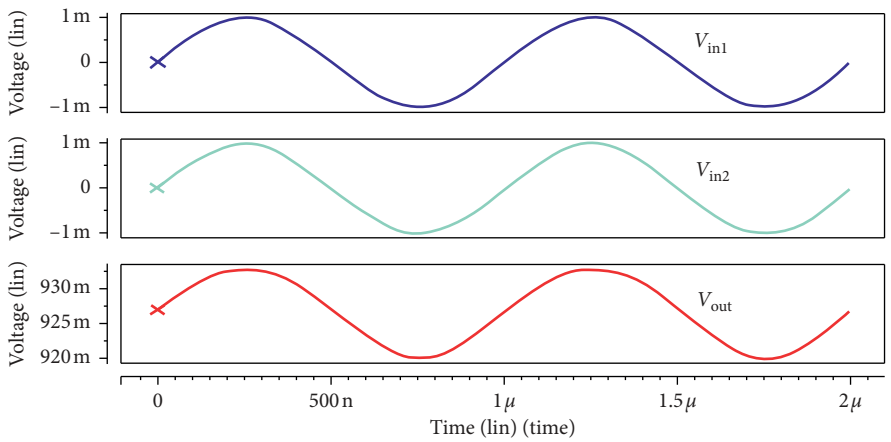

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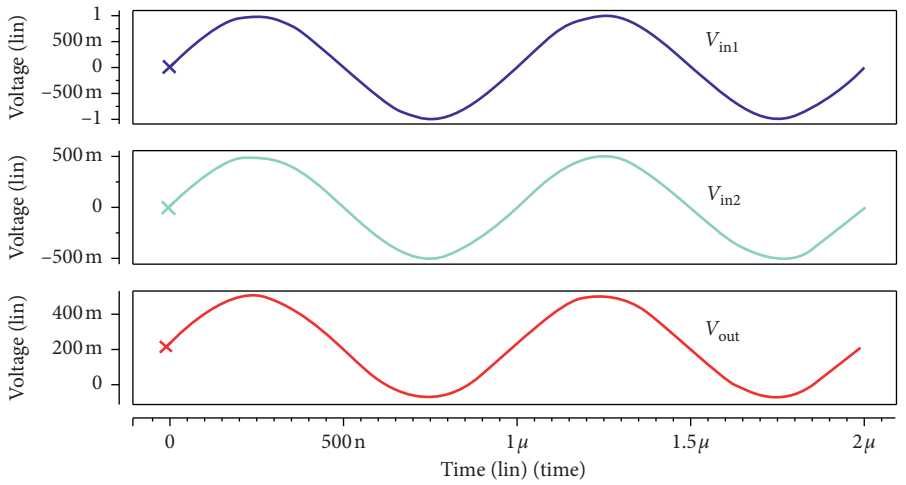

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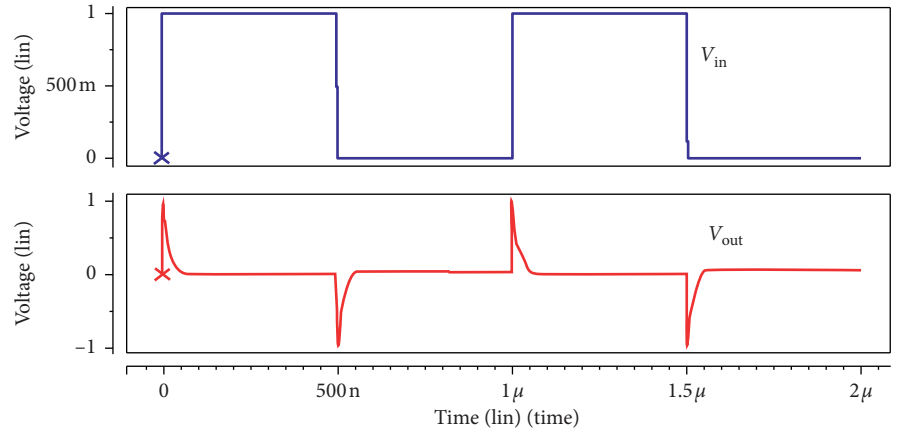

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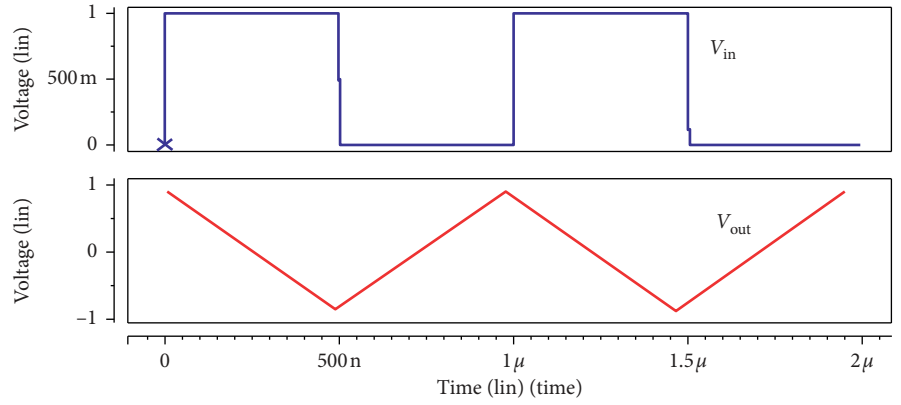

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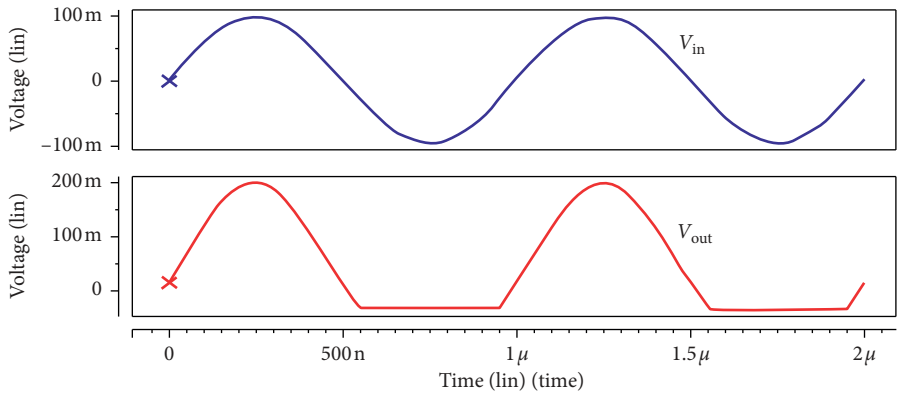

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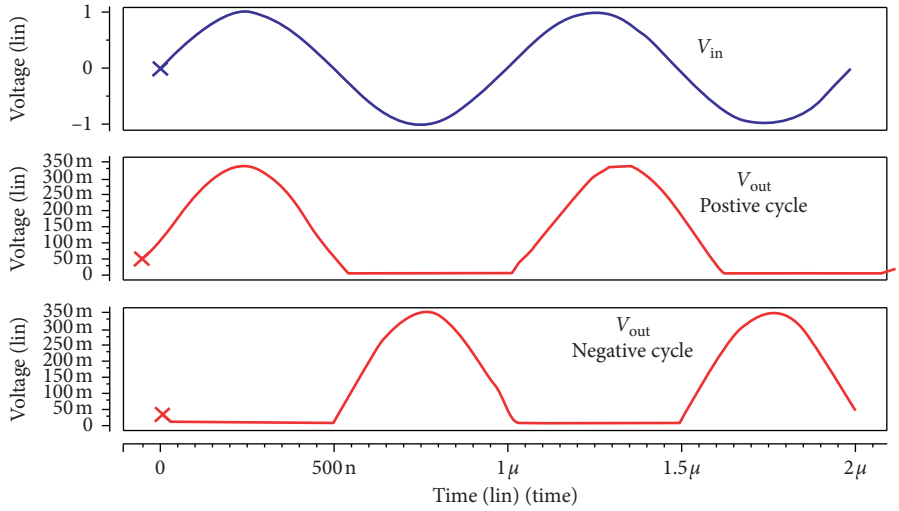

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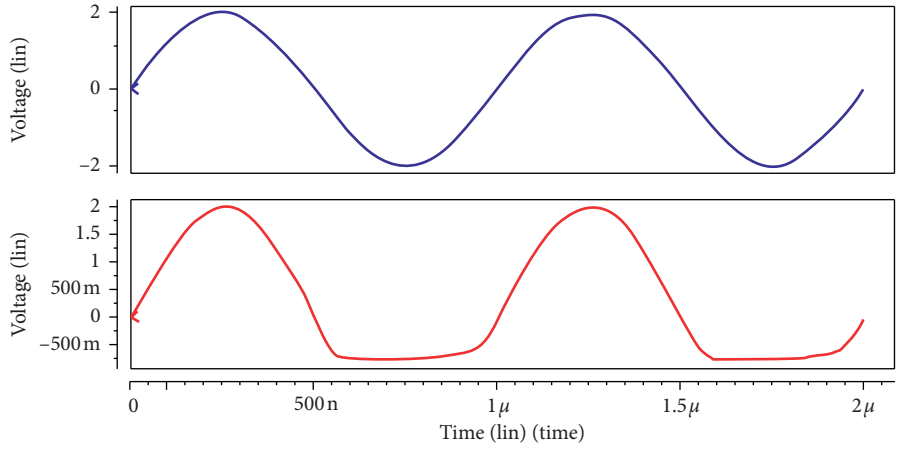

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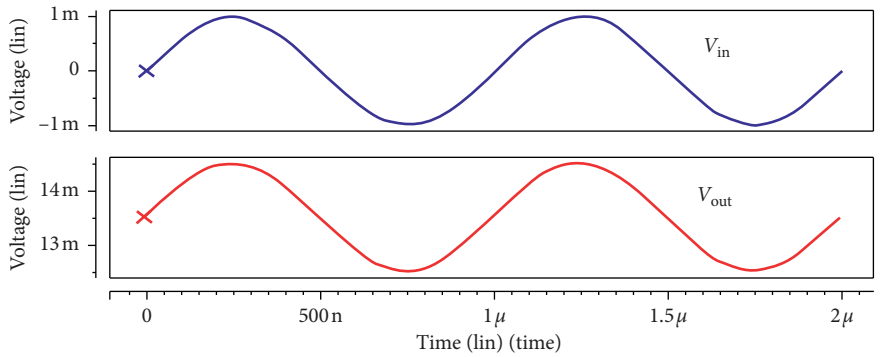

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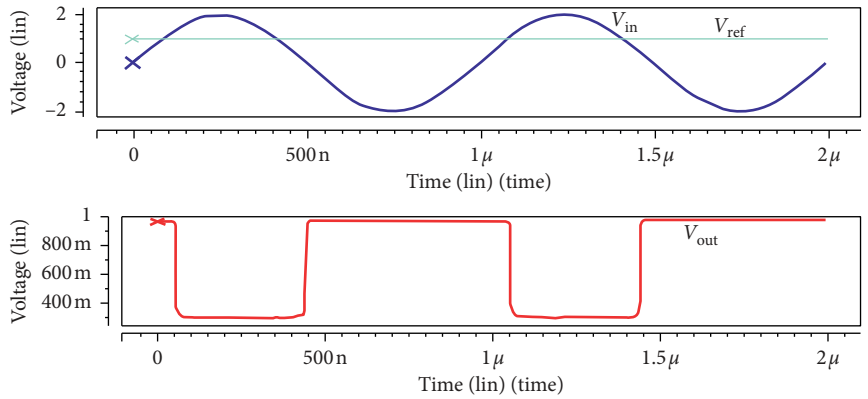
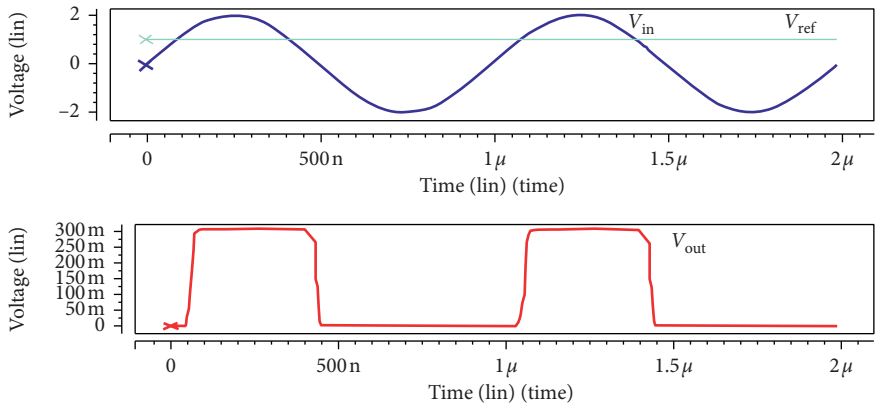
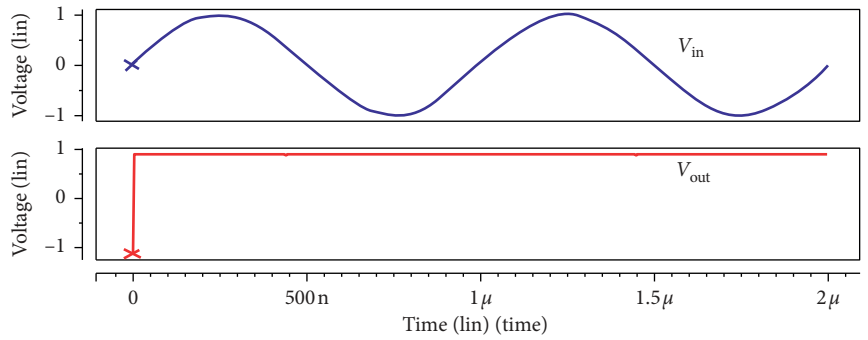


(k)



(l)



(m)

Figure 6: Continued.

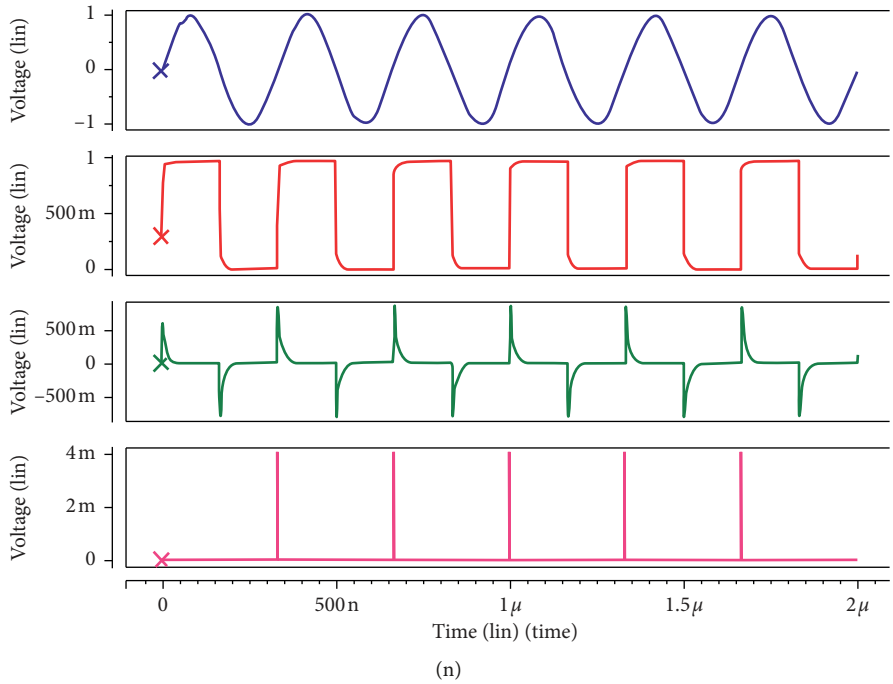


FIGURE 6: Input-output waveforms of different applications. (a) Noninverting amplifier. (b) Inverting amplifier. (c) Summer. (d) Subtractor. (e) Differentiator. (f) Integrator. (g) Half-wave rectifier. (h) Full-wave rectifier. (i) Clipper. (j) Clamper. (k) Inverting comparator. (l) Noninverting comparator. (m) Peak detector. (n) Zero crossing detector.

$$V_{\text{out}} = R_{\text{F}}\left(\frac{V1}{R_{\text{in1}}} + \frac{V2}{R_{\text{in2}}}\right). \tag{12}$$

4.4. CNFET-FCOA-Based Subtractor. A differential amplifier with unity gain can be used to provide an output voltage that is equal to the difference of two input voltages [30]. Such a circuit is called a subtractor and is shown in Figure 5(d). The net output result, as shown in Figure 6(d), is the difference between two input voltages V_{in1} and V_{in2} applied at the inverting and noninverting terminals of the op-amp, respectively [40]. For the designed subtractor, voltage gain is 1, since all the resistors are of same value, and the output voltage of the subtractor is evaluated using the following equation:

$$V_{\text{out}} = V_{\text{in1}} - V_{\text{in2}}. \tag{13}$$

4.5. CNFET-FCOA-Based Differentiator. In differentiator, the output voltage is proportional to the rate of change of its input voltage. Figure 5(e) gives the circuit diagram of a CNFET-FCOA-based differentiator. The circuit consists of input resistor R_{in} in series with capacitor C_{in} and pair of R_{F} and C_{F} in parallel in the feedback path. For the designed differentiator, output voltage is expressed by Equation (14). Figure 6(e) shows the corresponding output of differentiator:

$$V_{\text{out}} = -R_{\text{F}} \cdot C_{\text{in}}\left(\frac{dV_{\text{in}}}{dt}\right). \tag{14}$$

4.6. CNFET-FCOA-Based Integrator. In case of integrator, output voltage is proportional to the integration of its input voltage [30]. The circuit for the integrator can be as same as that of the differentiator, except that the position of the resistor and that of the capacitor is interchanged as shown in Figure 5(f). For the designed integrator, output voltage is expressed as shown in Equation (15). The corresponding input-output waveforms are shown in Figure 6(f):

$$V_{\text{out}} = -\frac{1}{RfC1}\int_{\infty}^{t} V_{\text{in}}\, dt. \tag{15}$$

4.7. CNFET-FCOA-Based Half-Wave Rectifier. Half-wave rectifier (HWR) is a circuit which allows only the positive cycle of input sinusoidal waveform with the help of forward-biased diode to reach at the output. Such a circuit of half-wave rectifier is shown in Figure 5(g). The op-amp output turns out to be positive only during the positive half cycle of the input waveform, which eventually makes the diode D1 forward biased and the positive half cycle waveform appears across the output terminal [30]. In contrast, during the negative half cycle, the op-amp output becomes negative, turning OFF diode D1. This will not allow the negative portion of input to appear across the output. The overall outcome is impeccable half-wave rectification, as epitomized in Figure 6(g).

4.8. CNFET-FCOA Full-Wave Rectifier. In contrast to half-wave rectifier, full-wave rectifier allows positive as well as negative half cycles of input waveforms to reach at the

output one after the other sequentially. Such a full-wave rectifier circuit is shown in Figure 5(h), which is actually the combination of two half-wave rectifier circuits. This is achieved using two different op-amps A1, A2 and diodes D1, D2. The op-amp A1 output turns out to be positive only during the positive half cycle of the input waveform. V′ becomes negative which eventually turns ON the diode D1 [41]. The voltage at the inverting terminal of A2 appears at the output, which is equal to the input, due to the virtual ground at the two input terminals of op-amp A2. Consider now the negative cycle of the input waveform. In this case, the V′ will be positive, making diode D1 OFF and D2 ON. Due to the virtual ground at the inverting input of op-amp A1, V2 = V1 = V [43]. This causes output voltage to be equal to the negative of the input voltage at A1 and thus positive. Therefore, outputs during two half cycles are same and full-wave-rectified output voltage is obtained as shown in Figure 6(h).

4.9. CNFET-FCOA-Based Clipper. As the name suggests, a clipper is a circuit that can remove certain portions of the input waveform near the positive or negative peaks, i.e., it avoids the output from going beyond a predetermined voltage level without adversely affecting the residual part of the input waveform. If such a circuit is implemented using op-amp, a diode is used at the output of op-amp, to remove off some portion of the input signal. CNFET-FCOA-based positive clipper is shown in Figure 5(i). This type of circuit confiscates negative peak of the input signal. The value of reference voltage V_{ref} decides the clipping portion. The positive input gets grounded initially when the V_{ref} is zero. Whenever input V_{in} is positive, the output will follow the input V_{in}, since the op-amp output becomes positive, turning ON the diode. The op-amp output will go negative during negative half cycle of the input. In this case, the final output V_o will follow the negative half cycle of the input till the input voltage is greater than the reference voltage only. Hence the portion of the negative half cycle will be clipped for which input voltage becomes less than the reference voltage. In order to adjust the clipping level, V_{ref} needs to be adjusted as per requirement.

4.10. CNFET-FCOA-Based Clamper. By using clamper circuits, the output is shifted up or down to a preferred DC level, i.e., a predetermined DC level is added to the input voltage. A variable DC level CNFET-FCOA-based clamper circuit is presented in Figure 5(j). This is a positive clamper because the input waveform is clamped at $+V_{ref}$ [41]. In this case, both AC and DC input voltages need to be applied and output of the clamper is a net result of AC and DC input voltages applied to the inverting terminal, and a potentiometer is connected to noninverting input terminals to vary V_{ref}. Initially, ponder $+V_{ref}$ at the noninverting input. The output voltage (V_o) will also be positive, which turns ON the diode D1 completing the feedback loop. The op-amp then works as a voltage follower, since capacitor C1 blocks DC voltage and V_o becomes equal to V_{ref}. Now, consider the voltage V_{in} at the inverting input. During its negative half cycle, capacitor C1 will charge to the negative peak value of the voltage (V_P) since diode D1 starts conducting. The peak voltage (V_P) across the capacitor acquired during the negative half cycle is retained because diode D1 turns OFF during the positive half cycle of V_{in} [40]. The output peak voltage V_o becomes equal to $2V_P$, since this voltage V_P is in series with the positive peak voltage V_P. Thus, the net output is $V_o = V_{ref} + V_P$; so, the negative peak of $2V_P$ is at Vref. The input and output waveforms are shown in Figure 6(j).

4.11. CNFET-FCOA-Based Comparator. As the name suggests, a comparator is a circuit that compares input signal at one terminal of op-amp with a known reference voltage at the other input of op-amp. Figure 5(k) shows CNFET-FCOA-based comparator. Consider a fixed reference voltage V_{ref} of +1V at the inverting input and the other time-varying signal V_{in} is applied to the noninverting input. This type of comparator is called as noninverting comparator. When input voltage V_{in} is greater than reference V_{ref}, output voltage V_o reaches to $+V_{sat}$ and when V_{in} becomes less than reference, V_o changes towards $-V_{sat}$. Thus, V_o varies from one level to another level whenever input increases or decreases with respect to V_{ref} as shown in Figures 6(k) and 6(l). Hence, this circuit is also termed as "voltage level indicator." Such inverting, noninverting comparators are needed to interface analog and digital blocks in mixed signal applications.

4.12. CNFET-FCOA-Based Peak Detector. As the name suggests, a peak detector is a circuit which detects the peak value of applied input signal [41, 43] as shown in Figure 5(m). This circuit detects the positive peak of the input signal. CNFET-FCOA-based peak detector consists of a series connection of a diode and a capacitor. The capacitor C1 gets charged to the peak value V_{pp} of the input voltage, whenever diode D1 becomes forward biased during every positive half cycle of the input. On the contrary, the charge/voltage across capacitor is retained during every negative half cycle of the input, since the diode D1 is nonconducting and the only discharge path for C1 is through the output terminal V_o [41, 43]. Thus, the capacitor retains the peak value even as the waveform drops to zero.

4.13. CNFET-FCOA-Based Zero Crossing Detector. As the name suggests, a zero crossing detector or ZCD is a circuit used to detect a zero crossing condition of input sinusoidal waveform during transition from positive to negative and vice-a-versa. The circuit is similar to the comparator except that the reference voltage is fixed and its value is permanently zero. Figure 5(n) shows inverting comparator with input as sinusoidal waveform. The corresponding input-output waveforms are shown in Figure 6(n).

Output of the ZCD, Vo, will be at positive saturation voltage $+V_{sat}$ for the values of input waveform greater than zero and will be at negative saturation voltage $-V_{sat}$ when input signal amplitude is less than zero. Every time when the output of op-amp changes from $+V_{sat}$ to $-V_{sat}$, the capacitor

C charges to $+V_{sat}$ and if the output of op-amp transits from $-V_{sat}$ to $+V_{sat}$, capacitor discharges through R1 to $-V_{sat}$. Whenever the square wave crosses zero voltage, the arrangement of C1 and R1 generates an output comprising of peaks at that time interval. The diode is used to remove the peaks at the zero crossings whenever input voltage crosses zero voltage in increasing direction.

The resulting waveforms of all the above applications are shown in Figure 6.

5. Conclusions

In this work, we designed and simulated folded cascode operational amplifiers (FCOA) using promising CNFET technology at 32 nm, a very deep submicron technology node, at 1 V power supply voltage. The relative exploration has discovered that the CNFET-based FCOAs have beaten the CMOS-based FCOAs extensively in the nanometer regime. The conventional CMOS technology is unable to produce significant gain due to the stringent nonideal effect in nanometer regime. Further, the stability analysis have revealed the CNTFET-based FCOA to be exceedingly stable.

The novel CNFET-FCOA is further used to develop analog signal processing circuits such as noninverting amplifier, inverting amplifier, summer, subtractor, differentiator, integrator, half-wave rectifier, full-wave rectifier, clipper, clamper, comparator, peak detector, and zero crossing detector. All these circuits are successfully implemented and are found considerably competent than that of conventional CMOS-based circuits in nanoscale regime. It has also been proved from simulation results that CNFET is a promising nanodevice especially for low-power analog circuit applications at very deep submicron technology nodes.

Data Availability

Any data and information used to support the findings of this study will be provided upon request to the corresponding author.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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References

[1] The International technology Roadmap for semiconductors: semiconductor industry association," February 2013, http://www.itrs.net/.

[2] F. Usmani and M. Hasan, "Design and parametric analysis of 32 nm opamp in CMOS and CNFET technologies for optimum performance," in *Proceedings of the Argentine School of Micro-Nanoelectronics, Technology and Applications*, pp. 87–92, San Carlos de Bariloche, Argentina, 2009.

[3] F. Rahman, "Performance evaluation of a 32-nm CNT-OPAMP: design, characteristic optimization and comparison with CMOS technology," in *Proceedings of 14th International Conference on Computer and Information Technology (ICCIT, 2011)*, Dhaka, Bangladesh, December 2011.

[4] M. A. Kafeel, M. Hasan, M. Shah Alam, A. Kumar, S. Prasad, and A. Islam, "Performance evaluation of CNFET based operational amplifier at technology node beyond 45-nm," in *Proceedings of Annual IEEE India Conference, INDICON*, Mumbai, India, December 2013.

[5] V. Sridevi and T. Jayanthi, "Determination of CNTFET OPAMP parameters," *National Journal on Electronics Sciences and Systems*, vol. 3, no. 2, pp. 56–62, 2012.

[6] P. A. Gowri Sankar and K. Udhaya kumar, "Design and analysis of two stage operational amplifier based on emerging sub-32 nm technology," in *Proceedings International Conference on Advanced Nanomaterials and Emerging Engineering Technologies*, pp. 587–591, Chennai, India, July 2013.

[7] V. Bendre, A. K. Kureshi, and S. Waykole, "A low power, high swing and robust folded cascode amplifier at deep submicron technology," in *Proceedings of 3rd International Conference on Information and Communication Technology for Competitive Strategies*, Udaipur, India, December 2017.

[8] S. K. Sinha and S. Chaudhury, "Comparative study of leakage power in CNTFET over MOSFET device," *Journal of Semiconductors*, vol. 35, no. 11, article 114002, 2014.

[9] J. Deng and H.-S. P. Wong, "A circuit-compatible SPICE model for enhancement mode carbon nanotube field effect transistors," in *Proceedings of International Conference Simulation of Semiconductor Processes and Devices*, pp. 166–169, Monterey, CA, USA, September 2006.

[10] G. Cho, F. Lombardi, and Y.-B. Kim, "Modelling a CNTFET with undeposited CNT defects," in *Proceedings of IEEE 25th International Symposium on Defect and Fault Tolerance in VLSI Systems*, Kyoto, Japan, October 2010.

[11] B. Young Kim, "A novel design methodology to optimize the speed and power of the CNTFET circuits," in *Proceedings of 52nd IEEE International Midwest Symposium on Circuit sand Systems*, Cancun, Mexico, August 2009.

[12] Y.-B. Kim, "Integrated circuit design based on carbon nanotube field effect transistor," *Transactions on Electrical and Electronic Materials*, vol. 12, no. 5, pp. 175–188, 2011.

[13] J. Deng and H. S. P. Wong, "A compact SPICE model for carbon nanotube field effect transistors including nonidealities and its application—Part II: full device model and circuit performance benchmarking," *IEEE Transactions Electron Devices*, vol. 54, no. 12, pp. 3195–3205, 2007.

[14] J. Guo, A. Javey, H. Dai, S. Datta, and M. Lundstrom, *Predicted Performance Advantages of Carbon Nanotube Transistors with Doped Nanotubes as Source/Drain*, Condensed Matter 0309039, 2003.

[15] A. Javey, R. Tu, D. B. Farmer, J. Guo, R. G. Gordon, and H. Dai, "High performance n-type carbon nanotube field-effect

transistors with chemically doped contacts," *Nano Letters*, vol. 5, no. 2, pp. 345–348, 2005.

[16] G. Cho, Y.-B. Kim, F. Lombardi, and M. Choi, "Performance evaluation of CNFET-based logic gates," in *Proceedings of IEEE Instrumentation and Measurement Technology Conference*, Singapore, May 2009.

[17] Z. Yao, C. L. Kane, and C. Dekker, "High-field electrical transport in single-wall carbon nanotube," *Physical Review Letters*, vol. 84, no. 13, pp. 2941–2944, 2000.

[18] M. S. Fuhrer, B. M. Kim, T. Dkop, and T. Brintlinger, "High-mobility nanotube transistor memory," *Nano Letters*, vol. 2, no. 7, pp. 755–759, 2002.

[19] P. L. McEuen, M. S. Fuhrer, and H. Park, "Single-walled carbon nanotube electronic," *IEEE Transactions on Nanotechnology*, vol. 1, no. 1, pp. 78–85, 2002.

[20] G. Pennington and N. Goldsman, "Semiclassical transport and phonon scattering of electrons in semiconducting carbon nanotubes," *Physical Review B*, vol. 68, no. 4, 2003.

[21] B. Q. Wei, R. Vajtai, and P. M. Ajayan, "Reliability and current carrying capability of carbon nanotube," *Applied Physics Letters*, vol. 79, no. 8, pp. 1172–1174, 2001.

[22] P. Dwivedi, K. Kumar, and A. Islam, "Comparative study of subthreshold leakage in CNFET and MOSFET @ 32-nm technology node," in *Proceedings of International Conference on Microelectronics, Computing and Communications (MicroCom)*, Durgapur, India, January 2016.

[23] F. A. Usmani and M. Hasan, "Carbon nanotube field effect transistors for high performance analog applications: an optimum design approach," *Microelectronics Journal*, vol. 41, pp. 395–402, 2010.

[24] D. Yang, L. Wang, Q. Zhao, and S. Li, "Fabrication of single-walled carbon nanotubes (SWNTs) field-effect transistor (FET) biosensor," in *Proceedings of 3rd International Conference on Biomedical Engineering and Informatics*, Dalian, China, October 2010.

[25] J. Zheng, Q. Zhang, X. He, M. Gao, X. Ma, and G. Li, "Nanocomposites of carbon nanotube (CNTs)/CuO with high sensitivity to organic volatiles at room temperature," *Procedia Engineering*, vol. 36, pp. 235–245, 2012.

[26] S. A. Loan, M. Nizamuddin, H. Shabir et al., "Carbon nanotube based operational transconductance amplifier: a simulation study," in *Transactions on Engineering Technologies*, G. C. Yang, S. I. Ao, X. Huang, and O. Castillo, Eds., Springer, Dordrecht, Netherlands, 2015.

[27] M. Nizamuddin, S. A. Loan, A. R. Alamoud, and S. A. Abbassi, "Design, simulation and comparative analysis of CNT based cascode operational transconductance amplifiers," *Nanotechnology*, vol. 26, no. 39, article 395201, 2015.

[28] A. Imran, M. Hasan, S. D. Pable, and M. W. Akram, "High performance optimized CNFET based current conveyor at 32 nm technology node," in *Proceedings of International Conference on Computer and Communication Technology, ICCCT*, Allahabad, India, September 2010.

[29] S. L. Murotiya and A. Gupta, "CNTFET based design of content addressable memory cells," in *Proceedings of 4th International Conference on Computer and Communication Technology, ICCCT*, Piscataway, NJ, USA, September 2013.

[30] P. A. G. Sankar and K. Udhayakumar, "A novel carbon nanotube field effect transistor based arithmetic computing circuit for low-power analog signal processing application," *Procedia Technology*, vol. 12, no. 7, pp. 154–162, 2014.

[31] L. Stoica, V. Solomko, T. Baumheinrich et al., "Design of a frequency signal conditioning unit applied to rotating systems in high temperature aero engine control," in *Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS*, Lisbon, Portugal, May 2015.

[32] J. S. Ajit, Y.-B. Kim, and M. Choi, "Performance assessment of analog circuits with carbon nanotube FET (CNFET)," in *Proceedings of 20th Great Lakes Symposium on VLSI*, pp. 163–166, Providence, RI, USA, May 2010.

[33] A. Balijepalli, S. Sinha, and Y. Cao, "Compact, modeling of carbon nanotube transistor for early stage process-design exploration," in *Proceedings of International Symposium on Low Power Electronics and Design*, pp. 2–7, New York, NY, USA, August 2007.

[34] T. J. Kazmierski, D. Zhou, and B. M. Al-Hashimi, "HSPICE implementation of a numerically efficient model of CNT transistor," in *Proceedings Forum on Specification and Design Languages*, pp. 1–5, Sophia Antipolis, France, September 2009.

[35] M. H. Moaiyeri, R. Chavoshisani, A. Jalali, K. Navi, and O. Hashemipour, "High-performance mixed-mode universal min-max circuits for nanotechnology," *Circuits, Systems, and Signal Processing*, vol. 31, no. 2, pp. 465–488, 2012.

[36] M. H. Moaiyeri, Z. Hajmohammadi, M. Rezaei Khezeli, and J. Ali, "Effective reduction in crosstalk effects in quaternary integrated circuits using mixed carbon nanotube bundle interconnects," *ECS Journal of Solid State Science and Technology*, vol. 7, no. 5, pp. M69–M76, 2018.

[37] S. Lin, Y.-B. Kim, F. Lombardi, and Y. J. Lee, "A new SRAM cell design using CNTFETs," in *Proceedings of IEEE International SoC Design Conference*, pp. 168–171, Busan, South Korea, November 2008.

[38] K. Abdelhalim, L. MacEachern, and S. Mahmoud, "A nanowatt successive approximation ADC with offset correction for implantable sensor applications," in *Proceedings of IEEE International Symposium on Circuits and Systems*, pp. 2351–2354, New Orleans, LA, USA, May 2007.

[39] R. Chavoshisani, M. H. Moaiyeri, and O. Hashemipour, "A high-performance low-voltage current-mode min/max circuit," *COMPEL International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, vol. 34, no. 4, pp. 1172–1183, 2015.

[40] D. Akinwande, S. Yasuda, B. Paul, S. Fujita, G. Close, and H.-S. P. Wong, "Monolithic integration of CMOS VLSI and carbon nanotubes for hybrid nanotechnology applications," *IEEE Transactions on Nanotechnology*, vol. 7, no. 5, pp. 636–639, 2008.

[41] P. A. Gowrisankar and K. Udhayakumar, "A novel carbon nanotube field effect transistor based analog signal processing circuits for low-power communication systems," in *Emerging Trends in Computing and Communication. Lecture Notes in Electrical Engineering*, S. Sengupta, K. Das, and G. Khan, Eds., vol. 298, Springer, New Delhi, India, 2014.

[42] D. Sethi, M. Kaur, and G. Singh, "Design and performance analysis of a CNFET based TCAM cell with dual-chirality selection," *Journal of Computational Electronics*, vol. 16, no. 1, 2017.

[43] S. Raj, D. R. Bhaskar, V. K. Singh, and R. K. Sharma, "Basic sinusoidal oscillators and waveform generators using IC building blocks," in *Sinusoidal Oscillators and Waveform Generators Using Modern Electronic Circuit Building Blocks*, Springer Nature, Cham, Switzerland, 2016.