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DESIGN OF EFFICIENT COPLANAR 1-BIT COMPARATOR CIRCUIT IN QCA TECHNOLOGY

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Abstract. *QCA technology is an emerging and promising technology for implementation of digital circuits in nano-scale. The comparator circuits play an important role in digital circuits. In this work, a new and efficient coplanar 1-bit comparator circuit is proposed and evaluated in the QCA technology. The designed coplanar 1-bit QCA comparator circuit is constructed based on majority gate, XNOR gate and inverter gate that are designed carefully. The functionality of the designed coplanar 1-bit QCA comparator circuit is verified by using QCADesigner version 2.0.3. The obtained results indicate that the designed 1-bit QCA comparator circuit requires 0.03 μm^2 area and 38 QCA cells. It also has 0.5 clock cycles delay. The comparison demonstrates that the designed QCA comparator circuit provides improvements in comparison with other QCA comparator circuits in terms of effective area, cell count, and delay as well as cost.*

Key words: *comparator, quantum-dot cellular automata, high-performance design, coplanar circuit*

1. INTRODUCTION

Two important issues in the VLSI design are scaling and reducing the computation time. The Quantum-dot Cellular Automata (QCA) technology is an emerging and promising technology to these issues at nano-scale [1]. The basic element in this technology is a square cell that has two free electrons in four dots [1-14]. The QCA cell is a building block for constructing QCA gates [1-14]. There are three basic gates in this technology: inverter gate, majority (M) gate, and XOR gate [3-4]. These gates are building blocks for constructing the logic circuits such as QCA multiplexers [5, 7], QCA full address [1-3, 6, 8] and QCA comparators [9-12, 15-18].

On the other hand, the comparator circuits play an important role in digital circuits such as micro controllers [6, 12, 15-18]. Thus, the implementation of high-performance comparator circuits has a great deal of attention, and a lot of effort [10-12, 15-18] has been invested in performance improvement in the QCA comparator circuits. Das and De [10] have presented a 1-bit QCA comparator that requires 0.343 μm^2 area and 319 QCA

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cells. Alshafi and Bahar [11] have presented a 1-bit QCA comparator, which requires 0.182 μm^2 area and 117 QCA cells. Shinha et al. [12] have proposed two QCA comparator circuits that require 40 and 37 QCA cells and 0.032 and 0.028 μm^2 area, respectively. Ghosh et al. [16] have presented a 1-bit QCA comparator circuit that requires 0.06 μm^2 area and 73 QCA cells. Akter et al. [17] have presented a 1-bit QCA comparator circuit, which requires 0.11 μm^2 area and 87 QCA cells. Bhoi et al. [17] have presented a 1-bit QCA comparator circuit that requires 0.23 μm^2 area and 220 QCA cells.

This study proposes an efficient coplanar 1-bit QCA comparator circuit. The designed QCA comparator is based on majority, XOR and inverter gates. The accuracy of the designed circuit functionality is demonstrated by using QCADesigner version 2.0.3. The simulation results show that the designed coplanar 1-bit QCA comparator circuit provides improvements compared with other 1-bit QCA comparator circuits in terms of cell count, area, delay time and cost.

The rest of this study is unified as follows: section 2 provides a review for QCA technology. In section 3, the designed QCA comparator circuit is presented. The results and comparison of the designed QCA comparator circuit are provided in section 4. The conclusion is presented in section 5.

2. BACKGROUND

2.1. QCA cell

Figure 1 shows the basic QCA cell and its possible stats. We can consider each QCA cell as a square including four quantum dots and a pair of electrons [1, 5]. Electrons can be located at diagonally opposite locations due to the Coulomb interaction between electrons in each cell. There are two different forms in each cell that their polarizations are specified as -1 and +1. These polarizations denote the binary values of 0 and 1, respectively [1, 5].

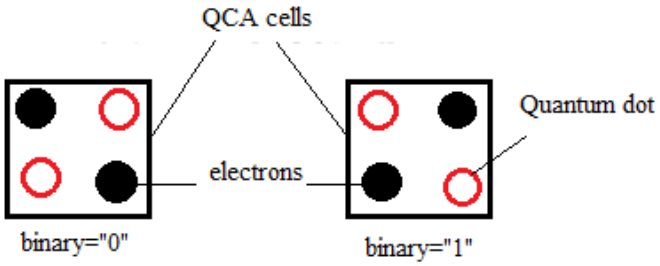


Fig. 1. The possible stats for the QCA cell [5]

2.2. QCA gates

There are three fundamental gates in this technology: inverter, majority, and XOR gates, which are used to construct the circuits in this technology [11, 13, 19]. Figure 2 shows these QCA gates [3, 13].

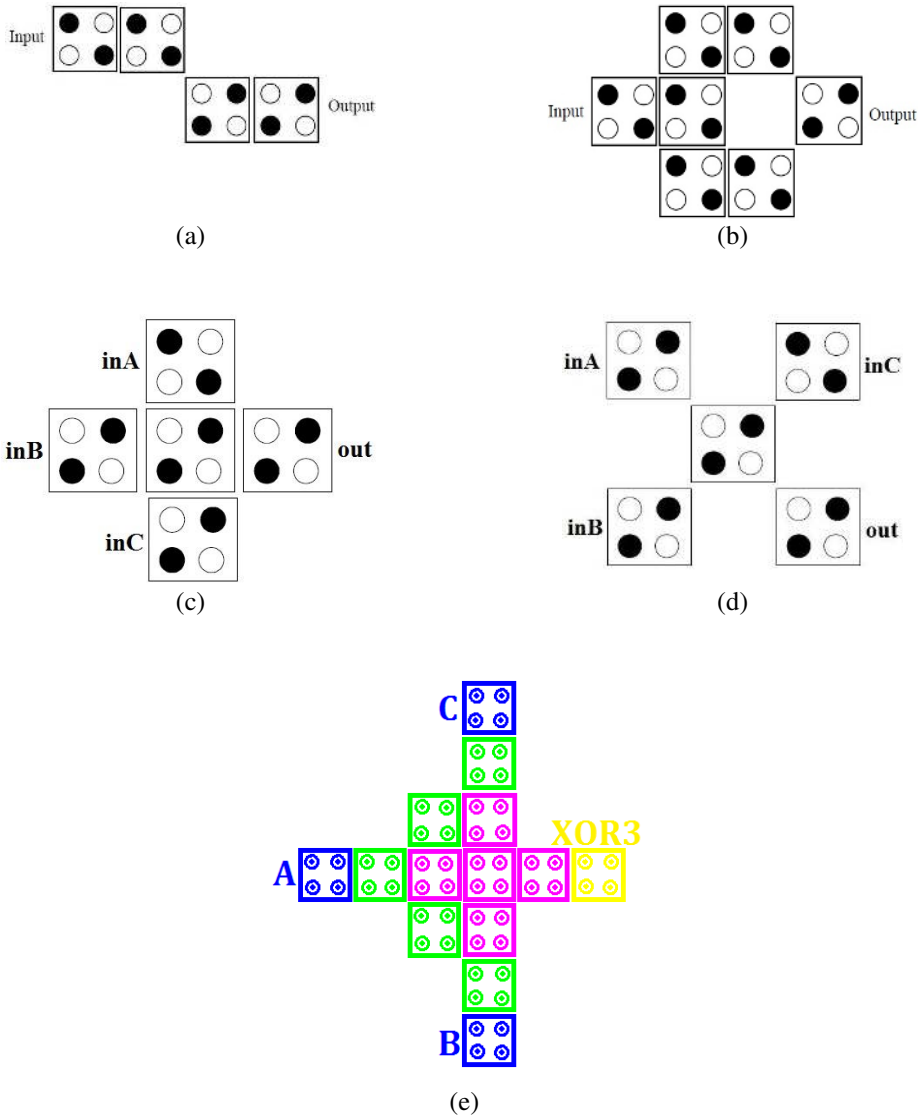


Fig. 2 QCA gates**:** (a) Corner inverter, (b) Robust inverter, (c) Original Majority Gate (OMG), (d) Rotated Majority Gate (RMG), (e) XOR gate [11, 3, 13, 19]

In Figure 2(a) and figure 2(b), the inverted polarization value of the input in each inverter is shown as the output. In Figure 2 (c) and figure 2 (d), two kinds of QCA three-input majority gates are shown. Figure 2 (e) shows three inputs QCA XOR gate [6, 13].

2.3. QCA comparator

Comparator circuits play an important role in digital circuits [9-12, 15-18]. This circuit compares their two inputs. Suppose A and B are two inputs of the comparator circuit, the outputs of this circuit are defined as follows [15]:

$$\begin{aligned} &\text{Output } (A<B) = \overline{A}.B \text{ where } A<B \\ &\text{Output } (A=B) = \overline{A \oplus B} \text{ where } A=B \\ &\text{Output } (A>B) = A.\overline{B} \text{ where } A>B \end{aligned} \quad (1)$$

For implementation of comparator circuit in the QCA technology, equation (1) is reformulated as follows [15]:

$$\begin{aligned} &\text{Output } (A<B) = M(\overline{A}.B, 0) \text{ where } A<B \\ &\text{Output } (A=B) = \text{XNOR}(A, B) \text{ where } A=B \\ &\text{Output } (A>B) = M(A, \overline{B}, 0) \text{ where } A>B \end{aligned} \quad (2)$$

2.4. Related works

Das and De [10] have developed a QCA comparator circuit by combining the Feynman and TR gates functional property, which is shown in figure 3.

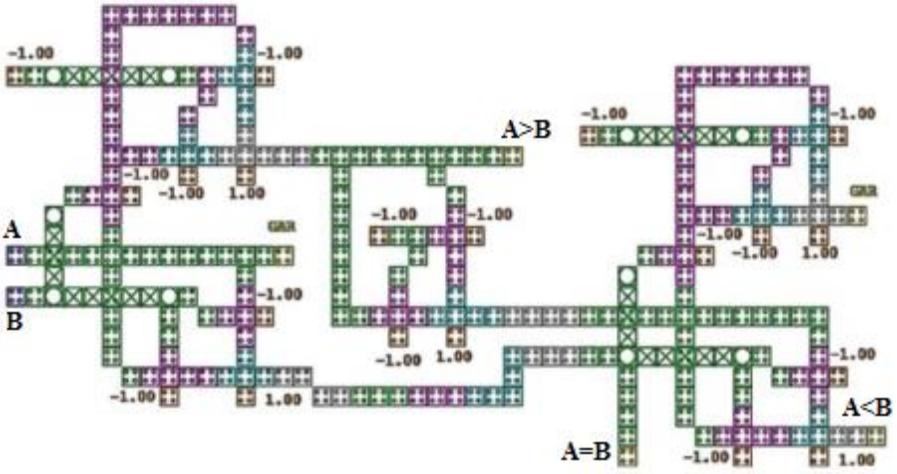


Fig. 3. The utilized QCA comparator circuit in [10]

This QCA comparator circuit requires 0.343 μm^2 area and 319 QCA cells.

Al-Shafi1 et al. [11] have developed a QCA comparator circuit without wire-crossing, which is shown in figure 4.

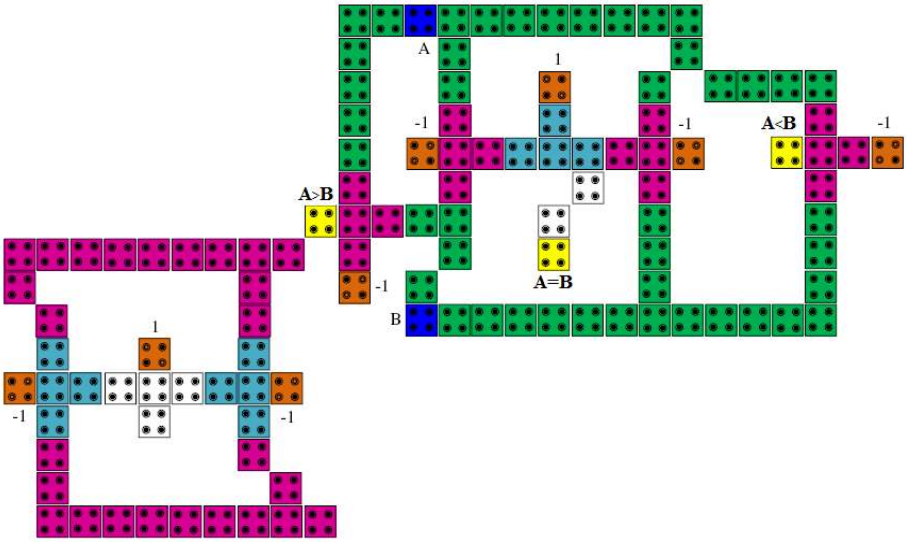


Fig. 4. The utilized QCA comparator circuit in [11]

This QCA comparator circuit requires 0.182 μm^2 area and 117 QCA cells.

Shinha Roy et al. [12] have developed a QCA comparator circuit based on layerd-T OR and AND gates, which is shown in figure 5.

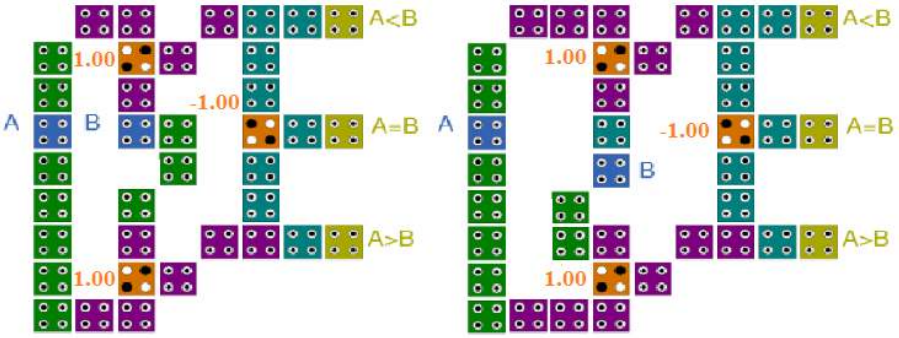


Fig. 5. The utilized QCA comparator circuits in [12]

This QCA multilayer comparator circuit requires 0.03 μm^2 area and 37 QCA cells.

Ghosh et al. [16] have developed a QCA comparator circuit, which is shown in figure 6.

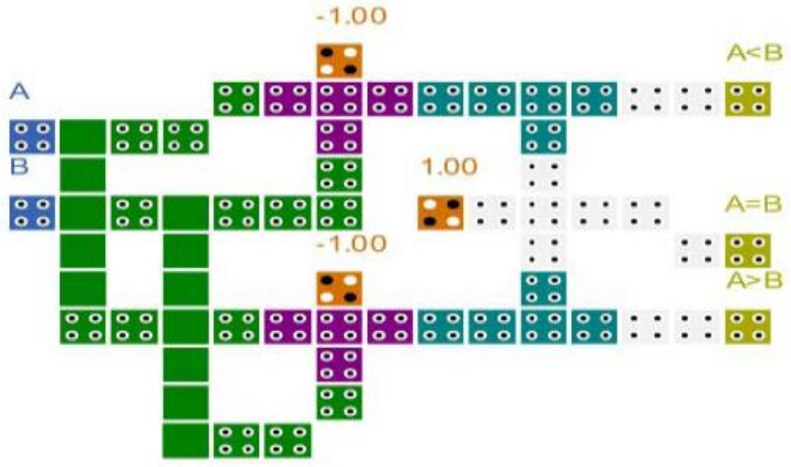


Fig. 6. The utilized QCA comparator circuit in [16]

This QCA comparator circuit requires 0.06 μm^2 area and 73 QCA cells.

Bhoi et al. [17] have developed a QCA comparator circuit, which is shown in figure 7.

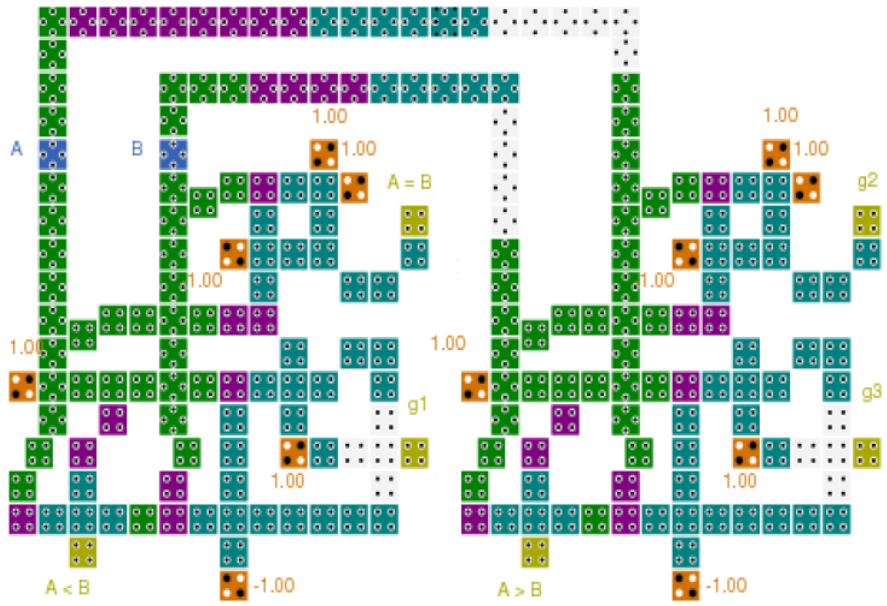


Fig. 7. The utilized QCA comparator circuit in [17]

This QCA comparator circuit requires 0.23 μm^2 area and 220 QCA cells.

Akter et al. [18] have developed a QCA comparator circuit based on TR and Feynman gates, which is shown in figure 8.

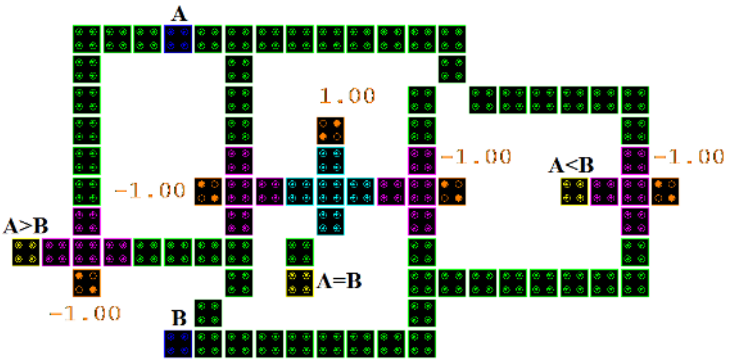


Fig. 8. The utilized QCA comparator circuit in [18]

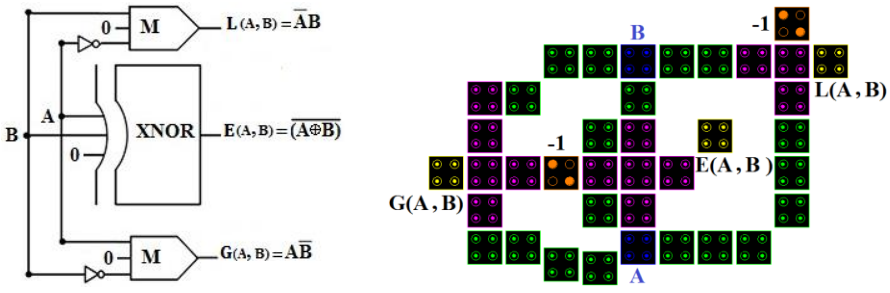
This QCA comparator requires 0.11μm^2 area and 87 QCA cells. Although, these QCA comparator circuits are suitable, the performance of the comparator can be improved as will be described in the next section.

3. The Proposed QCA Comparator Circuit

The proposed QCA comparator circuit has two 1-bit inputs and three 1-bit outputs. The inputs are indicated by A and B, and the outputs are indicated by L(A, B), E(A, B), and G(A, B). The relation between outputs and inputs are defined as follows:

$$\begin{aligned} L(A,B) &= \overline{A}.B \text{ where } A<B \\ E(A,B) &= \overline{A \oplus B} \text{ where } A=B \\ G(A,B) &= A.\overline{B} \text{ where } A>B \end{aligned} \quad (3)$$

As it is shown in equation (3), if the input A is less than the input B, the output L(A, B) is "1" and other outputs are "0". Moreover, if the input A is greater than the input B, the output G(A, B) is "1" and other outputs are "0". Otherwise, the inputs A and B are equal, the output E(A, B) is "1" and other outputs are "0". Figure 9 shows the designed 1-bit QCA comparator circuit.



(a) (b)

Fig. 9. The designed 1-bit QCA comparator circuit (a) block diagram (b) layout

The designed 1-bit comparators consist of 2 original majority gates (Fig.2 (c)), 3 inverter gates (Fig. 2 (a)) and an XOR gate (Fig. 2 (e)). The majority gates in the developed 1-bit QCA comparator circuit are used for implementation of AND gates. As a result, one input of these majority gates is set as logic "0". The designed 1-bit QCA comparator circuit requires 38 QCA cells.

4. Simulation Results and Comparison

The designed 1-bit QCA comparator circuit is simulated by using QCADesigner tool version 2.0.3. The following parameters are used for simulation: the number of samples: 12800, radius of effect [nm]:65.000000, the convergence tolerance: 0.00100, relative permittivity: 12.900000, clock low [J]: 3.800000e-023, clock high [J]: 9.800000e-022, clock shift: 0.000000e+000, and clock amplitude factor: 2.000000. Other simulation parameters are chosen as default. Figure 10 shows the simulation results of the designed 1-bit comparator circuit.

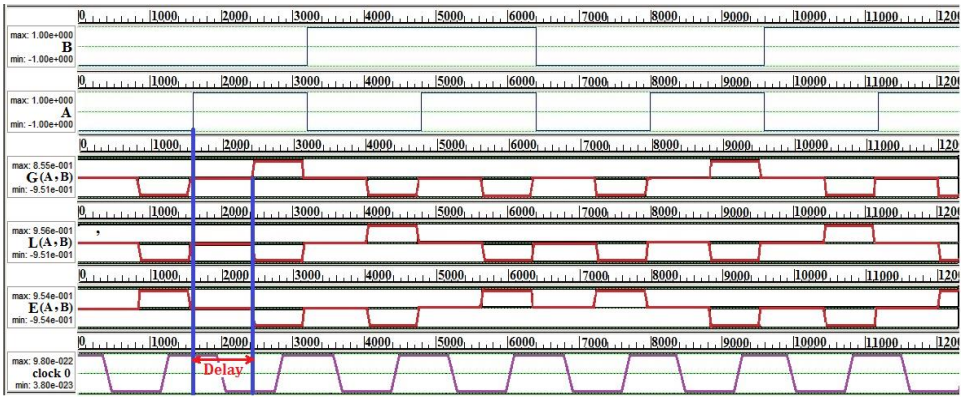


Fig. 10. The results for the designed 1-bit comparator circuit

These results demonstrate that the outputs of the designed 1-bit comparator circuit are correctly obtained after 0.5 clock cycles delay. Moreover, the designed 1-bit QCA comparator circuit requires 0.03 μm^2 area and 38 QCA cells. Table 1 summarizes the simulation results of the designed 1-bit comparator circuit compared with other 1-bit comparator circuits in [10-12, 16-18].

Table 1 The comparison table for 1-bit QCA comparator circuit

Reference	Cell count	area (μm^2)	Time delay (clock cycle)	Crossover	Cost
[10]	319	0.343	3	multilayer	1.029
[11]	117	0.182	1	coplanar	0.182
[12] design1	40	0.032	1	multilayer	0.032
[12] design2	37	0.028	1	multilayer	0.028
[16]	73	0.06	1	coplanar	0.060
[18]	87	0.11	0.50	coplanar	0.055
[17]	220	0.23	0.75	coplanar	0.172
This paper	38	0.030	0.50	coplanar	0.015

In this table, area and delay are shown in terms of μm^2 and clock cycle, respectively. Moreover, following equation is used to determine the cost value based on [1, 5, 7].

$$\text{Cost} = \text{Area} \times \text{Delay} \quad (4)$$

As it is shown in table 1, the designed 1-bit comparator circuit has advantages in terms of cost and area compared to [10-12, 16- 18]. For example, the cell count, area, delay and cost in the designed 1-bit QCA comparator circuit are improved compared to 1-bit QCA comparator circuits in [10] by about 88%, 91%, 83% and 98%, respectively. The only 1-bit QCA comparator circuit, which requires a slightly lower cell count and area than the designed QCA comparator circuit is the 1-bit QCA comparator circuit in [12] (design 2). However, this advantage has been resulted from the increased number of layers, not from logic design. In addition, the delay time and cost in the proposed 1-bit QCA comparator circuit are reduced by about 50% and 40% compared to the 1-bit QCA comparator circuit in [12] (design 2).

5. CONCLUSIONS

QCA technology is a promising technology for implementation of digital circuits in nano-scale [1-6]. The comparator circuits play important role in digital circuits [9-12, 16-18]. In this study, an efficient 1-bit QCA comparator circuit was proposed and evaluated. The designed 1-bit QCA comparator circuit was constructed based on majority gate, XNOR gate and inverter gate that were designed carefully. The functionality of the designed 1-bit comparator circuit was verified by using QCADesigner version 2.0.3. The obtained results indicate that the designed 1-bit comparator circuit requires 0.03 μm^2 area and 38 QCA cells. It also has 0.5 clock cycle delay. The results showed that the designed 1-bit comparator circuit provided improvements compared with other 1-bit comparator circuits in [10-12, 16-18] in terms of cell count, effective area, and delay as well as cost.

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