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Design of Five Stage CIC Decimation Filter for Signal Processing Applications

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Abstract

With the development of more compact and efficient ways of implementing digital logic on a silicon chip, most of the signal processing is being performed in the digital domain. The design of an efficient configurable digital decimation filter is focused in work. The Cascaded Integrator-Comb (CIC) filters are used as decimation filter. The five stage CIC filter is proposed in this paper. It does not require any multiplier circuit and also uses recursive or non-recursive filter[4]. CIC is the combination of equal number of Integrator and comb stages. The CIC filter is based upon a low-pass filtration system .These types of filter systems are utilized within the decimation that has the result upon decreasing the actual sample rate. The result of CIC filter impulse and magnitude response exposed using of MATLAB

Keywords: Decimation, CIC filter, Integrator, Differentiator and down sampler

1. Introduction

For managing signal processing, DSP is one of best technique which is used for many applications, like audio, wireless communication, telecommunication and speech recognition. Digital signal processing used different types of filter such as Finite Impulse Response (FIR) as well as Infinite Impulse Response (IIR) and Cascaded Integrator Comb filter (CIC) .Both FIR and IIR filters are referred as impulse responses. FIR generally assures stability, which is characterized by changing the power of coefficient. Similarly IIR filter requires less memory and faster. It is the most practical way to make use of when making regular filter

systems for example high-pass, band-stop filter as well as low pass filtration systems.

Decimation filter

The sampling rate conversion is the main block of decimation filter. The work of this filter is to convert the high resolution system into lower data frequency. This filter is applicable for many applications such as antenna technique and radar technique[6]. The process of this filter is to reduce the word range of the encoding signals. The decimation filtration system which comes after the modulator is actually necessary to take away the out-of-band interruption as well as decrease the sampling rate. A modulator oversampling rate represented as N_{tot}. The decimator input is 1 bit data that flow from the modulator. F_s is the decimation filter input and also the word rate of F_s is very high. The block diagram in the decimation filtration system will be shown in figure(1).The output of decimation filter denoted as $F_s/ N_{tot.}$ It classified into two methods, the effectual method is Sharpened Cascaded Integrator Comb and second method is Cascaded Integrator Comb.

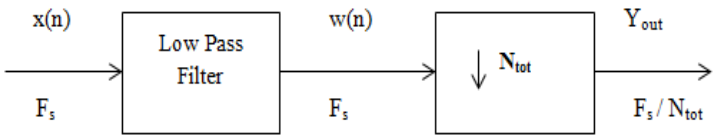

Figure 1: Block Diagram of Decimation Filter

2. Cascaded Integrator Comb filter

The present work is to design efficient decimation filter. This filter is known as Cascaded Integrator Comb filter. It is also known as Hogenaure filter. CIC filter consists of the equal amount of integrator as well as comb stages. This filter is created while using MATLAB. It involves delay and adders. The power reduction is the benefit of this filter. The CIC filter is the modification of moving average filter and it has equal number of weights.The impluse responses is given below

$$h(n)=\frac{1}{M} \; ; \; 0 \leq n \leq M-1 \; ,$$
$$= 0 \; ; \quad otherwise \quad (1.1)$$

where M denoted as a Decimation Factor.z-transform of average filter is given through

$H(z) = \frac{1}{M}\sum_{j=0}^{M-1} Z^{-j}$(1.2)

which can be modified to obtain transfer function regarding CIC filter as

$H(z) = \frac{1}{M}\frac{(1-z^{-M})}{(1-z^{-1})}$(1.3)

The frequency respons is given by

$H(e^{jw}) = \frac{1}{M}\frac{sin\left(\frac{wM}{2}\right)}{sin\left(\frac{w}{2}\right)}e^{-jw(M-1)/2}$(1.4)

It is usually seen from equation (1.4) that the CIC filter is a linear filter that displays sin (Mx) and sin(x) amplitude attribute. Figure(3) represented as frequency responses from the cic filter. If M is even the M/2 is spectral zeros and if M is odd the (M-1)/2 is spectral zero.

3. CIC Filter design

The anti-aliasing filter is the important role of decimation filter and also used to find out the less number of decimation stages that could provide useful implementation about cic filter.The cic filter block diagram is shown in figure (2)

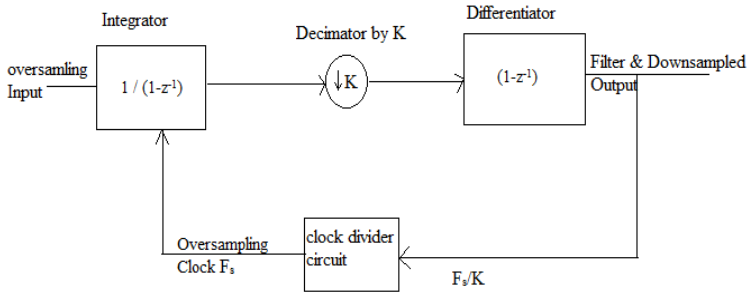

Figure 2: First Order CIC Fliter

The block of CIC filter is integrator stages.it is a single pole linear phase IIR filteration system which has unity feedback coefficient. The actual integrator is unpredictable because of the single pole from z = 1, due to this there's a higher possibility of data loss as well as excess of registers [3].To prevent this issues 2's complement number representation can be used. For higher order and very high sampling rate, these type of execution are very hard and contains more area. To prevent in this problem the decimation stage is launched in between integrator and differentiator stages. The clock Divider circuit is used to split the oversampling clock cycle after the integrator stages. The integrator is work with oversampling frequency F_s and differentiator is operated down sampling frequency range F_s/K.

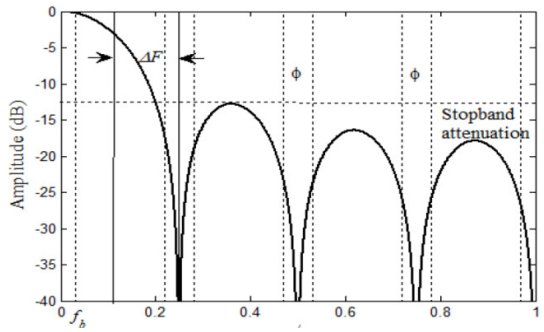

Figure 3: Frequency Response Of 1st order CIC filter

4. Design of Five Stage CIC Filter

The proposed system is to design the basic concept of the five stage CIC decimation Filter. Using MATLAB program, the efficient five stage CIC decimation filter is established. It is combination of five stage Integrator and comb stages. The clock Divider circuit is introduced between the integrator and comb filter. The oversampling frequency F_s is given to the integrator stage and the comb stage is operated at down sampling rate F_s /K [5].In this proposed work to increasing the maximum decimation ratio and also rising input as well as output word length. The integrator stages are increased compare to existing method.[4]

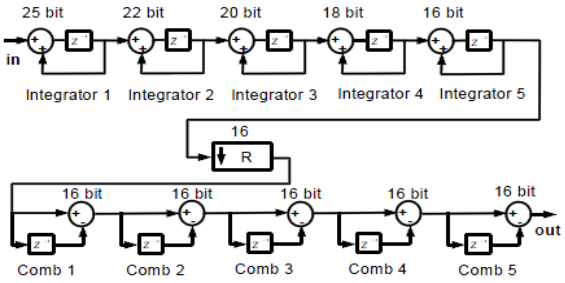

Figure 5: Five stage CIC filter

The higher stage filters include multiple spectral zeros together with multiplicity comparable to the actual order from the filter. The resultant occurrence of multiple spectral zeros is to increase stop band attenuation. The stop band attenuation is raised which used to improve the filtration system.

5. Results Analysis

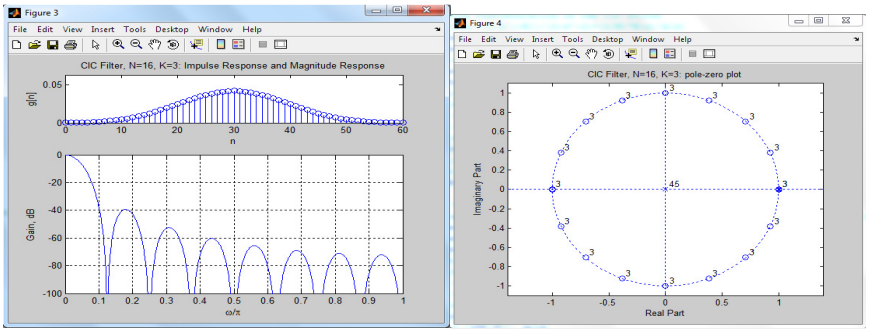

Figure 6: Three Stage CIC filter Impulse Response & Magnitude Response & Zero pole plot

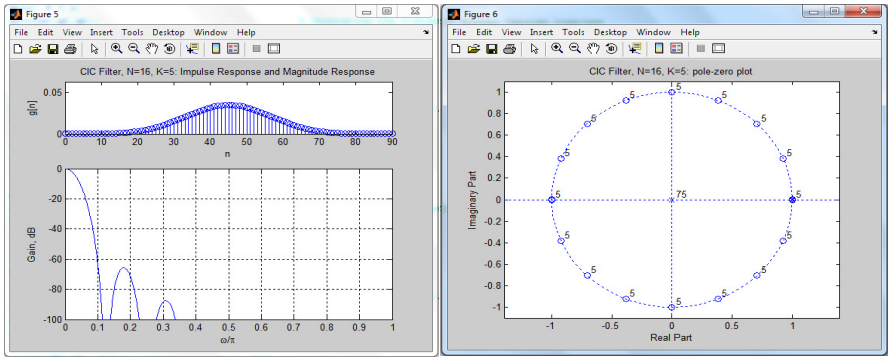

Figure 7: Five Stage CIC filter Impulse Response & Magnitude Response & Zero pole plot

The simulation result of five stage & three stage ,impulse & magnitude and Zero pole responses are displayed above. The decimation ratio N=16 and order K= 3 shown in figure 7.That result is represented as three stage cic filter.The present work of decimation ratio N=16 and ordeer K=5 shown in figure 8.That is donated as five stage cic filter.

7. Conclusion and Future Work

The Five stage CIC filter was designed and implemented using MATLAB tool. Decimation of the transmission signal which have higher rate of recurrence, utilizing FIR or IIR filters has been extremely complicated because it acquires many number of multipliers. To overcome this problem CIC filter was designed and also it does not require any multipliers. This structure is mainly used for DSP application. The order and decimation ratio of CIC filter was shown in simulation results. This proposed work has high performance and low complexity compared to existing methods [4], [1] and [2].The future plan of this work is to design a five stage CIC filter using hardware language and implemented in FPGA.

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