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NANYANG TECHNOLOGICAL UNIVERSITY

Design of High Performance Continuous Time Sigma Delta ADC

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SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

2011

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Last but not least, I want to dedicate this thesis to my parents. Their unconditional love and mental support demonstrated in so many admirable ways are still the strongest support throughout my life in Singapore.

Summary

ΣΔ technique has always been the popular choice for designing high resolution data converters due to the advantage of oversampling and noise shaping. In recent years, continuous time implementation of ΣΔ modulator is attracting more and more research attention for its superior potential to realize low power low voltage and/or high speed design. CT ΣΔ modulator relaxes amplifier's unity gain bandwidth requirements which greatly improves its achievable conversion speed. It also has the advantage of implicit anti-aliasing feature.

In this research, various design trade-offs and implementation issues have been introduced and discussed. Special focus has been put on the issue of clock jitter which is considered to be the major obstacle for CT ΣΔ modulator to be widely implemented. In this research, a special pulse shaping technique which is called fixed length return-to-zero method was proposed. Simulation shows that it almost achieves the best performance any pulse shaping method can achieve. It not only greatly improves CT modulator's jitter performance, but also exerts very little adverse effects such as increased power consumption, circuit overhead, and increased loop delay.

For the purposed of verifying various design concepts developed in this research, a 4^{th} order 1-bit prototype modulator integrated in 0.18 μm CMOS technology has been developed. Simulation shows it is able to achieve 85 dB SNDR for 25 kHz input signal range. And the FOM it achieves is 0.22pJ/conversion. The total chip occupies an area of $1.725mm^2$.

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Chapter 1
Introduction

1.1 **Motivation**

Until mid 70's, almost all signal processing was performed in the analog domain. With the advance of very large scale integration (VLSI) technology, implementing sophisticated digital signal processing functions on an integrated chip has become not only possible but also advantageous compared to the traditional analog signal processing. Digital signal processing offers enhanced functionality, increased resolution and higher noise immunity which are key to produce a high performance system. Nowadays, digital signal processing systems have penetrated almost every area of our world, from general consumer markets to military use. Its ubiquitous existence in our life makes this new millennium what we called a 'digital age'. State-of-the-art electronic gadgets like Digital Media Player, Handphone, Laptop, and HDTV etc. are all practical applications of digital processing.

Although the signal processing is done in digital domain, the signals in this world are still analog in nature and this will never change. Thus, interfacing between analog and digital signal is inevitable. This interfacing is what we referred to as Analog-to-Digital (A/D) and Digital-to-Analog (D/A) converters. In fact, it is the bottleneck of the overall system because it determines the accuracy that the entire system can achieve.

Generally, there are two broad categories of data converters, namely, Nyquist rate converter and oversampling converter. Nyquist rate converters generally achieve high speed conversion but with limited resolution. On the other hand, oversampling converters

are meant for high resolution applications. ΣΔ Converter is the most commonly seen oversampling converter.

ΣΔ technique has always been the popular choice for designing high resolution data converters due to the advantage of oversampling and noise shaping. Combined with the invention of switched capacitor technique, in the past decades, ΣΔ converters are mostly implemented in switched capacitor form, which are also referred to as Discrete Time ΣΔ Modulator because signal processing is done in discrete time domain. This kind of modulator possesses the advantages of relaxed circuit constraints and complexity, full compatibility with CMOS technology and scalability with sampling rate. However, due to stringent settling requirement on switched capacitor amplifier, it is difficult to extend its input bandwidth to a few megahertz without compromising its achievable resolution. A 5MHz bandwidth DT design has been reported but only with 7 bits of resolution [1].

In recent years, more and more attention has been paid upon implementing ΣΔ Modulator in continuous time domain (referred as CT ΣΔ Modulator). In fact this concept is not newfound as the starting concept and first few prototypes of ΣΔ converter are based on continuous time implementation. By implementing ΣΔ Modulator in continuous time domain, the speed requirement that was originally imposed on first stage integrator of ΣΔ modulator in DT implementation has been greatly relaxed. This offers a good prospect for a very power efficient design. Additionally, the inherent implicit anti-aliasing from CT implementation eliminates the need for anti-aliasing filter in the front end, further reducing the circuit complexity and power consumption. In [46], a CT ΣΔ modulator with an FOM of 0.054pJ/con was reported. This figure is far beyond the capability of DT modulators which normally achieve FOMs in several-pJ/conv range. On the other hand, speed performance of ΣΔ modulator can be significantly improved due to relaxed speed requirements for integrators. Modulator with 20MHz input bandwidth in 0.13 μm

technology with 12 bits of resolution has been designed [2]. This is not practical if DT implementation were to be used.

However, CT ΣΔ Modulator has its own limitations. First, unlike DT implementations, whose coefficients are determined by capacitor ratios in SC technique, in CT implementations, coefficients are determined by RC product or Gm/C which are subject to significant process variations and mismatches. Hence, stability and performance may suffer. Secondly, due to continuous nature of feedback pulses, excess loop delay becomes an important consideration because it can cause potential instability and performance degradations. Thirdly, due to integration operation of feedback pulse over time, CT modulators are sensitive to feedback related non-idealities. The most severe problem is created by clock jitters. Clock jitter always exists and it can only be minimized by careful clock generation circuit design. It causes non-uniform feedback pulses which are effectively considered as noise directly added to the input. This will add white noise floor to the original signal and subsequently degrade the resolution. It has been shown that jitter noise effect may exceed all other noise sources like quantization noise and circuit noise and become the limiting factor of the modulator design. Thus reduction of clock jitter effect and at the same time creating minimum impact on other aspects of the system's performance becomes an attractive and important research direction.

Audio Signal Processing

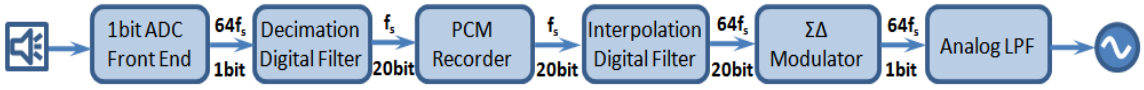


Figure 1-1 Conventional Audio Signal Processing Chain

Figure 1-1 shows the typical sequence of audio signal processing. The audio signal is first converted to a 1-bit Pulse Density Modulated (PDM) digital signal at an oversampled rate ($64f_s$) through an oversampling ADC. Then this 1-bit signal is down-sampled and filtered, generating an output of 44.1kHz/16bits (Pulse Code Modulation or PCM) which is to be stored on disc. When the stored information is to be read out, it is again up-sampled and converted to 1-bit format through multi-bit DAC. This 1-bit code is then low passed, generating analog sound.

The 1-bit coding in front end ADC is the most critical step which directly interfaces between analog sound and digital representation. This step is lossy in nature. It is usually performed by high resolution ΣΔ Modulator which may be implemented using either single-bit or multi-bit structure. If multi-bit ΣΔ modulators are used, extra digital signal processing step needs to be performed in order to obtain the 1-bit audio representation. Hence, though multi-bit ΣΔ modulator achieves better performance, it complicates the system and is less direct than their single-bit counterpart.

In recent years, a new coding format which is called direct stream digital (DSD) is proposed to replace traditional compact disc (CD) [3]. The signal chain architecture is shown in Figure 1-2.

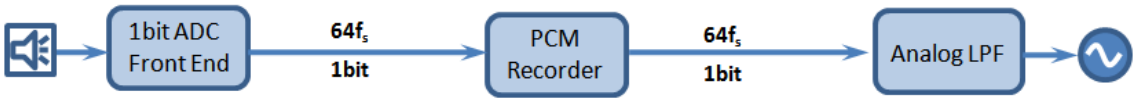


Figure 1-2 Audio Signal Processing Chain for DSD Technology

Instead of storing 44.1 kHz/16bits PCM code, the 1-bit 64 times oversampled PDM code is directly stored and processed. During read out, the 1-bit signal is directly fed to analog low pass filter, generating audio output. By using this structure, several digital processing steps can be removed, and it is believed that higher quality audio signal processing can be

achieved. Also, storing $64f_s$/1bit signal is much more efficient than traditional CD format. In this architecture, 1-bit front end ADC is still the most critical part.

1.2 Objective

This research aims to investigate the various design trade-offs of Continuous Time ΣΔ Modulator primarily targeting at audio sensor applications. The primary focus is on the aspects of achieving high performance design (i.e. high speed, high resolution). In the context of this research, achieving high resolution data conversion under strong non-ideal effects is the primary research focus. The most serious issue specifically related to Continuous Time ΣΔ Modulator-clock jitter noise is to be studied and analyzed in great depth. Various techniques to counteract the effect are to be explored and compared while optimum design methodology and possibly new techniques are to be proposed.

1.3 Thesis Organization

This thesis presents the theoretical analysis of CT ΣΔ A/D converters, differential behavioral modeling technique and non-idealities investigation. Timing non-idealities such as excess loop delay, jitter noise are discussed and proposed techniques are introduced. Circuit implementation is carried out as well. The remaining chapters are organized as following.

Chapter 2 introduces the fundamental theories of ΣΔ converter. Discrete Time approach is first presented. Then Continuous Time design is introduced. Advantages and disadvantages of each type are compared.

Chapter 3 presents the system design approach where major design trade-offs are introduced. Following that, differential behavioral modeling technique is presented, its advantages are demonstrated. With this modeling technique, non-idealities are investigated and their effects are visualized from simulation.

Chapter 4 analyses timing non-idealities in CT ΣΔ modulators which are key disadvantages of CT implementation over DT counterpart. Clock jitter is examined in great depth. A novel method for clock jitter noise reduction technique named Fixed-Length Return-to-Zero pulse shaping technique is introduced.

Chapter 5 gives an implementation example which is a 4^{th} order single-bit Continuous time sigma delta modulator. The entire design flow from topology selection to behavioral modeling, then to circuit implementation and chip layout is elaborated to show the design concept developed in this research.

Chapter 6 concludes the thesis and proposes possible future research directions.

Chapter 2
Overview of ΣΔ Converters

2.1 Sampling and Quantization

2.1.1 Sampling

The most basic operation in a digital system is sampling. An important characteristic of ideal sampling is that sampling in time is a completely reversible process given the condition that the sampled signal is band-limited and the sampling rate is high enough. Figure 2-1 shows a perfectly sampled signal (without aliasing). It is obvious that by low pass filtering the signal, the original signal can be recovered. This means proper sampling would not introduce any distortion to the original signal.

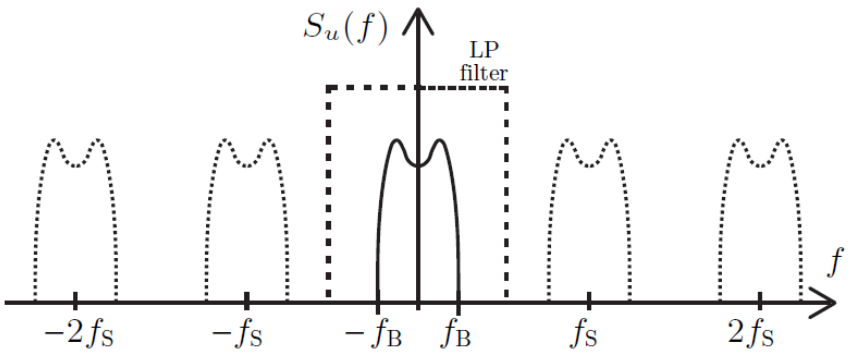


Figure 2-1 Spectral Sampling Operation

For a sampled signal to be re-constructible as in Figure 2-1, aliasing should not happen. This condition is ensured by the famous Nyquist Theorem [4] which states that the sampling rate f_s has to be at least twice the highest spectral component, f_b, of the signal,

i.e. $f_s \geq 2 * f_b$. The sampling rate which satisfies the Nyquist Theorem is called Nyquist Rate. If the sampling rate is much higher than Nyquist Rate, the sampling is called oversampling. The benefit of oversampling will be discussed shortly.

2.1.2 Quantization

Another basic operation in digital systems is called quantization. Different from sampling, quantization operation is a lossy process and hence irreversible. However quantization is inevitable in a digital system as a discretized signal can only be represented by a finite number of discrete levels. The difference between the actual value and the quantized value is called quantization error. The primary objective of ADC design is to minimize this error indeed.

The device that encodes analog signal and produce digital signal output is called a quantizer. The main distinguishing parameter of a quantizer is the number of bit which correlates with the number of output levels. If 2^B output levels output is available, the quantizer is called a B-bit quantizer. Quantizer bit is the most important performance indication of a quantizer as it determines the quantization error. As the input signal is quantized to the nearest quantization level, the interval between two quantization levels which is called quantization step width bounds the maximum quantization error. For uniform quantization, quantizer step width is defined as

$$\Delta = \frac{FS}{2^{B-1}} \tag{2.1}$$

where FS denotes the full scale output range. Thus, the quantization error is always bounded within $[-\frac{\Delta}{2}, \frac{\Delta}{2}]$. Obviously, the larger the quantizer bit, the smaller the average quantization error. Mathematically, total quantization noise is proved to be

$$\sigma_e{}^2 = \frac{\Delta^2}{12} \qquad 2.2$$

In general, quantizer can be divided into two categories according to their number of bits: single-bit quantizer and multi-bit quantizer (Figure 2-2).

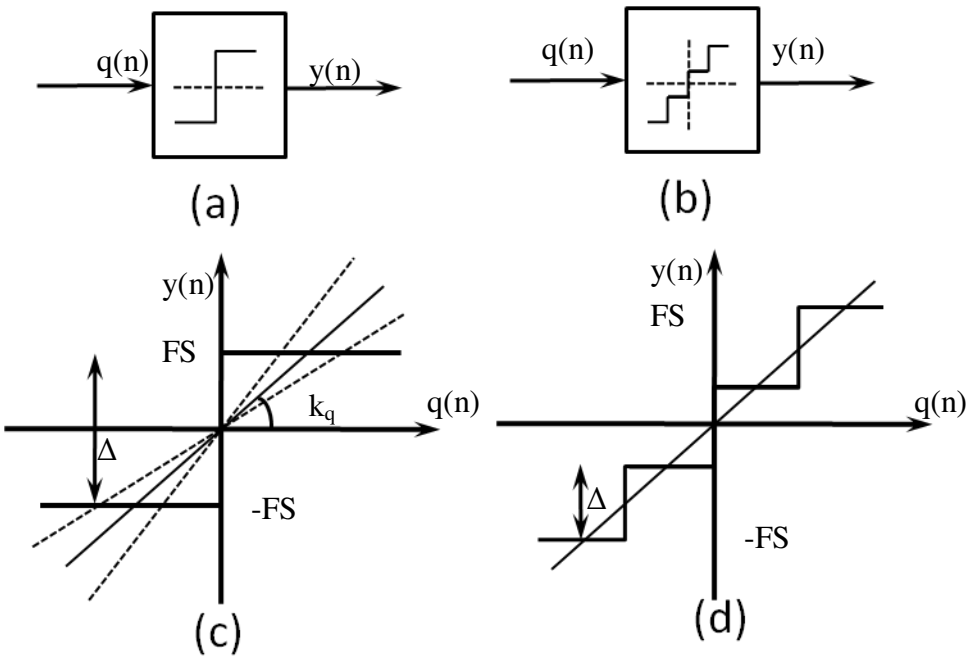


Figure 2-2 (a) Single-bit Quantizer (b) Multi-bit Quantizer (c)Single-bit Quantizer Transfer Curve (d) Multi-bit Quantizer Transfer Curve

Obviously, multi-bit quantizer will have much smaller quantization error than single-bit quantizer. However, this is not the only difference between the two quantizers.

As can be seen from the transfer curve (Figure 2-2) of the two quantizers, a noticeable difference between the two is for multi-bit quantizer, its quantizer gain is well defined (usually assumed to be 1) while for single-bit quantizer, its gain varies according to the input signal. This difference is non-trivial and may cause stability and performance difference in ΣΔ modulator which will be discussed in later section.

2.2 ΣΔ ADC Performance Metrics

The performance of an ADC governs how closely the digital signal matches its original analog input and also sets a limit on the fastest input signal the converter can digitize. The former represents the quantization operation of a converter. The latter simply represents the bandwidth of the input signal.

Fundamental differences in operating principle exist between Nyquist rate converter and ΣΔ converter, thus it is useful to clarify performance parameters that are usually used in characterizing ΣΔ converter.

Oversampling A/D converters minimize quantization errors through a sequence of samples while Nyquist rate converters do so on a sample to sample basis. Thus, static performance metrics like INL (Integral Nonlinearity) and DNL (Differential Nonlinearity) which measures the sample difference are not appropriate for ΣΔ converters. Instead, dynamic metrics such as mean square error, signal-to-noise ratio, and dynamic range are used to evaluate the performance of ΣΔ A/D converters. Some of the important metrics are introduced below.

Signal to Noise Ratio (SNR)

SNR defines the ratio between the power of the desired output signal and the power of the output noise. It is to be made clear that this output power defined here is the total power within converter bandwidth excluding the input signal and any harmonics of the input signal. This output noise is also called in-band-noise (IBN).

$$SNR_{dB} = 10\,log_{10}\frac{P_{SIG}}{P_{NOISE}} \qquad 2.3$$

Signal to Noise and Distortion Ratio (SNDR)

SNDR is similar to SNR, but all the undesired contents including all noise sources and non-linear harmonic distortions are incorporated into total noise.

$$SNDR_{dB} = 10\,log_{10}\left(\frac{P_{SIG}}{P_{HARMONICS} + P_{NOISE}}\right) \quad 2.4$$

Dynamic Range (DR)

The ratio between the maximum signal amplitude that can be resolved without saturating the converter, and the minimum signal amplitude that can be resolved without being mistaken for noise.

$$DR_{dB} = 10\,log_{10}\left(\frac{P_{SIG,MAX}}{P_{SIG,MIN}}\right) \quad 2.5$$

Effective Number of Bits (ENOB)

The effective resolution of the converter, with all non-ideal effects included. This parameter is the equivalent in bits to the SNDR.

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad 2.6$$

Spurious Free Dynamic Range (SFDR)

SFDR defines as the ratio of the signal power to the power of the strongest spectral tone. Its importance strongly depends on the application, since it dominates the resulting ADC linearity.

Figure of Merit (FOM)

This performance gauge serves as a useful tool for comparison among different implementations. It does not reflect a scientific relation between performance and power. Instead, it sets a straightforward comparison standard by combining a few important specifications in a single number. As a matter of fact, there are several different definitions of FOM. [5] summarizes and makes inspirational comments among them. The three most important FOMs are FOM related to thermal noise, FOM related to signal resolution and FOM including distortion. The primary difference is how the performance is quantified. These three FOMs use dynamic range, ENOB and SNDR respectively. For ΣΔ A/D converters, FOM including distortions provides the best way for fair comparison. In this research, we also adopt this definition. It can be expressed as following:

$$FOM = \frac{P}{SNDR \cdot BW} \tag{2.7}$$

2.3 ΣΔ Modulator Operating Principles

2.3.1 Oversampling

As introduced in previous section, for a sampling process to be performed without loss of information, Nyquist Theorem must be satisfied which means $f_s \geq 2 * f_b$. Thus normal Nyquist rate ADC must be band limited, which is ensured by the use of anti-aliasing filter (Figure 2-3). Usually the requirements on the anti-aliasing filter are very stringent, such as very narrow transition band, high attenuation in stop band and very small pass band ripple etc. All of these result in circuitry that is complex, area consuming and power hungry.

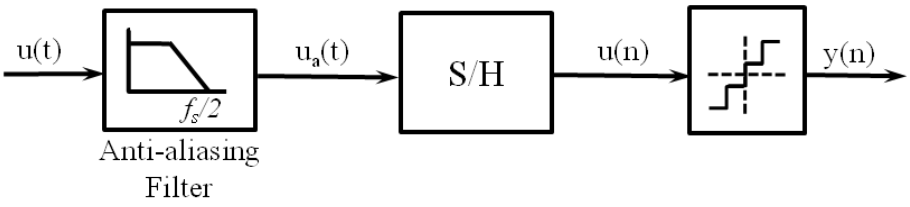


Figure 2-3 Conventional ADC Structure

One way of improving the situation is to increase the sampling rate to many times of its Nyquist rate. This is called oversampling. A measure of degree of oversampling is called oversampling ratio which is the ratio of actual sampling rate to its Nyquist rate, i.e.

$$\mathrm{OSR} = \frac{\mathrm{f_s}}{\mathrm{f_N}} \tag{2.8}$$

where f_N denotes the Nyquist rate. To understand why oversampling helps to relax the requirements for anti-aliasing filter, spectrum of an oversampled signal is shown in Figure 2-4.

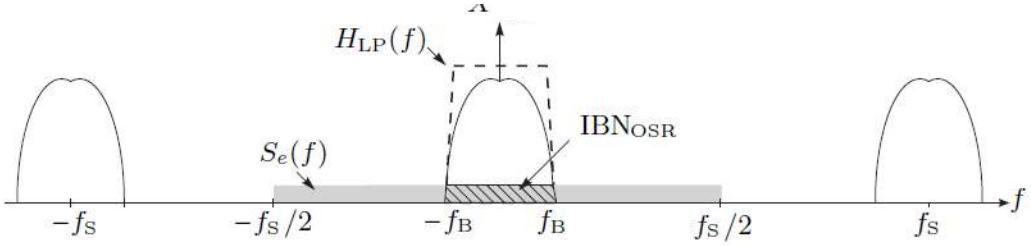


Figure 2-4 PSD of an Oversampled Signal

It is evident that the images of the signal band are not so close to one another, and hence the specifications of the anti-aliasing filter can be much relaxed.

However, this is not the only benefit that can be obtained from oversampling. A more important advantage of oversampling is that oversampling helps to reduce in band noise.

This is due to the fact that the total quantization noise power is independent from the sampling frequency which can be seen from Eqn. 2-2. With the increase of sampling frequency, quantization noise is more and more flatten out across the entire band. Figure 2-5 shows the effect graphically.

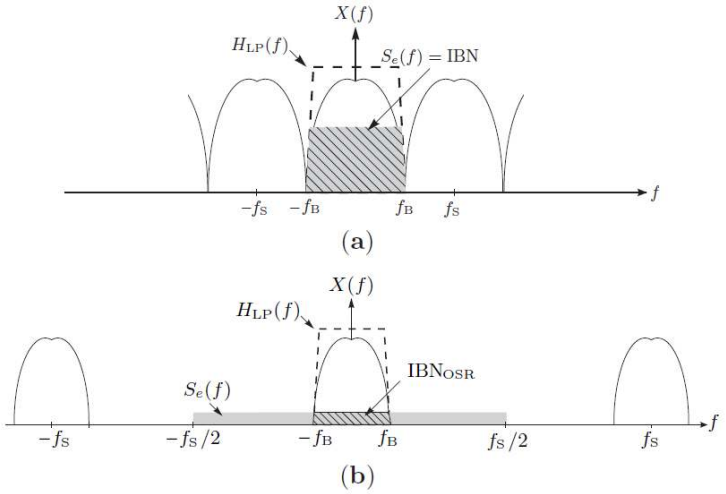


Figure 2-5 Spectral Effect of Oversampling

Thus the integrated in-band quantization noise can be calculated by

$$IBN_{OSR} = \int_0^{f_B} S_e(f)df = \frac{\Delta^2 * f_B}{12 * f_s} = \frac{\Delta^2}{6}\frac{1}{OSR} \qquad 2.9$$

This effect greatly helps to increase the achievable maximum SNR, which can be calculated as

$$SNR_{OSR} = 10\,log_{10}\left(\frac{P_{SIG|FS/2}}{IBN_{OSR}}\right) = 6.02B_{INT} + 10log_{10}OSR + 1.76\ (dB) \qquad 2.10$$

here $P_{SIG|FS/2}$ represents the power of largest sinusoidal input signal which has a magnitude of FS/2.

From Eqn.2.9, it can be inferred theoretically, every doubling of oversampling ratio will increase the maximum SNR by approximately 3dB or 0.5-bit.

Although oversampling is useful for reduction of in band noise, itself alone cannot make a highly efficient system. The benefit that can be obtained from enhancement of resolution may be offset by the increase in sampling rate, which corresponds to loss in conversion speed and an increase in power consumption. Fortunately, when combined with noise shaping technique, its advantage can be significant enough to make a great impact.

2.3.2 Oversampled Noise Shaping Converters: ΣΔ ADC

A further improvement in SNR can be achieved by further suppressing in band noise and at the same time preserving the desired signal, i.e. high pass on quantization noise, low pass on desired signal. Conventional Nyquist rate converters or oversampling converters are pure open loop systems, thus they cannot implement different filter function on signal and noise at the same time. However, this can be easily done in a closed loop systems. With additional controller in feedback or feed-forward path, different shaping characteristics can be obtained for quantization noise and the desired signal, which are defined respectively as noise transfer function (NTF) and signal transfer function (STF). This is the basic concept of noise shaping. Moreover, when oversampling concept and noise-shaping concept are combined, very significant noise suppression can be achieved, forming the well-know ΣΔ converter.

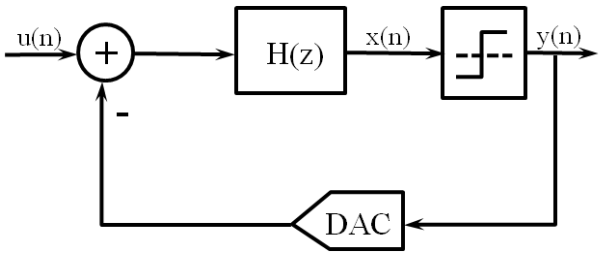


Figure 2-6 Noise-Shaped Oversampling Modulator

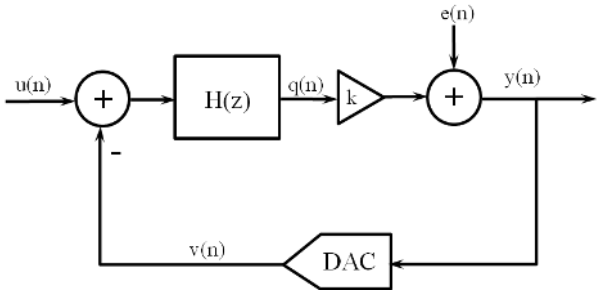


Figure 2-7 Linearized Model of ΣΔ Modulator

ΣΔ modulator is a highly non-linear system due to the presence of quantizer (Figure 2-6) which is a strong non-linear element inside the loop. For such non-linear system, rigorous analytical analysis has proven difficult or even impossible. Thus some linearization technique is required. The linearized model shown in Figure 2-7 is simple enough to provide some insights into the operation of the ΣΔ modulator, and also gives a rough estimation of the dynamic range performance of the modulator. [6]

Based on the linear model, the transfer function of the modulator can be written as

$$Y(z) = \frac{H(z)}{1 + H(z)} U(z) + \frac{1}{1 + H(z)} E_Q(z) \qquad 2.11$$

Here the gain factor, $\frac{\mathrm{H(z)}}{1+\mathrm{H(z)}}$, of the input signal $\mathrm{U(z)}$ is the signal transfer function (STF). And the gain factor, $\frac{1}{1+\mathrm{H(z)}}$, of the quantization noise $\mathrm{E_Q(z)}$ is the noise transfer function (NTF).

Note: derivation of eqn. 2-11 bears the assumption that input signal and feedback signal are processed by the same loop filter function $H(z)$*. If it is not the case, STF would become* $\frac{H_1(z)}{1+H_0(z)}$ *and NTF would become* $\frac{1}{1+H_0(z)}$*. However, the in-band characteristic doesn't change much for the two cases.*

We may note that if H(z) represents a low pass transfer characteristic, and has a very large gain within the band of interest, |NTF| would be nearly zero while |STF| would be nearly 1 within signal band. Figure 2-8 shows the stated NTF and STF characteristic. The noise shaping is clearly visible.

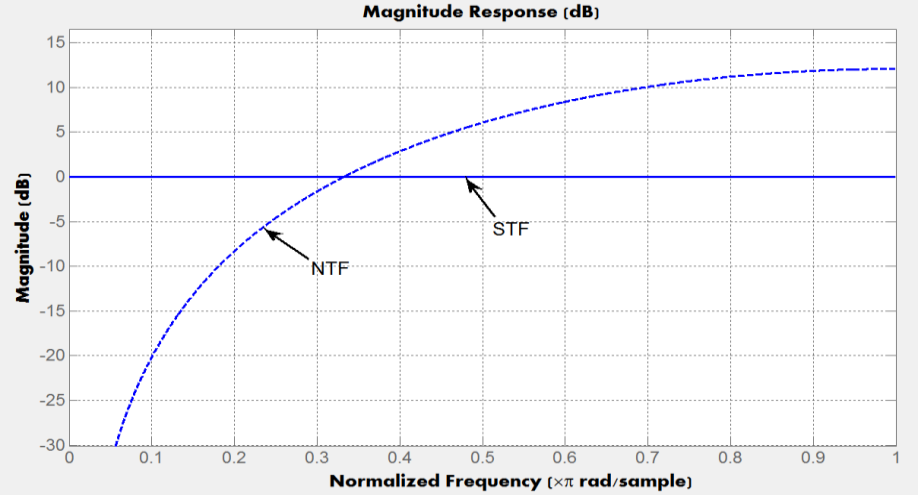


Figure 2-8 NTF and STF of a Second Order ΣΔ Modulator

If the non-idealities of forward path ADC and feedback DAC are included, the following model results as shown in Figure 2-9. [7]

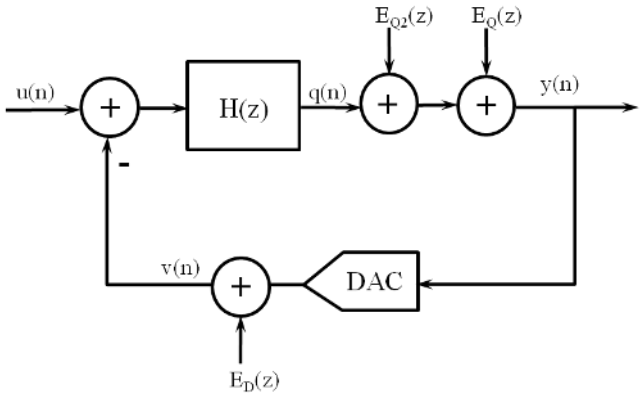


Figure 2-9 ΣΔ Modulator Model Including Non-idealities

And this model gives rise to the following transfer function

$$Y(z) = \frac{H(z)}{1 + H(z)}\big(U(z) - E_D(z)\big) + \frac{1}{1 + H(z)}(E_Q(z) + E_{Q2}(z)) \qquad 2.12$$

where the $E_D(z)$ denotes the feedback DAC error and $E_{Q2}(z)$ denotes the forward path ADC error.

From this model, we can draw an important conclusion. The non-idealities of the forward path ADC is noise shaped, just like the quantization noise. However, the non-idealities of the feedback path DAC are not noise shaped and directly corrupt the input signal. This insight is important in the sense that it tells the designer where the design emphasis should be put. We can conclude feedback DAC determines the performance of the whole modulator and must be designed with special care. The requirement for the ADC (quantizer) on the other hand is quite relaxed. Hence, heavy research attention into reducing DAC non-idealities is justified.

2.3.3 High Order Noise Shaping

The simplest ΣΔ modulator is a first order ΣΔ modulator, as shown in Figure 2-10.

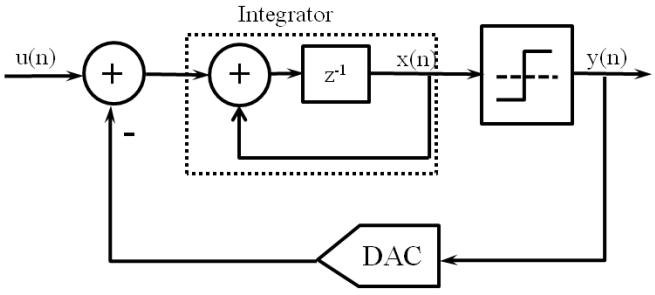


Figure 2-10 First Order ΣΔ Modulator

The first order ΣΔ modulator makes use of a first order loop filter with filter transfer function $H(z) = \frac{1}{z-1}$. As shown in the above figure, this low pass loop filter is realized

using a single stage integrator. With the simple ideal linearized model, we may derive the transfer function of this first order modulator:

$$Y(z) = z^{-1} \cdot U(z) + (1 - z^{-1})E_Q(z) \tag{2.13}$$

Where STF=z^{-1} and NTF=$1 - z^{-1}$.

The first order ΣΔ modulator can be extended to second order by cascading another integrator stage onto the original integrator as shown in Figure 2-11.

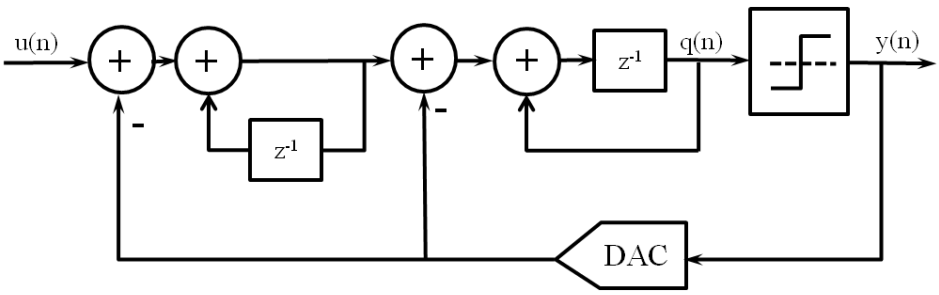


Figure 2-11 Second Order ΣΔ Modulator

And similarly, its transfer function is derived as

$$Y(z) = z^{-1} \cdot X(z) + (1 - z^{-1})^2 E_Q(z) \tag{2.14}$$

where STF is 1, and NTF is $(1 - z^{-1})^2$.

A simple comparison of first and second order transfer function reveals how the modulator order affects the noise shaping effectiveness.

In both first order and second order modulators, within frequency band of interest, |STF| has the same value 1. But the |NTF| for 1st order and 2nd order are different. The difference is demonstrated by the frequency domain plot of the |NTF| for the two modulators as shown in Figure 2-12.

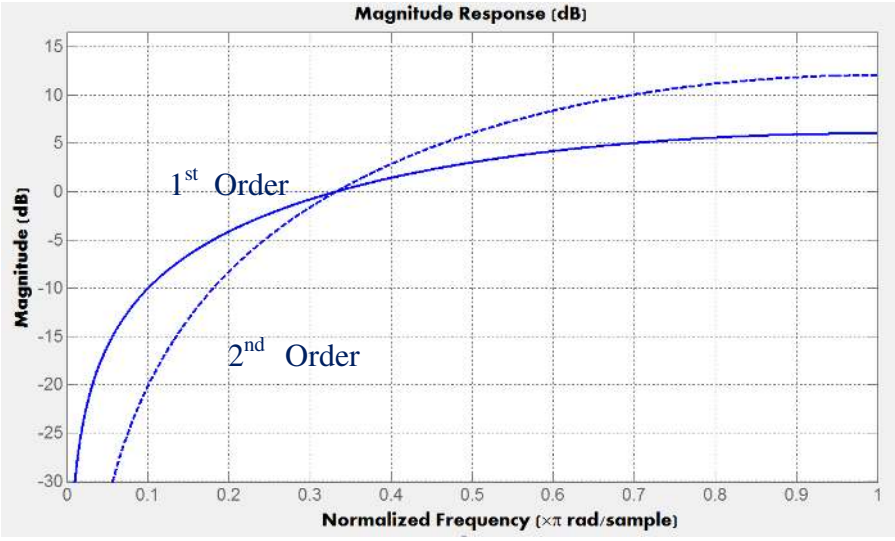


Figure 2-12 NTF of First Order and Second Order ΣΔ Modulator

It is obvious from the above plot that at low frequencies, 2nd order modulator achieves better in band noise suppression. However at higher frequencies, the 2nd order modulators tend to amplify noise much more significantly than 1st order counterpart. This out of band amplification of noise is called out of band gain (OBG) of NTF. OBG is non-trivial although its effect is outside the signal bandwidth. A large OBG may cause high frequency noise to flood the modulator and create potential stability problem. This problem will be discussed in latter sections.

Quantitative analysis of an Lth order modulator (L=1, 2, 3…) is given next to quantify the effect of modulator order on noise shaping performance. For an Lth order ΣΔ modulator, we assume the signal transfer function is expressed STF=1(non-delaying modulator), and the noise transfer functions as $NTF = (1 - z^{-1})^L$.

From the NTF given, total in band noise of an Lth order ΣΔ modulator can be estimated.

Since the quantization noise power spectrum density is calculated as $S_e(f) = \frac{\Delta^2}{6 \cdot f_s}$

Quantization noise with noise shaping is then

$$S_{eL}(f) = S_e(f)|NTF|^2 = \frac{\Delta^2}{6 \cdot f_s} 2^L sin^L(\pi f / f_s) \tag{2.15}$$

where NTF is expressed in frequency domain as

$$NTF = (1 - z^{-1})^L|_{z=e^{j2\pi f/f_s}} = \left(1 - e^{-j2\pi f/f_s}\right)^L = (-2je^{\frac{j\pi f}{f_s}} sin\left(\frac{\pi f}{f_s}\right))^L \tag{2.16}$$

Thus the total in band noise of the modulator can be estimated as

$$\begin{aligned} P_Q = \int_0^{f_B} S_{eL}(f)\, df = \int_0^{f_B} \frac{\Delta^2}{6 \cdot f_s} 2^L sin^L\left(\frac{\pi f}{f_s}\right) df \approx \int_0^{f_B} \frac{\Delta^2}{6 \cdot f_s} 2^L \left(\frac{\pi f}{f_s}\right)^L df \\ = \frac{\Delta^2 \pi^{2L}}{12 \cdot (2L+1)} \left(\frac{2f_B}{f_s}\right)^{2L+1} \end{aligned} \tag{2.17}$$

assuming $\frac{f_B}{f_s} << 1$, i.e. large oversampling ratio. Suppose the modulator has a n-bit quantizer, the full scale range signal can be approximated as

$$P_{SIG|\frac{FS}{2}} = \frac{A^2}{2} = \frac{(2^n - 1)^2 \Delta^2}{8} \tag{2.18}$$

Thus, the maximum dynamic range for this L[th] order modulator is

$$DR = \frac{P_{SIG|\frac{FS}{2}}}{P_Q} = \frac{3}{2} \frac{2L+1}{\pi^{2L}} OSR^{2L+1} (2^n - 1)^2 \tag{2.19}$$

This important expression shows ΣΔ technique has much more aggressive noise shaping compare to simply oversampling technique. For example, with a first order noise shaping, every doubling of OSR will improve DR and SNR by 9 dB or 1.5 bits. In comparison, as mentioned in the above section, for pure OSR technique, every doubling of OSR only creates 0.5 bit of resolution gain. By increasing the modulator order, more noise shaped effects can be obtained.

However, this does not mean modulator order can be increased without limit. As modulator order becomes higher, overloading effects (due to high NTF out-of-band gain) become more pronounced, consuming usable dynamic range, creating potential instability problem. Thus modulator's input range must be limited to ensure stability. This effect offsets the benefit brought from high order noise shaping and more so when the order goes higher and higher. Thus the achievable SNR will not increase without bound. Generally speaking, modulators order higher than 5 are not efficient and difficult to design due to stability concern.

2.3.4 Stability

Stability is defined as a modulator condition, where all internal state variables, which are the integrator outputs, remain bounded over time [8]. Research studies have shown that modulator order higher than two is only conditionally stable. In reality, to ensure stability, the integrator gain has to be scaled down with less aggressive noise shaping.

The reason for instability to occur can be twofold: the modulator input signal is too strong or the power of the out-of-band quantization noise is too high. For this reason, stability is always ensured in two ways. First is to limit the input signal amplitude. Unfortunately, there are no strict criteria as for how to ensure a clear bound on input signal. It is common belief that extensive experiments that constitute of input signal of different amplitude and different frequency must be carried out. Furthermore, long simulation sequence need to be taken since some of the instability can only be observed after long simulation. Another simulation method is presented in [20], where the author proposes that a ramp input to the quantizer and observe the quantizer input. The moment the quantizer input amplitude exceed 10, the input amplitude is found out and assumed to be the maximum stable

amplitude. The author claimed this method gives approximately same results as previous exhaustive simulation method while requiring much less simulation effort.

The second approach is to limit NTF out-of-band gain. This restricts the potential harmful effects of out-of-band quantization noise but at the expense of in-band noise shaping. Hence, theoretical signal-to-noise ratio as predicted in linearized model (Eqn. 2.19) cannot be achieved in practice. As a rule of thumb, in [16], it has been proposed to limit the out-of-band gain of single-loop single-bit modulators to be within 1.5. For multi-bit modulators, their out-of-band gain can be much relaxed to higher value. Values around 3.5 are achievable with proper design.

Besides simulation method, some other methods also exist for stability check. In [39], the method of root-locus plots has been adopted. This method is useful because it provide a closer insight into the behavior of the chosen modulator. This method is based on the linear approach of a strongly nonlinear modulator, especially single bit modulators. In this model, quantizer block is regarded as a variable gain block which is not defined in the case of a single-bit quantizer, and root-locus plot of the loop can be determined. To ensure stability, the root-locus must not exit the unit circle. The boundary condition can thus be found and hence the minimum quantizer gain. However, it should be noted that root-locus is only approximate approach and it still needs to be confirmed by behavioral simulation.

2.4 Continuous Time ΣΔ Modulators

The explanations and examples discussed in previous sections are all in z-domain. This is with the assumption that the ΣΔ modulator is implemented using switched-capacitor (SC) technology. And this type of modulator is operated in discrete time domain. This is

because ΣΔ modulators implemented using SC technology is most popular during the last few decades, thus most theories and analysis are developed for discrete time implementations. Continuous time ΣΔ modulators, although not entirely new, is not as well studied as their DT counterpart. However, as its name reveals, it still belongs to the ΣΔ modulator family, hence most concepts and understandings introduced thus far also applies to continuous time (CT) ΣΔ modulators, especially the noise shaping characteristics.

2.4.1 Theory of CT Modulators

Due to the presence of a sampler inside the loop, continuous time sigma modulator is inherently discrete [9]. This means both types of modulator may be analyzed in discrete time domain. Despite of this, the fact that continuous time filter exists in the system makes the intuitive analysis of these two types of modulators quite different from each other. For DT modulators, analysis is usually done in z-domain as the entire modulator is sampled system. For CT modulators, the loop filter is implemented in continuous time domain, thus s-domain analysis like Laplace transform is mostly implemented. Although as proposed in [10], a complete mapping between CT ΣΔ modulator and DT ΣΔ modulator is possible, the calculation is time consuming and what is more important, not all non-idealities can be migrated to discrete time domain. Thus, most analysis for CT ΣΔ modulators is still done in continuous time domain.

The primary difference between a DT modulator and CT modulator is where the sampling takes place. As can be seen in Figure 2-13, for DT modulator, sampling takes place at the input, thus any sampling non-idealities directly affect the modulator performance. Clearly, the upfront sampler in a DT modulator is the bottleneck of the entire system. On the contrary, sampling action takes place inside the loop for CT modulator, more

specifically, just before the quantizer. This is where noise suppression has the most significant effect. Thus, sampling errors introduced here are mostly noise suppressed and hence its performance is of no particular concern from system design point of view.

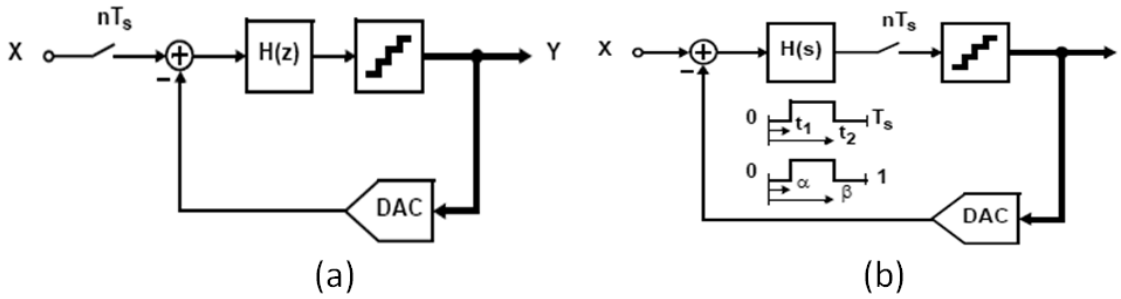


Figure 2-13 (a) DT ΣΔ Modulator (b) CT ΣΔ Modulator

However, as shown in section 2.3.2, non-idealities introduced by feedback DAC are not noise-shaped. And this problem gets aggravated for CT modulators because the modulator operation depends on continuous integration of DAC output over entire clock period. From signal processing point of view, the DAC feedback pulse is convoluted with loop filter impulse response in time domain to generate quantizer input signal. Thus the exact shape of feedback DAC is quite important. While for DT modulators, the settling requirement is more important. As long as the feedback charge is transferred within half of a clock period and output value settles well, the loop filter output is correct. Hence, exact feedback DAC pulse shape is not important. It is this difference that makes CT modulator more vulnerable to feedback pulse related problem such as finite rise/fall time, clock jitter etc.

Due to above discussed difference between DT and CT modulators, the implementation consideration for CT ΣΔ modulators is somewhat different from DT modulators. In

discussion of structure selection and tradeoff which comes in later section, special considerations for CT implementations are explicitly stated.

2.4.2 Features of Continuous Time ΣΔ Modulators

In recent years, as the need for low power low voltage, high bandwidth design becomes higher, discrete time design of ΣΔ modulator reveals severe limitations. On the other hand, their continuous time counterpart shows features which seem promising to resolve those issues. This explains why in recent years, more and more researchers turn their attention to this particular area.

Potential for Wideband Low Power Design

In a typical DT ΣΔ modulator design, due to stringent settling requirement of a SC integrator (input and output voltage needs to settle to a specific tolerance level within half a clock period), the op-amp used in a typical integrator is required to have a gain bandwidth product of over 8 times of sampling frequency. This severely restricts the highest bandwidth the modulator can achieve. Also, the high GBW requirement means high power dissipation in the op-amp.

On the other hand, in CT ΣΔ modulator design, the GBW requirement is very much relaxed. This is due to the fact that the feedback pulse is continuously fed into loop filter during the entire clock period and its output does not attempt to switch instantaneously as in the case of a switch-capacitor integrator. Figure 2-14 shows a representative output waveform employing CT waveform with DT feedback as reference. The voltage level in the integrator is not important, instead, the total charge being transferred is more of our concern. As a rule of thumb, GBW of two to three times of the sampling frequency is shown to satisfy the settling requirements for most feedback waveforms. Even lower

values of GBW are possible with acceptable performance impact [11]. A work by [12] is even able to push the GBW requirement in CT ΣΔ modulators to be below sampling frequency.

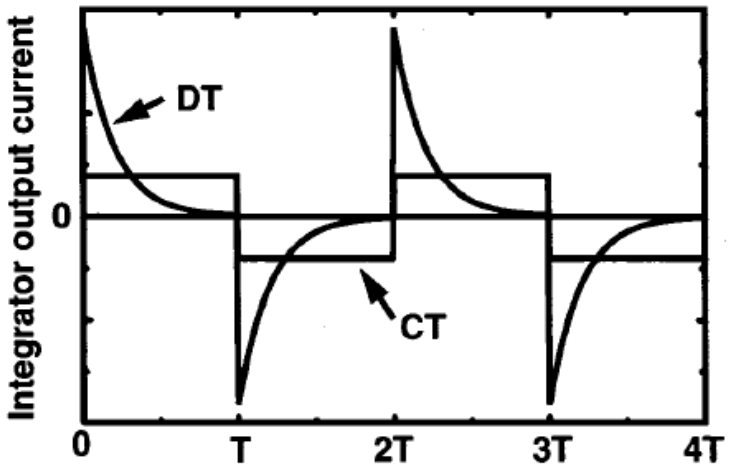


Figure 2-14 Integrator Output Current with CT Feedback vs. DT Feedback

Lowering of GBW requirements in CT design generates at least two benefits. First, higher bandwidth can be achieved than DT implementation where bandwidth is limited by Op-amp's GBW requirement. In DT ΣΔ modulator, the highest bandwidth reported is only 5MHz with resolution of just 7 bits [1]. In CT counterparts, bandwidth of 20 MHz with 12 bits of resolution has been designed [2]. Secondly, ultra low power design is possible. Relaxation of GBW requirement in the op-amp means a possible reduction in power dissipation. Also, in CT modulator, integrators in 2nd or higher stages will have an even more relaxed GBW requirement than the first stage due to noise shaping. This will further reduce the total power dissipation. Since GBW can be pushed down to a very low value, there is a possibility of designing the Op-amp for the integrator in sub-threshold region. Till now, there is no published design in this area, and this may be a promising research direction for ultra low power design.

Implicit anti-aliasing

Anti-aliasing filter (AAF) is important in mixed signal system because without it, out of band signal, especially those within the range [nf_s-f_b, nf_s+f_b], will alias into the signal band after sampling, corrupting the original signal. A very important trait of CT ΣΔ modulator that make it the more preferred choice over DT implementation is implicit anti-aliasing feature provided by continuous time filters. In CT ΣΔ modulator, when input signal is processed by STF, it is automatically attenuated around multiples of sampling frequency. Thus without AAF at input end, out of band signal around [nf_s-f_b, nf_s+f_b] is still heavily suppressed. This effect has been proven mathematically in [13] with a linear model. Here the simple conclusion is borrowed for demonstration purpose. The frequency domain input output relations can be expressed as

$$Y_S(mf_s - f) = \frac{G(f)}{dG(mf_s - f)} X(f) \qquad 2.20$$

In the above expression, $Y_S(f)$ represents the modulator output, $G(f)$ represents the loop filter function which is low pass filter and $X(f)$ is the input signal. The frequency of interest here is around sampling frequency which means $f \approx mf_s$. Hence, the numerator evaluates to a small value at high frequencies while denominator evaluates to a large number at low frequencies, therefore, we conclude a null is created around multiples of sampling frequency. From this expression, another conclusion can be drawn is the worst-aliasing occurs at the edge of the signal band.

Chapter 3
Continuous Time ΣΔ Modulator Design Issues

Due to the mixed nature of the CT ΣΔ modulator loop, the design procedure is more complicated in the case of continuous time ΣΔ Modulator design than their discrete time counterpart. However, the underlying principle remains unchanged for continuous time implementations. This makes designing CT modulator with equivalent DT modulator possible, and hence greatly reduces the design effort since the design process for DT modulator has been well established.

Despite the resemblance between CT and DT modulators in system level design, they differ a lot when circuit non-idealities are taken into consideration. Hence, modeling technique for continuous time ΣΔ Modulators is entirely different. In this chapter, the critical design issues for typical single loop CT ΣΔ Modulator are discussed.

3.1 Architecture Design Trade-offs Analysis

3.1.1 Feedforward vs. Feedback Loop Filter

As a highly non-linear feedback system, the stability of ΣΔ Modulator is of great concern. In order to achieve the best performance whilst maintain a certain degree of stability, the loop filter function requires careful placement of poles and zeros.

In order to realize specific noise transfer functions, loop filters can be configured in various topologies. The most commonly seen configurations are feedback type (Cascaded Integrator Feedback or CIFB) and feedforward type (Cascaded Integrator Feedforward or

CIFF) as shown in Figure 3-1. They achieve exactly the same noise shaping characteristic (NTF) with proper coefficient setting. But their abilities to process input signal are vastly different. This difference in turn creates deviated internal signal behavior.

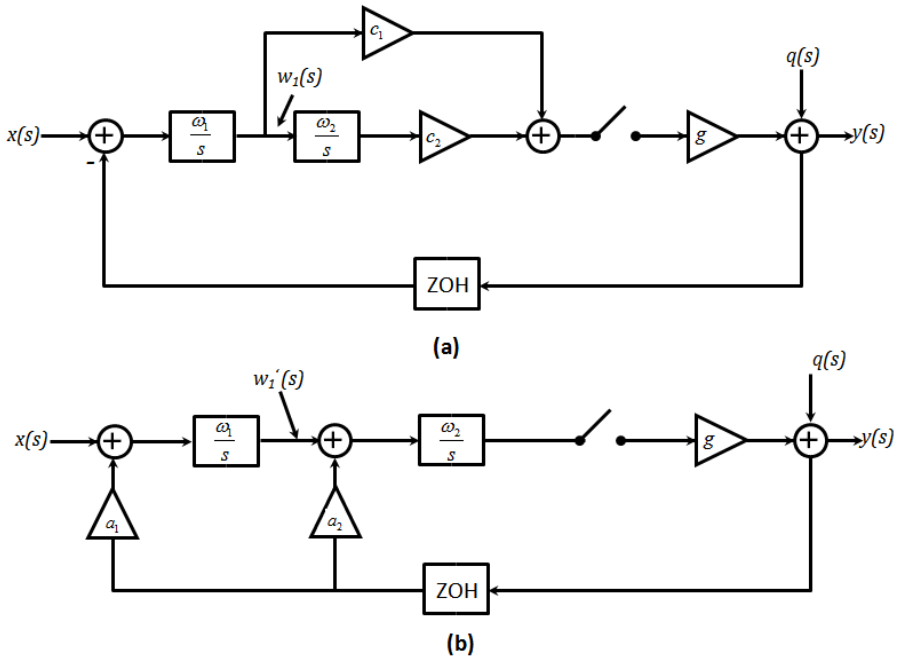


Figure 3-1 Linearized 2nd order (a) CIFF (b) CIFB Modulator

Power Efficiency

As mentioned, the noise processing abilities of feedforward and feedback architectures are the same, the difference lies in how they handle input signal differently inside the loop. Due to different signal filtering behavior, the signal swing inside the loop filter also differs which further leads to different power efficiency. This statement will be carefully explained next.

Take 2nd order modulator as example, for CIFF architecture as in Figure 3-1(a), the output of first integrator $w_1(s)$ can be represented as

$$w_1(s) \approx \frac{\omega_1 s}{s^2 + k(a_1\omega_1 s + a_2\omega_1\omega_2)} \cdot \big(x(s) - q(s)\big)$$

$$\approx \frac{s}{ka_2\omega_2} \cdot (x(s) - q(s)) \qquad 3.1$$

From the expression, we can infer that both signal and quantization noise at the output of first stage are high passed. We can further deduce that only quantization noise component is present in the internal nodes.

For feedback architecture as in Figure 3-1(b), the output of first integrator w_1'(s) can be represented as

$$w_1{}'(s) \approx \frac{\omega_1 s + ka_2\omega_1\omega_2}{s^2 + k(a_2\omega_2 s + a_1\omega_1\omega_2)} \cdot x(s) - \frac{a_1\omega_1 s}{s^2 + k(a_2\omega_2 s + a_1\omega_1\omega_2)} q(s) \qquad 3.2$$

This expression means that signal content is low-passed while quantization noise is high passed. This leads to the conclusion that the internal nodes consists a large portion of input signal.

Hence, it is not surprising that to achieve same noise shaping characteristic, feedback type suffer larger internal swing than their feedforward counterpart. Alternatively speaking, to achieve the same internal signal swing, feedback type integrator coefficient will have to be scaled more aggressively. This will reduce the first stage unity gain frequency. Reduction of first stage unity gain frequency has several implications.

Firstly, assuming the first stage implements active-RC integrator, its unity gain frequency can be expressed as $\omega_1 = {}^{1}/_{RC}$. Reduction of ω_1 would result in an increase of R or C value or both. Increasing R will reduce dynamic range which is undesirable, but increasing C would reduce amplifiers slew ability which may require higher power dissipation.

Secondly, from architecture level, it is beneficial to put early stage gain as high as possible so as to shape any non-idealities introduced in later stages.

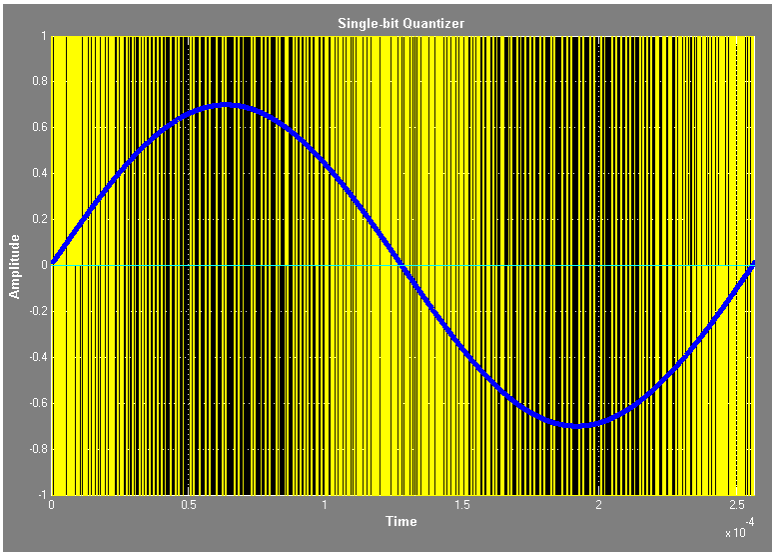
Furthermore, a closer examination of the two architectures reveals one more benefit of feedforward type configuration. As can be seen from Figure 3-1, feedforward type requires only one feedback DAC. But the feedback type has N (N is the loop filter order) feedback paths and therefore needs N feedback DACs to realize the loop transfer function. Each feedback path requires signal summation. The reduction in DAC number and summing circuit is another reason that makes feedforward architecture an attractive choice for low power design.

3.1.2 Single-bit vs. Multi-bit Quantization

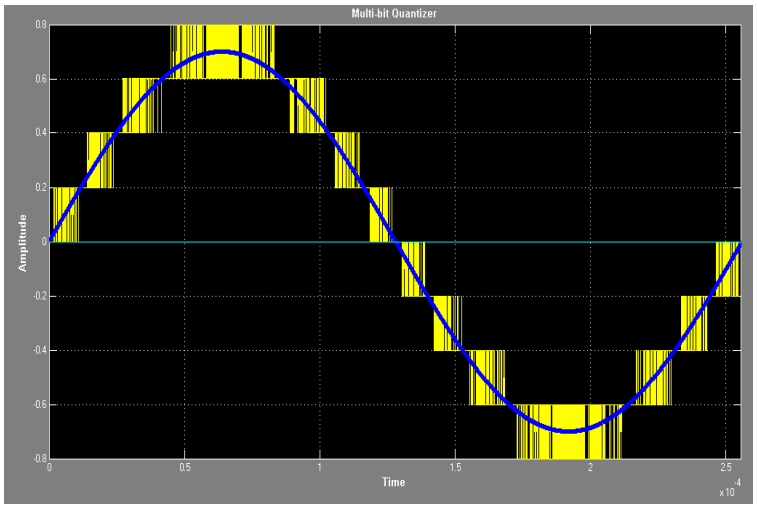
As described in chapter 2, the internal quantizer can be implemented either in single-bit or multi-bit form. These two different implementations result in different loop dynamics and require different design considerations. Hence, designers should make proper trade-offs that is most suitable for certain design goals.

Performance Achiever: Multi-bit Quantization

To understand how the difference comes from, a good starting point is to look at the comparison of output waveforms between them with input signal superimposed (Figure 3-2).



(a)



(b)

Figure 3-2 Output waveforms of (a) Single-bit Modulator (b) Multi-bit Modulator

A simple observation suggests that multi-bit output signal follow its input much more closely than single-bit counterpart. This results in much lowered quantization error in multi-bit structure. In theory, for multi-bit quantizer, its quantization error is distributed within [-Δ/2, Δ/2], where Δ is the quantization step width defined as $\frac{FS}{2^B-1}$. In single-bit quantizer, its quantization error is distributed within [*-FS/2, FS/2*]. The most direct

benefit from the reduction in quantization error is improved stability and SNR performance.

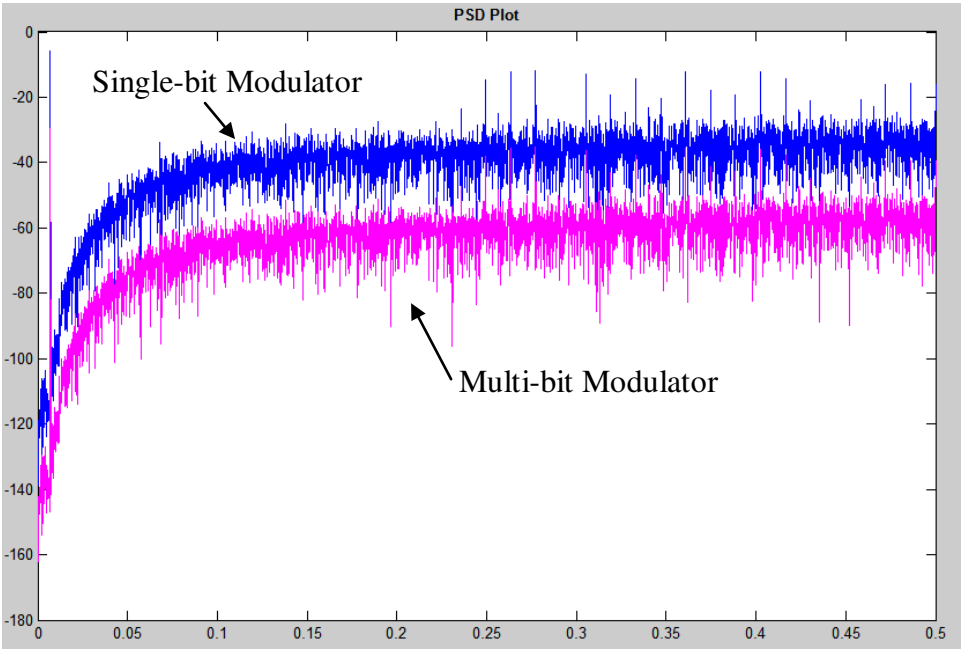


Figure 3-3 PSD plot of Single-bit Modulator vs. Multi-bit Modulator

Smaller quantization error lowers the out-of-band noise floor and hence can incorporate a larger input signal without causing overloading or instability. Figure 3-3 is a PSD plot of a single-bit modulator vs. multi-bit modulator. It is obvious that the both the in-band and the out-of-band noise are significantly lowered.

Usually, in multi-bit design, out-of-band gain can be set as high as 3. But in one-bit design, out-of-band gain normally cannot exceed 1.5 for reasonable dynamic range. This grants multi-bit structure higher achievable SNR.

Another advantage of multi-bit design is regarding its jitter performance. Jitter noise is strongly related to the activity of output pulse transitions. Intuitively speaking, smaller transitional changes and fewer transitions would result in less amount of charge variation due to jitter. [14] demonstrates that with large internal quantization level, the improvement in resolution can exceeds 11 dB.

Power Saver: Single-bit Quantization

Despite of the superior performance multi-bit quantization is able to achieve, it is punished on the power aspects. Fundamentally speaking, multi-bit quantization trades power and circuit complexity for performance. To achieve multi-bit quantization, an internal ADC is required. For stringent speed requirements, internal ADC is most likely implemented as flash ADC. Flash ADC is known for its high power consumption and large area occupation due to large number $(2^B - 1)$ of comparators required.

At the same time, multi-bit quantization requires multi-bit DAC feedback. The problem of DAC feedback is the linearity issue. This is due to the inevitable mismatch between current DAC cells. Such linearity issue impacts system directly since the DAC output current/voltage is directly feed into the input stage where no noise shaping is provided. Non-linearity of feedback DAC determines the achievable system performance and hence must be at least of modulator's overall resolution. For such stringent requirement, special circuit techniques like mismatch shaped DAC which employs randomization logic on current cells such as DWA, DEM and current calibration are necessary. Hence more chip area and power budget must be invested into this additional block. In CT ΣΔ modulator design, this block also introduces additional excess loop delay.

Single-bit internal quantization results in simplest modulator design. Hence, both area and power consumption can be saved, making compact, ultra-low power design possible. Author in [5] stated that single-bit internal quantization structure usually results in the most power efficient design. Hence, it is the best choice for ultra low power design with moderate performance requirement. In 1-bit design, the trade-off between conversion speed (bandwidth) and resolution (DR) is quite obvious.

Additionally speaking, power supply is another important system parameter that requires careful consideration. Reduced power supply voltage would impact single-bit and multi-bit quantizer in different manner. A reduced power supply voltage would results in reduced full scale range and hence reduced step size for ADC. In such case, multi-bit ADC is more susceptible to circuit noise than single-bit ADC. This is because circuit noise generally doesn't scale down with reduced power supply. Hence, relatively speaking, noise margin for multi-bit ADC shrink by a larger percentage while it affects single-bit ADC not so seriously. In this sense, single-bit implementation is superior to multi-bit implementation in the aspect of power supply scaling.

Table 3-1 briefly summarizes the above discussion on quantization bit.

Table 3-1 Comparison of Single-bit Quantizer and Multi-bit Quantizer

	Stability	Achievable SNR	Linearity Requirement	Circuit Complexity and Power Consumption	Jitter	Power Supply Scaling
Single-bit Quantizer	-	-	+	+	-	+
Multi-bit Quantizer	+	+	-	-	+	-

'+' denotes good, '-' denotes poor for that specific comparison

From the above comparison, it is clear that multi-bit quantizer is superior to single-bit quantizer in terms of achievable performance. But single bit design has particular advantage in the aspects of circuit simplicity and power consumption.

Single-bit Pulse Stream Generation in Audio Signal Processing

As introduced in Chapter 1, 1-bit pulse stream is the intermediate media format prior to conversion into CD format for audio signal processing. If multi-bit ΣΔ modulator is used as front end analog input encoding method, this multi-bit digital signal has to go through

further signal processing to be converted into 1-bit PDM stream. This step requires quite handsome amount of circuit overhead and introduces signal quality degradation. With the development of new media format (Direct Stream Digital, or DSD), the generation of 1-bit PDM stream is more and more important. Hence, it is beneficial to generate the 1-bit PDM directly for least amount of signal processing steps required. The key is to design a high performance single-bit ΣΔ modulator for that purpose.

3.1.3 DAC Pulse Shape

In discrete time sigma delta modulators, feedback is implemented in switch-capacitor form, and feedback charge is transferred within a very short duration. This is to ensure the voltage in the first integrator is settled to an acceptable error. Only the final settling accuracy is important and the actual shape of the feedback pulse is irrelevant to the modulator's performance.

On the contrary, the feedback DAC shape plays a critical role in determining the performance of a continuous time ΣΔ Modulator. Due to implementation of continuous time loop filter, the feedback pulses are continuously integrated from cycle to cycle and cannot be treated as simple digital pulses any more. Instead, it is more appropriate to treat it as another analog input. Hence, both its shape and timing information have impacts on the modulators' performance.

NRZ & RZ Feedback Pulse

In CT ΣΔ Modulator design, switched current feedback is the most commonly used feedback technique. For simplistic design, rectangular feedback pulse shape is preferred.

Based on the length of feedback pulse, rectangular pulse can be further subdivided into Non-Return-to-Zero type (NRZ) and Return-to-Zero type (RZ) as shown in Figure 3-4.

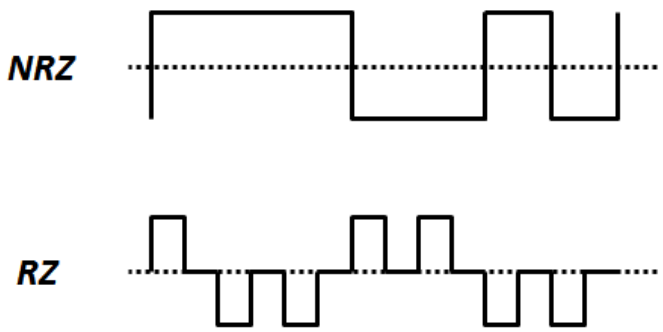


Figure 3-4 NRZ and RZ Feedback Pulses

It is easy to conclude that NRZ pulses feedback more charges than RZ pulses every cycle. This result in a difference in input signal dynamic range. For RZ feedback type modulators, input signal has to be scaled down to maintain stability and hence a certain amount of dynamic range is lost.

Generally speaking, NRZ feedback method is the most power efficient technique both because of its simple implementation and maximum amount of feedback. However, it does have several shortcomings which hinder its implementation in high performance system.

First, a dynamic error which is caused by unequal rise/fall time can occur during switching transient, which is also known as Inter-Symbol Interference (ISI). In NRZ feedback system, the ISI exhibits signal dependency, causing the appearance of distortion tones in the output spectrum and hence degrading the overall SNR. It is demonstrated in [15] that even order harmonic distortion will be generated. To understand this effect, an intuitive illustration is given below.

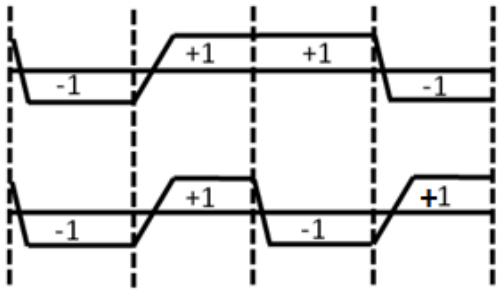


Figure 3-5 ISI Effect Demonstrated by Two DAC Feedback Sequences

From Figure 3-5, one can see that a 0110 pattern and 0101 pattern would results in different amount of feedback charges being integrated and is signal dependent. This effect will be further investigated later.

Another problem with NRZ feedback is excess loop delay. Research shows NRZ pulses are more sensitive to excess loop delay. Performance loss or even instability may result. This effect will be further discussed in detail in chapter 4.

Return-to-Zero (RZ) feedback technique justifies its existence by solving the problems related with NRZ feedback. Since feedback pulses returns to '0' level during every cycle, the transition behavior is identical in each cycle, eliminating any pulse dependency on the input signal. Furthermore, since RZ feedback pulses only operate half cycle, they have better immunity to excess loop delay than NRZ pulses.

In this research, RZ is the predominant research focus due to its flexibility for pulse shaping. Pulse shaping is a powerful method for solving jitter noise issue. Since NRZ pulse shape is fixed, its jitter performance depends on the quality of the clock. But RZ pulses can be shaped for jitter noise reduction. Pulse shaping technique will be thoroughly explained in chapter 4.

3.2 Modulator Coefficients Calculation & Scaling

3.2.1 DT-to-CT Transformation

Design procedure of DT ΣΔ modulators is quite well established in the past decades. Specifically, tools are available for automatic design synthesis [16] [17]. The design of a ΣΔ modulator is, to a large extend, the design of a NTF which satisfies the required noise suppression and dynamic range. Once the NTF is chosen, it can be mapped onto the selected filter topology, and hence the scaling coefficients for the loop filter can be determined.

For CT ΣΔ modulator design, its NTF can be determined through proper choice of filter function with added consideration about stability. Such method has been reported in several works [18].

However, although direct synthesis is straightforward and intuitive, it is not the optimal approach. This is because methodologies and tools in DT modulator design have been well developed. The design and synthesis is automated which requires almost no complicated filter design. If such established procedure can be utilized, the effort of synthesizing a CT ΣΔ modulator is much reduced. Such approach is possible with proper DT to CT transformation [19]. This concept works because of the fundamental equivalence between DT ΣΔ modulator and CT ΣΔ modulator as both systems can be regarded as sampled system.

Suppose there are a DT modulator and a CT modulator with same quantizer. As long as the loop filter outputs, which is also the point feeding into the quantizers, are same at every sampling instant for both the CT and DT modulators, the quantizers makes the

same decision. This means the two modulators are equivalent and have the same noise suppression characteristic. Mathematically, it can be analyzed as follows.

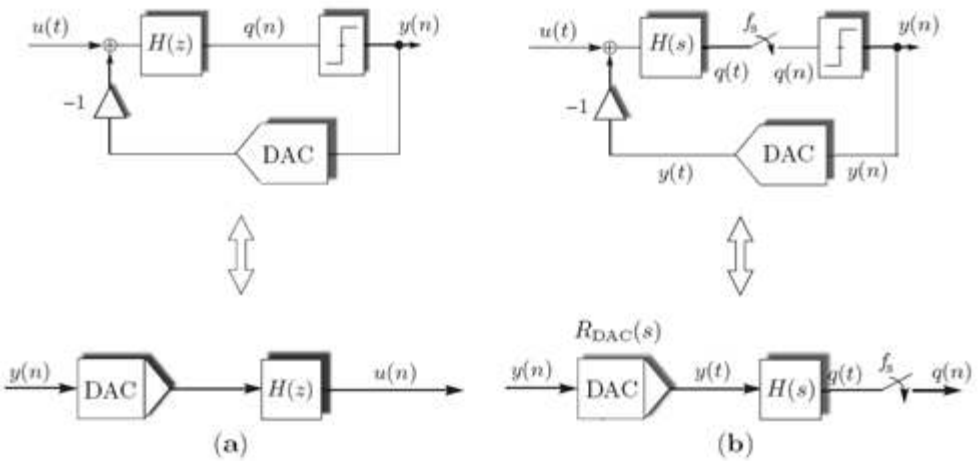


Figure 3-6 (a) DT Modulator and its Feedback Equivalence (b) CT Modulator and its Feedback Equivalence

Figure 3-6 shows a discrete time modulator and a continuous time modulator. Both loops are opened before the feedback DAC. These two system is equivalent if the input to both quantizers *q(n)* and *q(t)* are the same at the sampling instants, i.e.

$$q(n) = q(t)|_{t=nT_s} \tag{3.3}$$

Based on this equivalence, a DT loop filter can be transformed into its CT equivalence through a method called impulse invariant transformation (IIT). This idea is shown as equation 3.1, which states

$$Z^{-1}\{H(z)\} = L^{-1}\{R_{DAC}(s)H(s)\}|_{t=nT_s} \tag{3.4}$$

In the time domain, this leads to

$$h(n) = [r_{DAC}(t) * h(t)]|_{t=nT_s} = \int_{-\infty}^{+\infty} r_{DAC}(\tau) * h(t-\tau)\, d\tau|_{t=nT_s} \tag{3.5}$$

It can be inferred that this method can transform any feedback pulse shape as long as the DAC transfer function is provided. [19] provided a whole range of transfer functions for commonly used feedback pulse shapes.

3.2.2 Coefficient Calculation & Scaling: An Automated Approach

Thanks to the direct transformation from DT-to-CT, calculation of a CT loop filter transfer function now has almost the same complexity as its DT counterpart. And the whole process can be automated by Matlab commands. The calculation of coefficients roughly takes following steps:

- Using existing toolbox (in Matlab), calculate optimum NTF based on specific modulator parameters (modulator order, OSR, OBG). The obtained NTF is in z domain. From NTF(z), the discrete time domain equivalent loop transfer function $L_1(z)$ for feedback signal is calculated from the relation $NTF(z) = \frac{1}{1-L_1(z)}$.
- Perform DT-to-CT transformation on $L_1(z)$ using either IIT or modified z transform. Continuous time equivalent loop transfer function $L_1(s)$ is obtained. For rectangular shaped feedback pulses, this process can be carried out in Matlab by a simple command d2cm (for NRZ) or d2c (for RZ). For other pulse shapes, there is no express command available. Hence, one of the above methods has to be used. Symbolic math tool Maple is capable of doing the transformation that is too complicated for hand calculation. For some well studied pulse shapes like SCR (Switch-Capacitor Resistor), transformation tables are available in literature [19].
- After obtaining the continuous time loop transfer function $L_1(s)$, it is ready to be mapped onto the designed modulator architecture. By equating the obtained loop transfer function with modulator's loop transfer function expressed by unknown

coefficients, a set of equations is obtained. Solve the equations simultaneously, and the desired coefficients are obtained.

- The calculated coefficients in step 3 only ensures correct operation without considering circuit limitations like finite output swing of each integrator. Thus, coefficients must be further scaled. This process involves extensive simulation to find out the maximum swing at each node. In [17], it claims the worst case situation which induces maximum internal swing before modulator goes into instable condition is excited by injecting a slowly raised DC input with certain level of random noise. Usually the noise source has zero mean and 1% deviation from the DC level. The internal signal scaling is performed by reducing all incoming branches by a factor m and multiplying all outgoing branches by the same factor m as depicted in Figure 3-7. In this way, the signal in the main path is kept unchanged, preserving the original characteristics of the modulator. At the same time, internal state is scaled down to prevent circuit from signal clipping.

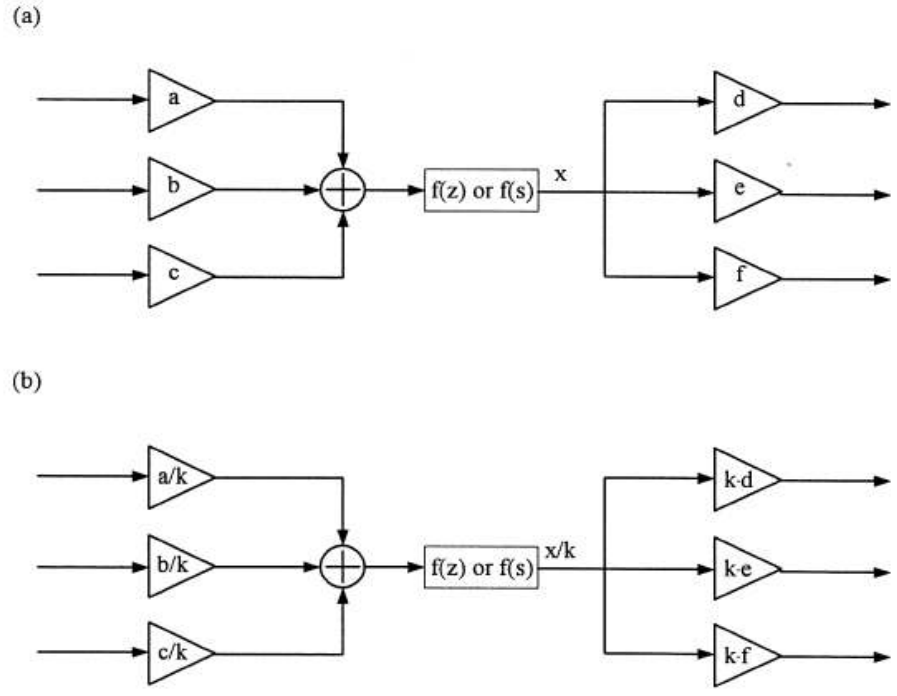


Figure 3-7 Signal Scaling in Integrator

3.3 Circuit Based Differential Behavioral Model

Nowadays, the most popular design methodology for system level design like ADC is top down design, bottom up verification. Behavior blocks are built with critical non-idealities being taken into consideration. The reason that top down design methodology has become the standard design procedure in nowadays ΣΔ modulator design is that it greatly improves the overall design efficiency. For a complicated system like a ΣΔ modulator, full transistor level simulation is extremely time consuming, hence, it is beneficial to obtain a confident specification for various circuit component before full circuit realization. This task can be accomplished by efficient behavioral level simulations. Behavioral model normally implement macro models and make necessary simplifications. Hence, it is sufficiently fast with of course some compromise in accuracy. However, if the modeling is thoroughly considered, a high level of confidence could be obtained as well.

In the past, modeling of critical circuit non-idealities has been reported in [20]. All of them use over-simplified block level modeling technique. Although they promise fast simulation speed, they provides little intuition about non-idealities and design considerations for circuit level implementation. Differential pseudo-circuit model developed in this project provides better way for behavioral simulation. At first, a Simulink-based model was developed [21]. Then it was transplanted to Cadence Spectre platform. Behavioral model in Spectre allows simulations with mixture of behavioral model and circuit level blocks. This feature is invaluable for block level performance verification and debugging, achieving seamless transformation from behavioral model to circuit implementation. This speeds up the design flow as well as providing a reliable way for backward performance verification. Firstly, modeling of some basic blocks is introduced.

Differential Op-Amps

Op-amp is the core component in an active-RC integrator. It is extremely important if it is used in first stage as it has no noise shaping to its non-idealities. Here a differential model is proposed using basic analog component.

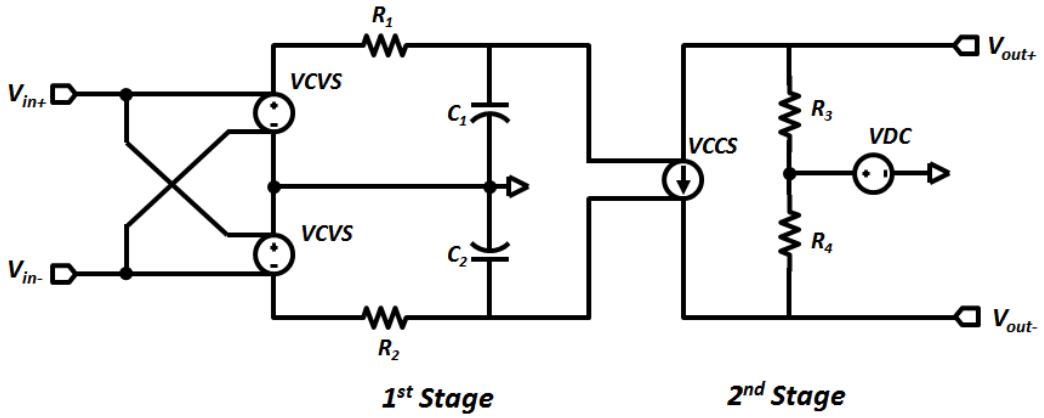


Figure 3-8 Behavior Model of First Stage Op-amp

This model is based on single pole model of a basic OTA structure. The DC gain can be varied through VCVS (Voltage Controlled Voltage Source) settings and its first pole location (or bandwidth) can be adjusted by the RC time constant in the first stage. The 2nd stage uses VCCS (Voltage Controlled Current Source) to define the OTA's current abilities and output resistance is defined through the two parallel resistors. The VDC in the 2nd stage defines the output common mode level.

Differential Transconductors

This block is quite similar to the differential Op-amp shown above. The VCCS source defines the transconductance and the parallel resistors model the realistic output resistances. Output common mode level can be defined using VDC sources as well.

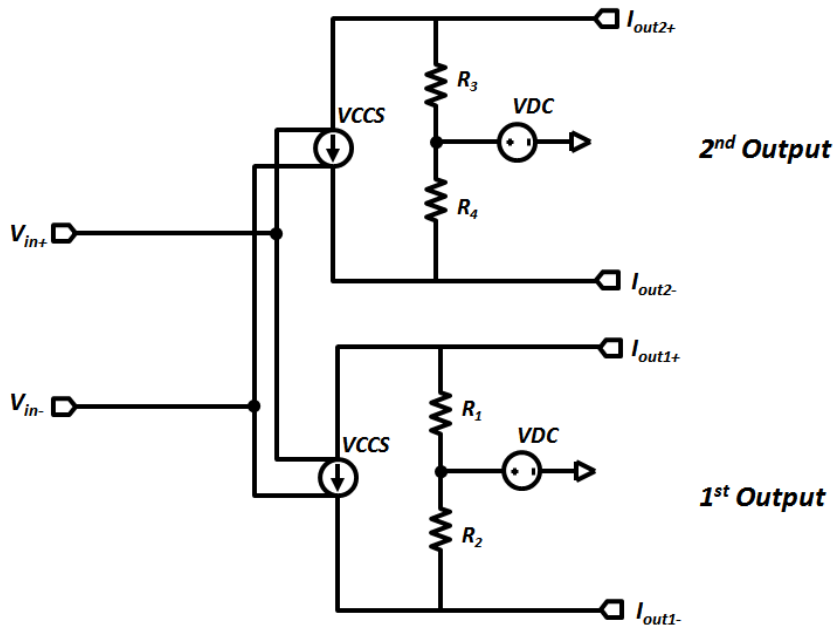


Figure 3-9 Behavior Model of Multiple-outputs Transconductor

Jittered Clock

Real clock signal suffers from imperfection called jitter (or phase noise). It has been demonstrated that clock jitter creates serious trouble for CT ΣΔ Modulator. Thus this effect must be accurately modeled and examined. In [22], a Verilog-A model of jittered clock has been proposed. Thanks to the capability of Cadence Spectre simulator, this Verilog-A model can be directly simulated with other circuit models, providing enormous modeling convenience.

3.4 Critical Circuit Non-idealities and Their Effects

As mentioned previously, correct and accurate modeling of individual blocks not only reduces the design turnaround time but also provides better performance prediction.

Hence, during the design of a ΣΔ Modulator, normally more than half of the time is spent with behavioral models.

ΣΔ Modulators (CT & DT) basically trades conversion speed for resolution. Due to noise shaping, harsh requirements on circuit are greatly relaxed. Noise and non-idealities in internal nodes are attenuated by the gain of previous stages, creating negligible trouble. But the input stage which typically includes 1st stage integrator and feedback DAC is not noise shaped and represents the most vulnerable point in the system. Any noise added here is indistinguishable from desired signal and reduce achievable SNR. Hence, most investigative effort is devoted in input stage for the purpose of avoiding ill design practice. During non-ideality analysis, each time only one non-idealities is in action in order to examine its true behavior. In this section, non-idealities at front end are examined. All simulations are carried out based on models developed in Simulink and Cadence Spectre environment, depending on the simplicity and accuracy for respective models.

3.4.1 Finite Gain Bandwidth Effect

Active-RC integrator is normally implemented as the 1st stage integrator for its superior linearity and wide input range. The ideal integrator transfer function $\frac{k \cdot f_s}{s}$ assumes an ideal Op-amp. However, this is far from reality. Real Op-amp has finite DC gain and bandwidth. To analyze this effect, we assume a simple singe-end model as shown in Figure 3-10.

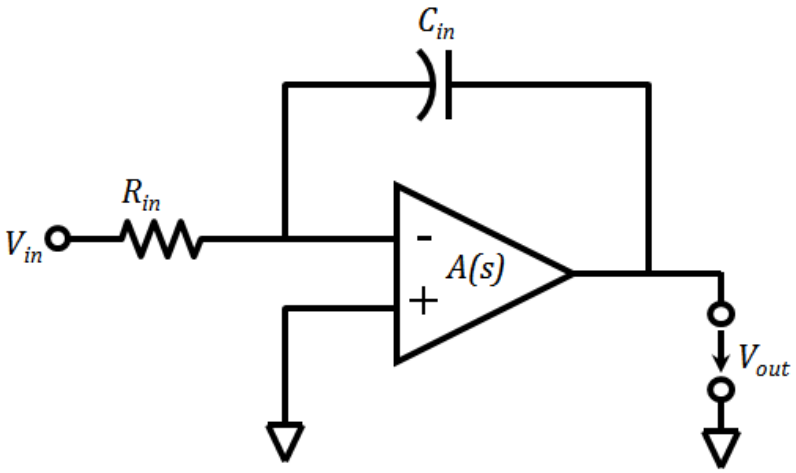


Figure 3-10 A Simplified Active-RC integrator Model

If we were to further assume a single pole model for the Op-amp used in the active-RC integrator, the integrator transfer function can be deduced in a simple way as shown below.

A single pole Op-amp characteristic can be expressed as

$$A(s) = \frac{A_{DC}}{1 + \frac{s}{\omega_1}} \tag{3.6}$$

Where A_{DC} is the finite DC gain and ω_1 is the 3-dB bandwidth.

By simple mathematical manipulation, the modulator transfer function in s-domain can be easily obtained as

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-1}{R_{in}} \cdot \frac{1}{\frac{1}{A_{DC}}\left(\frac{1}{R_{in}} + \frac{1}{R_{DAC}}\right) + \left[\frac{1}{\omega_u}\left(\frac{1}{R_{in}} + \frac{1}{R_{DAC}}\right) + \left(1 + \frac{1}{A_{DC}}\right)C\right]s + \frac{C}{\omega_u}s^2} \tag{3.7}$$

where $\omega_u = A_{DC} \cdot \omega_1$, which represents gain bandwidth product (GBW). In the above expression, the constant terms in the denominator of the second fraction can be ignored due to usually large DC gain. After rearrangement, the above expression is reduced to

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-1}{sR_{in}C} \cdot \frac{1 - \dfrac{\frac{1}{C}\left(\frac{1}{R_{in}} + \frac{1}{R_{DAC}}\right)}{\omega_u + \frac{1}{C}\left(\frac{1}{R_{in}} + \frac{1}{R_{DAC}}\right)}}{1 + \dfrac{s}{\omega_u + \frac{1}{C}\left(\frac{1}{R_{in}} + \frac{1}{R_{DAC}}\right)}} \qquad 3.8$$

The 1st part of Eqn. 3.8 represents the ideal transfer function, and the 2nd part is caused by finite GBW of the Op-amp. It is clear that the finite gain bandwidth introduces a reduction in gain as well as a 2nd pole into the ideal transfer function. The reduction in gain is equivalent to coefficient variation and the extra pole can be modeled as a delay and treated in the same way as excess loop delay [12].

If we further simplify Eqn. 3.8, even more intuitive results appear. Assume the input resistor is equal to feedback resistor which is almost always the case, then $\frac{1}{C}\left(\frac{1}{R_{in}} + \frac{1}{R_{DAC}}\right)$ can be replaced with $2k_{in}f_s$. And we replace ω_u with mf_s, we arrive at

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-1}{sR_{in}C} \cdot \frac{1 - \dfrac{1}{\dfrac{m}{2k_{in}} + 1}}{1 + \dfrac{s}{(m + 2k_{in})f_s}} \qquad 3.9$$

The extra pole due to finite GBW is several times away from $k_{in}f_s$. Such high frequency creates no effect on the input signal, but it imposes extra filtering effect on feedback signal as feedback signals contains wide band quantization noise. In [19], this filtering has been demonstrated as having the same effect as introducing a delay.

Reduction in gain reduces the aggressiveness of the noise shaping and hence results in increase of in-band noise. Suppose $k_{in} = 0.5$, if $m < 3$, a gain reduction of more than 25% is expected.

The delay effect of the GBW effect can be seen from the step response of the active-RC integrator as shown in Figure 3-11. Smaller GBW creates larger delay and such effect is dependent on output amplitude as well. At large voltage swing, the delay is also larger. This makes the prediction and compensation of GBW effect on overall performance highly challenging. Hence, usually the critical bound are to be found through extensive behavioral simulation.

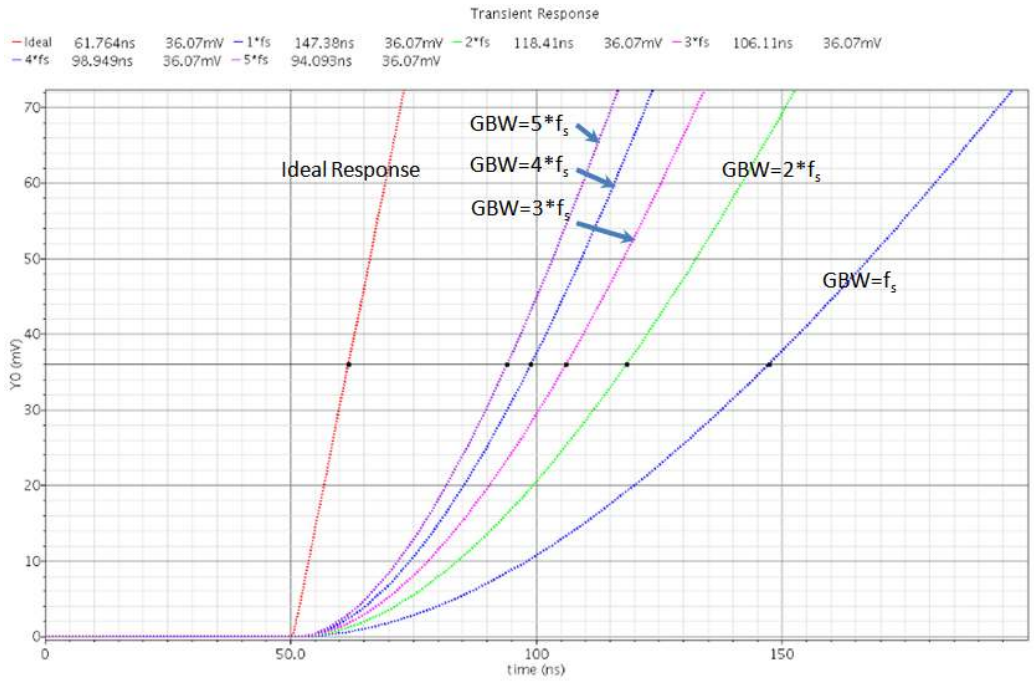


Figure 3-11 Step Response of Integrators with Different GBW Values

Behavioral simulation to show GBW variation effect on SNDR has also been conducted and the result is shown in Figure 3-12.

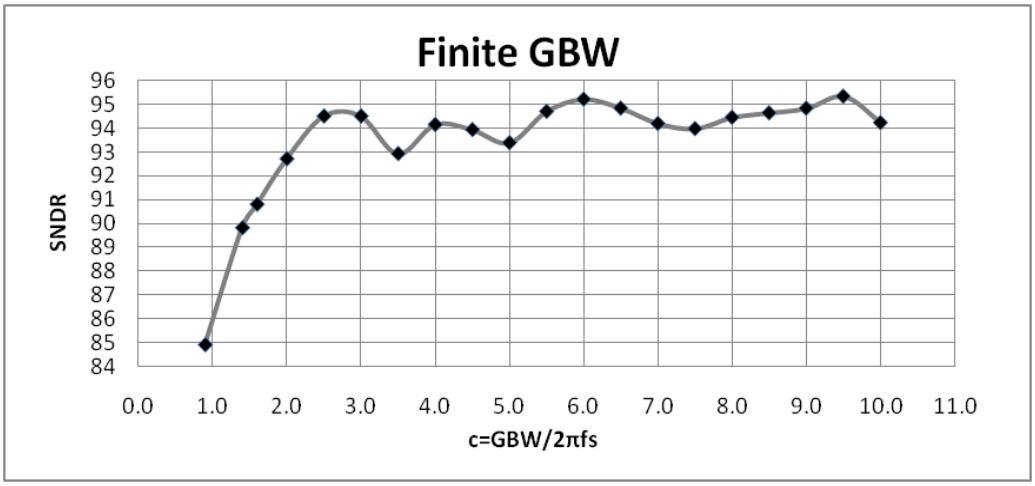


Figure 3-12 Finite GBW vs. SNDR for CT Modulator

The result shows that only with GBW greater than $3f_s$, excessive SNR degradation can be avoided. However, as explained above, the real requirements on the Op-amp depends on the scaling coefficients of first stage and varies from design to design.

3.4.2 Coefficients Variation

Coefficients variation is a main disadvantage of CT modulator comparing to its DT counterpart. In CT integrators, coefficients are determined either by RC product or Gm/C ratio, depending on implementation technique. Either implementation method is subject to significant process variations. Typically, in modern CMOS technology, matching accuracy and process spread of R and C are still quite poor. 30% or even more variations in RC time constant and g_m/C ratio may be expected for CT integrators. On the other hand, DT modulators implements switched-capacitor integrator whose coefficients are determined by capacitor ratios. Hence, matching accuracy of less than 1% is normal in DT implementations. Such variation causes performance deviation from expected value for CT integrators. To understand how such deviation occurs, we see how coefficients and circuit parameters are related.

For typical active-RC integrator

$$\frac{1}{RC} = kf_s \tag{3.10}$$

And for transconductor-C integrator

$$\frac{g_m}{C} = kf_s \tag{3.11}$$

Circuit components variations cause direct variations of scaling coefficients. Scaling coefficients in turn has implications on the noise shaping. Too aggressive noise shaping causes instability, while too mild noise shaping causes degradation in SNDR. Since the modulator is composed of several stages, the coefficients of the individual stage may shift together or in different way. However, the worst case happens when they shift in the same direction. This is because in such case, averaging effect is not happening, hence, creating the maximum loop gain deviation. To simulate the worst case scenario, we assume all the coefficients drift in the same direction. The SNDR plot vs. variation in coefficients is shown in Figure 3-13.

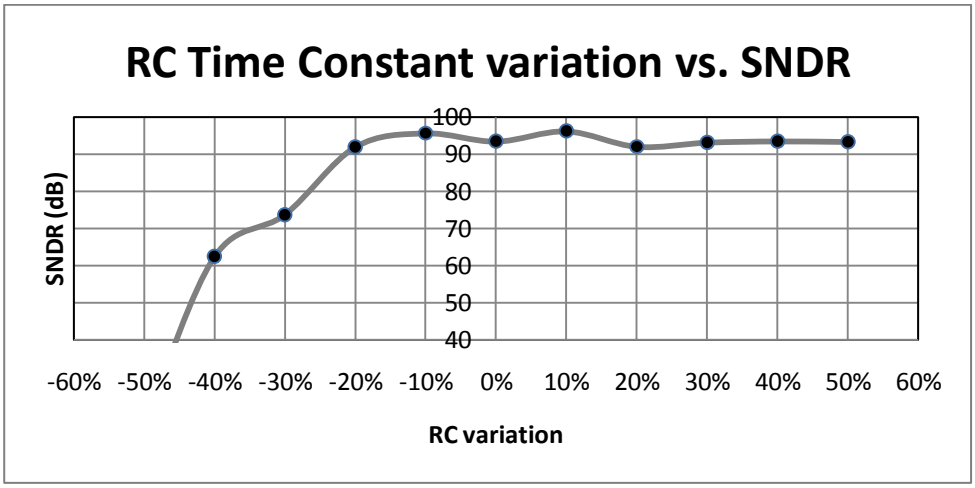


Figure 3-13 RC Product Variation vs. SNDR

The result is easily understood. If the coefficients vary in the negative direction (RC product in positive direction), the loop gain drops, meaning a less aggressive noise shaping, and hence a drop in SNDR. However, this does not lead to unstable condition. If coefficients get bigger (RC product gets smaller), the noise shaping becomes more aggressive, so the performance first rises, and then goes to instability.

Since it is all about noise shaping, it is logical to think a lower out-of-band gain would results in a more stable modulator, meaning a larger coefficients variation may be tolerated. But the sacrifice to make is the achievable peak SNDR.

Positive movement of coefficients also causes swing of internal nodes to increase accordingly. In a real design, this may lead to clipping hence distortion. For differential system, clipping causes odd order distortion but not even order distortion. For example, if the first stage coefficients are increased by 50%, the output swing of every integrator would increase by 50%, for a modulator whose internal nodes were originally scaled at 0.8, now the signal may reach 1.2. However, from investigation through simulation, clipping has limited effect on the modulator performance. For example, 50% increase in input stage coefficients leads to almost unnoticeable performance deviation. This is probably because clipping happens at every integrator output node which is subjected to at least one order of noise shaping. Only when coefficients deviation reach around 100%, the SNDR drop is considered significant which is around 7~10 dB. However, such a huge variation in circuit parameters may be too pessimistic to be realistic.

The results presented above provide useful insight into how to counteract the coefficients variation issue. In most cases, stability is the foremost concern. If the variation range is predictable in a given technology, the coefficients can be scaled towards a smaller value such that even if the worst case happens, instability can still be avoided. If the tolerable range is not wide enough, smaller out-of-band gain may be specified when computing

loop transfer function. However, such approaches trade stability for performance. If both stability and performance are important, then coefficient tuning is necessary. In active-RC or Gm-C integrators, capacitor array tuning is the most popular method for its wide tuning range and easy implementation. Other methods also exist as shown in [22][23]. However, it is best to keep tuning circuitry as simple and power efficient as possible.

3.4.3 Slew Rate Limitation

Slew rate is another important concern for the design of the first stage Op-amp. For multi-bit integrator where quantization error is small, it usually does not cause too much trouble. However, in single bit modulators, quantization error amplitude may be large enough to cause a problem. In most cases, in order to achieve ultra low power design, the current capability of the Op-amp is also reduced. However, due to non-linear nature of slew rate effect, it introduces strong non-linearity into the modulator if it actually happens. Figure 3-14 plots how the spectrum is affected by slew rate.

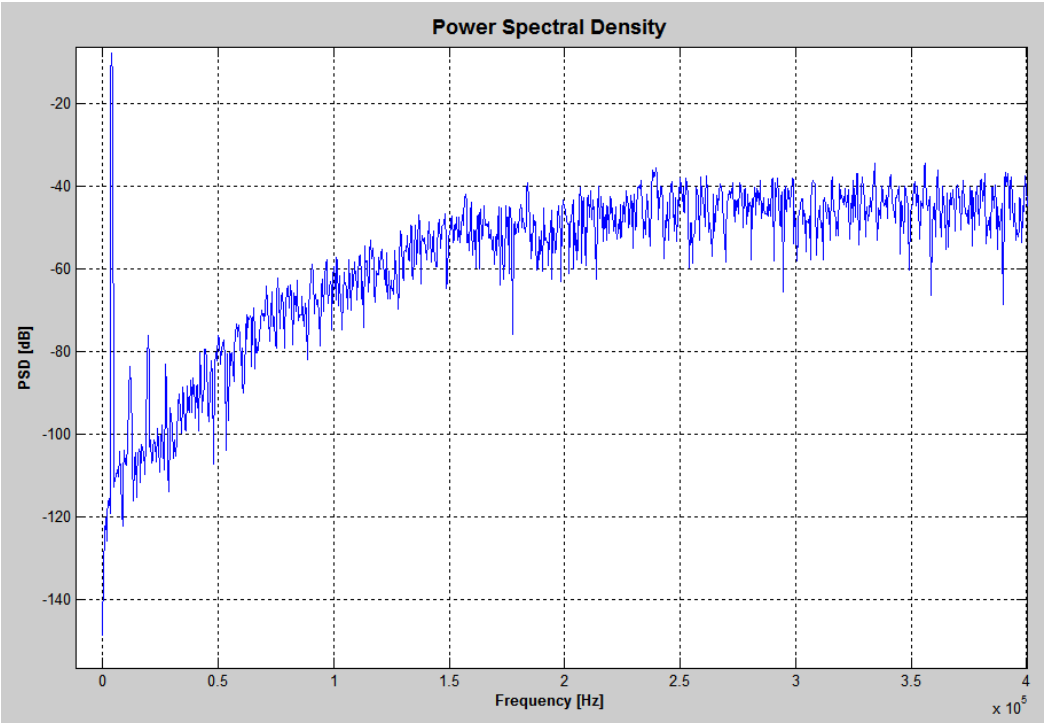


Figure 3-14 PSD of a CT Modulator under Slew Rate Limitation

From the PSD plot, it is very clear that strong tones are introduced. From a series of simulation, it can be shown that slew leads to rapid loss of SNDR and even causes instability.

In single-bit modulator, the slew rate requirement for the first stage integrator is quite easy to obtain. Since the input to the integrator is the derivation of its output, hence, this input is the actual rate of change of the output. For an integrator which takes sinusoidal input $Acos(\omega t)$, and supposes the integrator gain is kf_s, the slew rate requirement is $Akf_s cos(\omega t)$. The worst case happens when the input is DC signals which require a slew rate of Akf_s. This is especially true for the input to the first stage. Due to high oversampling ratio, the input signal can be regarded as constant during one clock cycle. And since the feedback pulse is of square shape, the worst case happens when these two magnitudes add together. Hence, the requirement for the slew rate of the first stage Op-amp is

$$\Delta = \frac{FS}{2^{B-1}} \tag{3.12}$$

For later (2^{nd}, 3^{rd}, 4^{th}) stages, as the low frequency band are gradually suppressed , plus noise shaping provided by previous stages, the slew rate requirements are generally lower than worst case values of respective stages. But simulation shows that performance degradation will also occur when internal nodes suffers serious slew rate limitation. Hence, this bound should be treated carefully.

3.4.4 Offset and Tones

In real circuit implementation, mismatch creates offset in the modulator. For example the input referred DC offset for the Op-amp in the first stage integrator and the offset of the input common mode level. During analysis, the most intuitive way to interpret the offset

is to refer various offset sources to the input and treat them as DC input signal. DC signal not only creates DC content in output spectrum but also develop regular patterns in 1-bit output sequence which is manifested as tones. Tones can be dangerous for audio system. While DC component can be eliminated by DC blocking mechanism in signal post processing, tones cannot be eliminated.

According to [13], it is shown that baseband tonal frequency occurs at

$$f_{tone} = \frac{v_{offset}}{FS} \cdot mf_s \qquad 3.13$$

It can be inferred from the above equation that a larger offset would make the tones to occur at higher frequencies. However, it is demonstrated that the power of the tones is also positively related to its frequency. At low frequencies, the tones are so low that in most of the cases they are buried in the noise floor. On the other hand, if the offset becomes too large, the dynamic range of the system will be affected. Simulation has been done to investigate this effect. It can be shown that an input referred offset voltage as large as 5mV for the Op-amp in the first stage integrator would not create much degradation in dynamic range and performance. Hence, offset induced tonal effect is not the primary concern for this research.

3.4.5 Inter-symbol Interference (ISI) in NRZ

ISI effect is considered to be a significant disadvantage of NRZ feedback implementation. To model this ISI effect, a rate limiter block is added after the DAC block to limit the rise and fall time of feedback signal. For a differential system, the effective rise and fall time are equal. Figure 3-15 below shows a 3rd order modulator with sampling rate of 3.2MHz under the effect of finite DAC rise/fall time.

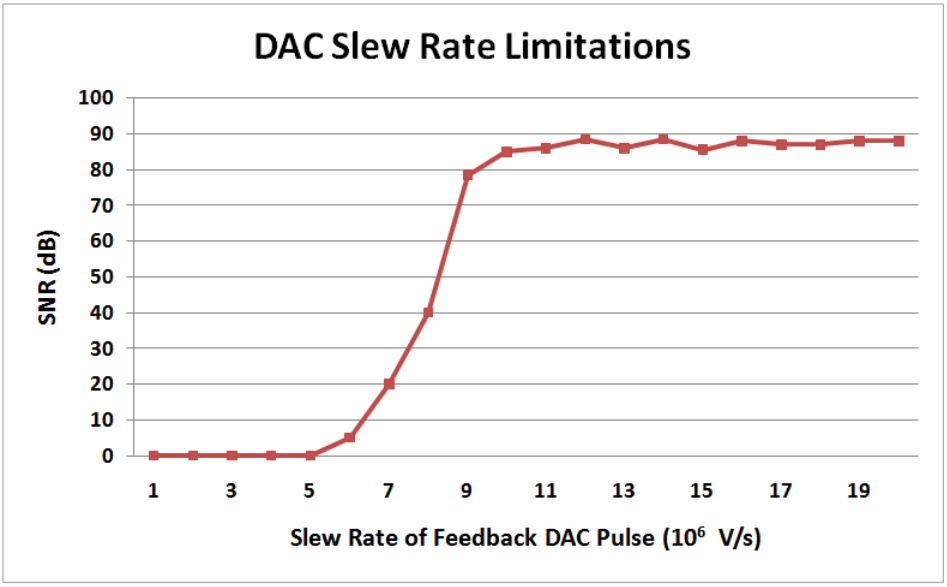


Figure 3-15 ISI Effect of CT ΣΔ Modulator

The results shows that the ISI effect would results in performance degradation only when the slew rate of the feedback DAC cell falls below 10V/μs. Under the simulation condition where the sampling rate is 3.2 MHz, rise and fall time occupy a large portion of clock period. This would results in an ill-shaped feedback pulse as shown in Figure 3-16.

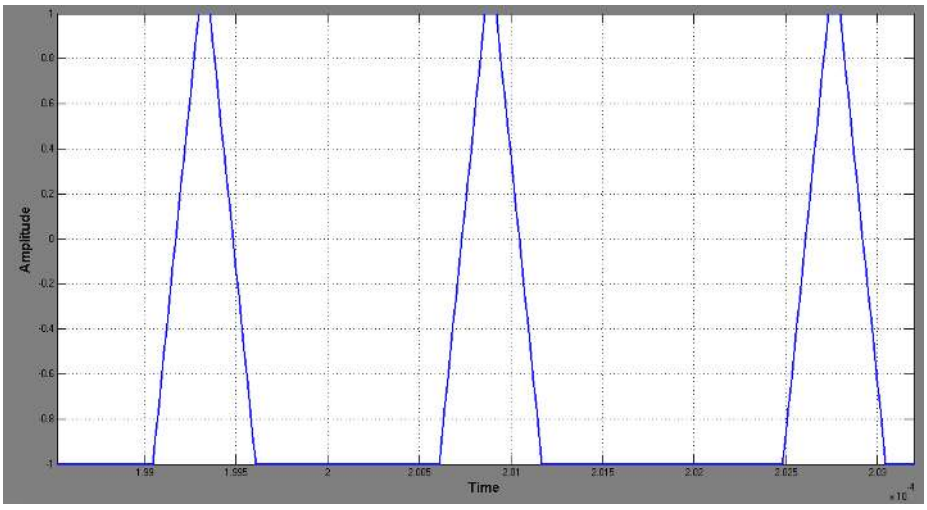


Figure 3-16 Feedback Pulse Shape under Strong Slew Rate Limitation

In relatively low speed system, such condition is quite easy to avoid. For example, in a modulator sampled at 3.2MHz, DAC pulse transition time of 10 ns only occupies around

5% of clock period. However, in high speed data conversion, ISI may be quite conspicuous. For example, for a modulator sampled at 400MHz, 2ns pulse transition time is detrimental as it occupies 80% of the entire pulse. Hence, it is evidential that for high speed ΣΔ modulator conversion, ISI should be considered seriously and maybe solved by using RZ pulse shaping.

In real circuit implementation, spike can be regarded as a form of ISI effect as well. At DAC output, due to fast pulse transition and parasitic coupling, spike is inevitable. It only happens when there is a transition. This is similar to having ISI effect. It also causes a finite amount of error charge which is signal dependent. Hypothetically speaking, this should create degradation for NRZ pulses. In this research, spike is modeled in behavioral level whose length and magnitude is adjustable. Simulation shows it introduces 3rd order harmonic content (Figure 3-18). But this is only when the spike is considerably strong (spike power is twice the feedback pulse power). Hence, in a well-designed system, feedback DAC spike should not create serious trouble for the system. But again, caution should be taken for high speed system.

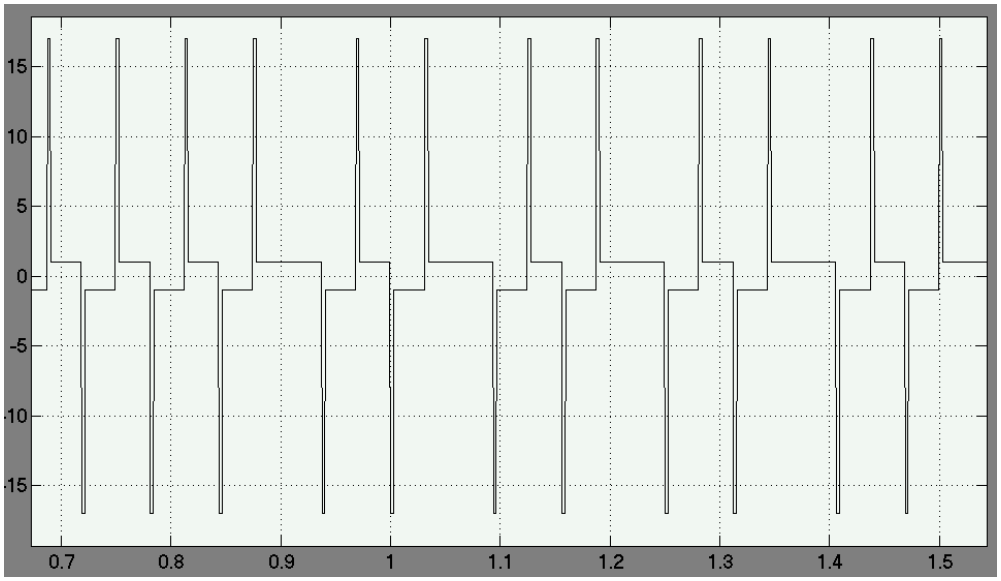


Figure 3-17 Model of Feedback Pulse Spike in Simulink

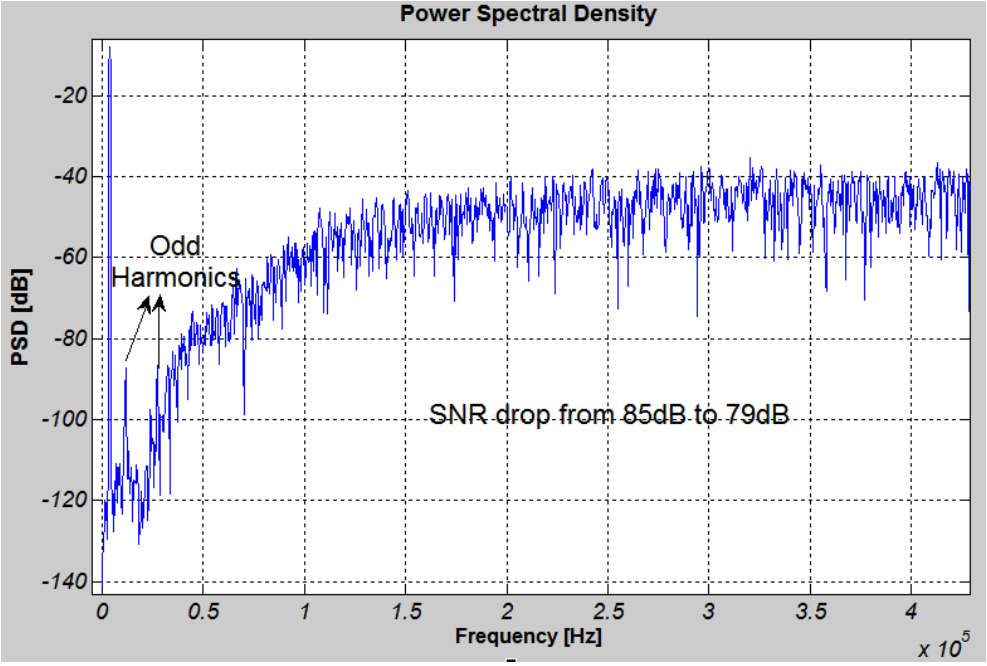


Figure 3-18 PSD of CT ΣΔ Modulator with Strong Feedback Spike

3.4.6 Thermal Noise

In ideal ΣΔ Modulator analysis, only quantization noise is being considered. But in real circuit implementation, other noise sources pop up. The most critical noise source is at the input of the modulator where no noise shaping is being provided. Hence, the amount of the noise at the input is the decisive factor for the achievable SNR.

Thermal noise is ubiquitous and it is usually preferable to make it the dominant noise source. There are two advantages by doing this. First, it is more power efficient to reduce quantization noise than thermal noise. As a matter of fact, reduction of almost all circuit noise would result in a sacrifice in power consumption. Second, since thermal noise is white Gaussian noise, it can works as a dither signal to minimize the idle tones of the modulator without incurring extra circuitry.

In a typical first stage design, Op-amp-RC integrator is usually implemented. And for a current steering DAC feedback, the input stage looks like Figure 3-19.

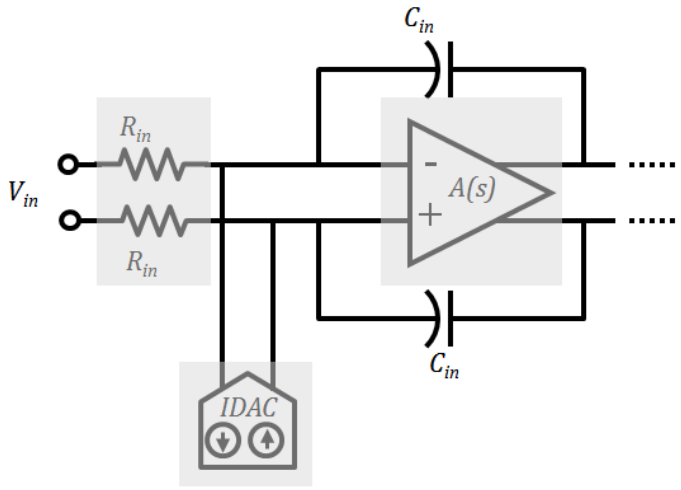


Figure 3-19 Input Stage of CT ΣΔ Modulator

There are three sources of thermal noise that should be taken into consideration. First is the thermal noise due to input resistors. It is simply expressed as $V_{R_{in}}^2(f) = 4kTR_{in}$.

The second sources of noise come from the differential Op-amp. Assume a simple differential pair, and only thermal noise is considered, the input referred noise is given by [47].

$$V_{OTA}^2(f) = \frac{16kT}{3}\left(\frac{1}{g_{m1}}\right) + \frac{16kT}{3}\left(\frac{g_{m2}}{g_{m1}}\right)^2\left(\frac{1}{g_{m2}}\right) \qquad 3.14$$

where g_{m1} is the transconductance of the input pair and g_{m2} is the transconductance of the current source load.

Further referring this amount to the input of the modulator, we get the following input-referred PSD of the op-amp:

$$V_{ref}^2(f) = V_{OTA}^2(f)|1 + j2\pi f R_{in} C_{int}|^2 \qquad 3.15$$

Since we are only concerning about noise within the signal band, for a high oversampling ratio, the term $2\pi f R_{in} C_{int} \approx 0$, and we arrive at

$$V_{ref}^2(f) = V_{OTA}^2(f) \tag{3.16}$$

The third source of noise comes from current feedback DAC. We take a simple current DAC cell (Figure 3-20) for an example.

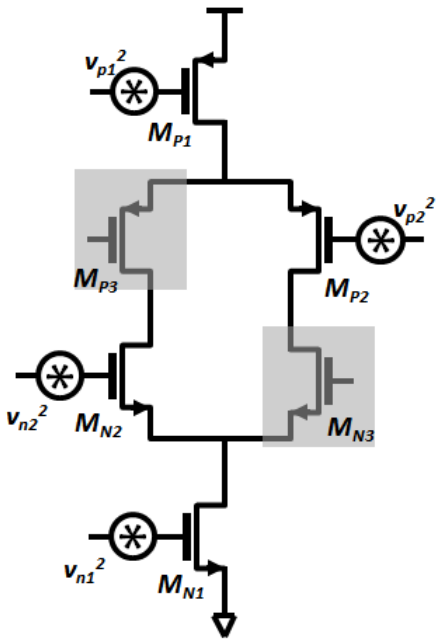


Figure 3-20 Noise Model of 1-bit DAC Cell

At one moment, only half of every branch is in active region. For example, if M_{N2} and M_{P2} are active, M_{N3} and M_{P3} are in cut-off region. And since the switch transistors work as cascade transistors, their effects are generally ignored. Noise contribution mainly comes from the current source device. The output noise current can be expressed as

$$I_{N1}{}^2(f) = V_{N1}{}^2(f) \cdot g_{mN1}{}^2 \text{ and } I_{P1}{}^2(f) = V_{P1}{}^2(f) \cdot g_{mP1}{}^2 \tag{3.17}$$

Where g_{mN1} and g_{mP1} are the transconductance of the current source devices. For simplicity, we assume the PMOS current source has the same transconductance as the NMOS device.

Neglecting flicker noise,

$$V_{N1}{}^2(f) = 4kT \cdot \frac{2}{3} \cdot \frac{1}{g_{mN1}} \tag{3.18}$$

Hence

$$I_{N1}{}^2(f) = \frac{8kT}{3} \cdot g_{mN1} \tag{3.19}$$

So the input referred noise voltage power is given by

$$V_{DAC}{}^2 = I_{N1}{}^2(f) \cdot R_{in}{}^2 = \frac{8kT}{3} \cdot g_{mN1} \cdot R_{in}{}^2 \tag{3.20}$$

These noise sources limit the dynamic range of the modulator which in turn determines the SNR/SNDR performance of the modulator. Hence, these front end circuit noise is the most fundamental performance consideration for any practical design.

Chapter 4
Theoretical Studies on Timing Non-idealities in CT ΣΔ Modulator

Timing non-ideality represents the biggest challenge in CT ΣΔ modulator design. This is because in CT ΣΔ design, the exact feedback pulse shape and position are important as it is convoluted with integrator transfer function in time domain over entire sampling period. Thus any non-ideal effects associated with feedback pulses introduce deviation from ideal performance. There are two well known effects specific to CT ΣΔ modulators, namely, excess loop delay and clock jitter. Studies show that these two effects are quite critical to the entire modulator's performance. Thus, careful study of these two effects is necessary.

4.1 Excess Loop Delay (ELD)

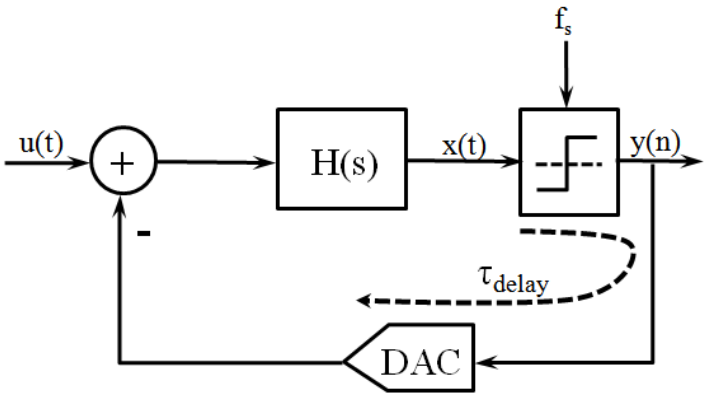


Figure 4-1 Excess Loop Delay Effect in Block Model

Excess loop delay is defined as the delay from quantizer sampling instant to the feedback DAC output. In idealized analysis, it is assumed the feedback DAC output the desired

value at the instant quantizer samples the input. However, this is practically impossible since the transistors in comparators of quantizer and the DAC require non-zero switching time. In the case of multi-bit quantizer design, linearization circuit like DWA (Data Weighted Average) may add further delay.

Since the time taken by comparator to resolve input value and make decision is time dependent, which creates a variable loop delay, the most common design practice is to add a DFF (D Flip-Flop) after comparator. This effectively creates a fixed delay. For the ease of designing clocking scheme and excess loop delay compensation, mostly the fixed delay is chosen to be 0.5 Ts or Ts. However, there is no performance implication on the choice of the delay for well designed system.

4.1.1 Effects of Excess Loop Delay

Though it universally exists in every practical CT ΣΔ modulator, its effects may vary for different feedback techniques. As briefly mentioned in previous chapter, NRZ is inferior to RZ implementation in terms of ELD immunity.

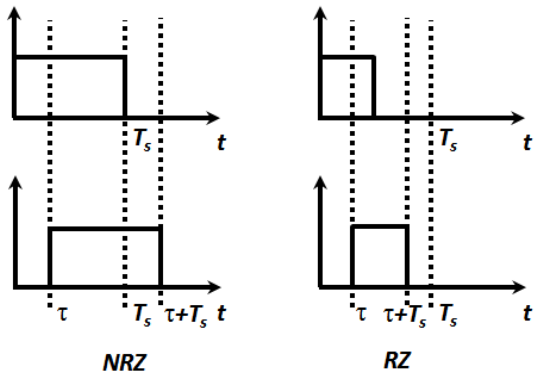


Figure 4-2 RZ & NRZ Feedback Pulse with Excess Loop Delay

As can be seen from Figure 4-2, both NRZ and RZ pulses are subjected to a delay. Any amount of delay would push part of the NRZ pulses into the next clocking period. On the

contrary, as long as the delay is small ($<(1-\delta)T_s$) enough, the RZ feedback pulse would still fall in the same clock cycle. This difference results in big difference in modulators stability. This issue has been well studied in [24]. It is demonstrated that pulses falling in the next cycle causes an increase of order in loop filter. Such increase of order pushes more quantization noise out of signal band and creates out-of-band peaking. This effect first creates an increased noise shaping performance but then degrades achievable SNR due to decreased stability. The peaking effect can be clearly seen from Figure 4-3 which is the PSD plot of a modulator subject to ELD.

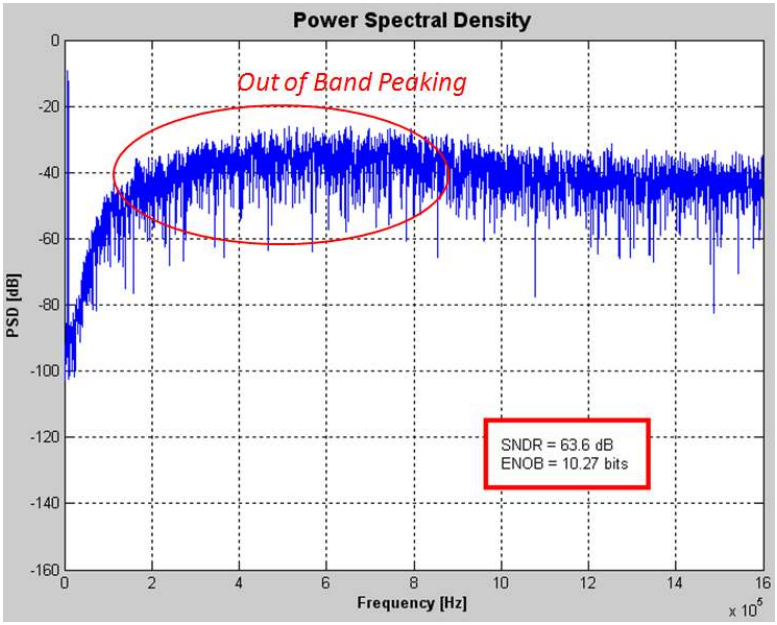


Figure 4-3 PSD Plot Showing Out-of-band Peaking due to ELD

When excess loop delay exceeds a certain limits, RZ feedback pulses also exhibit reduced stability due to part of the pulses being moved into the next cycle. A comparison of NRZ and RZ feedback system in terms of SNR versus excess loop delay is shown in Figure 4-4.

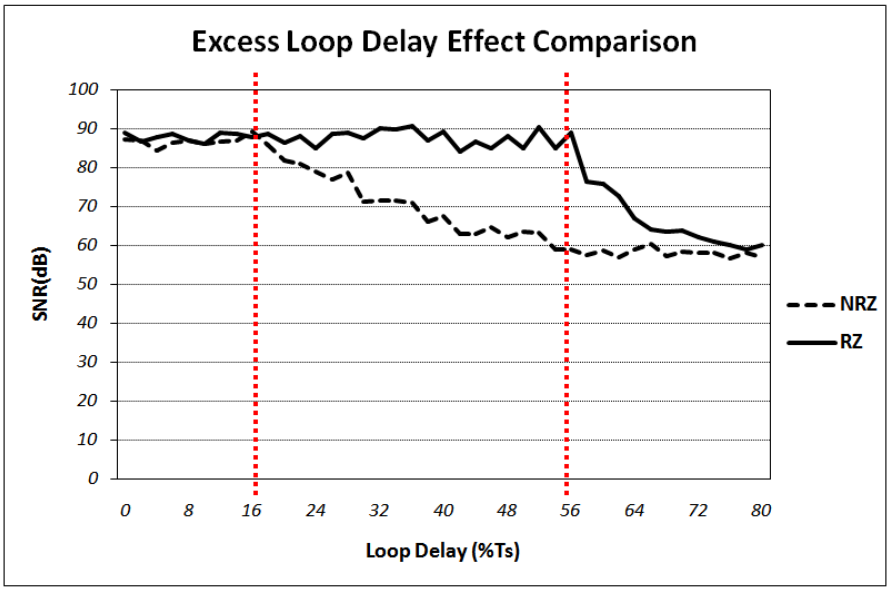


Figure 4-4 SNR vs. ELD for RZ & NRZ Feedback Pulse

4.1.2 Solutions to Tackle ELD Problem

Compensation for excess loop delay can be divided into two cases, depending whether the delayed pulse falls into the next cycle.

If the feedback pulse is not delayed into the next cycle, the effect is like a modification to the modulator's coefficient, only slight SNR degradation may occur. To compensate this, a new set of coefficient can be calculated with ELD included.

On the other hand, if feedback pulse is delayed into the next cycle, a change in modulator's structure would be needed. This is because an originally N^{th} order system now becomes $(N+1)^{th}$ order. It is impossible to compensate an $(N+1)^{th}$ order system with N^{th} order loop filter unless one more degree of freedom is created. Various ELD compensation techniques have been developed just to accomplish this simple task.

In [24], Half-Return-to-Zero paths are added to provide the extra degree of freedom. In [25], compensation was achieved using a digital differentiator. This technique is aimed at

avoiding adding an additional path in front of the quantizer. In [26], a digital compensation method is also proposed.

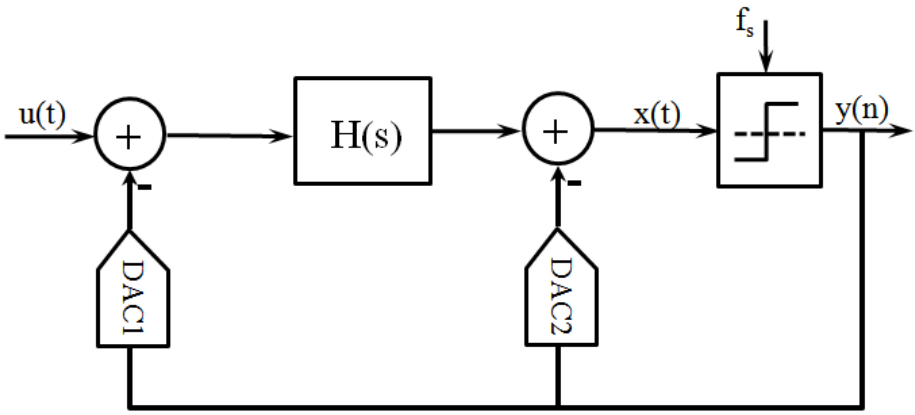


Figure 4-5 Compensation of ELD Effect with Direct Feedback Method

Despite the various designs that have been invented, the most intuitive and classical way to achieve this design goal is by the insertion of an additional feedback path around the quantizer as shown in Figure 4-5. This creates a 0^{th} order loop in the simplest way possible. However, from circuit implementation point of view, it incurs the primary disadvantage that an additional DAC and a differential summing amplifier. However, this disadvantage can be removed if certain design topologies are adopted. For example, the extra summing amplifier can be saved if switched current feedback is used and current summation is used rather than conventional voltage summation. Hence, as the most reliable and simplest realization method, this 0^{th} order compensation technique is still the most widely used technique. Along with this technique, coefficient calculation method for such architecture is thoroughly investigated in [27].

4.2 Clock Jitter Effect

Clock Jitter effect introduces detrimental performance degradation in a CT ΣΔ Modulator. It hampers the further development and wide implementation of CT ΣΔ Modulators. In this section, we examine clock jitter and how it creates trouble in detail with the purpose of solving this detrimental issue eventually.

Nowadays, in an integrated mixed signal system like ΣΔ AD converter, clock signal is normally generated on chip by either a PLL (Phase Lock Loop) or VCO (Voltage Controlled Oscillator). Due to various noise sources of the clock generating circuitry, for e.g. thermal noise, power supply noise etc., the clock transition edges suffers from a random variation. Effectively, this alters the clock pulse width and position.

Clock jitter as a result of imperfection in clock generation circuit has been studied with great detail. From examining its effect on CT ΣΔ modulator point of view, detailed modeling technique and complicated mathematical proof are irrelevant in this context. Instead, generalized model is appropriate for the stated purpose.

4.2.1 Synchronous Jitter vs. Accumulated Jitter

Without losing much generality, we assume the clock signal is generated by an on-chip PLL circuit. There are two types of clock jitter inside a general-purpose PLL, namely, synchronous jitter and accumulated jitter.

Synchronous jitter exhibits itself in driven systems such as PFD/CP and FDs. These blocks accepts an input and produce an output accordingly. The important characteristic of synchronous jitter is that jitter in each clock edge is independent from any other clock

edges. This variation in clock edge position exhibits white Gaussian characteristic. A simple mathematical expression describing such a clock is

$t_n=nT_s+\alpha_n$, n=0,1,2…,N-1 where α_n is typically i.i.d (independent and identically distributed).

Accumulated jitter on the other hand exists in systems that are not driven such as oscillator and VCO. In these blocks, output transitions are not a direct result of their transitions at input. For such blocks, each transition is relative to the previous transition and exhibits slightly more complicated effects. Simplified mathematical expression for asynchronous jitter is

$t_n=nT_s+\alpha_n$, n=0,1,2…,N-1 where $\alpha_n=\Sigma\tau_i$ and $\tau_0=0$. And τ_i is the jitter of the sampling interval *i* and is modeled as i.i.d Gaussian noise.

It is difficult to make clear distinction between these two types of jitter in time domain. However, in frequency domain, the difference is much more prominent since jitter is essentially phase noise in frequency domain. Figure 4-6 shows the power spectrum of a clock modeled with synchronous jitter versus accumulated jitter. It is clearly seen that accumulated jitter exhibits a noise skirt in its power spectrum whereas synchronous jitter exhibits white noise floor. Generally speaking, these two types of jitter exhibits similar influence in the system and they can be related through a simple expression which states $\delta_{j,acc}=\delta_{j,syn}/\sqrt{N_{pts}}$ (where N_{pts} is the number of simulation points) [28]. Verilog-A model of both types of jitter is proposed in [29] and was also used in this project for simulation of jittered clock sources.

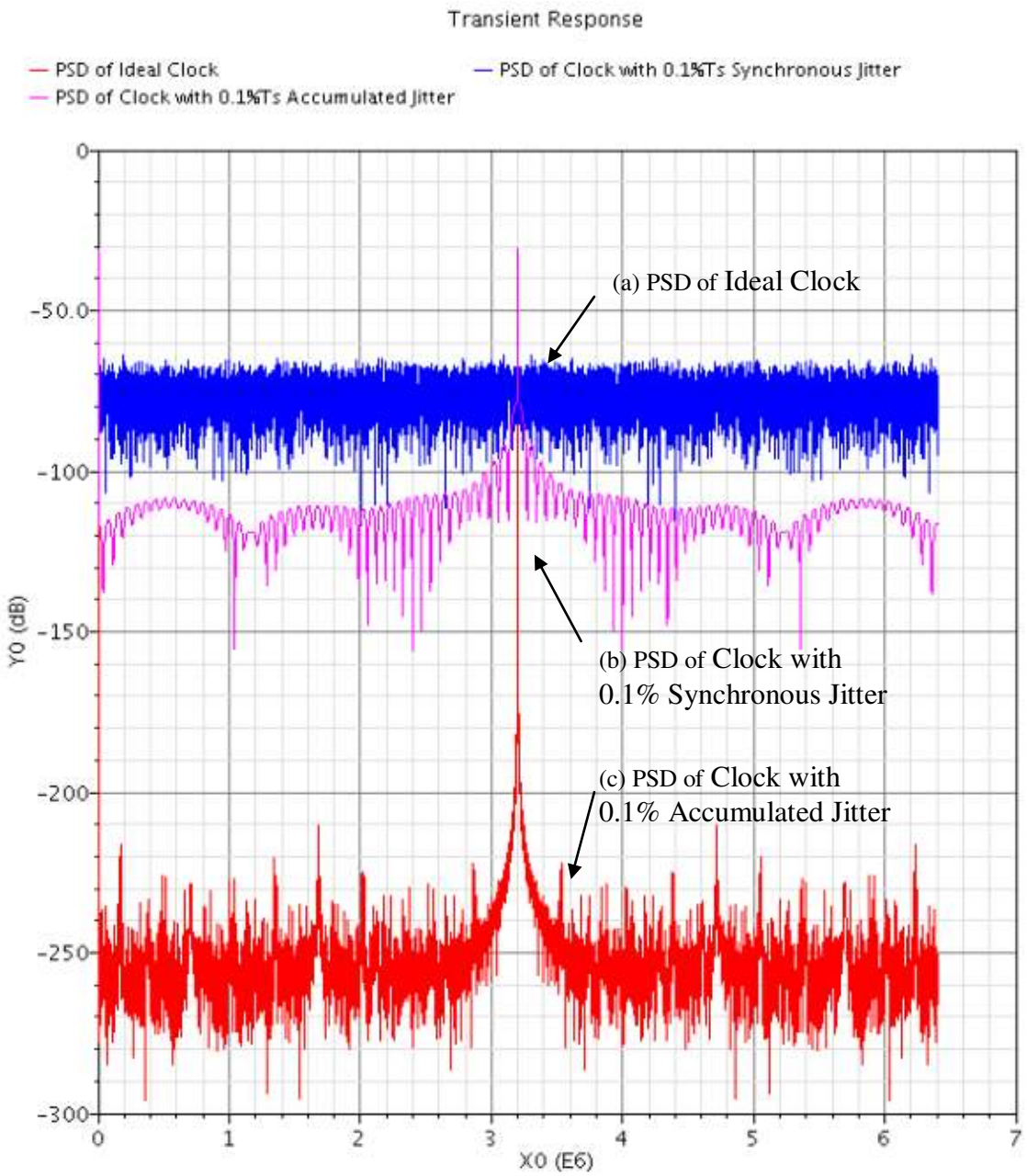


Figure 4-6 PSD Plot of Clock with (a) ideal clock (b)0.1% synchronous jitter (c)0.1% accumulated jitter

4.2.2 Pulse Width Jitter vs. Pulse Position Jitter

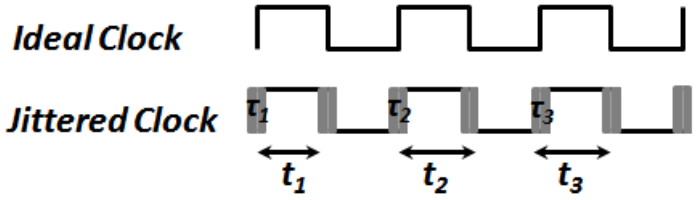


Figure 4-7 Time Domain Visualization of Jittered Clock

Jittered clock deviates from ideal clock, creating both pulse position error and pulse width error. Both type of jitter would cause performance degradation in CT ΣΔ Modulator. This could be easily understood from the example of a Return-to-Zero pulse (Figure 4-8).

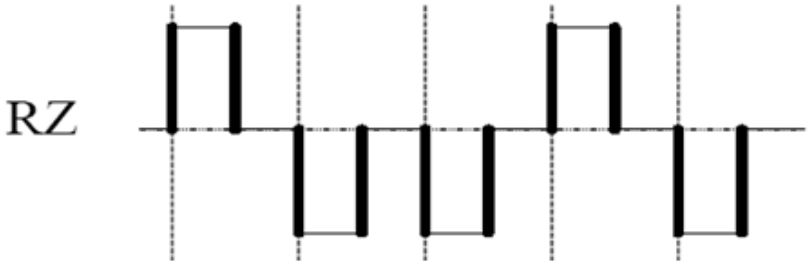


Figure 4-8 RZ Feedback Pulse with Jitter

From [19], the RZ feedback DAC transfer function can be expressed as

$$R_{RZ}(s) = \frac{e^{-st_d}(1 - e^{-st_p})}{s} \tag{4.1}$$

Hence the loop transfer function would be

$$L_{RZ}(s) = L(s)R_{RZ}(s) = L(s)\frac{e^{-st_d}(1 - e^{-st_p})}{s} \tag{4.2}$$

It is clear that, the loop transfer function is a function of both pulse delay t_d and pulse length t_p.

However, pulse width jitter and pulse position jitter affect the system differently. In general, pulse width jitter is detrimental to the system because it directly affects the amount of charge being fed back which in turn determines the loop filter output voltage. Pulse position jitter on the other hand has a much smaller effect partly because it does not affect the total feedback charges. It is stated in [28] that its effect is at least 1^{st} order shaped.

The above statement in fact leads to a simple conclusion: if clock width jitter can be eliminated, the jitter effect is greatly relieved. This forms the fundamental idea of some of the techniques that are aimed to alleviate jitter issue in CT ΣΔ modulators.

4.2.3 Jitter Effects in CT Modulators

In CT ΣΔ Modulators, clocking takes place in both quantizer and feedback DAC. The sampling error created by the quantizer block appears as additional quantization error and effectively noise shaped by the preceding stages and hence introduces negligible effects. However, the sampling error on feedback DAC is added to the input node without any form of noise shaping and hence imposes serious limitations on the overall performance of the modulator. This random modulation of feedback pulse can be viewed as modulation of the feedback coefficients which flattens the power spectral density of the quantization noise in the band of interest and degrades its resolution.

Since clock jitter affect the system through modulation on the feedback pulse, it is obvious that the pulse shape would be strongly related to the modulator's jitter performance. In most literature, jitter effect estimation is done by considering the feedback pulse jitter error as additive noise sequence. And the calculation of SNR boundary is by assuming the jitter induced noise dominates the performance. Quantitative analysis on two most popular feedback pulses RZ and NRZ has been well established,

hence, in this section, the derivation results from [30] are directly used and comparison is made.

In general, the jitter bounded SNR is calculated as

$$SNR_{jitter} = \frac{P_{SIGNAL}}{P_{jitter}} = \frac{A^2/_2}{\sigma^2/OSR} \tag{4.3}$$

where σ^2 denotes the variance of a particular noise

For NRZ feedback pulses,

$\sigma^2{}_{e|NRZ} = \sigma^2{}_{\Delta y|NRZ} \frac{\sigma^2{}_{\Delta t}}{T_s{}^2}$, hence

$$\mathrm{SNR_{jitter|NRZ}} = \frac{\mathrm{P_{SIGNAL}}}{\mathrm{P_{jitter}}} = \frac{\mathrm{A^2/_2}}{\sigma^2{}_{\mathrm{e|NRZ}}/\mathrm{OSR}} = \frac{\mathrm{A^2 \cdot OSR}}{2\sigma^2{}_{\Delta \mathrm{y|NRZ}} \cdot \left(\sigma_{\Delta t}/\mathrm{T_s}\right)^2} \tag{4.4}$$

where $\sigma^2{}_{\Delta y|NRZ}$is the standard deviation of the adjacent output difference, and $\sigma^2{}_{\Delta t}$ is the standard deviation of the clock jitter.

For RZ feedback pulses,

$$\sigma^2{}_{e|RZ} = 2\sigma^2{}_{y|RZ} \frac{\sigma^2{}_{\Delta t}}{T_s{}^2} \tag{4.5}$$

Hence

$$\mathrm{SNR_{jitter|RZ}} = \frac{\mathrm{P_{SIGNAL}}}{\mathrm{P_{jitter}}} = \frac{\mathrm{A^2/_2}}{\sigma^2{}_{\mathrm{e|RZ}}/\mathrm{OSR}} = \frac{\mathrm{A^2 \cdot OSR}}{4\sigma^2{}_{\mathrm{y|RZ}} \cdot \left(\sigma_{\Delta t}/\mathrm{T_s}\right)^2} \tag{4.6}$$

where $\sigma^2{}_{y|RZ}$ is the standard deviation of the output sequence. Notice here the factor 2 in $\sigma^2{}_{e|RZ}$ is due to the fact that a RZ pulse is affected by clock jitter twice per cycle.

Thus, a comparison can be made as

$$\frac{SNR_{jitter|NRZ}}{SNR_{jitter|RZ}} = \frac{2\sigma^2{}_{y|RZ}}{\sigma^2{}_{\Delta y|NRZ}} \quad 4.7$$

If single bit quantizer is used, it is shown that the NRZ pulse shape is around 5dB better than RZ pulse shape in terms of jitter performance. This conclusion can be confirmed by behavioral simulation results as shown in Figure 4-9.

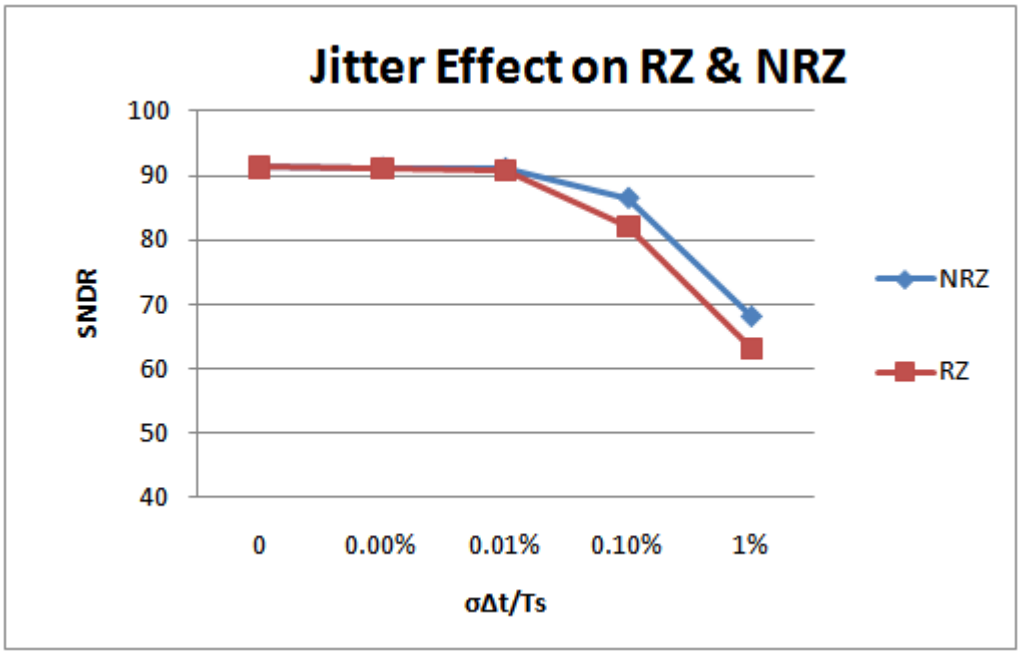


Figure 4-9 Simulated SNDR with Jitter Noise for RZ and NRZ Feedback Pulse

For multi-bit quantizer, the benefit of using a NRZ pulse is even larger compare to RZ feedback in terms of jitter performance. However, NRZ pulse shape is fixed and its jitter performance is solely bounded by clock quality whereas RZ pulse provides freedom and possibility to achieve better jitter performance.

Eqn. 4.4 and Eqn. 4.6 suggest that the performance bounded by jitter is actually determined by the quantity $\sigma_{\Delta t}/T_s$, which is the clock jitter normalized to clock period. This reveals the fact that a high speed system is more severely impaired by clock jitter. Because jitter in clock generation circuit is relatively a weak function on the output clock

frequency, the jitter percentage becomes higher and higher with the increment of clock frequency. For example, if a PLL with at 30ps ($\sigma_{\Delta t}$) jitter accounts for 0.1% jitter in a system sampled at 30MHz, while accounts for up to 1% in a system sampled at 300MHz, which makes huge difference in achievable SNR.

In current state of the art technology, very low jitter can be achieved in PLL design. However, sacrifice in power consumption and circuit complexity must be made. For example, sub-pico second jitter performance has been achieved, but LC tank must be used. For conventional PLL, jitter of several tens of pico second would be good general estimation. Without any jitter optimization technique, in order to avoid performance degradation, normalized jitter should not exceed 0.1% as shown in Figure 4-9. This limits the conversion speed of a CT ΣΔ modulator which is primary obstacle that is hindering the development of CT ΣΔ modulator into high speed application.

4.2.4 Clock Jitter Effect Minimization Techniques

With trend of achieving high speed data conversion in CT ΣΔ modulator, clock jitter issue has become a critical concern for researchers and developers.

A well known simple solution for clock jitter issue is to use multi-bit NRZ feedback DAC. The reason is pretty obvious. With reduced step size from cycle to cycle, the clock edge being affected is very much reduced in magnitude and hence the amount of charges. However, multi-bit DAC may not be the optimum choice for example in very low power design or may not even be allowed in certain applications. In such cases, other techniques have to be considered.

Over the years, various research efforts have been put into this field. Theoretical analysis has been introduced in [31] [32] [33] to quantify clock jitter effect. From the analysis, it is

proven that by designing NTF properly, clock jitter performance can be improved by up to 10 dB. However, this technique requires a designable NTF which requires manual synthesis of NTF. Another technique filters the feedback DAC pulses with FIR filters before letting it interact with input signal. This is equivalently spreading the feedback pulse over several clock cycles and hence reducing the noise floor created by jitter noise. In this way, a single bit feedback can achieve jitter performance of multi-bit feedback. Such approach has been reported in [34][35]. The problem of such approach is the increased complexity of the circuit as well as increased power consumption.

In fact, the most popular approach to tackle clock jitter problem is by pulse shaping. One of the most important methods is Switched Capacitor Resistor (SCR) feedback technique. It serves as a good example to explain how pulse shaping method works.

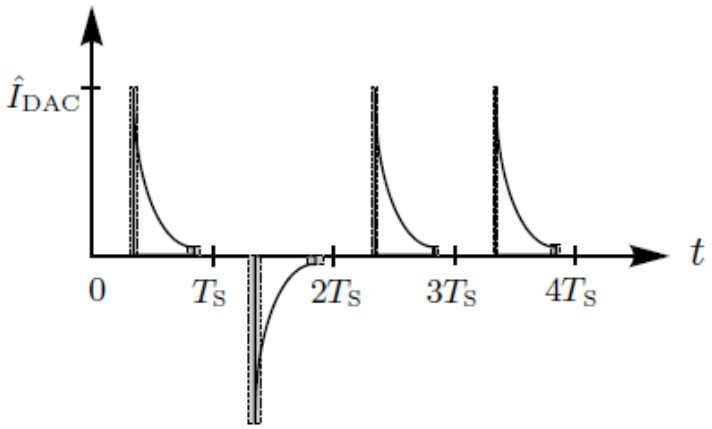


Figure 4-10 Pulse Jitter Effect for SCR Shaped feedback

This technique was first proposed in [36]. The feedback DAC is realized by a capacitor which is discharged through a resistor, creating an exponentially decreased current as shown in Figure 4-10. Since most of charges concentrate at the start of the clock period, the variance in length of the pulse would create very much reduced effect on the total amount of charges per clock cycle. From the pulse shape, it is obvious at the end of every pulse, the magnitude is very small, and hence the charge affected by timing error is quite

small. The sensitivity of the pulse is defined by time constant $\tau=C_R R_R$. This technique very much resembles the feedback implementation in DT modulators, only with an explicit resistor on the discharging path to control the discharge rate. In fact, in some other works ([37][38]), the DT feedback technique is directly implemented in a CT modulator design, creating a jitter noise rejection as good as DT modulators.

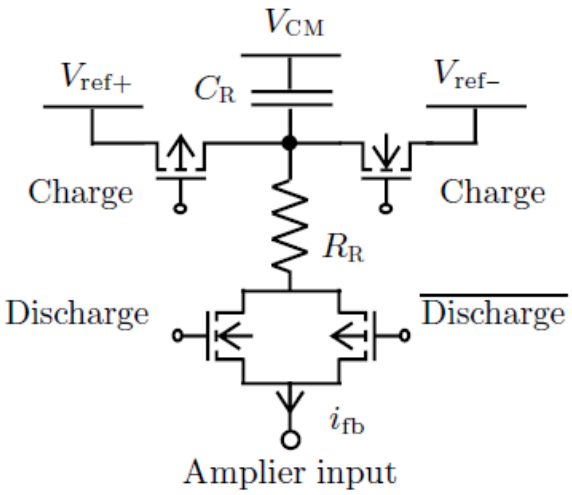


Figure 4-11 Implementation of SCR Pulse Shaping DAC in [36]

Quantitative analysis of SCR pulse's jitter effect is provided in [19] and the in-band noise power is shown to be

$$\text{IBN}_{\text{jitter|SCR}} = \frac{\text{P}_{\text{SIGNAL}}}{\text{P}_{\text{jitter}}} = \frac{\Delta^2}{2\text{OSR}}\left(\frac{\text{k}_{1|\text{SCR}}}{\text{k}_{1|\text{NRZ}}}\right)^2 \left(\text{e}^{-\text{T}_s(\beta-\alpha)/\tau_{\text{DAC}}}\right)^2 \left(\frac{\sigma_t}{\text{T}_s}\right)^2 \quad 4.8$$

From the derived expression, it can be seen the IBN is exponentially suppressed. Also this expression indicates the design parameters in an exponentially shaped pulse. Jitter noise suppression can be adjusted by tuning the value of the time constant τ_{DAC}.

Exponential pulse like SCR and SC feedbacks inherits the good jitter rejection characteristic from DT feedback technique, but it also inherits the problems. Comparing to rectangular feedback pulse, exponential pulse transfers significantly less amount of

charges per clock cycle. This means the dynamic range at the input is greatly reduced. For example, in [39], only -15 dBFS max input is achieved with SCR feedback. Another problem is the increased power consumption in first stage integrator. In order for exponential feedback pulse to achieve good jitter rejection, its amplitude must settle to a magnitude that is low enough. This is equivalently putting a settling requirement as in DT modulator. Hence a much larger GBW requirement for the first stage Op-amp is expected. As a result, exponential feedback does not result in an optimum design.

4.2.5 Novel Fixed-Length Return-to-Zero Feedback

In this research, a novel pulse shaping technique which is named Fixed-Length Return-to-Zero (FLRZ) feedback technique is proposed. The fundamental theory behind this technique is to eliminate pulse width jitter completely, leaving only pulse position jitter. In previous section, the pulse position (PP) jitter and pulse width (PW) jitter have been compared and we see that PW jitter is the primary culprit for the system performance degradation. In fact, pulse position jitter limits the best performance achievable for pulse shaping technique. This is because there is no ideal reference clock in this world, hence, it is impossible to synchronize a jittered clock and determine the ideal location where every cycle should be started. Fortunately, pulse position jitter is 1st order noise shaped and the performance boundary created by it is reasonably satisfactory in most applications.

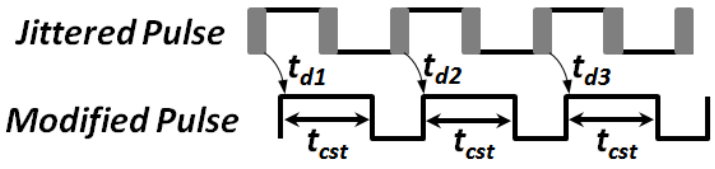


Figure 4-12 Concept of Transforming Pulse Width Jitter to Pulse Position Jitter

Elimination of pulse width jitter means transforming a variable length feedback pulse into a fixed length pulse. This concept is shown in Figure 4-12.

In [40], a similar idea has been used. In this publication, the author manipulates clock directly, creating an internal clock which is of fixed length. Complicated loop using digital and analog circuit is used to generate the internal clock.

In [41], a simple and elegant feedback technique which was named Switched Shaped Current (SSI) was proposed. The author made a rectangular-like feedback pulse. The total charges fed back by the pulses are determined by charges stored on a capacitor and hence are independent of clock width variations. However, this method cannot control the length of the pulse precisely, making it difficult to design the best coefficients. Also, this design is not suitable for low voltage design due to inevitable stacking of diode configured transistors.

In this work, I propose to use RC discharging circuit for accurate pulse width definition. The implementation is as shown in Figure 4-13.

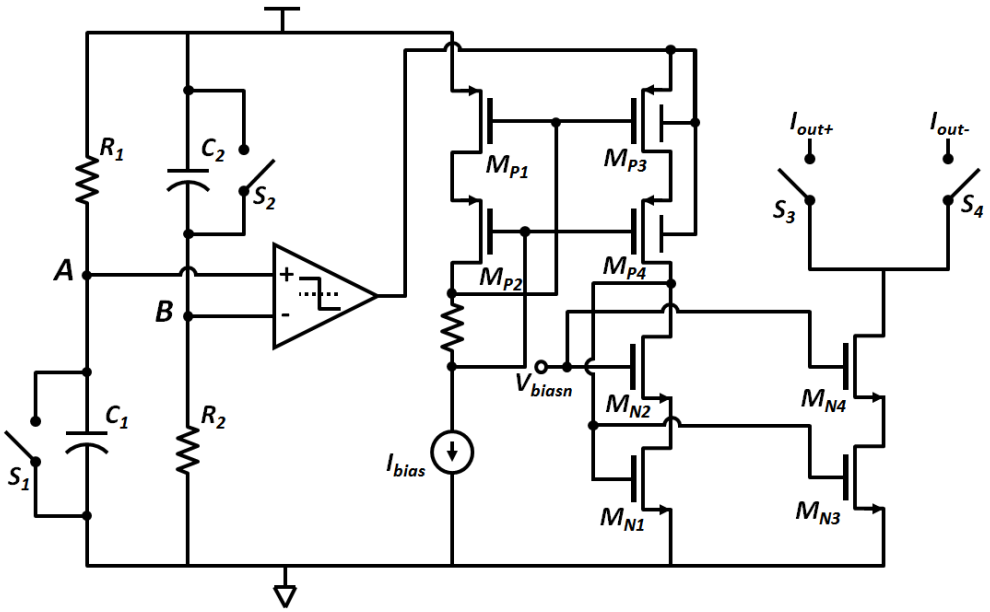


Figure 4-13 Implementation of Proposed FLRZ DAC

When clock is at 'reset' state, the two switches S_1 and S_2 are closed, shorting the two nodes *A* and *B* to ground and *VDD* respectively. At this state, $V_A<V_B$, the comparator outputs '1'. Once the clock changes to 'on' state, the two switches are opened, and the charging and discharging of the two capacitors C_1 and C_2 starts. The voltage at *A* and *B* follows the following relationship.

$$v_A(t) = V_{DD}(1 - e^{-\frac{t}{R_1 C_1}}) \tag{4.9}$$

and

$$v_B(t) = V_{DD} e^{-\frac{t}{R_2 C_2}} \tag{4.10}$$

Normally, for design simplicity, we set $R_1 = R_2 = R, C_1 = C_2 = C$. At a particular time point, the two voltage level meets and crosses. When V_A becomes smaller than V_B, the comparator output falls to '0'. During this process, the time interval between the voltages at nodes *A* and *B* starts to move freely and the two voltages arrive the same level is solely determined by *RC* time constant which can be easily derived by setting $v_A(t) = v_B(t)$, and we have

$$t_{cst} = RC \cdot ln2 \tag{4.11}$$

Such time interval is ideal for the definition of pulse length as it alters the dependency on the clock pulse transitions, which in turn solves the clock jitter issue. The simulation of comparator output pulse is shown as below.

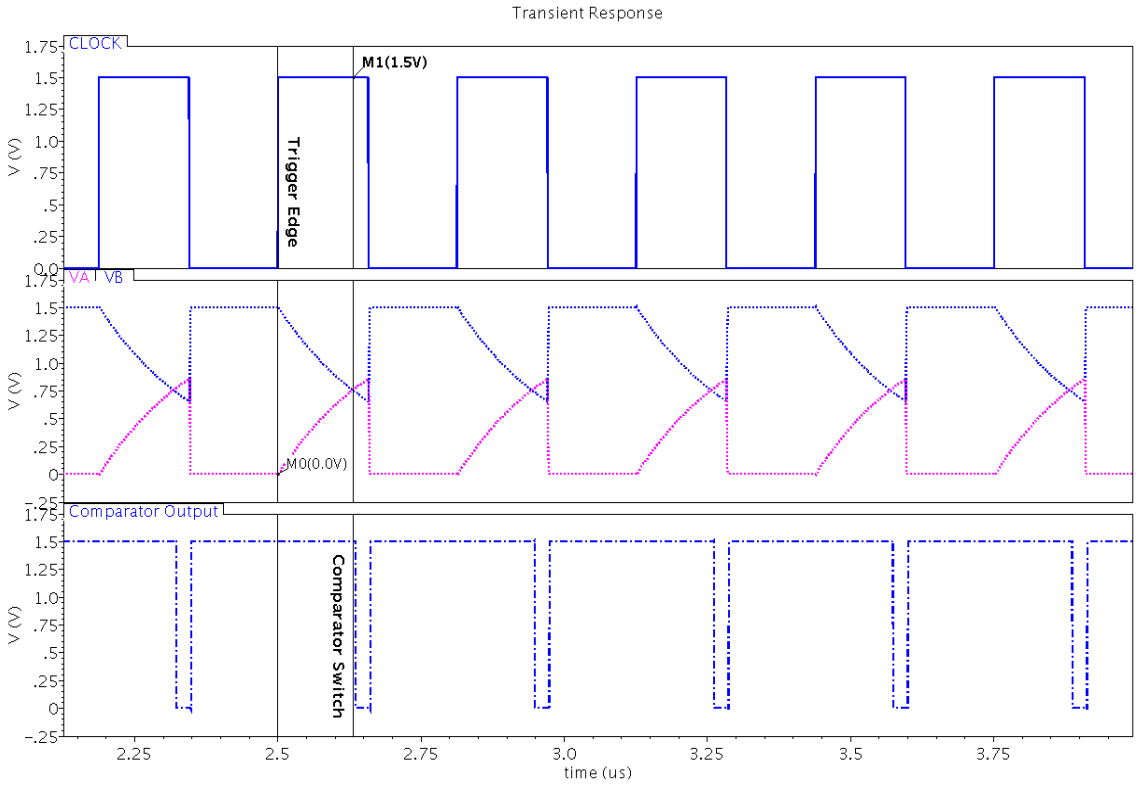


Figure 4-14 Output Waveform for Fixed Length Pulse Core Generation Circuit

In this work, generated pulse at comparator output is used to regulate a current DAC cell. As can be seen from Figure 4-14, the comparator output serves as the supply to the branch containing diode connected device M_{N1} and $M_{N2.}$ In 'reset' state and before comparator output falls to '0', this branch is in normal operation and the supply is VDD. Hence it simply mirrors current from I_{bias} branch through the PMOS current mirror. This current is also mirrored to the output branch. But once the comparator output switches to '0', the current flowing inside the diode connected branch drops instantly to 0 as well. This current is then faithfully mirrored to the output branch through M_{N1} to M_{N4} current mirror, creating a return-to-zero edge. This edge is asynchronous with clock falling edge. When true clock falling edge arrives, it will only sample a zero current and hence achieve the great jitter rejection characteristic.

Design Considerations

For normal clocking scheme (0.5 T_s duty cycle), it is easily understood that the constant time period cannot exceed 0.5 T_s because at least some time must be allocated to reset the switches. This could be a potential limiting factor due to the decrease of amount of charge fed back comparing to conventional RZ feedback regime. As discussed in previous chapter, this leads to inevitable loss in stable input range and power consumption.

This limitation can be lifted by proper sequencing of clock signals. Figure 4-15 is one possible clocking scheme.

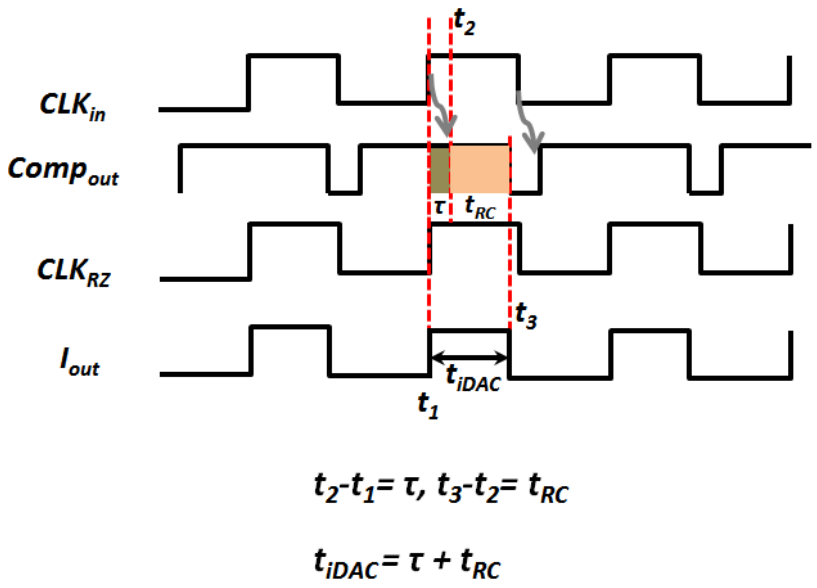


Figure 4-15 Proposal of Clocking Scheme for FLRZ DAC Implementation

In this figure, CLK_{in} is the original jittered clock which is normally used to clock the fixed length pulse core generation circuit. Here, a delayed version of this CLK_{in} is used to clock the fixed length pulse core generation circuit. Hence, the comparator output pulse is shown as $Comp_{out}$ which is also a delayed version. It can be clearly seen that the reset edge is τ delay from original CLK_{in} falling edge.

At output branch, if the output switches is clocked by CLK_{RZ} which is synchronized with the original clock CLK_{in} , then the amount of pulse clocked by output switches and appears at the output is $\tau+t_{RC.}$ Though t_{RC} may not reach 0.5 $T_{s,}$ the shortage can be compensated with delay τ.

Here it should be noted that if the $\tau+t_{RC}$ is 0.5 T_s, then the length of CLK_{RZ} must be greater than 0.5 T_s in order to achieve desired clock jitter rejection effect. So this CLK_{RZ} must be generated from original clock. Fortunately, generation of CLK_{RZ} is not very troublesome. The realization is introduced in next chapter.

Noise Considerations

This fixed length pulse generation circuit also has pretty good noise rejection. Next we will conduct a simple noise analysis on the core circuit. Taking all circuit components into consideration, 3 types of noise sources can be identified as shown in Figure 4-16.

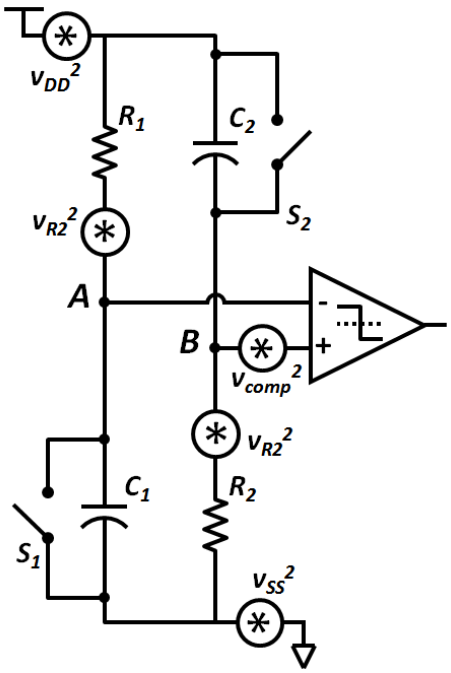


Figure 4-16 Noise Model for the Fixed Length Pulse Generation Core Circuit

Firstly, noise may come from VDD and ground. However, from Eqn. 4.11, it is clear the pulse length t_{cst} is independent of power supply. This is easily understandable. The noise from power supply and ground affect the two branches in the same manner. When the two voltages at nodes ***A*** and ***B*** compare with each other, the noise is cancelled out.

Secondly, thermal noise from the two resistors may come into effect. Hence, Eqn. 4.9 and Eqn. 4.10 need to add in noise voltage term $\overline{v_{R_1}}$and $\overline{v_{R_2}}$respectively, and again, equating node voltage at nodes ***A*** and ***B*** we have

$$V_{DD}\left(1 - e^{-\frac{t}{RC}}\right) + \overline{v_{R_1}} = V_{DD}e^{-\frac{t}{RC}} + \overline{v_{R_2}} \qquad 4.12$$

Lump $\overline{v_{R_1}} - \overline{v_{R_2}}$ into one term, and normalized with V_{DD}, we denote it as $\overline{v_R}$, the pulse length can be calculated as

$$t_{cst} = RC \cdot ln2 - RC \cdot \ln\left(\overline{v_R} + 1\right) \qquad 4.13$$

The pulse length error $RC \cdot \ln\left(\overline{v_R} + 1\right)$ is an extremely small value. For example, suppose $R = 500K\Omega$, $C = 1pF$, the error term is only 64fs.

Also, the comparator may contaminate the output pulse as well. However, this can be well controlled in an optimal design where noise in comparator is well managed. Sub-pico range jitter can be expected.

To sum up, this technique provides excellent robustness again various noise sources. Hence, well matched results can be expected between chip realization and simulation.

High Speed Compatibility

As mentioned above, for high speed applications, the jitter requirement is extremely stringent on CT ΣΔ modulator design. The above analysis shows this implementation is

good candidate for solving jitter issue in high speed application as well due to its great ability for circuit noise immunity. Also, the entire implementation imposes almost no constraint on high speed operation. Probably a high speed comparator require more design effort, but still achievable. This implementation is also compatible with multi-bit RZ design. And the circuit overhead is quite small as the pulse generation core circuit can be used to bias all current DAC cells.

4.2.6 Performance Simulation & Comparison

Figure 4-17 plots the jitter performance of the proposed technique. The jitter is normalized with clock period for fair comparison. The simulation is carried out in a 4th order single loop single-bit behavior model in Cadence Spectre. The fixed length return to zero DAC cell is implemented in full circuit level. All other modulator blocks are behavioral models.

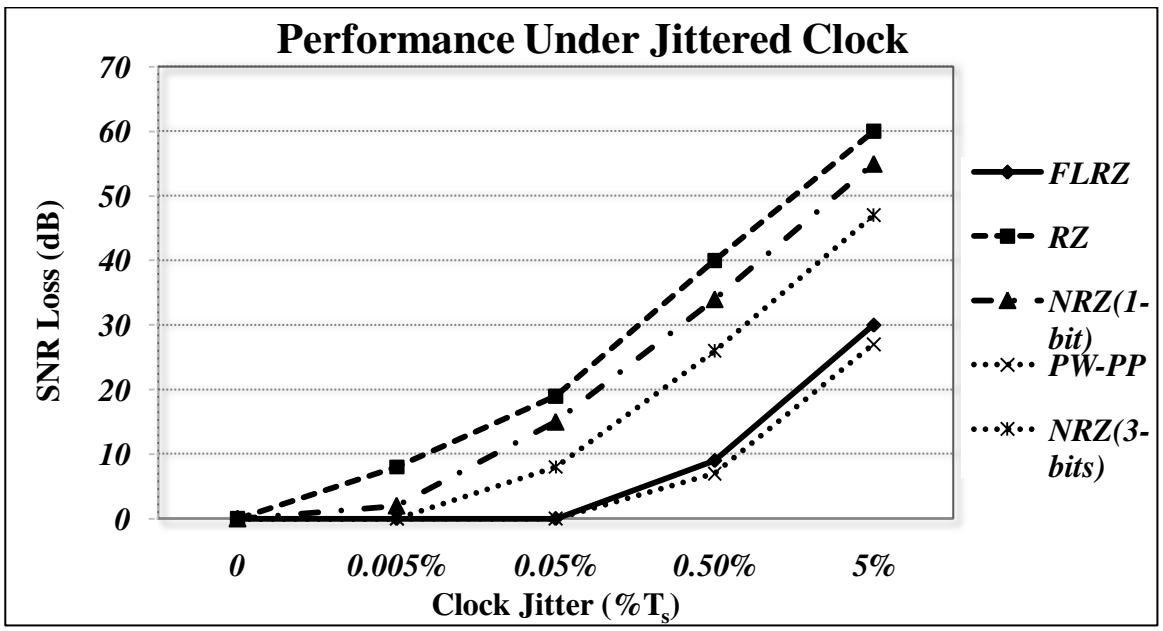


Figure 4-17 Behavioral Simulation for Different Feedback Pulse Scheme

Firstly, it is clearly shown that the proposed method indeed greatly improves the jitter performance of CT modulators. Although it cannot completely eliminate jitter degradation, the SNR loss is reduced to acceptable range. For jitter smaller than 0.5% T_s, less than 10-dB loss in performance is suffered. This method also shows much improved jitter performance over multi-bit modulators which are well-known for their good jitter rejection.

Secondly, this results shows the behavioral simulation coincides well with theoretical analysis. The proposed Fixed Length Return-to-Zero (FLRZ) pulse is based on the idea of transforming pulse width jitter to pulse position jitter (PW-PP), hence its best achievable performance is bounded by PW-PP method. From the figure, this relationship is very well demonstrated.

Comparison with Other Methods

In fact, conducting fair comparison of jitter performance is difficult as there are no well accepted jitter related FOM available. Performance is hard to compare across different methods as different researchers or literatures use different set of criteria to gauge performance. However, from Figure 4-17, it is still possible to make relative comparison. For pulse shaping methods such as SCR, SCSR, Sine-Shaped Pulse, their jitter performance is bounded by pulse position jitter performance limitation and they generally may achieve high jitter rejection. For PWM-FIR, FIR methods, they usually achieve multi-bit performance which is considered good but still not comparable to pulse position jitter performance in high jitter range. For NTF design, the jitter performance improvement is reported in absolute quantity and it is subjected to a lot of design constraints. The proposed FLRZ pulse shaping method has the same jitter performance as other pulse shaping method, but achieve closer to optimum performance at lower price.

In the following table, comparison is made in the aspects that the author of this research deems important. And again, the proposed method shows its advantage in terms of realization simplicity, achievable jitter performance etc.

Table 4-1 Comparison of Various Jitter Reduction Techniques

Method	**Performance**	**Realization Complexity**	**Pros**	**Cons**
SCR[36]	High	Simple	• Simple implementation	• Reduced dynamic range • High power consumption
SCSR[42]	High	Complex	• Retained dynamic range	• Large circuit overhead
Sine Shaped pulse[43]	High	Complex	• Retained dynamic range	• High implementation cost
PWM-FIR[35]	Medium	Complex	• Retained dynamic range	• Limited jitter rejection • High implementation cost
FIR[34]	Medium	Complex	• Retained dynamic range	• Limited jitter rejection • High implementation cost
NTF Design[44]	Low	Simple	• No extra circuitry	• Only in Multi-bit design • Complicated NTF design • NTF peaking
This Work	***High***	***Medium***	• ***Excellent Performance*** • ***Low cost*** • ***Robust design*** • ***Compatible with multi-bit design***	• ***Rely on RC time constant*** • ***Not verified on chip level***

Chapter 5
Implementation of a 4th Order Single-bit Continuous Time ΣΔ Modulator

In this chapter, implementation of a 4th order single-bit Continuous time sigma delta modulator is presented. Entire design flow is showcased. From architecture design to behavioral modeling, and at last to circuit level realization, various design choices are being justified. Also, the proposed Fixed-Length Return-to-Zero feedback technique is implemented for chip level verification with its jitter reduction ability.

5.1 Modulator Architecture Design

For audio applications, the input bandwidth we need to cater for is around 25 kHz. In this design example, we assume that the ADC is used in the audio signal process chain where 1-bit PDM code is the intended output format. Hence, in order to avoid extra signal processing circuitry and achieve lowest possible power consumption, 1-bit internal quantizer is most appropriate. In order to achieve around 90 dB SNR, the optimum choice is 4th order loop filter with OSR=64.

As discussed in previous chapters, feedforward loop filter architecture achieves the best power efficiency. Although slight suffering in anti-aliasing features and out-of-band STF peaking indeed exist, they do not create critical threat for intended audio application. Hence, conventional CIFF loop architecture is adopted with local feedback around 3rd and 4th integrator to create in-band zero for optimum noise shaping characteristic [45].

In the mean time, one-bit feedback is incorporated for even greater power efficiency and lower architectural complexity. Feedback DAC implements the proposed FLRZ current

switching technique and the duty cycle is set as 50%. In the quantizer design, $0.5T_s$ fixed delay is purposely included to replace effect of time varying excess loop delay. In this way, excess loop delay can be compensated with coefficient tuning. Figure 5-1 shows the block level representation of the proposed modulator architecture.

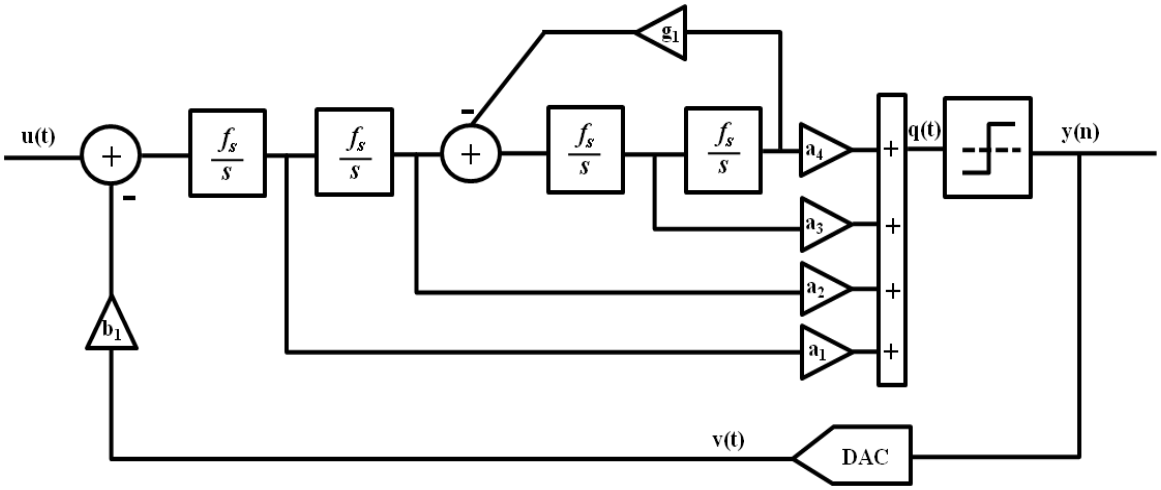


Figure 5-1 Block Level Model of Proposed Modulator Architecture

5.2 Coefficient Calculations & Mapping

Delta sigma toolbox developed by R.Schreirer is used in Matlab to determine optimum NTF(z). Suppose the modulator is of 4th order, OSR=64, OBG=1.5 and with optimization of in-band zeros enabled. Thus we have

$$NTF(z) = \frac{z^4 - 3.998\,z^3 + 5.997\,z^2 - 3.998\,z + 1}{z^4 - 3.194\,z^3 + 3.89\,z^2 - 2.134\,z + 0.444} \quad 5.1$$

Since loop transfer function $NTF(z) = \frac{1}{1+L_1(z)}$,

$$L_1(z) = \frac{1}{NTF(z)} - 1 \quad 5.2$$

From the obtained $L_1(z)$, its s-domain equivalent can be calculated using d2c command. Assume RZ feedback pulse with 50% duty cycle and half Ts delay. Hence

$$\mathrm{L_1(s)} = \frac{0.671\ \mathrm{s^3} + 0.248\ \mathrm{s^2} + 0.05566\ \mathrm{s} + 0.006166}{\mathrm{s^2}(\mathrm{s^2} + 0.00172)} \quad 5.3$$

From the modulator, the loop transfer function for feedback signal can be represented as:

$$L_1(s)' = \frac{a_1c_1\ s^3 + a_2c_1c_2\ s^2 + (a_1c_1c_4g_2 + a_3c_1c_2c_3)s + (a_4c_1c_2c_3c_4 + a_2c_1c_2c_4g}{s^2(s^2 + c_4g_2)} \quad 5.4$$

Equating $L_1(s)$ and $L_1(s)'$ term by term, and solve the obtained set of equations, the obtained coefficients are

$$a_1 = 4.0378, a_2 = 1.4897, a_3 = 0.3251, a_4 = 0.0339$$

$$c_1 = c_2 = c_3 = c_4 = 1$$

$$g_2 = 0.0017$$

$$b_1 = c_1$$

Here, c_1 through c_4 are manually set to 1 since at the moment no internal state scaling is performed. Moreover, the input scaling b_1 is set to be equal to feedback scaling c_1 for maximally flat STF.

Now with the set of coefficients available, simulation can be performed in Simulink. Next is to scale the coefficients again to limit internal state swing. In this design example, the swing is limited to 0.3 for clipping not to happen in real circuit implementation.

After a series of simulation, the resultant scaled coefficients are:

$$a_1 = 8.3909, a_2 = 5.2837, a_3 = 4.1331, a_4 = 4.5423$$

$$c_1 = 0.3397, c_2 = 0.5625, c_3 = 0.3571, c_4 = 0.0978$$

$$g_2 = 0.0171$$

$$b_1 = c_1 = 0.3397$$

5.3 From Single-End Model to Differential Model

The above block level behavioral model makes no indication about how the blocks are to be realized and is in single end mode. Nowadays, most signal processing circuits are implemented in differential manner. Differential implementation has the advantage of improved coupling noise performance and reduction of harmonic content. This design also makes no exception. The next step is to determine the implementation method of various blocks and make single to differential transformation. The most critical blocks are the loop filter integrators. Integrator can be implemented in various topologies, for e.g. active-RC, Gm-C, MOSFET-C etc. All of them have their pros and cons and could results in vastly different circuit behavior. The table below compares briefly the features of the three implementations.

Table 5-1 Comparison of Integrator Implementation Methods

	Active-RC	**MOSFET-C**	**Gm-C**
Linearity	Excellent	Modest	Modest
Power Consumption	High	High	Low
Speed	Modest	Modest	High
Input Range	High	Modest	Low

The comparison presented in Table 5-1 explains the usefulness of different implementations for particular purposes. Active-RC integrators achieve good linearity performance at the expense of power consumption. Also, the operation speed is limited by the active Op-amp core. G_m-C is a good candidate for high speed low power design

due to its open loop configuration, but it has performance limitations in terms of linearity. MOSFET-C integrators are not widely used.

As explained in previous chapter, the linearity of the first stage integrator is quite stringent. Hence, performance should not be compromised at this end of the modulator. For best linearity requirement, active-RC integrator is the natural choice. An added advantage is that it is able to incorporate very large input range. In fact, for 1-bit ΣΔ modulator design where the input to the first stage integrator is so large, active-RC integrator is probably the only implementation choice. For later stages where linearity requirement is much relaxed, the power efficient Gm-C integrator can be used. In this design example, Gm transconductor with multiple outputs is used to achieve more power saving. A natural advantage provided by Gm-C loop filter is that all signals can be processed in current domain, making addition of feedforward signal before quantizer an easy task and this could save quite a significant amount of power.

The feedback DAC is implemented with the proposed Fixed-Length Return-to-Zero current-switching DAC. The differential behavioral model is shown in Figure 5-2.

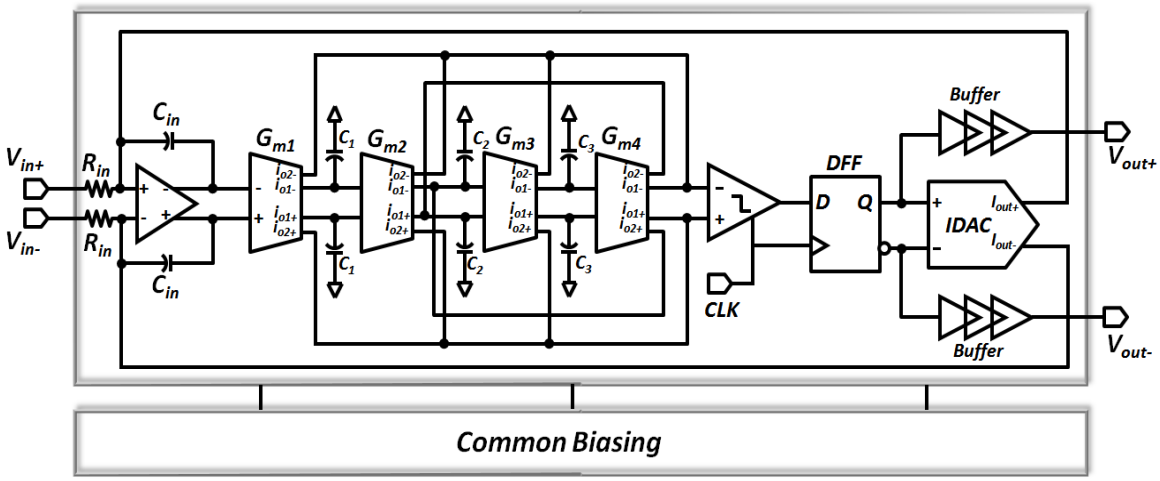


Figure 5-2 Differential Model of the Proposed Modulator

Having this differential model, now the coefficients can be mapped into circuit parameters.

For Op-amp-RC first stage,

$$b_1 f_s = \frac{1}{R_{in} C_{in}} \rightarrow R_{in} C_{in} = \frac{1}{b_1 f_s} = 9.2 \times 10^{-7}$$

Setting $R_{in} = 100k\Omega$ for acceptable dynamic rage, we have $C_{in} = 9.2pF$.

For later transconductor-C stages, the general form for coefficients mapping is

$$k f_s = \frac{g_m}{C}$$

Since there are four transconductors used in the modulator, it is convenient to use a common transconductance value. Also, since in this design, multiple-output transconductor cells are used, for good current mirror, the coefficients need to be rounded to integers or the half of two integers (like 1.5 or 2.5 etc.).

Hence for the direct forward path,

$$c_2 f_s = \frac{g_{m2}}{C_2/2} \rightarrow C_2 = \frac{2 g_{m2}}{c_2 f_s}$$

$$c_3 f_s = \frac{g_{m3}}{C_3/2} \rightarrow C_3 = \frac{2 g_{m3}}{c_3 f_s}$$

$$c_4 f_s = \frac{g_{m4}}{C_4/2} \rightarrow C_4 = \frac{2 g_{m4}}{c_4 f_s}$$

For internal feedback coefficient g_2, the situation is a bit different, g_{mfb} is determined from C_3 whereby

$$g_2 f_s = \frac{g_{mfb}}{C_3/2} \rightarrow g_{mfb} = \frac{g_2 f_s C_3}{2}$$

For feedforward path, what really matters is the ratio of those coefficients a_1 to a_4. Since the feedforward quantity is current, so the ratio of feedforward coefficients is actually ratio of $g_{m1}', g_{m2}', g_{m3}'$, g_{m4}. Here $g_{m1}', g_{m2}', g_{m3}'$ are secondary outputs of the multiple-output transconductor cells.

Circuit parameters are tabulated as shown below.

Table 5-2 Circuit Components Values

	Transconductor 1 (G_{m1})		**Transconductor 2 (G_{m2})**		**Transconductor 3 (G_{m3})**		**Transconductor 4 (G_{m4})**	
Item	g_{m1}	g_{m1}'	g_{m2}	g_{m2}'	g_{m3}	g_{m3}'	g_{m4}	g_{mfb}
Value(S)	360n	4×360n	360n	2.5×360n	360n	1.5×360n	496n	17.17n
Item	R_{in}	C_{in}	C_1	C_2	C_3			
Value	100kΩ	9.2pF	400fF	630fF	2.3pF			

5.4 Circuit Implementations

In this research, 0.18µm CMOS technology is used. The design need to cater for a supply voltage of 1.5V. At input, the common mode level is roughly in the middle of the supply rail which is 700mV.

5.4.1 Class AB Op-amp in First Stage Active-RC Integrator

The Op-amp in first stage active-RC integrator has to satisfy a set of specifications predicted from behavioral simulation. The key design parameters are listed below.

Table 5-3 Key Specifications for Op-amp in 1st Stage Integrator

Input CM Voltage	0.7 V
Output CM Voltage	0.5 V
GBW	Around 9.6 MHz
DC Gain	>60 dB
Slew Rate	>3MV/s

In order to achieve good power efficiency, class AB output stage was used. The circuit implementation of this OTA is presented in Figure 5-3[46]. This design adopts two-stage architecture. Besides achieving higher output swing, it is also proven that a two-stage design has better performance in terms of reducing in-band noise related to op-amp non-linearity.

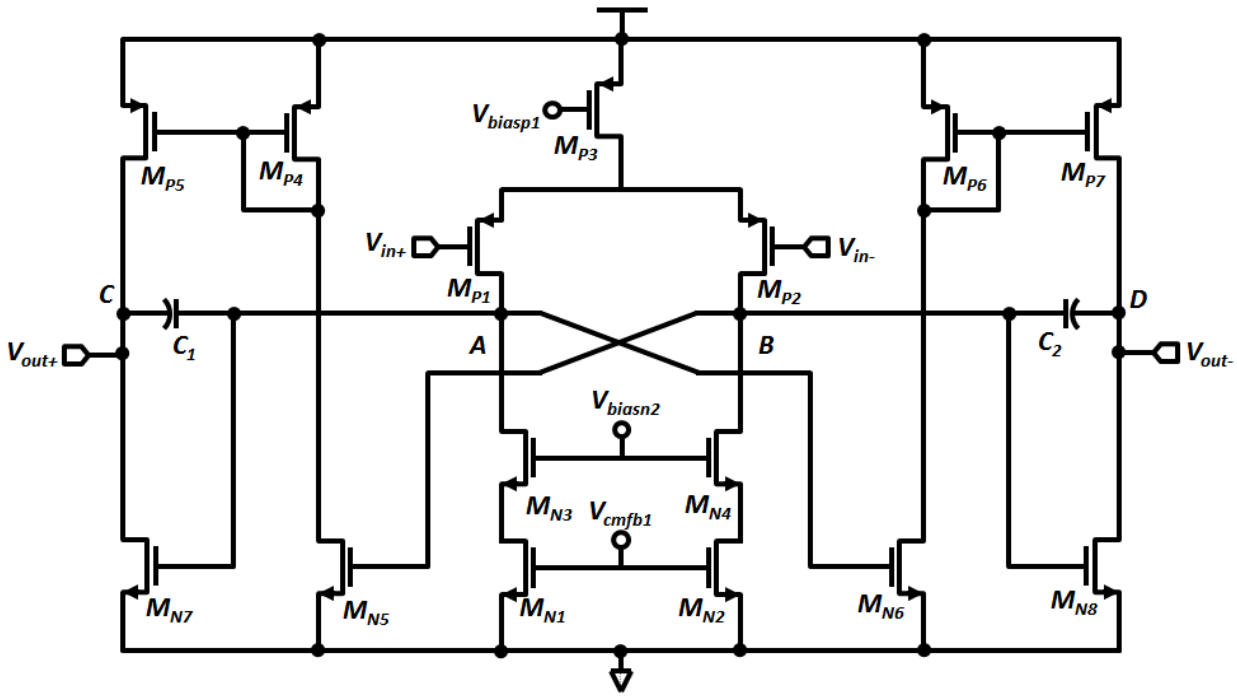


Figure 5-3 ClassAB Op-amp Implemented in 1st Stage Integrator

The input stage is critical in the aspect of input referred noise. Since input transistor M_{P1}, M_{P2} and current source load M_{N1}, M_{N2} are most significant noise contributor, they are dimensioned with long channel (L=10μm) for low flicker noise and thermal noise. The first stage biasing current is set to 12 μA so as to contain noise and avoid slew. The 2nd stage comprises of M_{P4}~M_{P7} and M_{N5}~M_{N8} which are configured in classAB operation. The quiescent current in the output branches are roughly 10 μA and the peak current can be as high 30 μA.

Due to differential operation, both stages require common mode feedback circuit to stabilize the common mode voltage at respective nodes. At nodes A & B, the expected the voltage swing is small, so CMFB with two transistor pairs [47] are used as shown in Figure 5-4.

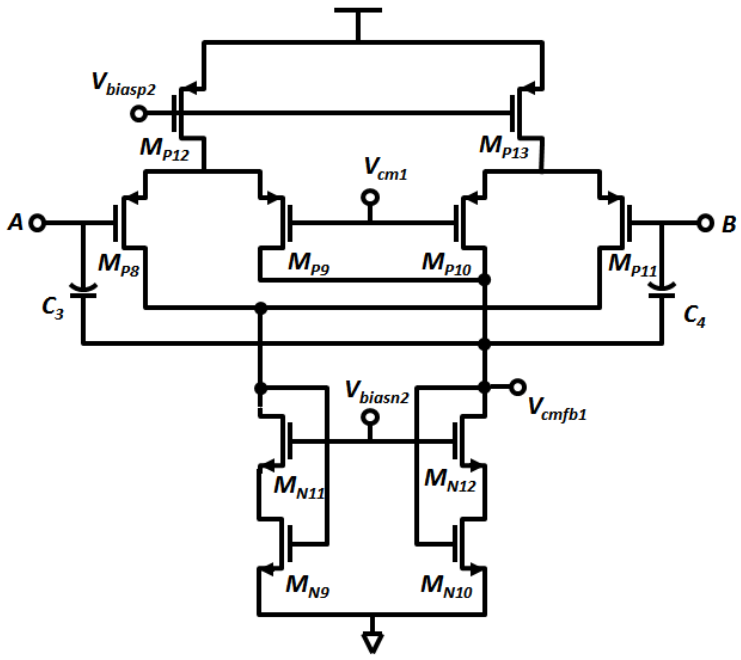


Figure 5-4 CMFB for 1st Stage Output of the ClassAB Op-amp

The two capacitors C_3, C_4 are added to bypass high frequency signals so that stability is improved. V_{cmfb1} is the control voltage for first stage current load biasing which in turn sense and correct the common mode voltage.

Since the output stage need to accommodate large signal swing, so the job of sensing output common mode is more appropriately done by resister divider. The implementation is shown in Figure 5-5.

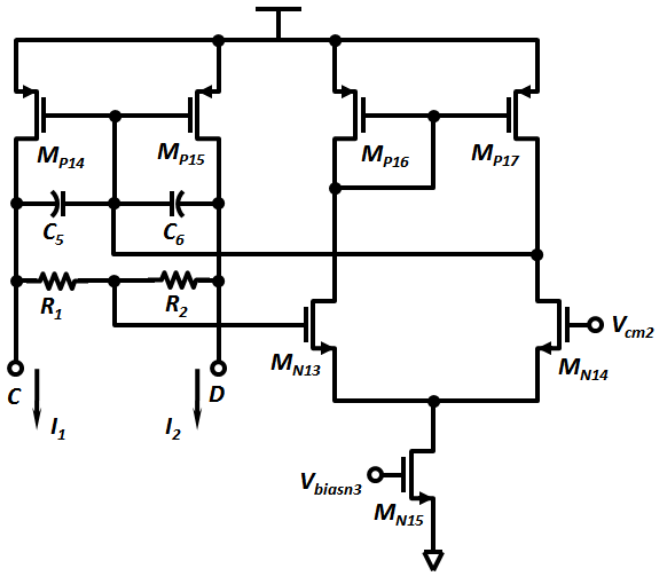


Figure 5-5 CMFB for 2nd Stage Output of the ClassAB Op-amp

In order not to load output nodes, sensing resistors R_1, R_2 are usually large. In this case, they are set to be 1M ohms. Since there is no available gates to control the biasing current in the output branch, direct current feedback is used. Currents I_1, I_2 are the extra current being fed into the output branches and perform as the regulation current to control the output common mode level. The quiescent value of these two currents should not be set very high. Otherwise the slew rate might be suffered as this part of current does not respond to normal signal swing. In this case, I_1, I_2 are set as 1.5μA per branch comparing to output quiescent current of 10 μA per branch.

Finally, the bode plot of this classAB Op-amp is shown in Figure 5-6.

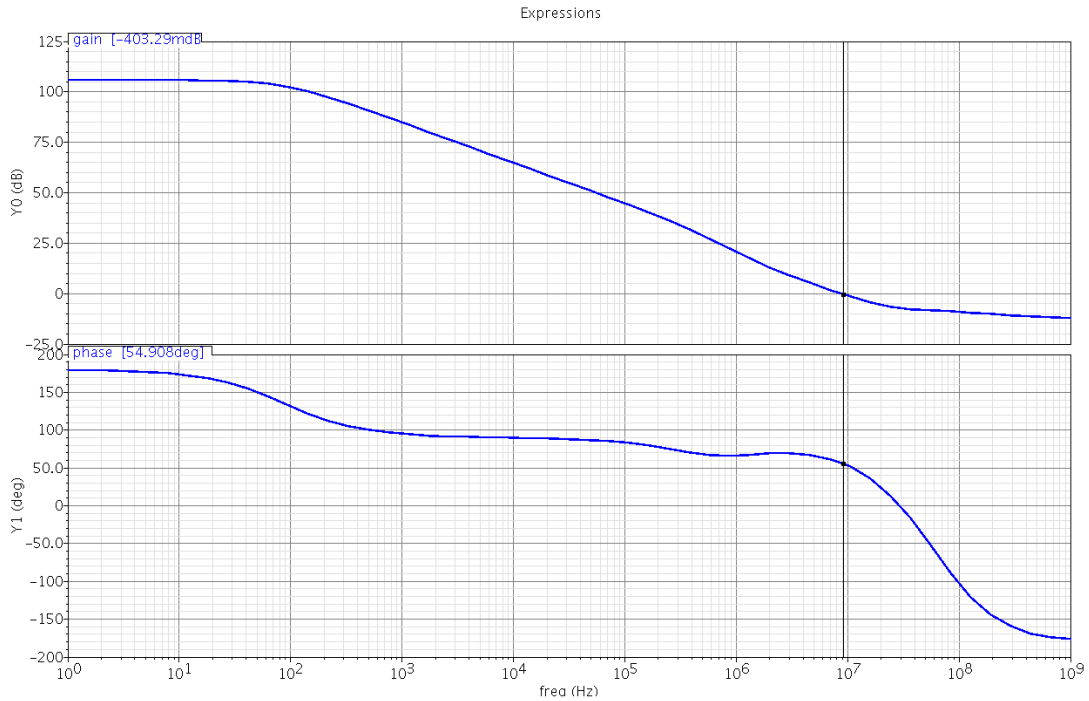


Figure 5-6 Bode Plot of the ClassAB Op-amp

The following table tabulates the key performance achieved by this classAB amplifier.

Table 5-4 Performance Summary of the ClassAB Op-amp

Specification	**Value**
DC Gain	106dB
Phase Margin	55^o
Gain Bandwidth Product	9MHz
Slew Rate	6MV/s
HD3	79dB
Current Consumption	36 µA

5.4.2 Multiple-output Transconductor

Triode based transconductor was implemented in later stages (2^{nd}~4^{th} stage) as the core component of G_m-C filter. This type of transconductor has simple form as well as the ability to provide multiple outputs. This feature helps to save the number of transconductors that has to be used and reduces total power consumption. The core of this transconductor is shown in Figure 5-7.

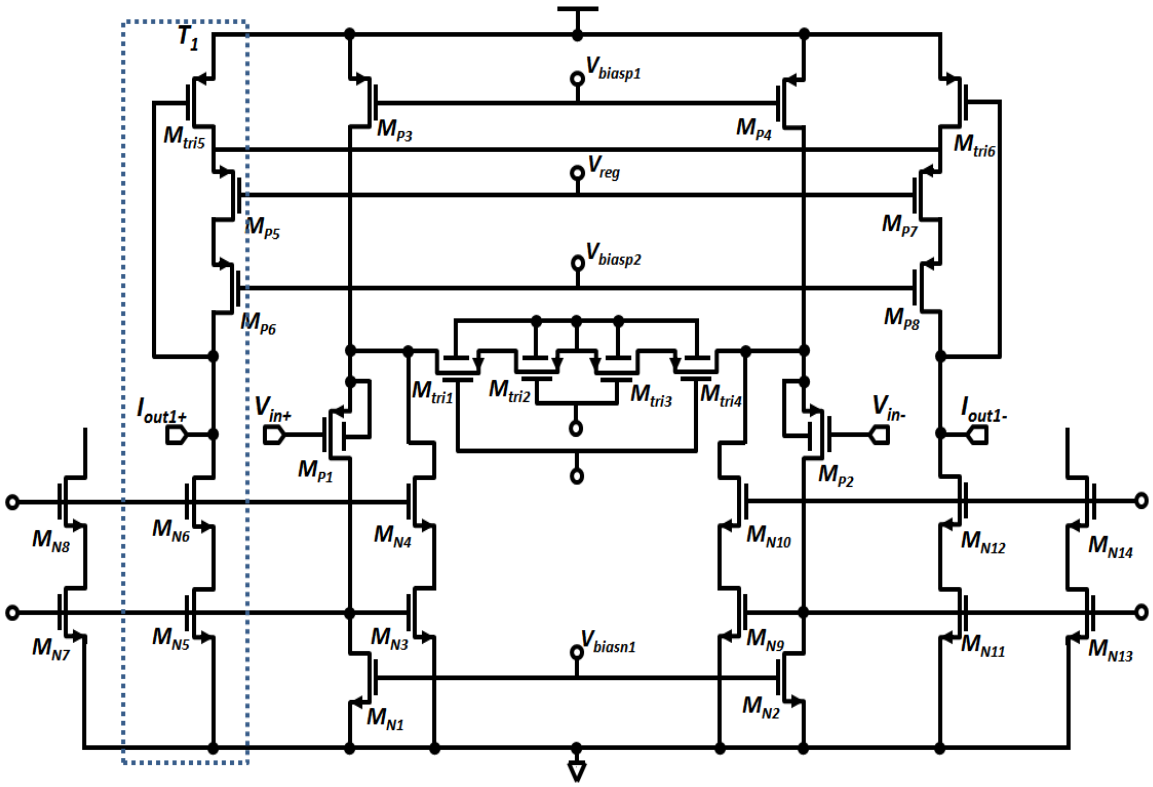


Figure 5-7 Schematic of Triode Based Multiple-output Transconductor

In this implementation we use p-channel input configuration to accommodate an input common mode voltage of 0.5V. According to design, specification, swing of 0.4 at input node must be accommodated. M_{tri1}~ M_{tri4} operate in triode region and can be treated as series connected resistors. Here four transistors are used to realize the transconductance which is different from the conventional design as introduced in [48]. Using more devices helps to reduce electron mobility degradation effect and improves linearity.

Common Mode Feedback

Common mode feedback circuit normally consumes extra power as well as limits the output range of the transconductor.

Differential transconductors need common mode feedback to accurately define its output common mode voltages. Most CMFB implementations would need auxiliary amplifiers and reference voltage for sensing and feedback control. This will inevitably consume extra power. The most power efficient CMFB technique is probably the deep triode based feedback method. As shown in Figure 5-7, transistor M_{tri5} and M_{tri6} operate in deep triode region. They sense the voltage at output node I_{out1+} and I_{out1-}, and then control the biasing current in output branches. It is clearly seen that using such technique, no extra power dissipation is suffered. And the amount of power saved by such implementation is quite significant considering there are at least four transconductor cells.

However, a drawback of this technique is the common mode level is not accurately defined. It is strong function of the triode device parameters such as aspect ratio and threshold voltage. In [49], the author proposes to use reference branch for better common mode level definition. But it does not solve the issue completely. In this project, we also use reference branch, but with an extra auxiliary amplifier and reference voltage for better control. The circuit schematic is shown in Figure 5-8.

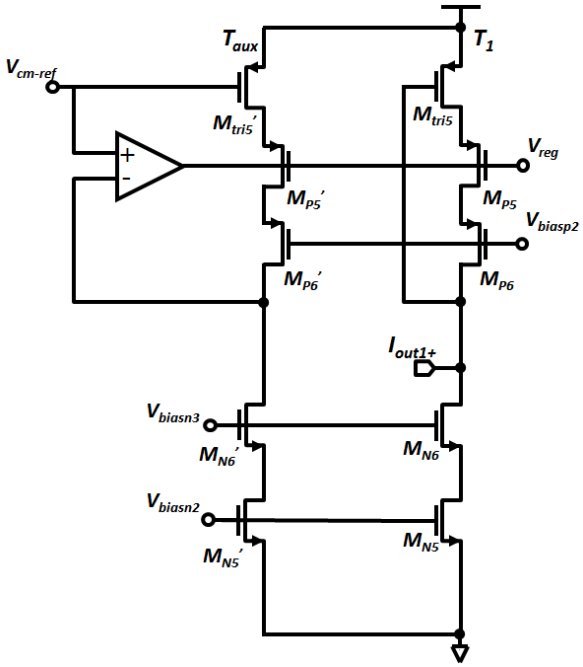


Figure 5-8 Accurate Definition of Common Mode Level Using Auxiliary Amplifier

In reference branch, gate of M_{P5} is dynamically controlled by the output of the auxiliary amplifier V_{reg}. Even if there is a parameter shift in the triode device or even the current mirror devices, the reference output still maintains a voltage level same as $V_{cm\text{-}ref}$. The key is to ensure a good matching between the reference branch and actual output branch. This requires careful layout attention.

Here although we use an extra branch and extra amplifier, they do not create huge power consumption overhead. This is because the regulation voltage generated by this reference branch can be used in all transconductor cells. For example in this case, the current consumed by this reference branch and auxiliary amplifier is 3 μA, averaging less than 1 μA extra current in each transconductor cell.

The biasing current flowing down each output branch is set at 1 μA. The common mode definition circuit roughly took up 4 μA, but it was used to regulate all four transconductors and hence this extra current does not create excessive power consumption.

Linear Range of the Transconductor

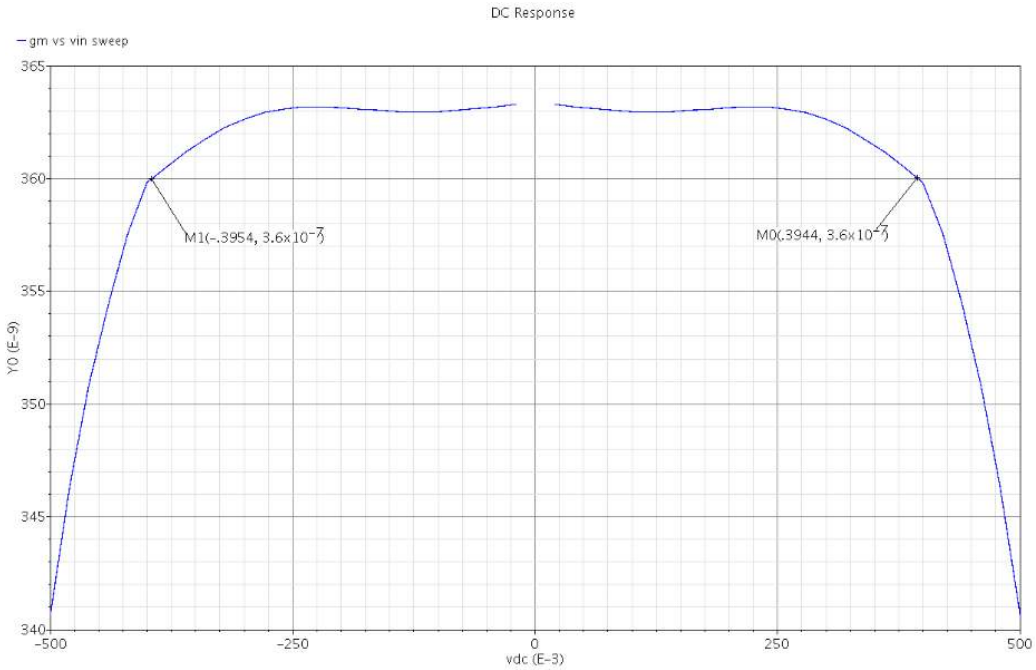


Figure 5-9 Linear Range Plot of the Multiple Output Transconductor

Testing of linear range shows the designed transconductor exhibits good enough linearity (1% variation or around 40 dB linearity) with input voltage below 400 mV. This range is wide enough to accommodate the intended voltage swing from last stage which in this design is around 300 mV.

5.4.3 Quantizer

Thanks to current summing, an adder that is normally needed can be saved. Output current can be directly feed into quantizer and compared through a current comparator. We adopts the current comparator topology, but with an added pre-amp to avoid kick-back noise. The circuit schematic is shown in Figure 5-10.

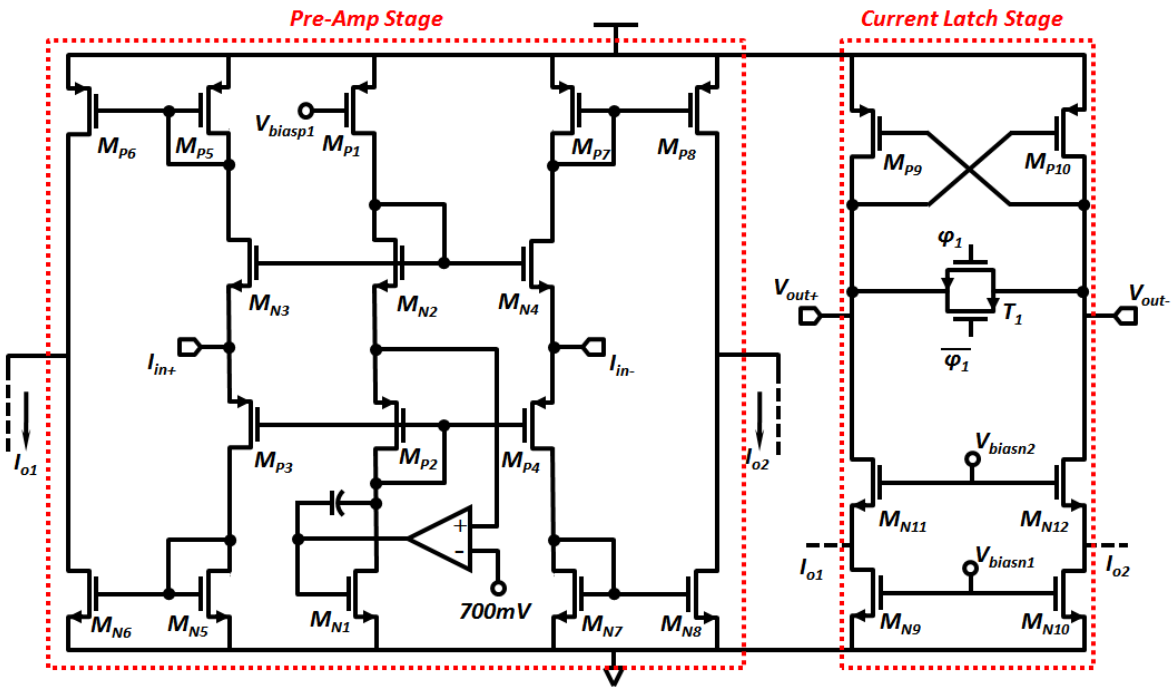


Figure 5-10 Schematic of the 1-bit Current Latch Quantizer

The pre-amp provides amplification to the input signal and improves the settling time in the 2nd latching stage. It also isolates the latch from the loop filter output, preventing the kick-back noise. It should be noted here, the current input nodes are very low impedance nodes. Hence, their DC voltages are quite well defined. In this case, it is defined by the auxiliary amplifier which fixed it around 700mV. So output ports from Gm-C integrators which connect directly to the two current input pins require no common mode regulation from transconductors themselves.

The 2nd stage is a cross-coupled latch which performs the sampling and comparison operation. During the 1st phase, the transmission gate is closed and the latch is reset, and the two output voltages are brought to the same level, preferably the middle of the pulse swing (around 700 mV). This minimizes the switching time needed when the two output changes states. During 2nd phase, the transmission gate opens, and the latch starts comparison. The cross coupled latch is configured in positive feedback manner. It senses small difference in input current and quickly amplifies it. The simulation of a 1nA current

input is shown in Figure 5-11. The quantizer is able to respond with fast speed even at small input current level.

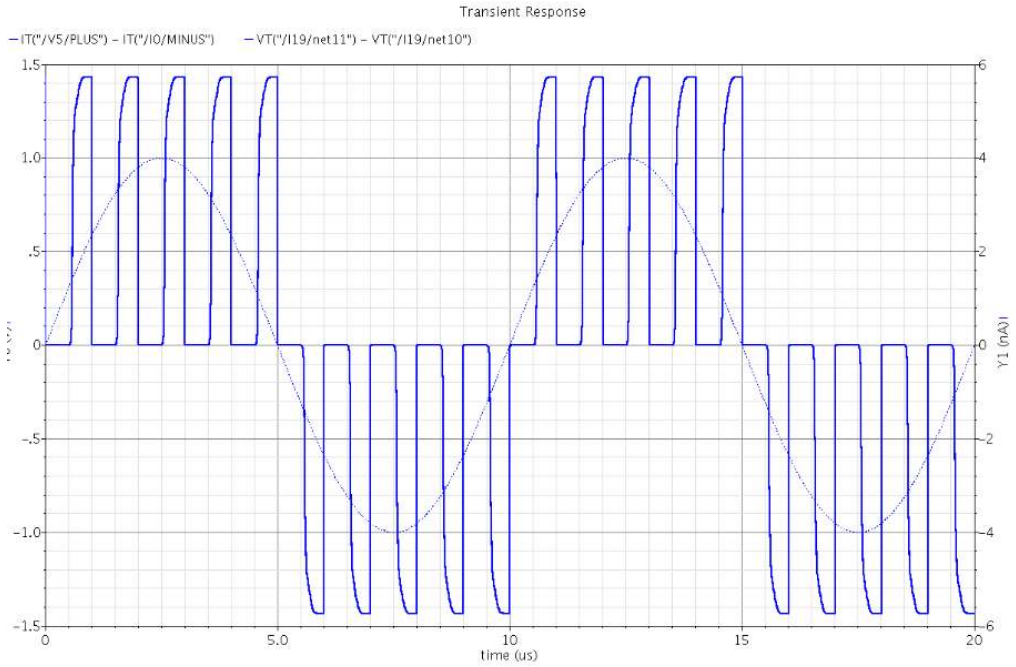


Figure 5-11 Output Waveform of the Quantizer with 1nA Amplitude Current Input

5.4.4 The Fixed Length Return-to-Zero DAC Cell

The fixed length return-to-zero DAC proposed in Chapter 4 has been implemented. The schematic is shown in Figure 5-12. The operation principle of this DAC cell has been thoroughly explained in Chapter 4.

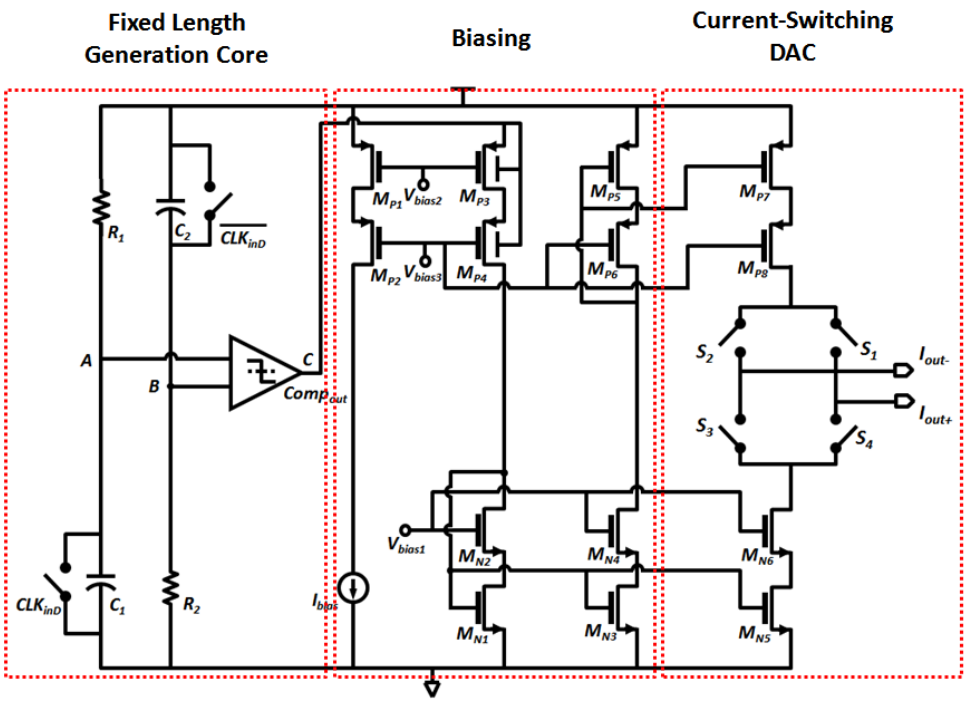


Figure 5-12 Schematic of the Proposed FLRZ DAC Cell

The clocking of various switches is critical to the achievable performance. Following the proposed clocking scheme as introduced in chapter 4, the extra clock control generation circuitry is shown in Figure 5-13.

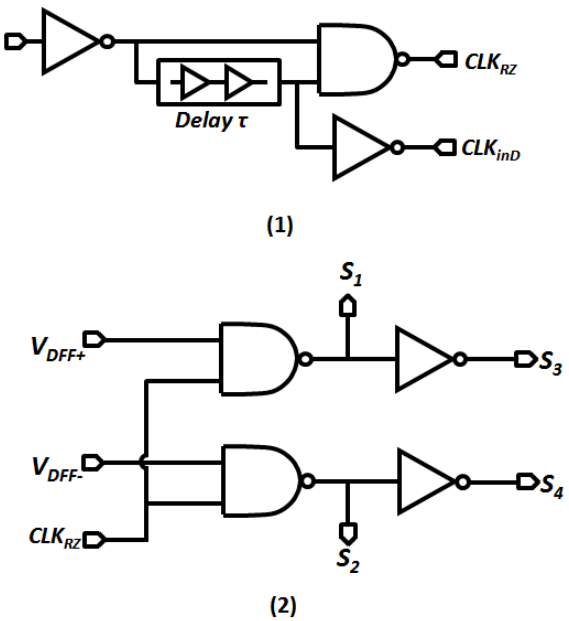


Figure 5-13 Internal Control Signal Generation Circuit

CLK_{inD} is used to clock the fixed length pulse core generation circuit. CLK_{RZ} is further processed in the 2nd part to generate switch control signals for S1~S4. The output current pulses generated by the proposed DAC cell are shown in Figure 5-14.

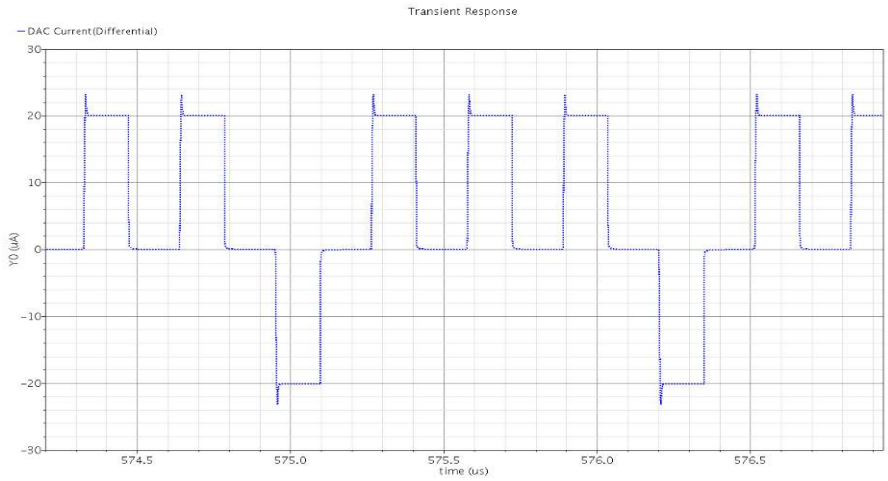


Figure 5-14 Output Current Waveform of the FLRZ DAC Cell

5.5 Layout Considerations

ΣΔ modulator is a complicated mixed signal system which requires careful planning during layout. High resolution and linearity do not just depend on circuit operations. They also depend on effects such as mismatch, parasitic, noise coupling etc. These effects are highly related to how well the circuit is being laid out.

Typically, in ΣΔ modulator design, circuits can be broadly divided into two domains: analog domain and digital domain. This division is important as layout consideration for analog circuit and digital circuit are different. Generally speaking, layout for analog cells is much more difficult because their immunity to noise (ground, power line), interference and mismatch are quite poor. Digital circuitry on the other hand is born with high immunity to noise and hence require much less layout effort. Not only this, the digital circuits tend to couple more noise into ground and power line. It is for this reason that in

most practices, analog portion and digital portion will have their individual ground and power supply. For CT ΣΔ modulator in particular, analog blocks like loop filter, DAC are at front end which is the most vulnerable point in the entire system while digital blocks sit at back end, being noise shaped by previous stages. Hence, most of the layout effort should be put on the blocks directly related to the input stage, namely, the 1st stage integrator and feedback DAC.

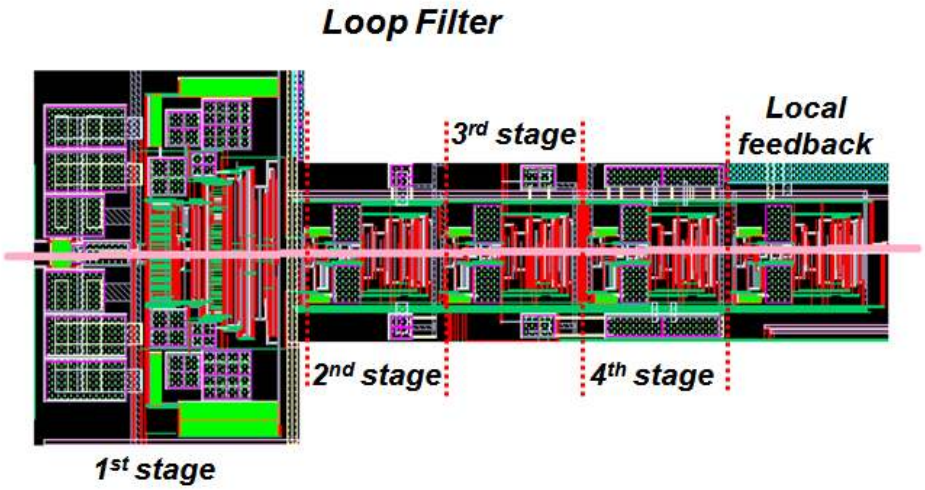


Figure 5-15 Layout View of Loop Filter

Differential circuit is designed to fight noise and even order distortion provided the circuit is fully symmetrical. So symmetry and matching is important in analog front end. With this in mind, the loop filter is being laid out with a virtual line of symmetry as shown in Figure 2-1. And the floor plan of the individual integrators also follows the direction of the signal flow. Within each cell, critical matching devices such as differential pair, current mirror are being laid out with common centroid technique. Resistors are being inter-digitized. Dummies are also added to further improve matching condition. For the main signal path such as the inputs and outputs of each integrator, each line is shielded with analog ground on both sides to reduce potential signal coupling between the two differential paths (Figure 5-16).

Figure 5-16 Shielding of Signal Line

Ideally speaking, feedback DAC should work in a third domain which should also be very quiet. This is to reduce the noise which may cause elevation of the system jitter noise. However, in this design, this is not critically important as the operation speed is considered moderate which does not cause serious noise issue. Hence, we put this DAC also in analog domain with guard ring surrounded.

The entire layout with pad is shown in Figure 5-17. It occupies an area of 1.725mm^2.

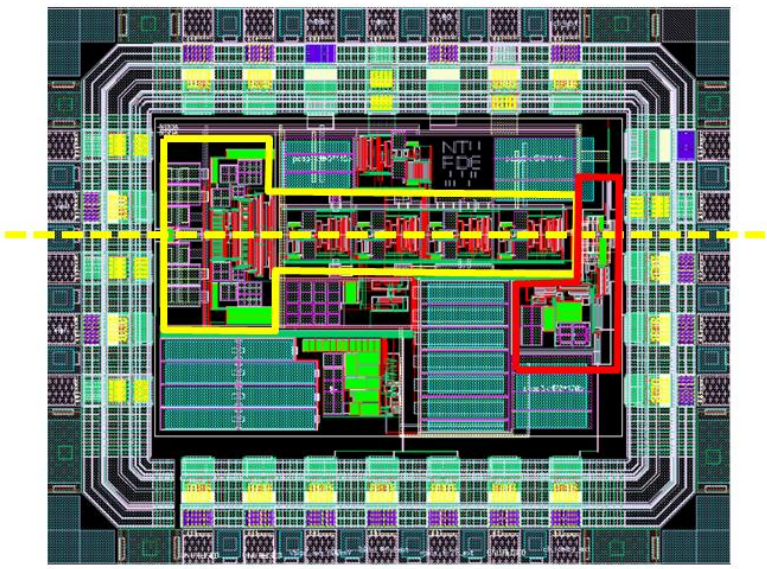


Figure 5-17 Layout View of Entire Modulator with Pads

5.6 Simulation Results

The entire circuit level transient simulation has been carried out. To ensure reasonably good indication of stability, at least 8192 sampling point must be taken. A few hundreds of sampling points at the beginning of the simulation were discarded due to incomplete settling. Blackman window was used to perform FFT on output waveform. The input dynamic range plot is shown in Figure 5-18.

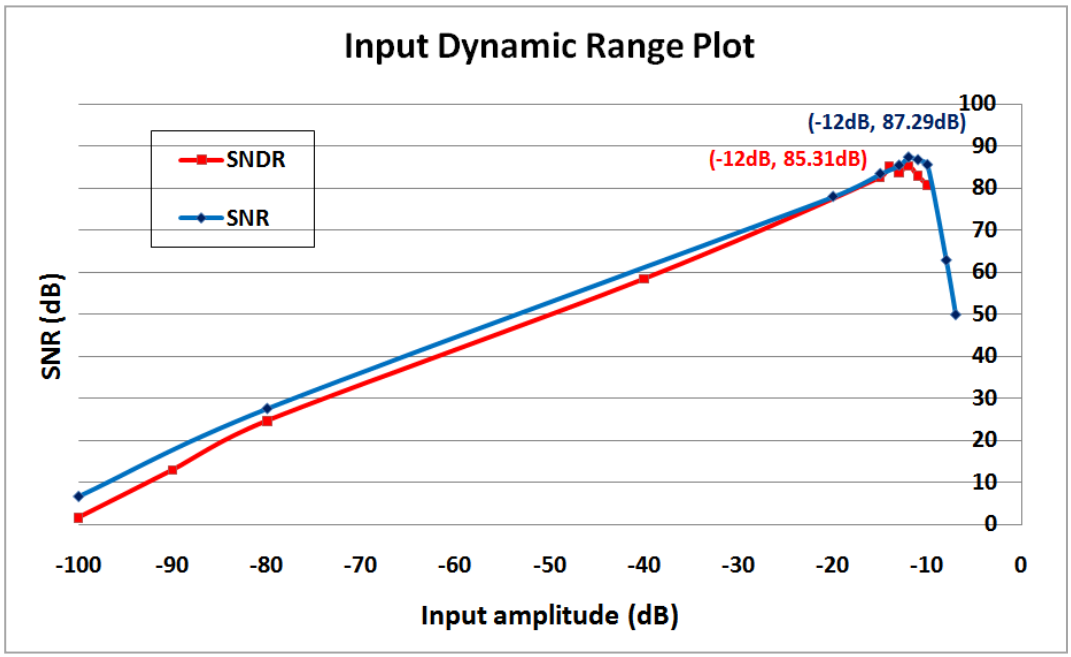


Figure 5-18 Dynamic Range Plot of the Designed Modulator

SNDR plot was simulated with input frequency below BW/3 while SNR plot was simulated with input frequency between BW/2 and BW.

From the dynamic range plot, it can be seen the overload level for input signal is around -10 dBFS. The internal nodes states for an -10dBFS input signal are shown in Figure 5-19.

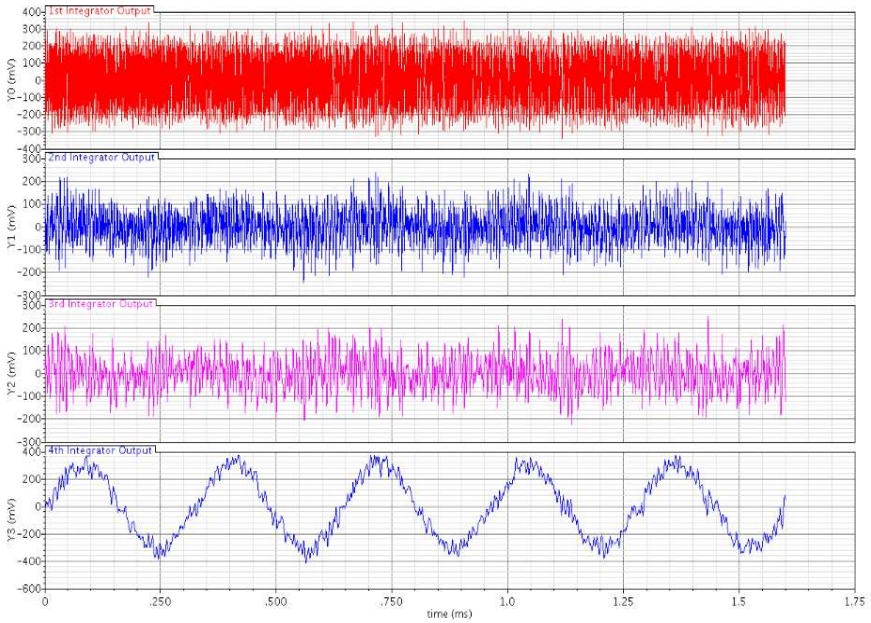


Figure 5-19 Signal Swing for Internal Nodes (Output of Each Integrator)

It can be observed that all internals nodes swing is well defined within around 0.3 which is predicted from behavioral simulation.

The overall performance is summarized in Table 5-5.

Table 5-5 Performance Summary of the Modulator

Specifications	**Results**
Process	Chartered 018 IC CMOS process
Supply Voltage	1.5 V
Peak SNDR	85.31 dB
Peak SNR	87.29 dB
Dynamic Range	90 dB
ENOB	14.2 bits
Power Consumption	Total:207µW (excl. biasing)
	Analog: 120 µW
	Digital: 87 µW
	Biasing: 24 µW
FOM	0.22 pJ/conversion
Die Area	1.725mm^2

Lastly, this work is compared with some other reported works with similar specifications. In this case, only designs with bandwidth below 25 kHz (audio band) are included. The comparison is mainly in the aspects of FOM which is shown in Table 5-6.

Table 5-6 Comparison of Several Reported Works

Ref	BW (Hz)	OSR	ENOB (bits)	DR (dB)	Peak SNR (dB)	Power Consumption	Supply Voltage (V)	FOM (pJ/con.)
[13]	3.4k	64	13.0	80	80	0.21mW	2.2	3.78
[36]	25k	48	10.7	81	66	0.25mW	1.5	3.07
[50]	25k	48	11.8	80	73	0.15mW	1.5	0.74
[40]	20k	128	16.2	106	99	18mW	3.3	6.18
[51]	20k	300	12.5	95	77	2.2mW	1.5	9.51
[46]	24k	64	15.4	93.5	92	90μW	1.5	0.054
This work	25k	64	14.1	90	87	0.2mW	1.5	0.22

Chapter 6
Conclusions & Future Work

6.1 Conclusions

In this thesis, the fundamental working principles of ΣΔ have been thoroughly reviewed. Since DT ΣΔ modulator is most well studied and its design synthesis most well developed, DT modulator is first introduced. By showing DT modulator's limitations and CT modulator's great potential to counteract them, CT ΣΔ modulator's existence and development is well justified. Although there is no fundamental difference between the two types of modulator, the design procedure and design consideration are still different.

Focusing on audio range CT implementations, various design trade-offs regarding power performance efficiency have been introduced and explained. In CT ΣΔ modulator design, probably the most critical design phase is the modeling of modulator's non-idealities. In order to eliminate or minimize them for best performance, a thorough understanding of their effects on different system topology becomes necessary. In this research, various non-ideal effects including finite GBW, coefficients variation, slew rate limitation, offset, ISI effect and thermal noise etc. have been investigated. The significance of doing so is to help determining critical boundaries conditions for specific design target.

Architectural timing non-idealities are the biggest obstacle for CT ΣΔ modulators to be implemented in high speed data conversion and hence are the major disadvantage of CT modulators comparing to their DT counterpart. Timing non-idealities mainly includes excess loop delay (ELD) and clock jitter issues. ELD problems may be solved by coefficients tuning or extra feedback path technique and the solution is well established. But the clock jitter issue is more difficult to solve and it may lead to detrimental effect if

not treated properly. In this research, a special pulse shaping technique which is called fixed length return-to-zero method was proposed. Simulation shows it almost achieves the best performance pulse shaping method can achieve. It not only greatly improves CT modulator's jitter performance, but also exerts very little adverse effects such as increased power consumption, circuit overhead, and increased loop delay. This is one of the primary contributions of this research.

For the purposed of verifying various design concepts developed in this research, a 4^{th} order 1-bit prototype modulator has been developed. Simulation shows it is able to achieve 85 dB SNDR for 25 kHz input signal range. And the FOM it achieves is 0.22pJ/conversion. This value is quite competitive in comparison with some other design with similar specifications.

6.2 Future Works

In the course of this research, there are numerous times when some interesting thoughts had come to my mind. However, due to limited time frame and resources, not all of them can be investigated further. But they are suitable for future research.

Firstly, in this project, the design requirement for the proposed FLRZ DAC is not very stringent. Theoretically speaking, the FLRZ DAC is able to work in very high sampling rate and it is compatible with multi-bit design. However, none of these two theories has been verified in this research yet. Hence, it is more convincing to implement this proposed DAC into high speed applications and generates satisfactory results.

Secondly, for continuous time ΣΔ design, first integrator Op-amp is always the primary target for power reduction. In theory, several methods have been proposed to reduce Op-amp's GBW requirement. However, they are not viable in practical sense due to close

relationship between GBW and slew rate. One way to strike a balance is to use multi-bit feedback technique such that slew rate requirement is very much reduced. The challenge is to perform accurate GBW compensation for the multi-bit feedback. Since this research mainly deals with single-bit design, this was not explored and might be potential future direction.

Also, this research mainly concentrates on low speed single bit design for best power performance balance. In future work, a potential area for new breakthrough is to explore the power saving techniques on multi-bit design. Some initial ideas include stepping down of sampling frequency for quantizer and DAC cell, tracking of input signal range for selective comparators operation and more effective DEM technique etc.

Author's Contribution

[1]. Y.H. Leow, F. Zhang and L.L. Teh, "A circuit based behavioral modeling of Continuous-Time Sigma Delta modulators," Proceedings of IEEE International Symposium on Integrated Circuits, 2009, pp. 109-112.

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Appendix
Circuit Dimensions

I. Circuit Parameters for Proposed FLRZ DAC in Figure 4-13.

Device Name	Dimension		Device Name	Dimension
R_1,R_2	300kΩ		C_1,C_2	600fF
I_{bias}	2μA		M_{P1}~ M_{P4}	$\frac{0.22\mu m}{0.18\mu m}$
M_{N1}~ M_{N2}	$\frac{0.22\mu m}{0.18\mu m}$		M_{N3}~ M_{N4}	$\frac{0.22\mu m}{0.18\mu m} \times 5$

II. Circuit Parameters for Proposed ClassAB Op-amp in Figure 5-3.

Device Name	Dimension		Device Name	Dimension
M_{P1}~ M_{P2}	$\frac{8\mu m}{2\mu m}$		M_{P3}	$\frac{1\mu m}{1\mu m}$
M_{P4}~ M_{P7}	$\frac{2\mu m}{1\mu m}$		M_{N1}~ M_{N2}	$\frac{1\mu m}{10\mu m}$
M_{N3}~ M_{N4}	$\frac{2\mu m}{6\mu m}$		M_{N5}~ M_{N8}	$\frac{1\mu m}{0.8\mu m}$
C_1,C_2	1.5pF			

III. Circuit Parameters for 1st stage output CMFB of ClassAB Op-amp in Figure 5-4.

Device Name	Dimension		Device Name	Dimension
M_{N9}~ M_{N10}	$\frac{1\mu m}{10\mu m}$		M_{N11}~ M_{N12}	$\frac{2\mu m}{6\mu m}$

M_{P8}~ M_{P11}	$\frac{8\mu m}{2\mu m}$		M_{N12}~ M_{N13}	$\frac{1\mu m}{1\mu m}$
C_3,C_4	125fF			

IV. Circuit Parameters for 2nd stage output CMFB of ClassAB Op-amp in Figure 5-5.

Device Name	Dimension		Device Name	Dimension
M_{P14}~ M_{P15}	$\frac{2\mu m}{2\mu m}$		M_{P16}~ M_{P17}	$\frac{4\mu m}{1\mu m}$
M_{N13}~ M_{N15}	$\frac{2\mu m}{1\mu m}$		C_3,C_4	300fF
R_1,R_2	1MΩ			

V. Circuit Parameters for Triode-Based Multiple-Output G_m in Figure 5-7.

Device Name	Dimension		Device Name	Dimension
M_{tri1}& M_{tri4}	$\frac{0.6\mu m}{20\mu m}$		M_{tri2}& M_{tri3}	$\frac{0.6\mu m}{4.8\mu m}$
M_{tri5}& M_{tri6}	$\frac{0.8\mu m}{4\mu m}$			
M_{P1}~ M_{P2}	$\frac{4\mu m}{1\mu m}$		M_{P3}~ M_{P4}	$\frac{2\mu m}{2\mu m}$
M_{P5}& M_{P7}	$\frac{2\mu m}{1\mu m}$		M_{P6}& M_{P8}	$\frac{2\mu m}{0.4\mu m}$
M_{N1}~ M_{N2}	$\frac{2\mu m}{4\mu m}$		M_{N3}, M_{N5} M_{N9}, M_{N11}	$\frac{1\mu m}{0.8\mu m}$
M_{N4}, M_{N6} M_{N10}, M_{N12}	$\frac{1\mu m}{2\mu m}$			

VI. Circuit Parameters for CMFB of Triode-Based Transconductor in Figure 5-8.

Device Name	Dimension		Device Name	Dimension
M_{N5}'~ M_{N5}	$\frac{1\mu m}{0.8\mu m}$		M_{N6}'~ M_{N6}	$\frac{1\mu m}{2\mu m}$
M_{P5}'~ M_{P5}	$\frac{2\mu m}{1\mu m}$		M_{P6}'~ M_{P6}	$\frac{2\mu m}{0.4\mu m}$
M_{tri5}'~ M_{tri5}	$\frac{0.8\mu m}{4\mu m}$		$M_{cm\text{-}ref}$	500mV

VII. Circuit Parameters for 1-bit Current Latch Quantizer in Figure 5-10.

Device Name	Dimension		Device Name	Dimension
M_{N1}	$\frac{4\mu m}{1\mu m}$		M_{N2}~ M_{N4}	$\frac{10\mu m}{0.5\mu m}$
M_{N5}& M_{N7}	$\frac{4\mu m}{1\mu m}$		M_{N6}& M_{N8}	$\frac{12\mu m}{1\mu m}$
M_{N9}~ M_{N10}	$\frac{1\mu m}{1\mu m}$		M_{N11}~ M_{N12}	$\frac{20\mu m}{0.5\mu m}$
M_{P1}	$\frac{6\mu m}{1\mu m}$		M_{P2}~ M_{P4}	$\frac{10\mu m}{0.5\mu m}$
M_{P5}& M_{P7}	$\frac{6\mu m}{1\mu m}$		M_{P6}& M_{P8}	$\frac{18\mu m}{1\mu m}$
M_{P9}~ M_{P10}	$\frac{0.22\mu m}{0.6\mu m}$			