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Design of inductively degenerated common source RF CMOS Low Noise Amplifier

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Abstract. The Low Noise Amplifier (LNA) is the first stage in RF CMOS receivers. The Common Gate (CG) LNA and Inductively Degenerated Common Source (CS) LNA are one of the widely used topologies for realizing RF CMOS receivers. The present work emphasizes a simple and exhaustive search procedure for the synthesis and analysis of CMOS CG and Inductively Degenerated CS LNA circuits. The width (W), gate source voltage (V_{gs}) and drain source voltage (V_{ds}) of the transistors constitute the design space in the circuit design. The design first involves the use of a circuit simulator (HSPICE) to obtain the small signal parameters of the circuit for various W, V_{gs}, and $V_{ds}$of the transistors and then to generate a Look-Up Table (LUT) for all design points using the obtained values. This LUT is used to meet the target performance specifications along with appropriate analytical expressions derived from the circuit in a numerical simulator (MATLAB). This will enable one to explore the whole design space quickly and fastly for arriving at the optimal values for the device dimensions, bias voltages and bias currents of the two LNA circuits. The design methodology is demonstrated by designing CG and Inductively Degenerated CS LNA circuits using 90 nm CMOS technology library in which Inductively Degenerated CS LNA gets high gain and low noise figure than CG LNA.

Keywords. Design space exploration; design points; CG-LNA; CS inductive degenerated LNA.

1. Introduction

Radio Frequency Integrated Circuits (RFIC) normally work between 300 MHz to 30 GHz. RFIC applications include a mobile phone, WLAN, UWB, GPS and Bluetooth devices, etc. The optimal design of CMOS RF circuits that meets all target specifications is a challenging task. The success of a receiver's design is measured in multiple dimensions: receiver sensitivity, selectivity, and proclivity to reception errors. It calls for intuition, prior design experience, and time-consuming simulations to be carried out with circuit simulators. In the design of CMOS RF circuits, the main challenge to meet the design specifications is in the optimum selection of the sizes of the various transistors and the associated DC bias levels. Given a set of device dimensions and bias voltages, circuit simulators can evaluate the performance of the circuit with very high accuracy. But the simulation time required to exhaustively explore the entire design space (all permissible devices dimensions and bias voltages) is difficult to estimate and is normally prohibitively very high.

The first stage of a CMOS RF receiver is Low Noise Amplifier (LNA). The LNA plays an undisputed importance in the receiver design. Its main function is to provide enough gain to amplify extremely low signals without adding noise, thus preserving the required signal to noise ratio of the system at extremely low power levels. The design methodology for Radio Frequency (RF) CMOS LNA using current-based Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) model was converted from weak to strong inversion regions including moderate inversion by Baroncini *et al* [1]. The inductor realization constraints are not considered and hence noise expressions require some corrections. The transistors that operate in moderate inversion are larger than those in strong inversion. As the integrated inductors are much bigger, the area is increased and NF of 1.4 dB is obtained for 2.5 GHz frequency.

An inductorless LNA with an active balun for radio applications between 100 MHz and 6 GHz was proposed by Blaakmeer *et al* [2]. A combination of a CG stage and an admittance-scaled CS stage with replica biasing is exploited to maximize balanced operation simultaneously canceling the noise and distortion of the CG stage. NF close to or below 3 dB is achieved for 0.2–5 GHz frequency and 1.2 V power supply and good linearity is obtained when the CS-stage is carefully optimized.

*For correspondence

A broadband inductorless LNA design utilizing simultaneous noise and distortion cancellation is exploited by Chen *et al* [3]. The minimum internal gain of 14.5 dB and NF of 2.6 dB is achieved for 800 MHz to 2.1 GHz frequency and 1.5 V supply voltage by drawing 11.6 mA current.

Manstretta *et al* [4] extended a broadband single-ended input differential output LNA for canceling second order distortion. The second-order distortion products in the differential output are cancelled effectively by using a linear feedback from the common mode output to the single-ended input. The sensitivity to process, supply voltage, and temperature variations are reduced by replica bias. The NF of 2.25 dB in the Very High Frequency (VHF) band and 2 to 4 dB in the Ultra High Frequency (UHF) band are derived for 230 MHz to 470 MHz frequency with the power dissipation of 7.8 mW.

Ansari *et al* [5] performed a full on-chip CMOS LNA topology for cognitive radios with very low power consumption by exploiting the combination of CG stage for wideband input matching and CS stage for canceling the noise and distortion of CG stage. Both n-Channel Metal-Oxide Semiconductor (NMOS) and p-Channel Metal-Oxide Semiconductor (PMOS) transistors are used in CS stage for improving the Second Order Input Intercept Poin t(IIP2). The output impedance of 50 Ω is achieved by paralleling a resistor with the output node. The Noise Figure (NF) of 2.3 dB to 2.8 dB, Input Reflection Coefficient (S11) less than −10 dB, the power gain of 12 dB and IIP2 of 20 dBm are obtained for the range of 50 MHz to 10 GHz frequency and 1 V power supply with power consumption of 6 mW.

The comprehensive noise performance analysis of CMOS LNA including channel noise and induced gate noise in MOS devices was performed by Dong Feng *et al* [6]. A new analytical noise factor formula based on noisy two-port network theory is exhibited which shows that distributed gate resistance and other losses in series with the gate have both direct and indirect contributions to the noise factor. Design tradeoffs between power dissipation, overdrive voltage, and noise figure are balanced appropriately and high performance is achieved.

The design of CMOS CG LNAs using a design space exploration for all inversion regions, from weak to strong is investigated by Fiorelli *et al* [7]. The exploration is performed in terms of current consumption, gain and noise figure in the design space (*ID, gm/ID*) and the short channel effects are neglected, hence results measured are inaccurate. For smaller NF, transistor works in strong inversion and hence current consumption increases and for higher NF it is vice versa.

A 0.13 μm CMOS Balun-LNA for ultra-wideband applications is investigated by Reddy *et al* [8] using a common gate amplifier with source degenerated inductance for input matching. The balanced operation is maximized and noise of the CG stage is cancelled by emphasizing the combination of a CG stage and an admittance-scaled CS stage with replica biasing. The NF < 2.8 dB, S11 less than −10 dB and maximum gain of 17.8 dB is obtained for 2.1 GHz–9.5 GHz frequency and 1.2 V supply with a power consumption of 18.5 mW.

Tulunay *et al* [9] reported a stand-alone design automation tool tailored for RF CMOS LNA designs to obtain faster optimization. Design exploration is emphasized using circuit simulator which is time-consuming. NF less than 2.78dB is measured for 900 MHZ frequency and 2.5 V power supply. An automatic synthesis tool for Radio Frequency Integrated Circuits (RFIC) design is demonstrated by Tulunay *et al* [10]. The tool incorporated built-in numerical simulators for fast evaluation of the performance metrics. The duration of the overall optimization process is reduced which eliminates the need for circuit simulators. Nonlinearity is modelled using Volterra series method and additionally provides the on-chip inductors. NF of less than 0.75 dB is derived for 900 MHz frequency and 3.3 V power supply.

The rest of the paper is organized as follows. Section 2 describes the proposed design methodology. Section 3 discusses the simulation results that validate the proposed design methodology. Finally, section 4 provides the conclusions of the present work.

2. Proposed design methodology

The design of CMOS LNA circuits using small signal models has been widely used but has some limitations in its accuracy. For example, the small signal model approach used by Tuluna *et al* [10] with reverse isolation is not valid for all LNA designs. Another small signal model approach is used by the BSIM3v3 [11] model considers reverse isolation. However, the extraction of the values of the associated model parameters is not straightforward. These limitations can be overcome by the proposed design.

2.1 *Small signal parameters extraction*

In RF CMOS circuits, the transistors are normally designed with large widths. For the fixed length of the transistor, the small signal parameters are obtained for different bias voltages for a particular width. This procedure is repeated for various widths. In the present work, the small signal parameters are extracted using circuit simulators (HSPICE). The parasitic capacitors associated with all the terminals of the transistor are modeled as frequency dependent current sources as described in figure 1. The various current sources of figure 1 can be expressed as follows.

$$I_{ds} = g_m V_{gs} + g_{mbs} V_{bs} + g_{ds} V_{ds} \tag{1}$$

$$I_g(s) = s\left(C_{gg} V_g + C_{gs} V_s + C_{gb} V_b + C_{gd} V_d\right) \tag{2}$$

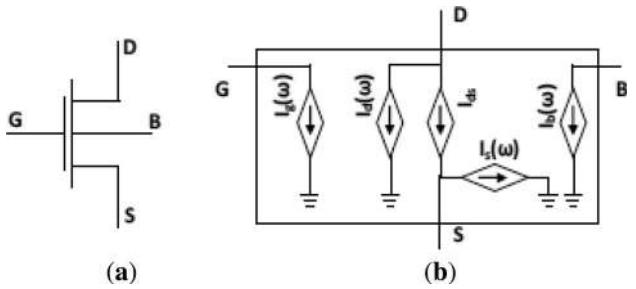

Figure 1. CMOS transistor **(a)** symbol, **(b)** proposed small signal model.

$$I_d(s) = s(C_{dg}V_g + C_{ds}V_s + C_{db}V_b + C_{dd}V_d + C_{jd}V_{db}) \quad (3)$$

$$I_s(s) = s\left(C_{sg}V_g + C_{ss}V_s + C_{sb}V_b + C_{sd}V_d + C_{js}V_{sb}\right) \quad (4)$$

$$I_b(s) = s\left(C_{bg}V_g + C_{bs}V_s + C_{bb}V_b + C_{bd}V_d\right) \quad (5)$$

In Eqs. (1)–(5), g_m, g_{mbs}, g_{ds} are the gate to source transconductance, bulk to source transconductance and drain to source transconductance, respectively. V_{gs}, V_{bs}, V_{ds}, V_{sb} represent gate to source voltage, bulk to source voltage, drain to source voltage and source to bulk voltage, respectively. Similarly, V_g, V_b, V_s, V_d are gate voltage, bulk voltage, source voltage and drain voltage with respect to ground, respectively. The symbol C_{xy}, (x,y = g,d,s,b) represents the capacitance relating the rate of change of charge in x terminal respect to change in voltage in y terminal.C_{jd}, C_{js} represent the junction capacitance at the drain and source terminals, respectively.

The transistor's small signal parameters depend directly on width, length and bias voltage at the source, drain, bulk and drain terminals. In this work, the transistors are designed at the fixed length, fixed source and bulk voltages and hence small signal parameters depend only on the width and varying gate and drain bias voltages. Thus the three parameters, namely width (W), the gate-source voltage (V_{gs}) and drain source voltage (V_{ds}) of the transistors constituting the design points in the circuit that forms the design space. A LUT is created over different bias voltages for different width with the fixed length of the transistor. The LUT contains the various device transconductances, parasitic capacitances and other DC quantities like drain source current. During the design exploration procedure, this LUT is used by the MATLAB.

2.2 *Steps to explore the design space*

For determining the performance analysis of the LNA circuits the appropriate analytical expressions are derived. The analytical expressions are then used in MATLAB along with the created LUT to explore the design space and to arrive at the feasible design point. The steps to explore the design space are as follows:

2.2a *Creation of LUT*: For the chosen fixed transistor length and particular width, LUT is created using the obtained DC and small signal parameters. This is carried out by performing DC simulation in HSPICE for various V_{gs} and V_{ds}.

2.2b *Defining the design space:* For the circuit topology, the design points are W, V_{gs}, and V_{ds} of all transistor. The size of the design space depends on the number of transistors used.

2.2c *Deriving the analytical expressions*: For the circuit under the considerations, the analytical expressions for determining the performance of LNA are derived using the proposed small signal model of the circuit. The analytical expressions derived include Input Reflection Coefficient (S11), Forward Gain (S21), and Noise Figure (NF).

2.2d *Exploring the design space*: The performances of the circuit are analyzed from the derived analytical expression in MATLAB by loading LUT. Save the design points that satisfy the performance requirement as feasible design points.

2.2e *Select the optimal design*: Sort the feasible design points obtained in Step 4 above with optional additional constraints on the performance and select the best possible design.

The above design space exploration is also depicted in the form of a flowchart in figure 2.

2.3 *Design of LNA circuits*

Two important specifications for an LNA are a power impedance match and low noise figure. The NF of an LNA using MOSFETs can be made low by increasing the transconductance (g_m) of the device and with proper layout. The source impedance that yields minimum NF is inductive in character and generally unrelated to the conditions that maximize power transfer [12, 13]. Furthermore, the gate (input impedance) of a MOSFET is predominantly capacitive by providing a good match to a 50 Ω source without degrading noise performance. Since presenting a known resistive impedance to the external world is an almost critical requirement of LNAs.

The circuit topologies that provide resistive impedance are

- Resistive termination
- Series-shunt feedback
- Common gate connection
- Inductor degeneration

2.3a *Common gate LNA design*: The proposed methodology is exhausted on commonly used inductor less CG LNA as in figure 3 and its small signal model is in figure 4. Small signal parameters and LUT has been created using 90 nm CMOS technology in HSPICE. Next the design points W,

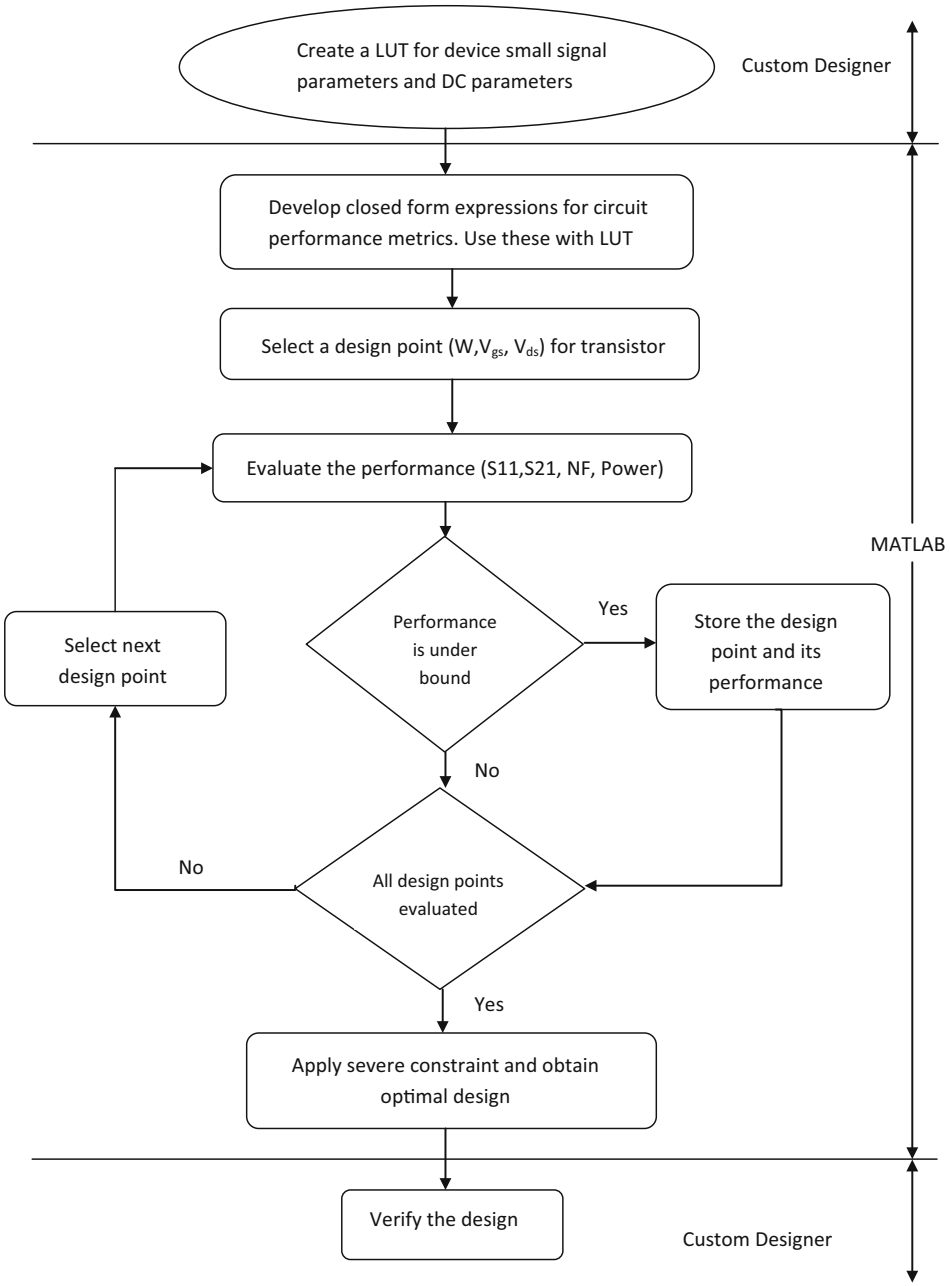

Figure 2. Flow Chart for Design Space Exploration of LNA circuits.

V_{gs}, and V_{ds} are defined for each transistor in the circuit. The dimension of the design space is three for CG.

The input is applied to source terminal MOS and the output is taken from the drain terminal. The drain terminal is connected to the power supply through the load resistor. By properly choosing W, V_{gs} and V_{ds} voltage and load resistor the input is amplified and is obtained at the output.

With reference to figure 4, the parasitic dependent Input Impedance of the CG LNA can be expressed as,

$$Z_{in}(s) = \frac{a_1 + sa_2}{b_1 + sb_2 + s^2 b_3} \tag{6}$$

where,

$$a_1 = 1 + g_{ds} * R_L$$

$$a_2 = C_D * R_L + C_{DB} * R_L$$

$$b_1 = g_m + g_{mbs} + g_{ds}$$

$$b_2 = G_m * C_{DB} * R_L + G_m * C_D * R_L + g_{ds} * C_{dg} * R_L - C_{DB} * C_{dg} * R_L - C_D * C_{dg} * R_L + C_{BB} a_1$$

$$b_3 = C_{dg} * R_L(C_{DB} + C_D) + C_{BB} * R_L(C_{DB} + C_D)$$

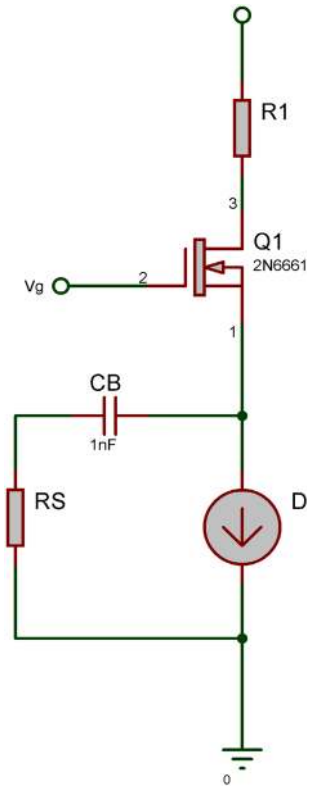

Figure 3. Common gate LNA.

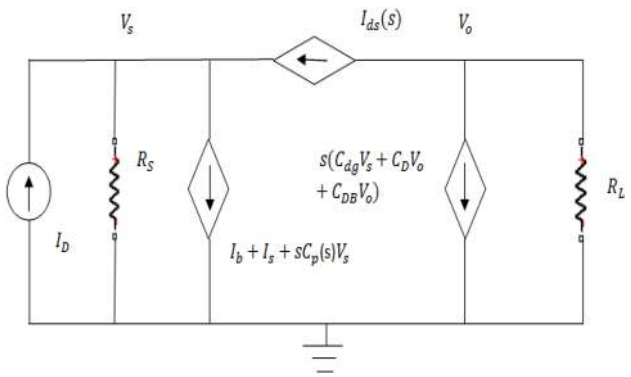

Figure 4. Small signal model of CG LNA.

$$G_m = g_m + g_{ds} + g_{mbs}$$

$$C_{DB} = C_{db} + C_{ds} - C_{jd}$$

$$C_{BB} = C_{ss} + C_{sb} + C_{bs}$$

$$C_D = C_{dd} + C_{jd}$$

Given $Z_{in}(s)$ as in (6), the Input Reflection Coefficient can be expressed as,

$$S_{11}(s) = \frac{Z_{in}(s) - R_s}{Z_{in}(s) + R_s} \tag{7}$$

In a similar manner, the Forward Gain can be expressed as,

$$S_{21}(s) = \frac{c_1 - sc_2}{d_1 + sd_2 + s^2d_3} \tag{8}$$

where,

$$c_1 = G_m$$

$$c_2 = C_{dg}$$

$$d_1 = g_{ds} + (1/R_L) - (G_m * (R_S/R_L))$$

$$d_2 = g_{ds} * R_L\left(-C_{dg} - C_{BB} + C_p\right) + C_{DB} + C_D - C_{BB} * (R_S/R_L) - G_m * C_{DB} * R_L - G_m * C_D * R_L - G_m * (R_S/R_L)$$

$$d_3 = C_{DB} * R_S\left(-C_{BB} + C_p\right) + C_p * C_D * R_S - C_{BB} * C_D$$

Noise Factor (F) is also defined as,

$$F = \frac{\text{total output noise power}}{\text{output noise due to input source}} \tag{9}$$

The NF is F expressed in decibels. With reference to figure 5, the F is given by,

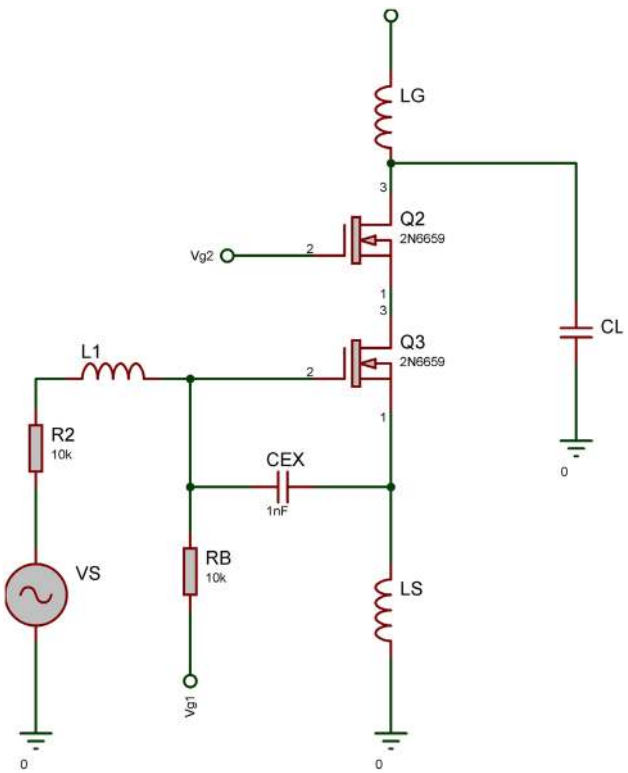

Figure 5. Inductively degenerated common source LNA.

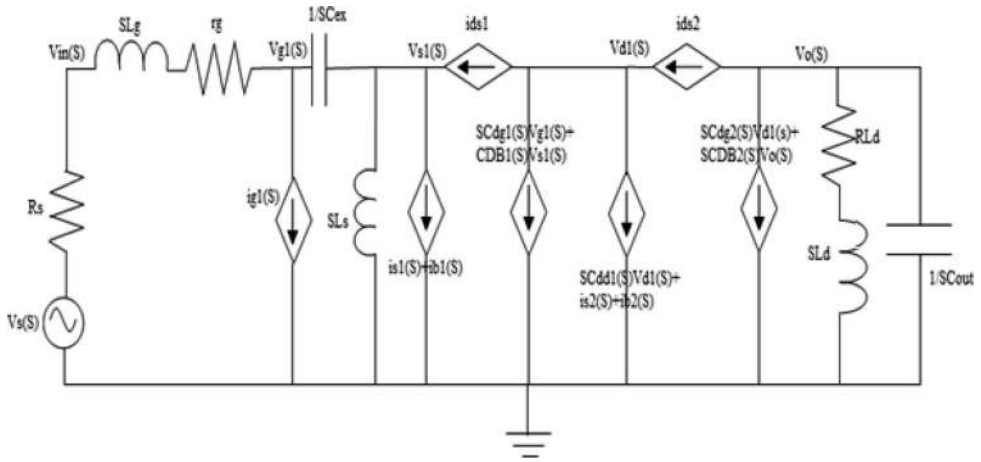

Figure 6. Small Signal Model of Inductively degenerated Common Source LNA.

$$F = 1 + \frac{((1/R_S) + s(C_{dg} + C_{BB} + C_p))^2 * \overline{i_d^2}}{(G_m - sC_{dg})^2 * \overline{i_S^2}} + \frac{((1/R_S) + G_m + s(C_{BB} + C_p))^2 * \overline{i_L^2}}{(G_m - sC_{dg})^2 * \overline{i_S^2}} \quad (10)$$

where,

$$\overline{i_d^2} = 4kT\left(\frac{2}{3}g_m\right)\Delta f$$

$$\overline{i_L^2} = 4kT\frac{1}{R_L}\Delta f$$

$$\overline{i_S^2} = 4kT\frac{1}{R_S}\Delta f$$

The NF of the circuit is given by,

$$NF = 10 * \log(F) \quad (11)$$

2.3b *Inductively degenerated common source LNA*: Inductively degenerated common source LNA is most commonly used in narrowband applications because it has resistorless input impedance for having low noise figure. To have proper impedance matching inductor is used in the source of the M1 transistor. Capacitor C_{ex} is used to adjust the Q-point of the transistor. The circuit for inductively degenerated common source LNA is shown in figure 5. The input is applied to source terminal M1 and the output is taken from the drain terminal of M2. The drain terminal of M2 is connected to the power supply through the load resistor. By properly choosing W1, W2, V_{gs1}, V_{ds1}, V_{g2}transistor the input is amplified and is obtained at the output.

Similar to CG LNA the analytical expressions for Input Impedance, Forward Gain and Noise Figure of Inductively Degenerated CS LNA are derived using the small signal model given in figure 6. The parasitic dependent Input Impedance of Inductively Degenerated CS LNA can be expressed as,

$$Zin(s) = Zin1(s) + rg + (s*L_g) \quad (12)$$

In a similar manner, the Forward Gain of Inductively Degenerated CS LNA can be expressed as,

$$S_{21}(s) = \left(\frac{1}{R}\right) * \left(\frac{nev}{dev}\right) \quad (13)$$

The F of Inductively Degenerated CS LNA is given by,

$$F = 1 + \frac{Vo2}{Vo1} + \frac{Vo3}{Vo1} + \frac{Vo4}{Vo1} \quad (14)$$

From these equations, the Input Reflection Coefficient, Forward Gain and Noise Figure of Inductively Degenerated CS LNA is calculated for all design points and its optimized results are in table 3.

The design points were identified with the sweep of design variables. For the Common Gate model, the widths of the transistors M range from 10 μm to 300 μm in a step of 50 μm. The drain to source voltages ranges from 0.2 V to 1.6 V and gate to source voltages ranges from 0.4 V to 1.7 V. These ranges chosen for the free parameters are considered large enough to cover all feasible design cases.

For the Inductively Degenerated Common Source LNA, the width of the transistor M1 ranges from 50 μm to 400 μm in a step of 50 μm. The drain to source voltages of transistor M1 ranges from 0.2 V to 1.6 V, the gate to source voltages of transistor M1 ranges from 0.4V to 1.7 V and the gate voltage of M2 transistor ranges from 0.5 V to 1.8 V. The design constraints are chosen for the CG LNA and Inductively Degenerated CS LNA are given in Table 1. Under these constraints, the feasible points were obtained using LUT in conjunction with analytical expressions in MATLAB by performing an exhaustive search among various design points.

Table 1. Design specifications.

Design specifications	Value
Supply voltage (V_{dd})	1.8 V
Input reflection (S_{11})	< -10 dB
Forward gain (S_{21})	> 10 dB
Noise figure (NF)	< 5 dB
Bias current (I_{ds})	< 25 mA
Resonant frequency	2 GHz/10 GHz
Source impedance	50 Ω
Load impedance	5 pF
CMOS technology	90 nm

3. Results and discussion

The RF CMOS CG LNA is designed using 90 nm CMOS technology in HSPICE and simulated using MATLAB. The number of design points in this space exploration process is defined by the number of free parameters, the step sizes of the free parameters and their respective minimum and maximum value. In this work W, V_{gs} and V_{ds} of the transistor were used as design points for the CG LNA design explorations and W1, W2, V_{gs1}, V_{ds1}, V_{g2} of the transistors were used as design points for inductively degenerated CS LNA. Each design point is validated in less than a millisecond using any circuit simulator. The time required to arrive at the feasible design points using a circuit simulator alone will be very high, and in addition, it would require intense manual effort.

The effective use of LUT obtained from HSPICE in conjunction with MATLAB completes the search and arrives at the feasible results of CG LNA and inductively degenerated CS LNA within a few seconds. The size of the search space increases as the number of design points increases which in turn increases as the number of transistors in the circuit increase, and this leads to an increase in the simulation.

The small signal parameters are obtained for various design points (W, V_{gs}, and V_{ds}). Look Up Table is formed for various design points using the obtained small signal parameters from the design as shown in figure 7. The highlighted values in figure 7 are considered for the design.

The small signal parameters are obtained for various design points (W1, W2, V_{gs1}, V_{ds1}, V_{g2}). Look up table is formed for various design points using the obtained small signal parameters as shown in figure 8. Tables 2 and 3 contain the feasible design points of CG LNA and Inductively Degenerated CS LNA, respectively obtained by MATLAB for operating frequency of 2GHz. Each row in tables 2 and 3 corresponds to the feasible design points optimized in any single objective. The highlighted values in figure 8 are considered for the design. The design parameters are global since the operating frequency and supply voltage is common to the entire circuit. The Gate source voltage and drain source voltage is maintained globally.

3.1 *Parasitic effects*

Inductive degeneration is popular because of package parasitics. The parasitics in LNA design can be reduced during package. This requires good model pf package and bond wires. The inductance of the input loop depends on the arrangement of bond wires, die size and pad locations. The

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q
2																	
3	W	Vgs	Vds	R1	Id	Ibs	Ibd	Vbs	gm	gds	gmb	Power	Cgs	Cgb	Cgd	Cgg	Cdb
4	50u	400m	200m	102000m	1.8255m	748.775f	-79.3590f	129.985m	25.586m	2.0167m	5.1279m	904.6734u	47.6188f	77.4965f	26.0545f	77.4965f	50.3211f
5	50u	400m	600m	102000m	2.9504m	4.7137p	-428.9954f	-428.9954f	35.4886m	2.2592m	6.7326m	2.3098m	54.4448f	76.0717f	19.0450f	76.0717f	41.9110f
6	50u	400m	800m	356000m	3.5141m	7.6475p	-616.2248f	193.7752m	39.3706m	2.4775m	7.3707m	4.6946m	56.6731f	75.9534f	17.0489f	75.9534f	39.0847f
7	50u	400m	1200m	257000m	6.1551m	12.0875n	-826.3454f	383.6546m	51.6310m	3.2677m	8.0356m	8.7456m	62.8546f	79.3940f	15.5876f	79.3940f	36.9019f
8	50u	400m	1600m	257000m	9.1902m	9.1902m	-1.0249p	585.0689m	59.4964m	3.8976m	7.7513m	16.1127m	65.7148f	81.2343f	15.0909f	81.2343f	35.7573f
9	50u	400m	1800m	303000m	10.5447m	417.9273u	-1.1547p	654.9006m	61.9365m	4.2200m	7.6149m	21.3361m	66.4616f	81.7422f	14.9540f	81.7422f	35.2247f
10	50u	600m	200m	102000m	10.4659m	1.8579p	-52.3273f	155.8774m	48.5673m	13.3153m	9.9954m	2.6328m	66.4514f	93.6439f	26.5457f	93.6439f	52.4544f
11	50u	600m	600m	298000m	12.9606m	12.4905p	-303.3952f	206.6047m	57.8453m	4.7482m	11.2059m	8.0567m	67.2278f	91.7392f	24.0303f	91.7392f	47.9708f
12	50u	600m	800m	420000m	14.5428m	26.1581p	-584.2027f	225.7973m	60.0054m	4.4531m	4.4531m	13.8560m	67.6449f	86.5359f	18.4692f	86.5359f	40.9698f
13	50u	600m	1200m	367000m	17.7123m	3.4269n	-858.7321f	351.2679m	62.3284m	4.5160m	10.5487m	23.1962m	68.6425f	84.5004f	15.7277f	84.5004f	37.1187f
14	50u	600m	1600m	347000m	21.7360m	20.4453u	-1.0352p	574.7657m	64.0872m	4.7976m	8.9240m	36.6459m	69.6659f	84.5967f	15.0581f	84.5967f	35.8304f
15	50u	600m	1800m	345000m	23.3811m	348.5701u	-1.1599p	649.7832m	64.7396m	5.0995m	8.4747m	44.5386m	69.9570f	84.6873f	14.8940f	84.6873f	35.2744f
16	50u	800m	200m	233000m	18.8970m	1.4415p	-59.8076f	148.8279m	34.6996m	49.0212m	8.1265m	5.0120m	68.8248f	96.5756f	27.7569f	96.5756f	54.9016f
17	50u	800m	600m	273000m	25.4907m	25.6127p	-384.7482f	225.2518m	58.9974m	6.0184m	11.7294m	16.7386m	69.9545f	94.9481f	25.0839f	94.9481f	48.6770f
18	50u	800m	800m	392000m	26.7697m	41.6392p	-572.1849f	237.8151m	60.2024m	5.4110m	11.8043m	23.4894m	70.0888f	92.0797f	22.0921f	92.0797f	44.7424f
19	50u	800m	1200m	296000m	29.5748m	457.3467p	-910.4888f	299.5112m	61.6961m	5.1151m	11.3788m	37.0556m	70.4602f	86.7115f	16.4387f	86.7115f	37.7316f
20	50u	800m	1600m	340000m	34.2269m	8.5425u	-1.0577p	552.2663m	62.7799m	5.2729m	9.2096m	56.5754m	71.1795f	85.9768f	15.2117f	85.9768f	35.9827f
21	50u	800m	1800m	335000m	36.0386m	193.9090u	-1.1761p	633.7013m	63.2081m	5.5798m	8.6537m	66.9907m	71.3544f	85.8927f	14.9686f	85.8927f	35.3671f
22	50u	1200m	200m	335000m	28.6024m	86.4888p	137.4173f	256.6647m	14.4079m	109.8956m	4.2420m	7.4932m	66.0343f	100.4035f	35.5408f	100.4035f	72.0285f
23	50u	1200m	600m	263000m	48.7576m	138.2302p	-341.2623f	268.7377m	54.1767m	11.8531m	10.9788m	30.6462m	71.7826f	97.5595f	26.4748f	97.5595f	50.5014f
24	50u	1200m	800m	172000m	50.6903m	179.9533p	-534.4750f	275.5250m	56.9728m	7.7962m	11.3331m	41.4625m	71.8475f	97.2058f	26.0341f	97.2058f	48.9716f
25	50u	1200m	1200m	422000m	53.5557m	274.4366p	-923.6201f	286.3799m	58.8771m	6.3224m	11.5089m	66.4996m	71.9074f	93.2429f	21.9710f	93.2429f	43.3081f
26	50u	1200m	1600m	273000m	58.1402m	686.7705n	-1.1225p	487.4505m	59.8595m	6.1014m	9.6486m	94.4698m	72.2234f	87.8251f	16.3489f	87.8251f	37.0031f

Figure 7. Look up table using small signal parameters of CG LNA.

Variable Editor - textdata

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
1	W1	W2	Vgs1	Vds1	Vgs2	Ls	Cex	Lg	Rld	gm1	gds1	gmb1	gm2	gds2	gmbs2	Cdd1	Cgs1	Cgd1
2	50u	50u	400m	200m	500m	0.1n	10f	5.5n	600m	9.045m	82.9367m	3.4366m	8.2089m	80.4103u	1.1457m	123.8961f	112.7128f	72.909f
3	50u	50u	600m	200m	500m	0.2n	20f	6n	100m	8.9004m	83.5201m	3.4087m	8.2106m	80.4288u	1.1459m	124.4484f	112.4719f	73.2721f
4	50u	50u	800m	200m	500m	0.4n	50f	6.5n	700m	8.7585m	84.0984m	3.3812m	8.2085m	80.4066u	1.1457m	124.9868f	112.235f	73.6261f
5	50u	50u	1000m	200m	500m	0.3n	100f	50n	800m	8.6192m	84.6608m	3.3543m	8.2082m	80.4029u	1.1457m	125.5117f	112.0021f	73.9714f
6	50u	50u	1200m	200m	500m	0.5n	150f	55n	900m	8.4825m	85.2183m	3.3278m	8.2079m	80.3992u	1.1456m	126.0235f	111.7729f	74.3081f
7	50u	50u	1400m	200m	500m	0.6n	75f	10n	1000m	8.3483m	85.7675m	3.3018m	8.2075m	80.3955u	1.1456m	126.5228f	111.5474f	74.6367f
8	50u	50u	1600m	200m	500m	0.7n	64f	15n	500m	8.2165m	86.3085m	3.2763m	8.2092m	80.4141u	1.1457m	127.0099f	111.3254f	74.9573f
9	50u	50u	400m	400m	700m	0.7n	202f	20n	600m	21.8361m	49.411m	6.4562m	6.6484m	64.4609u	1.004m	72.5473f	133.8087f	39.8728f
10	50u	50u	600m	400m	700m	0.5n	300f	25n	300m	21.5147m	6.404m	73.3842m	6.6494m	64.47u	1.0041m	73.3842f	133.5573f	40.3754f
11	50u	50u	800m	400m	700m	0.8n	15f	32n	350m	21.1991m	50.9347m	6.3544m	6.6492m	64.4685u	1.004m	74.2325f	133.2977f	40.8859f
12	50u	50u	1000m	400m	700m	0.1n	25f	40n	450m	20.8891m	51.6801m	6.3048m	6.6489m	64.4654u	1.004m	75.0913f	133.0305f	41.4057f
13	50u	50u	1200m	400m	700m	0.3n	28f	43n	560m	20.5845m	52.4148m	6.2562m	6.6486m	64.4621u	1.004m	75.9593f	132.756f	41.9281f
14	50u	50u	1400m	400m	700m	0.4n	32f	10n	670m	20.2854m	53.1391m	6.2084m	6.6482m	64.4588u	1.004m	76.8354f	132.4747f	42.4583f
15	50u	50u	1600m	400m	700m	0.6n	85f	11n	780m	19.9914m	53.8531m	6.1614m	6.6479m	64.4554u	1.0039m	77.7183f	132.1871f	42.9936f
16	50u	50u	400m	600m	900m	0.12n	100f	10.7n	100m	37.9828m	15.8126m	8.8846m	9.6745m	94.0314u	1.6299m	53.6179f	139.445f	29.1616f
17	50u	50u	600m	600m	1100m	0.23n	202f	17.2n	300m	37.6173m	16.4939m	8.8326m	65.4642m	780.4947u	11.2273m	53.7532f	139.4557f	29.2323f
18	50u	50u	900m	600m	1400m	0.31n	302f	19n	720m	37.0547m	17.5488m	8.7539m	91.5681m	1.8967u	1.8967m	53.9652f	139.4653f	29.3437f
19	50u	50u	1200m	600m	1500m	0.42n	152f	23n	500m	36.4768m	18.64m	8.6745m	93.7437m	2.3091u	20.4078m	54.1884f	139.467f	29.4617f
20	50u	50u	1400m	600m	1700m	0.53n	215f	53n	700m	36.084m	19.3859m	8.6214m	94.7079m	3.2577u	21.0169m	54.344f	139.4638f	29.5444f
21	50u	50u	1600m	600m	900m	0.67n	112f	57.7n	320m	35.6859m	20.1449m	8.568m	9.6723m	94.0107u	1.6297m	54.5051f	139.4569f	29.6305f
22	50u	50u	1800m	600m	900m	0.79n	179f	33.7n	450m	35.2834m	20.9158m	8.5146m	9.671m	93.9984u	1.6295m	54.6722f	139.4464f	29.7201f
23	50u	50u	400m	800m	1100m	0.13n	297f	37n	430m	44.3927m	4.6172m	9.7046m	5.7385m	56.3812u	1.132m	50.4687f	139.9293f	27.875f
24	50u	50u	600m	800m	1100m	0.45n	173f	23.5n	370m	44.2837m	4.7472m	9.678m	5.7388m	56.3839u	1.132m	50.5155f	139.9678f	27.8985f
25	50u	100u	900m	800m	1200m	0.76n	159f	54.3n	130m	44.1139m	4.951m	9.6378m	27.2621m	278.1674u	5.2572m	50.5856f	140.0217f	27.9335f
26	50u	150u	1200m	800m	1200m	0.34n	300f	63n	630m	43.9365m	5.1663m	9.5974m	40.6919m	415.1232u	7.8651m	50.6558f	140.0713f	27.9683f

Figure 8. Look UP Table using small signal parameters of inductively degenerated CS LNA.

Table 2. Design result of CG LNA at F = 2 GHz.

Sl.No	W (μm)	V_{gs} (mV)	V_{ds} (mV)	R_L (Ω)	Optimized parameters and its value
1.	50	400	200	102	Minimum Power – 904.6734 μW
2.	50	600	800	420	Maximum S21 – 13.6333 dB
3.	300	1600	1800	397	Minimum NF – 0.7798 dB
4.	50	400	200	102	Minimum S11 – 17.5212 dB

Table 3. Design result of inductively degenerated CS LNA at F = 2 GHz.

Sl.No	W1 (μm)	W2 (μm)	V_{gs1} (mV)	V_{ds1} (mV)	V_{ds2} (mV)	L_s (nH)	Cex (pF)	L_g (nH)	Rld (Ω)	Ld (nH)	Rg (Ω)	Optimized parameters and its value
1.	300	30	700	400	700	0.54	101.5	63.1	0.64	0.01259	0.2782	Minimum Power – 1.0353 mW
2.	250	150	900	1200	1500	0.13	89	32.7	0.51	0.01223	0.3328	Maximum S21 – 31.9719
3.	100	150	1200	700	1200	0.24	202.5	60.2	0.37	0.01206	0.8285	Minimum NF – 0.0630 dB
4.	50	50	1000	400	700	0.1	25	40	0.45	0.01253	1.6645	Minimum S11 – 24.3172 dB

changing flux generates an EMF around the circuit loop and it causes undesired mutual inductance to other parts of the circuit. Many designs also require ESD protection which manifests as increased capacitance on the pads.

Figure 9 shows the comparison of CG LNA and Inductively Degenerated CS LNA at F = 2 GHz. The performance of Inductively Degenerated CS LNA is high compared to CG LNA.

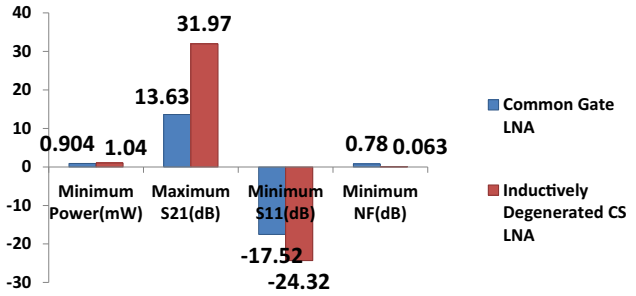

Figure 9. Comparison of CG LNA and Inductively Degenerated CS LNA at F = 2 GHz.

4. Conclusion

The RF CMOS CG LNA and Inductively Degenerated CS LNA is designed for space exploration and the synthesis is carried out by an exhaustive search to obtain the feasible design points which provide minimum power, maximum gain, minimum noise figure, and minimum input reflection coefficient at a 2 GHz frequency. In this, CS Inductively Degenerated LNA is high in performance compared to CG LNA with 57.35% of the increase in gain and 91% of reduced noise figure.

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