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Design of Linear CMOS Transconductance Elements for Alpha-Power Law Based Mosfets and an Automatic Compensation Technique for Temperature

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Abstract A model on alpha-power law MOSFETs based source-coupled differential pair (SCDP) is discussed and a simple design procedure for realizing a linear CMOS SCDP transconductance element is proposed. The proposed or modified SCDP circuit using this procedure is an alternative to that of conventional SCDP and the circuit discussed has superior linearity for a wide range ±(0-300mv) of input differential voltage at a supply voltage of 1.2v. The modified SCDP also includes the circuitry needed to suppress the variation in the quiescent current with respect to input common-mode voltage noise. The SPICE results are used to verify theoretical predictions. The results show close agreement between the predicted model behavior and the simulated performance. The simulated result on Total Harmonic Distortion (THD) shows that the modified SCDP circuit is better than the conventional SCDP by about four times at input differential voltage amplitude of ±100mv. An example circuit, a second order continuous time gm-C band-pass filter is constructed using the fully differential modified SCDP and the fully differential conventional SCDP circuit and the result shows that the modified transconductor circuit is better in linearity (THD) than the conventional SCDP by about two times at the input differential voltage amplitude of ±100mv. An automatic digital compensation scheme for temperature is also presented and the temperature coefficient of output current is reduced by about eight times to 250ppm/deg.C after compensation for the maximum change in temperature of 150deg.C and at the input differential voltage of 100mv.

Keywords CMOS Transconductor, SCDP Circuit, Linearity, Total Harmonic Distortion (THD), Gm-C Filter, SPICE Models, Temperature Compensation, Flash ADC

1. Introduction

Linear transconductance elements [1]-[14] are useful in building blocks in analog signal-processing systems and the literature on this topic is rich indeed. A cross-coupled quad cell is proposed by [1]. An inverter-based transconductor is discussed in [10] and [13]. In [9], a bias-offset cross-coupled transconductor is realized. In [1] and [8], the linearity with input differential voltage is achieved by CMOS pairs and floating voltage sources. In [6], the linearity is achieved with two additional PMOS SCDP pairs. The source degeneration linearization is used in [11]. A four MOS transistor cell to obtain a linear transconductor is realized in [12]. In [14], the linearity is obtained with a quadritail cell. In all of these transconductors discussed, only the square law devices are considered but in the present paper, a model for SCDP based on the alpha-power law devices is proposed.

The objective of this paper is to present a model for the alpha-power law based CMOS SCDP transconductors and a simple design procedure for the realization of linear CMOS modified SCDP transconductance block for both single-ended and fully differential outputs. The modified SCDP doesn't require any special cell and includes the same circuit as required in a conventional SCDP as the base circuitry. Also the linearity and the input voltage range of the proposed design are superior to that of the conventional source-coupled differential pair. The computer simulation results are presented.

All MOSFET's are assumed to be enhancement-mode types biased in saturation and the transistor behavior is approximated by the relation,

$$I=\frac{kp}{2}\left(V_{gs}\text{-}vth\right)^{\alpha}\left(1+\lambda V_{ds}\right) \qquad (1)$$

where vth is the total threshold voltage inclusive of body-effect. $kp=KP\left(W/L\right)$ is the transconductance parameter, W and L are the width and length of the channel, λ is due to the effect of channel length modulation and α is the alpha-power law value.

A theory on modeling a transconductance parameter for a SCDP transconductor based on alpha-power law MOSFETs is described in section-2. A condition to achieve the linearity

in the transconductance parameter is discussed in section-3. Section-4 proposes a simple design procedure used to cancel out the third degree term in the transconductance and to make a perfect linear transconductor. The section-4 also includes the circuitry that is needed to minimize the variation of quiescent current with respect to input common-mode voltage. The section-5 presents the results, one with alpha-power law devices and the other with square law devices for both SCDP and the modified SCDP. The section-6 describes on how the various output conductances (channel length modulation) are included in the present model for the fully differential modified transconductor. A gm-C band-pass filter based out of the conventional SCDP and the modified SCDP is described in section-7. Using this filter, a comparison between the conventional SCDP and the modified SCDP in terms of %THD is made in section-7. An automatic temperature compensation scheme for the discussed modified transconductor is also presented in section-8. Section-9 concludes about the modified SCDP circuitry based on alpha-power law MOSFETs.

2. Theory on Basic Cmos Scdp Transconductor Based on Alpha-Power Law Mosfets

Let I_1 and I_2 be the drain currents in the two branches of the SCDP circuit (Fig.1) and V_{gs1} and V_{gs2} be the gate-source voltages of the respective NMOS MOSFETs in the SCDP. vth is the total effective threshold voltage of NMOS MOSFETs including body-effect. The body-effect's dependence on input differential voltage is considered in section-3. Neglecting channel length modulation for time being (it is accounted later in the section-6), we have from (1) as,

$$V_{gs1}=\left(\frac{2I_1}{kp}\right)^{1/\alpha}+vth \quad ; V_{gs2}=\left(\frac{2I_2}{kp}\right)^{1/\alpha}+vth \tag{2}$$

$$V_{in}=V_{gs1}-V_{gs2} \ ; \tag{3}$$

Using (2) and (3), we obtain,

$$V_{in}^2=\left(\frac{2}{kp}\right)^{2/\alpha}\left[I_1^{2/\alpha}+I_2^{2/\alpha}-2\left(I_1I_2\right)^{1/\alpha}\right] \tag{4}$$

Noting that

$$\left(I_1-I_2\right)^2=\left(I_1+I_2\right)^2-4I_1I_2=Iss^2-4I_1I_2, \tag{5}$$

where Iss is the quiescent current for SCDP.
From (4) and (5), we have,

$$V_{in}^2=\left(\frac{2}{kp}\right)^{2/\alpha}\left\{I_1^{2/\alpha}+I_2^{2/\alpha}-\frac{2}{4^{1/\alpha}}\left[Iss^2-\left(I_1-I_2\right)^2\right]^{1/\alpha}\right\} \tag{6}$$

and this could be written using (2) as,

$$\left(V_{gs1}-vth\right)^2+\left(V_{gs2}-vth\right)^2-V_{in}^2=\left(\frac{2}{kp^{2/\alpha}}\right)\left[Iss^2-\left(I_1-I_2\right)^2\right]^{1/\alpha} \tag{7}$$

Expanding (7) we arrive at,

$$I_D=I_1-I_2=\sqrt{Iss^2-\left(\frac{kp^2}{2^\alpha}\right)VX} \tag{8}$$

where VX is given by

$$VX=\left[V_{gs1}^2+V_{gs2}^2-2vth\left(V_{gs1}+V_{gs2}\right)+2vth^2-V_{in}^2\right]^\alpha \tag{9}$$

Let V_{cm} be the input common-mode voltage. V_P is the node voltage at the point P in Fig.1. Let V_{gs1} and V_{gs2} be written as,

$$\begin{aligned} V_{gs1}&=V_{cm}+\frac{V_{in}}{2}-V_P \ ; \\ V_{gs2}&=V_{cm}-\frac{V_{in}}{2}-V_P \end{aligned} \tag{10}$$

$$\left(V_{gs1}+V_{gs2}\right)=2\left(V_{cm}-V_P\right) \tag{11}$$

From equations (9), (10) and (11), VX can be written as,

$$VX=\left(2K\right)^\alpha\left(1-\frac{V_{in}^2}{2K}\right)^\alpha \tag{12}$$

where K is given by

$$K=\left(V_{cm}-V_P-vth\right)^2+\frac{V_{in}^2}{4} \tag{13}$$

The differential current I_D for a source-coupled pair can be written as,

$$I_D=a_0V_{in}+a_1V_{in}^3+(\text{higher order terms}) \tag{14}$$

and let biasing current Iss be written as,

$$Iss=I_0+m_qV_{in}^2+(\text{higher order terms}) \tag{15}$$

Now consider in equations (8), (12) and (13), we have,

$$\frac{kp^2\left(2K\right)^\alpha}{2^\alpha}=kp^2\left(V_{cm}-V_P-vth\right)^{2\alpha}\left\{1+\frac{\left(V_{in}^2/4\right)}{2\left(V_{cm}-V_P-vth\right)^2}\right\}^\alpha \tag{16}$$

Expanding the curly bracket term by binomial series and neglecting higher order terms and noting that the above equation should be equal to Iss^2 since the dc term of equation (14) is zero, we have equation (16) that could be written from equations (8), (12), (13) and (15) as,

$$Iss^2\approx I_0^2+2m_qI_0V_{in}^2\approx kp^2K^\alpha\approx I_0^2\left\{1+\frac{\left(\alpha V_{in}^2/8\right)}{\left(V_{cm}-V_P-vth\right)^2}\right\} \tag{17}$$

From which we obtain,

$$m_q=\frac{(\alpha I_0/16)}{(I_0/kp)^{2/\alpha}} \quad (18)$$

where

$$I_0=kp(V_{cm}-V_P-vth)^{\alpha}. \quad (19)$$

Now writing equation (12) by binomial series, we obtain,

$$VX=(2K)^{\alpha}\left[1-\frac{\alpha V_{in}^2}{2K}+\frac{\alpha(\alpha-1)V_{in}^4}{8K^2}-\left(\frac{\text{higher order}}{\text{terms}}\right)\right] \quad (20)$$

provided

$$|V_{in}|\le\sqrt{2K} \quad (21)$$

where

$$K^{\alpha}=(Iss/kp)^2 \quad (22)$$

Substituting equations (20) and (22) in equation (8) we arrive I_D after neglecting higher order terms as,

$$I_D=G_m V_{in}\sqrt{1-\frac{(\alpha-1)}{4K}V_{in}^2} \quad (23)$$

where

$$G_m=\sqrt{\frac{\alpha}{2K}}Iss \quad (24)$$

Equations (23) and (24) constitute the required equations for the output differential current which are similar to the one in square law based SCDP circuit.

3. Condition for the Compensated SCDP

Let Iss be written as,

$$Iss=I_0+mV_{in}^2+(\text{higher order terms}) \quad (25)$$

with new ' m ' in equation (15) required to cancel out the cubic degree dependency of I_D on V_{in}.

Considering only the second degree dependency on V_{in}, we have Iss can be written as ,

$$Iss=I_0+mV_{in}^2 \quad (26)$$

Equation (26) accounts for all second degree input differential voltage effects including the V_P and vth dependence on V_{in}^2.

Substituting (25) in (23), we get

$$I_D=\sqrt{\frac{\alpha}{2}}kp^{1/\alpha}V_{in}\left\{(I_0+mV_{in}^2)^{2-2/\alpha}-\frac{(\alpha-1)kp^{2/\alpha}V_{in}^2}{4}(I_0+mV_{in}^2)^{2-4/\alpha}\right\}^{1/2} \quad (27)$$

Which upon expanding by binomial series and grouping like terms can be written as (also by neglecting higher order terms),

$$I_D\approx\sqrt{\frac{\alpha}{2}}kp^{1/\alpha}V_{in}\left\{I_0^{2-2/\alpha}+V_{in}^2\left[I_0^{2-2/\alpha}\frac{m(2-2/\alpha)}{I_0}-I_0^{2-4/\alpha}\frac{(\alpha-1)kp^{2/\alpha}}{4}\right]\right\}^{1/2} \quad (28)$$

provided

$$|V_{in}|\le\sqrt{\frac{I_0}{m}} \quad (29)$$

The equation (28) shows that the term in the square bracket should be zero to achieve a linear transconductance. This result can be stated as,

$$m=\frac{(\alpha I_0/8)}{(I_0/kp)^{2/\alpha}} \quad (30)$$

For square law based SCDP circuit,

$$m=kp/4 \quad (31)$$

Equation (31) is the result obtained by [1] for a square law based SCDP circuit. Equation (30) is the required condition to eliminate third degree term in the transconductance value in equation (23). Also to be noted is the following relation between the condition 'm' required to cancel out the cubic degree dependency of I_D on V_{in} and the coefficient ' m_q ' in Iss for a basic SCDP.

$$m=2m_q \quad (32)$$

Equation (32) implies that twice the variation of Iss with respect to V_{in}^2 than conventional SCDP is required for I_D to cancel out the cubic degree dependency.

Consider in Fig.1, V_P can be written as,

$$V_P=V_{P0}+\delta V_{in}^2 \quad (33)$$

The threshold voltage vth is given approximately by,

$$vth=vth0+K_1\left(\sqrt{\Phi_s+V_P}-\sqrt{\Phi_s}\right)+K_2V_P \quad (34)$$

where K_1 and K_2 are due to non-uniform substrate doping and Φ_s is the surface potential.

Using equation (33), vth can be written as,

$$vth=vth0+K_1\sqrt{\Phi_s S}\left(\sqrt{1+\frac{\delta V_{in}^2}{\Phi_s S}}-\frac{1}{\sqrt{S}}\right)+K_2V_{P0}+K_2\delta V_{in}^2 \quad (35)$$

where S is given by,

$$S=1+\frac{V_{P0}}{\Phi_s} \quad (36)$$

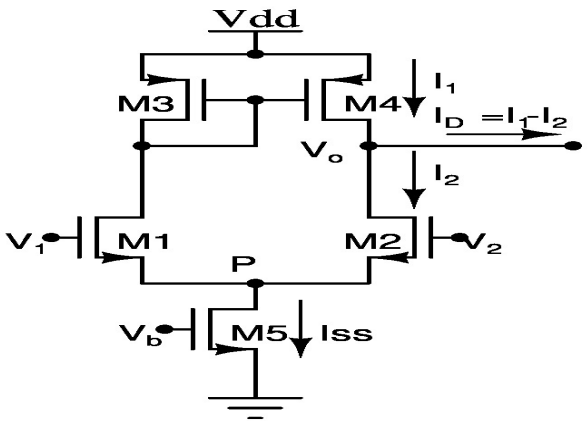

Figure 1. The Conventional Source-coupled pair – (Single ended output). $V_1=V_{cm}+V_{in}/2$ and $V_2=V_{cm}-V_{in}/2$; $V_{in}=V_1-V_2$.

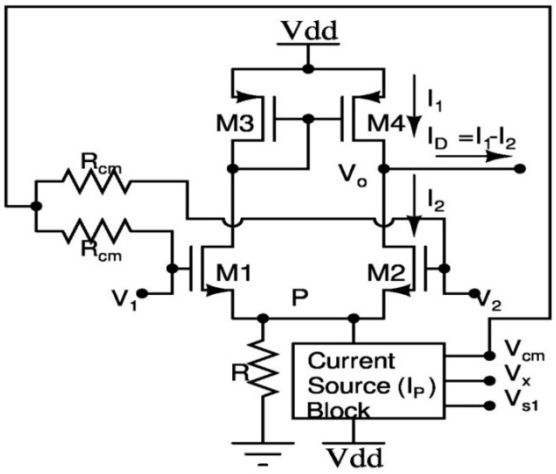

Figure 2. The Modified Source-coupled pair – (Single ended output). $V_1=V_{cm}+V_{in}/2$ and $V_2=V_{cm}-V_{in}/2$; $V_{in}=V_1-V_2$.

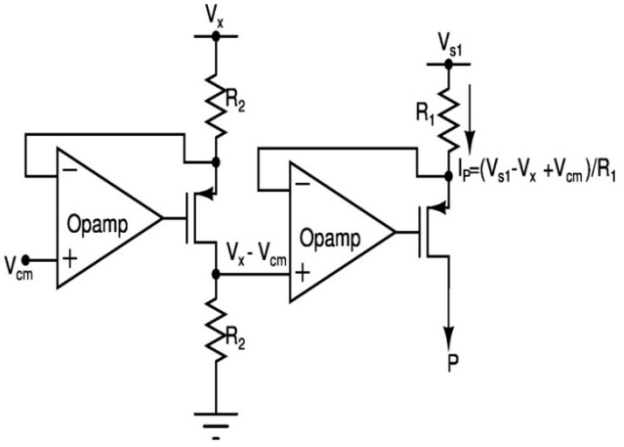

Figure 3. The current source block as in Fig.2.

Expanding the bracket term in the above equation (35) by binomial series, we obtain after neglecting higher order terms as,

$$vth \approx vth0+K_1\sqrt{\Phi_s}\left(\sqrt{S}-1\right)+K_2V_{P0}+\delta K_P V_{in}^2 \quad (37)$$

provided

$$|V_{in}| \le \sqrt{\frac{\Phi_s S}{\delta}} \quad (38)$$

where K_P is given by,

$$K_P=K_2+\frac{K_1}{2\sqrt{\Phi_s S}} \quad (39)$$

From equations (19), (33) and (37), we have the modified I_0 as,

$$I_0^{'}=kp\left(V_{cm}-vth-V_{P0}-\delta V_{in}^2\right)^{\alpha}=kpV_{PM}^{\alpha}\left(1-\frac{\delta(1+K_P)V_{in}^2}{V_{PM}}\right)^{\alpha} \quad (40)$$

where

$$V_{PM}=\left[V_{cm}-vth0-K_1\left(\sqrt{S}-1\right)\sqrt{\Phi_s}-V_{P0}(1+K_2)\right] \quad (41)$$

Writing the equation (40) by binomial series, we obtain (after neglecting higher order terms and keeping only the V_{in}^2 term) as,

$$I_0^{'} \approx kpV_{PM}^{\alpha}\left[1-\frac{\alpha\delta(1+K_P)V_{in}^2}{V_{PM}}\right]=I_{0M}-m_{qm}V_{in}^2 \quad (42)$$

provided

$$|V_{in}| \le \sqrt{\frac{V_{PM}}{\delta(1+K_P)}} \quad (43)$$

where

$$I_{0M}=kpV_{PM}^{\alpha} \quad (44)$$

and

$$m_{qm}=\frac{\alpha\delta(1+K_P)I_{0M}}{V_{PM}} \quad (45)$$

Now the biasing current from equation (26) can be rewritten as,

$$Iss=I_{0M}+m(new)V_{in}^2 \quad (46)$$

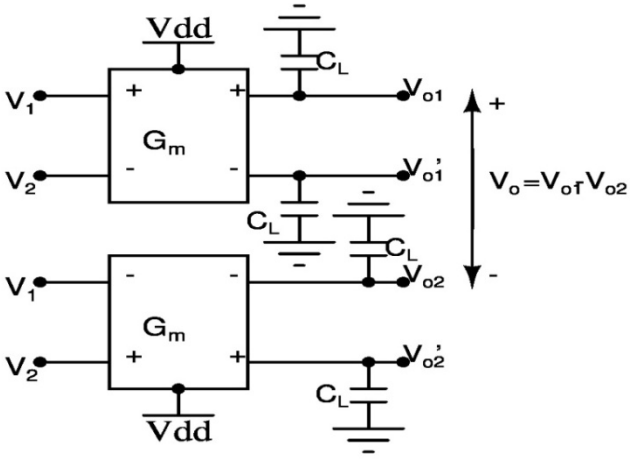

Figure 4. A Fully differential Transconductor using two single ended output cells. $V_{in}=V_1-V_2$.

Equation (26) includes all the effects varying with second degree input differential voltage (including the effects of V_P and vth varying with V_{in}^2) and the equation (46) is rewritten from (26) only to include higher order terms other than V_{in}^2 term. The $m(new)$ value accounts for these higher order terms in addition. The zero differential voltage based current I_{0M} is the same as I_0. Now the modified ' m ' can be rewritten from equation (30) using equation (42) as,

$$m(new)=\frac{\alpha}{8}kp^{2/\alpha}\left(I_0'\right)^{1-2/\alpha}=\frac{\alpha}{8}kp^{2/\alpha}\left[I_{0M}-m_{qm}V_{in}^2\right]^{1-2/\alpha} \quad (47)$$

Upon expansion of $m(new)$ value by binomial series and neglecting higher order terms, we get the following equation.

$$m(new)\approx\frac{\alpha I_{0M}}{8}\left(\frac{kp}{I_{0M}}\right)^{2/\alpha}\left\{1-\frac{(1-2/\alpha)m_{qm}}{I_{0M}}V_{in}^2\right\} \quad (48)$$

Now Iss can be written from using equations (46) and (48) as,

$$Iss=I_{0M}+\frac{\alpha I_{0M}V_{in}^2}{8(I_{0M}/kp)^{2/\alpha}}-\frac{\alpha(1-2/\alpha)m_{qm}V_{in}^4}{8(I_{0M}/kp)^{2/\alpha}} \quad (49)$$

The inclusion of V_P and vth varying with V_{in}^2 has already been accounted in the second term of above equation (49) and its effect makes explicit presence in the third term of equation (49). The modified ' m ' after neglecting higher order terms can be written as,

$$m(new)=\frac{\alpha I_{0M}}{8}\left(\frac{kp}{I_{0M}}\right)^{2/\alpha} \quad (50)$$

which is same as the equation (30).
The next section discusses on how to achieve the condition (50) to make a perfect linear transconductor.

4. Design of Modified SCDP with Compensation for Linearity

The modified SCDP circuit with compensation for linearity is shown in Fig.2 and Fig.3. This is exactly the same circuit as the basic SCDP but with a little difference in the biasing circuit.

The ' m ' value can be obtained from the low value of biasing resistor R (Fig.2) as described below. The input CM voltage, V_{cm} is sensed from input voltages through R_{cm} as shown in Fig.2 and this V_{cm} becomes the output CM voltage of the first stage for the next stage of modified SCDP circuit if any. The value of R_{cm} should be high to avoid any loading on the output. From Fig.2 and Fig.3, we obtain Iss using equation (33) as,

$$Iss=\frac{V_P}{R}-\frac{\left[V_{s1}-(V_x-V_{cm})\right]}{R_1}+\frac{V_P}{R_{out}} \quad (51)$$

$$=V_{P0}\left(\frac{1}{R}+\frac{1}{R_{out}}\right)-\frac{(V_{s1}-V_x+V_{cm})}{R_1}+\left(\frac{1}{R}+\frac{1}{R_{out}}\right)\delta V_{in}^2 \quad (52)$$

where R is the biasing resistor and R_1 is the resistor as shown in Fig.3. R_{out} is the output resistance seen from the point P as shown in Fig.3. V_{s1} and V_x are the fixed potentials as shown in Fig.3. R_2 and V_x provide the value of (V_x-V_{cm}) for equation (51) as per Fig.3. Here R_2 is chosen to be much larger than R and R_1 for reduced power consumption.

From (46) and (52), we find,

$$m(new)=\left(\frac{1}{R}+\frac{1}{R_{out}}\right)\delta \quad (53)$$

and

$$I_{0M}=V_{P0}\left(\frac{1}{R}+\frac{1}{R_{out}}\right)-I_P \quad (54)$$

where

$$I_P=\left(\frac{V_{s1}-V_x+V_{cm}}{R_1}\right) \quad (55)$$

Note that due to noise voltage changes in V_{cm}, the quiescent current I_{0M} varies and changes the output common-mode voltage. Without I_P current, the low value of R leads to larger variation in I_{0M} with respect to V_{cm}. The circuits shown in Fig.2 and Fig.3 provide the value of I_{0M} with lesser variation with respect to V_{cm} at dc. By differentiating I_{0M} with respect to V_{cm} in equations (54) and (55), we get,

$$\frac{\partial I_{0M}}{\partial V_{cm}}=\left(\frac{1}{R}+\frac{1}{R_{out}}+s(C_{out}+2C_{bs})\right)\frac{\partial V_{P0}}{\partial V_{cm}}-\frac{1}{R_1} \quad (56)$$

where C_{out} is the output capacitance of the current source block I_P seen from the point P as in Fig.3 and C_{bs} is the bulk-to-source capacitance of the transistor M1or M2. By differentiating equation (19), we obtain as,

$$\frac{\partial V_{P0}}{\partial V_{cm}}=1-\frac{1}{\alpha}\left(\frac{I_{0M}}{kp}\right)^{1/\alpha}\frac{1}{I_{0M}}\left(\frac{\partial I_{0M}}{\partial V_{cm}}\right) \quad (57)$$

By substituting (57) in (56), we obtain as,

$$\frac{\partial I_{0M}}{\partial V_{cm}}=\frac{\left(\frac{1}{R}+\frac{1}{R_{out}}+s(C_{out}+2C_{bs})\right)-\frac{1}{R_1}}{1+\left(\frac{1}{R}+\frac{1}{R_{out}}+s(C_{out}+2C_{bs})\right)\frac{1}{\alpha}\left(\frac{I_{0M}}{kp}\right)^{1/\alpha}\frac{1}{I_{0M}}} \quad (58)$$

and

$$\frac{\partial G_m}{\partial V_{cm}} = \sqrt{\frac{\alpha}{2}} \left(\frac{kp}{I_{0M}} \right)^{1/\alpha} \left(1 - \frac{1}{\alpha} \right) \frac{\partial I_{0M}}{\partial V_{cm}} \quad (59)$$

By making $R_1 \simeq R$, we have I_{0M} that varies minimally with respect to V_{cm} at dc as shown in equation (58).

A fully differential circuit can be made with two single ended SCDP circuits as shown in Fig.4. The following design procedure steps are required to design a compensated fully differential modified SCDP transconductor.

1. The value of quiescent current (I_{0M}) and kp should be chosen to achieve the transconductance ($2G_m$) for a fully differential circuit (Fig.4) as required for the given design specifications.
2. The biasing resistor (R) should be adjusted to provide the required value of ' m ' as in equation (53) for compensation.
3. The value of sourcing current (I_P) in equation (55) needs to be tuned to provide the required value of I_{0M} as in equation (54). That is, the potentials V_{s1} and V_x are to be chosen accordingly. Note that in the modified SCDP, the power dissipation is more than the conventional SCDP due to this sourcing current and the opamp's power supply currents as in Fig.3.

The current I_{0M} also varies with the input differential voltage amplitude as per equation (46). If we assume a single sinusoidal input differential voltage of amplitude V_a and frequency ω in Fig.2, the value of Iss is,

$$\begin{aligned} Iss &= I_{0M} + m(new) V_a^2 \sin^2(\omega t) \\ &= I_{0M} + \frac{m(new) V_a^2}{2} - \frac{m(new) V_a^2}{2} \cos(2\omega t) \end{aligned} \quad (60)$$

Note here that the dc value of Iss is changed and is more due to the input differential voltage amplitude. At higher input differential amplitudes, the dc current I_{0M} is more and this is the reason why two transconductors based fully differential circuit is studied and not a single transconductor based fully differential circuit. In a single transconductor based fully differential circuit, as I_{0M} increases there is no room to accommodate the increased current, I_{0M} in M3 and M4 as the gate voltage of these two transistors is fixed (M3 and M4 operate as current sources). Hence, the output common-mode voltage drops due to the channel length modulation effect. In a two transconductors based fully differential circuit (Fig.4), as I_{0M} increases, the transconductances (g_m) of M3 and M4 (M3 and M4 are current mirrors) increase and hence the output common-mode voltage tries to maintain approximately at the same level.

5. Results on Transconductors

The SPICE model library chosen for simulation is 130nm,1.2v, IBM Technology process. There are two examples for a fully differential transconductor shown here, one with alpha-power law characteristic and the other with square law characteristics.

Example 1: At higher biasing currents of SCDP, the MOSFETs behave deviated from square law characteristic for the chosen model library. The biasing current is chosen as I_{0M} =310uA. From model library, KP =40uA/v$^{\alpha}$, $vth0$ =0.366v, α =1.17 and Vdd =1.2v. The differential pair MOSFETs have W =20u and L =0.15u .The ideal value of transconductance $2G_m$ (fully differential) is 5.4mA/v. The various design parameters are V_{cm} =0.65v, V_x =1.15v, V_{P0} =71mv, R=R_1 =0.12k, V_{s1} =0.5328v and δ =0.59/v. From equation (50), $m(new)$ =5.87mA/v^2 but the realized value is 4.9mA/v^2.

The SPICE simulated differential output current versus input differential voltage characteristics (for input V_{cm} =0.65v and output V_{cm} =0.65) are shown in Fig.5 for ideal (straight line), conventional SCDP and modified SCDP circuits.The normalized linearity error in % vs input differential voltage characteristics are given in Fig.6 for both SCDP and modified SCDP circuits.

The transient simulations were performed with a sinusoidal input frequency of 100MHz and an output load capacitance of C_L =10pf. The obtained % total harmonic distortion (%THD) Vs input differential voltage amplitude characteristics are shown in Fig.7. It is noted that at higher input voltages the distortion is higher for conventional SCDP than modified SCDP.

A change of 4.42% in quiescent current I_{0M} is observed for 20mv input common-mode voltage noise at V_{in} =50mv for the fully differential modified SCDP whereas for the fully differential conventional SCDP, the change in I_{0M} is 8.03%.

Also a change in output common-mode voltage of 6.92% is noticed as the input differential voltage amplitude is changed from V_{in} =10mv to 300mv at input V_{cm} =0.65v for the fully differential modified SCDP whereas for the fully differential single transconductor based conventional SCDP, the change is 62.62% (A high change in output CM voltage!!!).

The output noise spectral voltage density at 100MHz for this example-1 transconductor design is 64.7nv/√Hz (for both conventional and modified SCDP) without any output load capacitor. The input referred noise spectral voltage density at 100MHz is 3.4nv/√Hz.

Example 2: At lower biasing currents of SCDP, the MOSFETs behave as square law characteristic for the chosen model library. For this example, the biasing current is chosen as I_{0M} =45uA. The model parameters are KP =40uA/v^2,

$vth0$ =0.366v, α =2.0 and Vdd =1.2v. The differential pair MOSFETs have W =20u and L =0.15u. The ideal value of $2G_m$ (fully differential) is 970uA/v. The design parameters are V_{cm} =0.65v, V_x =1.2v, R=R_1 =0.5k, V_{P0} =144mv, V_{s1} =0.6715v and δ =0.8/v. The realized value of $m(new)$ is 1.56mA/v^2 but its theoretical value is 1.33mA/v^2.

The simulated output differential current versus V_{in} characteristics (for input V_{cm} =0.65v and output V_{cm} =0.65v) are shown in Fig.8 for ideal, conventional SCDP and modified SCDP circuits. Fig.9 shows the normalized errors in % Vs V_{in} characteristics for both SCDP and modified SCDP.

The obtained % THD Vs V_{in} (amplitude) characteristics are shown in Fig.10 for an input frequency of 100MHz and with an output load capacitance of C_L =10pf.

For this case, a change of 5.8% in quiescent current I_{0M} is obtained for 20mv input common-mode voltage noise at V_{in} =50mv for the fully differential modified SCDP whereas for the fully differential conventional SCDP, the change in I_{0M} is 2.39% .

Also a change in output common-mode voltage of 6.29% is noticed as the input differential voltage amplitude is changed from V_{in} =10mv to 300mv at input V_{cm} =0.65v for the fully differential modified SCDP whereas for the fully differential single transconductor based conventional SCDP, the change is 36.46% (A high change in output CM voltage!!!).

For this example-2, the output noise spectral voltage density at 100MHz is 115nv/√Hz for both conventional and modified SCDP circuits without any output capacitor. The input referred noise spectral voltage density at 100MHz is 6.7nv/√Hz.

6. The Effect of Output Conductances

Consider a fully differential modified SCDP as shown in Fig.4.

Let I_{D1} and I_{D2} be the output currents of the each single transconductor and let g_{ds1} and g_{ds2} be the output conductances of transistors M1 and M3 (or M2 and M4) respectively. Let V_{o1} and V_{o2} be the output voltages of each transconductor in a fully differential circuit. Let V'_{o1} and V'_{o2} be the output voltages at the opposite sides (M1 and M3) of each transconductor. Now we have the output currents as,

$$I_{D1}=\left[\left(\frac{G_m V_{in}}{2}+g_{ds1}V'_{o1}+s\left(C'_L+2C_{gs}\right)V'_{o1}\right)N-g_{ds2}V_{o1}\right] -\left(\frac{-G_m V_{in}}{2}+g_{ds1}V_{o1}\right) \quad (61)$$

$$I_{D2}=\left[\left(\frac{-G_m V_{in}}{2}+g_{ds1}V'_{o2}+s\left(C'_L+2C_{gs}\right)V'_{o2}\right)N-g_{ds2}V_{o2}\right] -\left(\frac{G_m V_{in}}{2}+g_{ds1}V_{o2}\right) \quad (62)$$

where g_m is the transconductance of transistor M3 or M4 and C_{gs} is the gate-to-source capacitance of M3 or M4. where

$$N=\frac{g_m}{g_m+g_{ds2}} \quad (63)$$

and

$$C'_L=C_L+C_o \quad (64)$$

where C_L is the load capacitance at V_{o1} and V_{o2} and C_o is the sum of bulk-to-drain capacitances of M2 and M4 (or M1 and M3) respectively as shown in Fig.2. The voltages V'_{o1} and V'_{o2} can be obtained from,

$$V'_{o1}=\frac{sC'_L V_{o2}+\frac{G_m V_{in}}{2}(1+N)-(g_{ds1}+g_{ds2})V_{o1}}{\left[g_{ds1}+s\left(C'_L+2C_{gs}\right)\right]N} \quad (65)$$

$$V'_{o2}=\frac{sC'_L V_{o1}-\frac{G_m V_{in}}{2}(1+N)-(g_{ds1}+g_{ds2})V_{o2}}{\left[g_{ds1}+s\left(C'_L+2C_{gs}\right)\right]N} \quad (66)$$

The output voltage is given by,

$$V_o=V_{o1}-V_{o2}=\frac{(I_{D1}-I_{D2})}{sC'_L} \quad (67)$$

Substituting equations (65), (66) and (67) in equations (61) and (62), we obtain V_o as,

$$V_o=\frac{\frac{G_m(1+N)}{sC'_L}}{\left(1+\frac{g_{ds1}+g_{ds2}}{sC'_L}\right)} \quad (68)$$

Where N and C'_L are defined in (63) and (64) respectively. The equation (68) shows the effect of various output conductances on V_o. Using example-1 as discussed in the previous section, we have 4.48% change in V_o due to output conductances neglecting C_o. For the example-2 in the previous section, the change is 2.56% due to output conductances.

7. A Second Order Gm-C Bandpass Filter

A second-order continuous time Gm-C bandpass filter is constructed using both fully differential conventional SCDP and modified SCDP circuits. This circuit is shown in Fig.11.

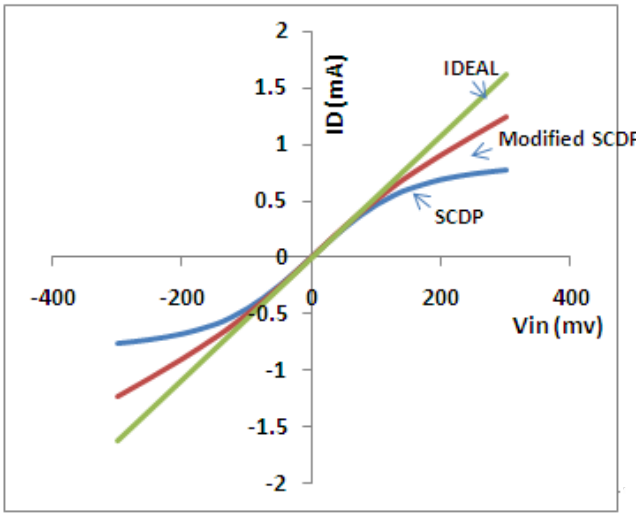

Figure 5. Transfer Characteristics – I_D Vs V_{in}. Simulated at I_{0M}=310uA, Input V_{cm}=0.65v, Output V_{cm}=0.65v and Vdd=1.2v.

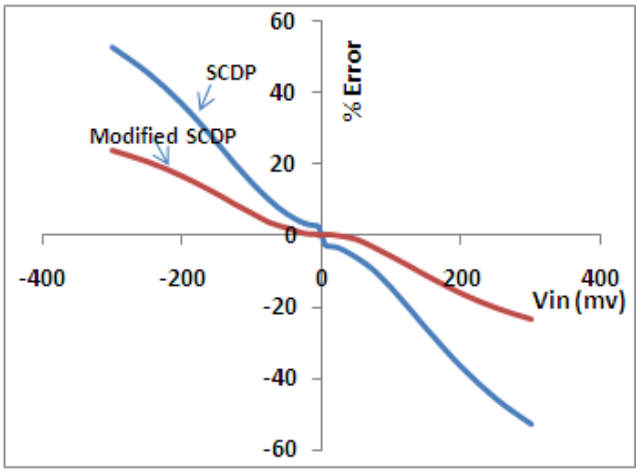

Figure 6. Departure from linearity in % error of Fig.5.

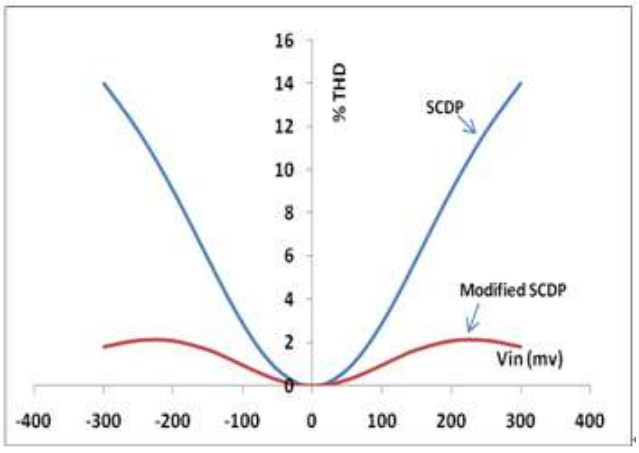

Figure 7. %THD Vs V_{in}(amplitude) characteristics. Simulated at I_{0M}=310uA, Input V_{cm}=0.65v, F_{in}=100MHz, C_L=10pf and Vdd=1.2v.

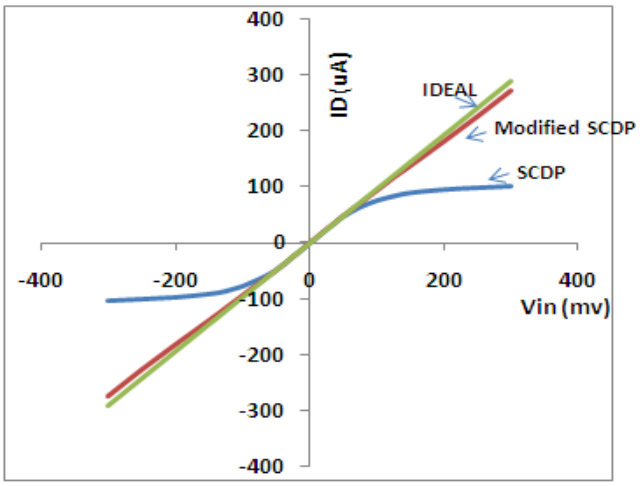

Figure 8. Transfer characteristics - I_D Vs V_{in}. Simulated at I_{0M}=45uA, Input V_{cm}=0.65v, Output V_{cm}=0.65v and Vdd=1.2v.

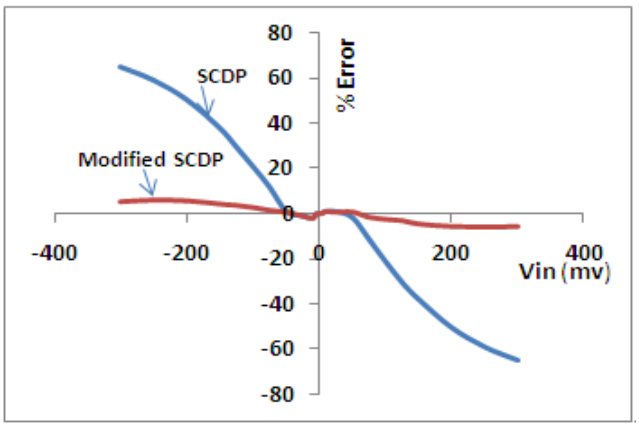

Figure 9. Departure from linearity in % error of Fig.8.

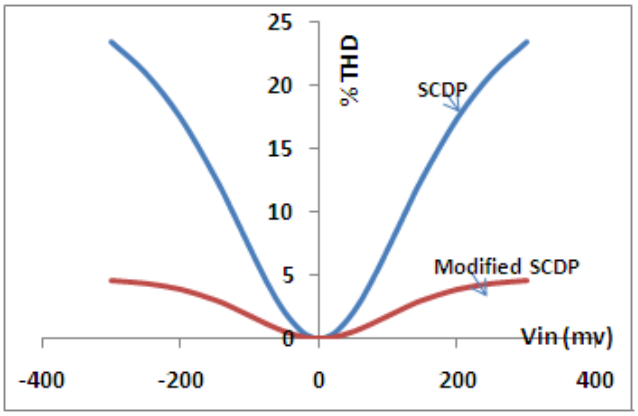

Figure 10. %THD Vs V_{in}(amplitude) characteristics. Simulated at I_{0M}=45uA, Input V_{cm}=0.65v, F_{in}=100MHz, C_L=10pf and Vdd=1.2v.

The transfer function of this second-order bandpass filter is given by,

$$H(s)=\frac{V_o(s)}{V_i(s)}=\frac{Gs\left(\frac{\omega_o}{Q}\right)}{s^2+s\left(\frac{\omega_o}{Q}\right)+\omega_o^2} \quad (69)$$

Where G is the gain and is chosen as 1.0 at the center frequency.

$$\omega_o = \frac{2G_{m1}}{C_1} = \frac{2G_{m2}}{C_2} \quad \text{and} \quad \left(\frac{\omega_o}{Q}\right) = \frac{2G_{m4}}{GC_2} = \frac{2G_{m3}}{C_2} \quad (70)$$

The various design parameters chosen are

$\omega_o = 2\pi * 100.0e06$ rad/sec , $Q=4$, $C_1 = C_2 = 6.175$pf ,

$2G_{m1} = 2G_{m2} = 3.88$mA/v and

$2G_{m3} = 2G_{m4} = 0.97$mA/v .

The bulk-node of all the NMOS transistors is tied to ground whereas bulk-node of all the PMOS transistors is tied to Vdd . The input common-mode voltage is chosen as $V_{cm} = 0.65$v. The biasing voltage (V_b) in the biasing circuit (Fig.1) is adjusted to provide all the required transconductance values for the case of conventional SCDP. For modified SCDP, the resistor (R) and the current (I_P) in the biasing circuit (Fig.2) are adjusted to provide all the wanted transconductances. Any suitable gain (G) can be achieved by independently varying G_{m4} .

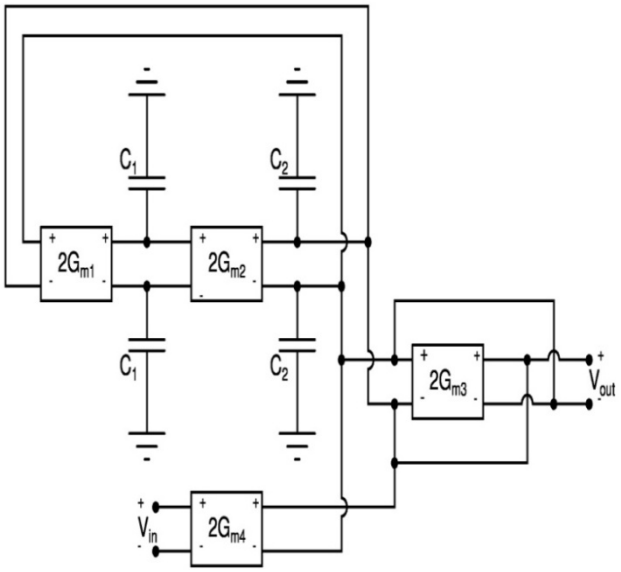

Figure 11. A second order Gm-C Bandpass Filter using fully differential transconductors

The 3dB bandwidth obtained is around 40MHz both for the conventional and the modified SCDP. The transient simulations were carried out for an input frequency of 100MHz with different input differential voltages. The obtained values of total harmonic distortion in % for different input voltage amplitudes are tabulated in Table.1 for both conventional and modified SCDP. Also the power dissipated by the bandpass filter circuit is tabulated in Table.1 for various V_{in} and both for the conventional SCDP and the modified SCDP.

This filter can be operated at any center frequency and the higher frequency limitation is imposed by the sum of bulk-to-drain capacitances (C_o) of NMOS (M2 or M1) and PMOS (M4 or M3) in the individual transconductors as shown in equations (64) and (68). As long as the sum of load capacitance and the total bulk-to-drain capacitances (C_o) of M2 and M4 is equal to C_1 or C_2 , the circuit can operate at higher center frequencies. In the present BPF circuit, the circuit operates up to 960MHz as the center frequency.

Table 1. The Band-pass Filter Performance Parameters studied in section-7.

Performance Parameters	V_{in}=50mv (amplitude)	V_{in}=100mv (amplitude)	V_{in}=250mv (amplitude)
Conventional SCDP %THD Power Dissipation	0.166 % 1.90mW	0.540 % 1.93mW	2.295 % 1.97mW
Modified SCDP %THD Power Dissipation	0.094 % 2.68mW	0.314 % 2.77mW	0.802% 3.11mW

8. A Temperature Compensation Scheme for the Modified Transconductor

The various output current versus input differential voltage characteristics for different values of temperature (-50deg.C, 25deg.C and 100deg.C) before compensation and after compensation (as explained below) for the case of example-2 studied in section-5, are shown in Fig.14. A temperature compensation circuit for the modified SCDP is shown in Fig.12. A two 2-bits digital technique has been used to compensate for the temperature above 25deg.C and below 25deg. C just to illustrate for the example-2, discussed in section-5.

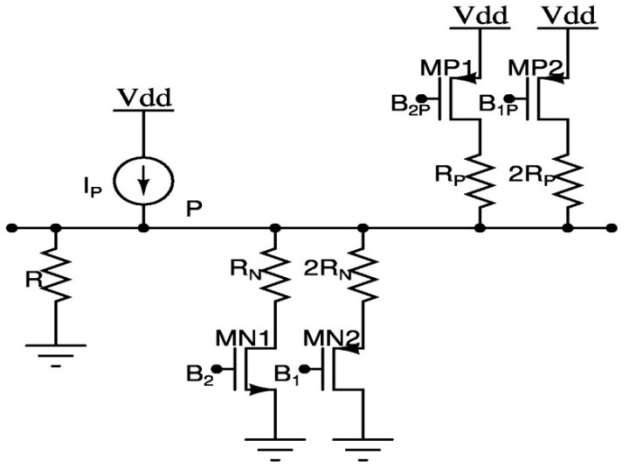

Figure 12. A Temperature compensated biasing circuitry.

It is observed that above 25deg.C without temperature compensation, the G_m value is lower and hence it requires more quiescent current value for compensation. Below

25deg.C, the modified transconductor requires less quiescent current. The Fig.12 is used to provide this adjusted biasing current value based on temperature. The designed values of R_N and R_P are 11.06k and 58.13k.

The current I_R, and hence the drop V_R in Fig.13 is used to sense the temperature(T) variation. For the example-2 discussed in section-5, the drop V_R varies from 0.440v (-50deg.C) to 0.487v (deg.100C). The designed value of R_R is 2.15k.

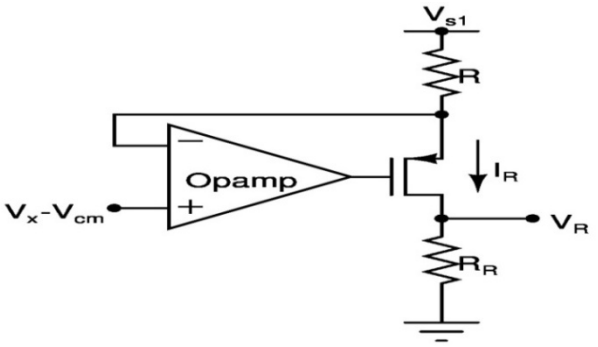

Figure 13. A temperature sensing circuitry for the modified SCDP.

A flash Analog-to-digtal converter (ADC) as shown in Fig.15 is used to get the bits B_2, B_1 (for T>25deg.C) and the bits B_{2P}, B_{1P} (for T<25deg.C) from the drop V_R which varies with respect to temperature. These bits are obtained directly from the V_R drop using this ADC and hence the modified transconductor is automatically compensated for temperature. The high dc gain comparators are used in Fig.15. The upper half of Fig.15 is for temperatures > 25deg.C and the lower half is for temperatures < 25deg.C. The designed values of various parameters used in Fig.15 are I_F =1u, R_F =2.8k, R_G =10k, V_{N1} =0.474v and V_{N2} =0.447v.

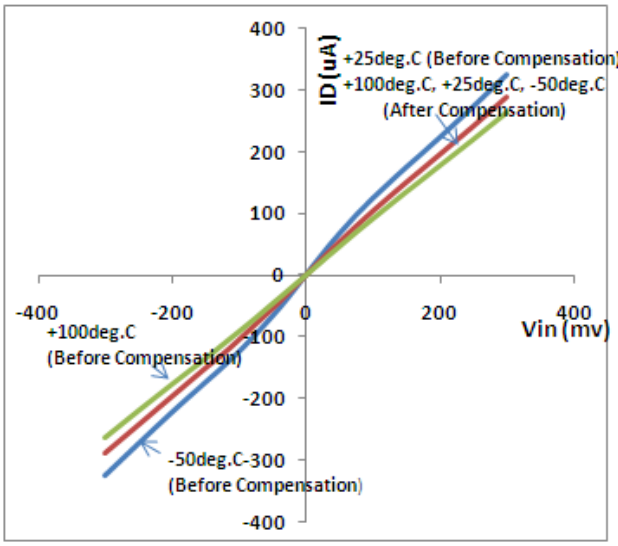

Figure 14. I_D Vs V_{in} Characteristics for different temperature corners. Simulated at I_{0M}=50uA, Input V_{cm}=Output V_{cm}=0.65v and Vdd=1.2v

For the case of example-2 studied in section-5, the temperature coefficient of output current before compensation is 2081ppm/deg.C at ΔT =150deg.C(maximum), V_{in} =100mv, input V_{cm} =0.65v and I_{0M} =50uA and the new value of temperature coefficient after compensation is 256ppm/deg.C.

For the example-1 studied in section-5, the temperature coefficient of output current before compensation is 2914ppm/deg.C at ΔT =150deg.C(maximum), V_{in} =100mv, input V_{cm} =0.65v and I_{0M} =310uA whereas the new value of temperature coefficient after compensation is 563ppm/deg.C.

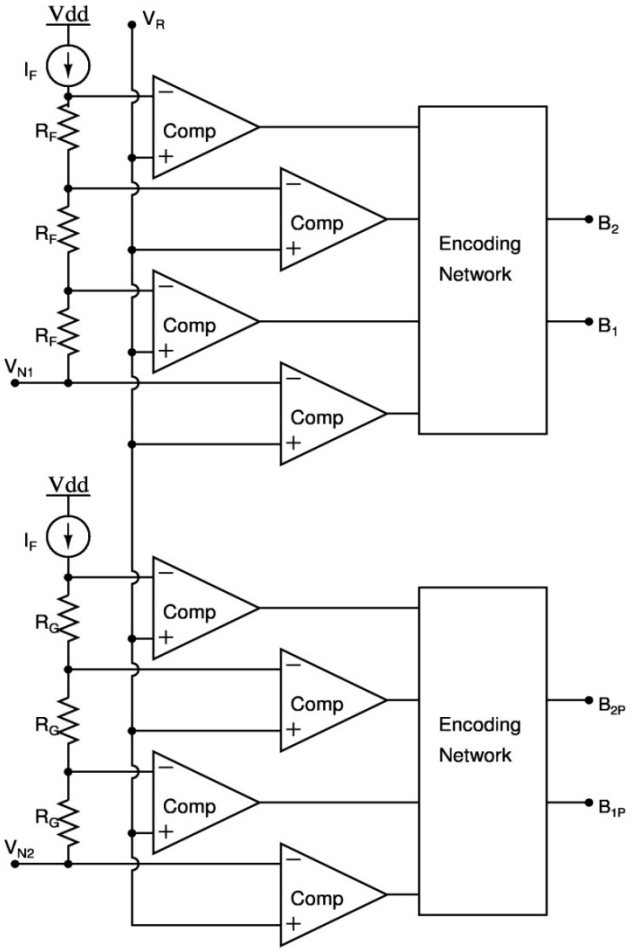

Figure 15. A Flash ADC for Temperature Compensation.

9. Conclusions

A theoretical model for a source-coupled differential pair for alpha-power law based MOSFETs has been discussed and a simple design procedure for the circuit compensation technique for realizing a linear SCDP transconductor was proposed. This modified fully differential SCDP has linearity much better than the conventional fully differential SCDP for a wide range of input differential voltages. Also the variation of the quiescent current with respect to input

common-mode voltage noise was minimized in the proposed design. The output differential voltage dependence on the transistor output conductances has been discussed. An example circuit, a Gm-C bandpass filter has been used to verify linearity in the transconductance value between the fully differential modified SCDP and the fully differential conventional SCDP. An automatic temperature compensation technique for the transconductance value has also been discussed.

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