Design of Low-Loss Transmission Lines in Scaled CMOS by Accurate Electromagnetic Simulations

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***Abstract*—Transmission lines are becoming of common use at mm-wave to implement on-chip functions as impedance matching, filtering and interconnects. Lack of an accurate and fast simulation method is nonetheless evident for transmission lines in scaled CMOS where metal dummies inserted for IC planarization make their physical structure extremely complicate. Although lines are not uniform due to displacement of small dummies, they are still periodic. In this paper, we describe an analytical procedure, leveraging lines periodicity and based on Floquet's theorem, in order to derive electromagnetic parameters from simulations. Conventional, slow-wave and shielded CPWs have been realized in a 65 nm CMOS technology. Thanks to the developed method, an optimum line design has been made possible. The lossy CMOS substrate, responsible for a significant performance degradation, can be effectively shielded and achieved performances are comparable with other technologies considered better suited to implement low-loss, high frequency passive components. Shielded CPW lines show attenuation as low as 0.65 dB/mm at 60 GHz, a record in scaled CMOS.**

***Index Terms*—CMOS, EM simulators, millimeter-wave integrated circuits, transmission lines, wireless transceivers.**

I. Introduction

MILLIMETER-WAVE CMOS RF circuits are drawing more and more attention, motivated by the new wave of consumer products exploiting the 60–100 GHz frequency range: short-distance, high data-rates and point-to-point inter-building communications, anti-collision automotive radars, passive and active imaging representing possible applications [1], [2].

Due to the very high operating frequency, the signal wavelength becomes comparable with typical IC dimensions, making transmission lines attractive to implement on-chip functions as impedance matching, filtering and interconnections between different blocks [3]–[7]. One of the key merits of transmission lines is easy model scalability, in contrast with lumped-element components, e.g., integrated capacitors or spiral inductors, which require a dedicated characterization procedure [8]. A well-designed RF circuit based on transmission lines also minimizes (or even completely removes) the need for a parasitic extraction tool, since all interconnect parasitics are already taken into account in the line model. Moreover, precise measurements of capacitors or inductors are problematic because of the small value of components typically needed at these high frequencies. On the contrary, line characterization can be performed on prototypes of arbitrary length, from which unit-length parameters can always be obtained allowing design of scaled length lines.

Many papers have been published in recent years reporting various different line topologies on Silicon substrates, including standard geometries (like microstrip (MS) and coplanar waveguides (CPW) [9]–[12]) and more complicated ones (like slow-wave lines [3], [4], [13], [14]), which exploit the dense stratification of modern processes to improve the line characteristics–in terms of attenuation, quality factor, substrate shielding, occupied area—and, consequently the RF circuit performance.

However, to the authors' knowledge, no rigorous methodology has been yet developed in order to provide a rapid and accurate simulation tool for transmission lines in scaled CMOS. Moreover, a significant performance gap between transmission lines realized in bulk CMOS versus SOI or SiGe is evident from published literature.

In this paper, a method dedicated to the simulation of transmission lines on CMOS substrates is presented, guiding the design and optimization of the line geometry with commercial full-wave electromagnetic (EM) software, while considering all the details of the stratification, the actual substrate effects and the design constraints set by modern CMOS processes (e.g., density rules). This method allows rapid simulation of both conventional lines, with uniform geometry along the propagation direction, and "slow-wave" lines, which feature a periodic variation of their geometry along the propagation direction.

A set of transmission lines on standard 65 nm bulk CMOS process has been designed and their measurement is presented, achieving 1 dB/mm attenuation for conventional CPW lines and a record 0.65 dB/mm attenuation for a shielded-CPW line, which compares favorably with alternatives implemented in other technologies.

The paper is organized as follows. Section II describes the simulation methodology, Section III reports the design and measurement of different types of lines, Section IV compares results with state of the art and Section V draws conclusions.

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II. Accurate and Fast Analysis of Periodic Lines

Standard transmission lines are usually uniform structures, i.e., their cross-section is constant along the propagation direction. In this case the propagation characteristics of the line can be derived considering its cross-section only, by using a 2-D EM analysis method [15]. On the other hand, lines realized in ultra-scaled CMOS technologies are usually periodic, rather than uniform, the periodicity being introduced intentionally, as in the slow-wave line shown in Fig. 1(a), or resulting from technological constraints, e.g., when a usually periodic pattern of dummy metals cells is introduced in order to guarantee IC planarity, as shown in Fig. 1(b). In these cases, 2-D EM analysis methods cannot be used, or may prove inaccurate whenever dummy metals cannot be placed far enough from line's conductors. Three-dimensional (3-D) EM analysis—leading to the representation of a line section in terms of scattering parameters from which its propagation characteristics are deduced—may require very long simulation times and memory resources, due to the huge number of unknowns resulting from the discretization of a large structure with fine geometrical details. Moreover, a multi-modal representation of the structure and/or sophisticated de-embedding techniques are often needed, since dummy cells and metal bars represent discontinuities very close to the reference sections of the ports, thus exciting higher-order modes [16]. Accuracy can be improved by considering longer line sections or a higher number of propagation modes on the port sections but this has an enormous impact on simulation time.

To speed up simulation without loss of accuracy, we propose a different approach based on the periodic nature of the lines. In fact, propagation characteristics of periodic structures can be studied by considering their "unit cell", enclosed by periodic boundaries defined on surfaces normal to the propagation direction [see Fig. 1(c)]. This approach has been followed to characterize periodically screened coplanar waveguides on semi-insulating GaAs substrate in [17], where the unit cell was analyzed according to circuit theory, by simply cascading short sections of CPW with and without metal bars, represented by their ABCD matrices. In this paper we extend this approach to the full-wave electromagnetic analysis of the unit cell, in order to consider all the discontinuity effects that cannot be accounted for by a circuit analysis.

According to Floquet's theorem [18], the problem can be formulated in order to find an EM field (Floquet's mode), solution of the Maxwell's equations inside the unit cell, which satisfies the following periodicity condition:

$$\vec{E}_2 = \vec{E}_1 e^{-\gamma d} \quad \vec{H}_2 = \vec{H}_1 e^{-\gamma d} \tag{1}$$

where γ is the complex propagation constant, $\vec{E}_1, \vec{H}_1, \vec{E}_2, \vec{H}_2$ are the electric and magnetic fields on surfaces S_1 and S_2, and d is the length of the unit cell [see Fig. 1(c)].

The standard procedure for determining Floquet's modes and their propagation constants consists in finding, at a given (angular) frequency ω, a matrix relationship between the discretized fields on S_1 and S_2, and determining the propagation constant as an eigenvalue of that matrix [19] (since we are interested in the quasi-TEM mode of the periodic structure, only the first eigenvalue must be evaluated). Repeating the procedure for different values of ω, the dispersion curve $\gamma = \gamma(\omega)$ of the quasi-TEM mode can be obtained. Unfortunately this procedure cannot be applied in conjunction with commercial EM solvers (e.g., Ansoft HFSS™), since they usually do not provide the system matrices generated during the solution (FEM matrices, in the case of HFSS). Therefore, specialized solvers must be developed [20], [21].

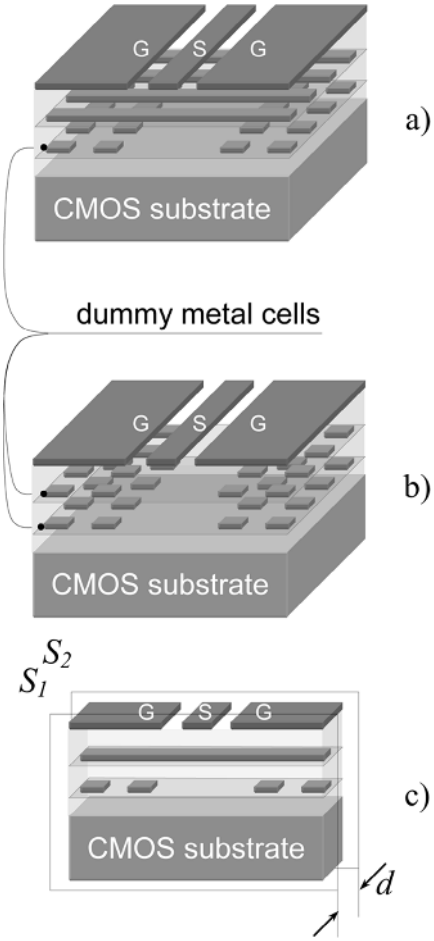

Fig. 1. Transmission lines in scaled CMOS: (a) slow-wave CPW, and (b) standard CPW. Line characteristics can be obtained from unit cell analysis (c).

In order to be able to exploit the flexibility of commercial electromagnetic solvers, HFSS in particular, we adopt a different procedure for finding the dispersion curve of the quasi-TEM Floquet's mode of the structure. The approach is similar to the one described in [21] in the context of a Finite-Difference Frequency-Domain algorithm, and consists in considering an equivalent resonant-cavity model of the periodic cell, obtained by imposing the following periodic boundary conditions on surfaces S_1 and S_2:

$$\vec{E}_2 = \vec{E}_1 e^{-j\theta} \quad \vec{H}_2 = \vec{H}_1 e^{-j\theta} \tag{2}$$

where θ is a given periodic phase shift. As discussed in [21], the complex propagation constant $\gamma = \alpha + j\beta$ of the quasi-TEM mode of the periodic structure is deduced from the complex resonant frequency $\Omega = \omega_r + j\omega_i$ of the first mode of the cavity obtained by solving a suitable eigenvalue problem. When the periodic structure can be considered lossless, the procedure is

straightforward, since in this case γ is imaginary ($\gamma = j\beta$) and Ω is real ($\Omega = \omega_r$), ω_r representing the frequency at which the fields of the quasi-TEM mode satisfy the periodicity condition (2). Therefore the value of β at ω_r is simply given by $\beta = \theta/d$. Actually, in the lossless case the two procedures are equivalent, the only difference being how the $\omega-\beta$ diagram is obtained, i.e., finding β for a given ω when using the standard procedure, or finding ω for a given $\beta = \theta/d$ when using the equivalent resonant-cavity model. When losses cannot be ignored, as in the case of CMOS transmission lines, the eigensolution inside the equivalent resonant-cavity model is in terms of damped quasi-sinusoidal fields, and therefore the eigenvalue Ω is complex. Its real part has the same meaning as in the lossless case (and thus the $\omega - \beta$ diagram is obtained in the same way as before), whereas the imaginary part accounts for the damping which, according to the theory of resonant cavities, can be expressed in terms of the well-known quality factor Q [22]

$$Q = \frac{\omega_r}{2\omega_i}. \tag{3}$$

Moreover, it is possible to translate the time-domain damping factor Q into a distance-related attenuation factor α, i.e., into the real part of the propagation constant of the quasi-TEM Floquet's mode [21], [23]:

$$\alpha = \frac{v_p}{v_g}\frac{\beta}{2Q} \tag{4}$$

where $v_p = \omega/\beta$ and $v_g = \partial\omega/\partial\beta$ are the phase- and group-velocity of the mode, respectively. Equation (4) can be simplified in our case, since very low dispersion is expected for the quasi-TEM mode, and β has an almost linear dependence on ω (this condition can be verified from the $\omega - \beta$ diagram in Section III). If this condition holds, $v_p \approx v_g$, and from (3) and (4) we finally have

$$\alpha = \beta\frac{\omega_i}{\omega_r} = \frac{\theta}{d}\frac{\omega_i}{\omega_r}. \tag{5}$$

Note that (5) is consistent with the usual definition of the quality factor of a transmission line [23]:

$$Q_L = \frac{\beta}{2\alpha}. \tag{6}$$

The procedure described above can be easily implemented by using HFSS as EM solution engine. In fact, condition (2) can be imposed by using a master–slave boundary condition [24] on surfaces S_1 and S_2 of the unit cell, assigning a given value $\bar{\theta}$ for the periodic phase shift. To calculate the propagation constant at a target frequency ω, an initial value of $\bar{\theta} = \omega\sqrt{\varepsilon_r}d/c$ is chosen, where c is the velocity of light and ε_r is the relative dielectric constant of the oxide. Then the structure is analyzed by using the so-called eigenvalue solution, in order to find the first (i.e., smallest magnitude) eigenvalue $\bar{\Omega} = \bar{\omega}_r + j\bar{\omega}_i$. Its real part gives the value of the frequency corresponding to $\bar{\beta} = \bar{\theta}/d$ and (5) is used to calculate α at $\bar{\omega}_r$. By iterating the procedure for different values of $\bar{\theta}$, the dispersion and the attenuation curves of the periodic line in a given frequency range is obtained.

Finally, the resonant electric and magnetic fields $\vec{E}_r$ and $\vec{H}_r$, obtained as eigensolution associated with the eigenvalue $\bar{\Omega}$ found for any value of $\bar{\theta}$, can be used to calculate the characteristic impedance of the quasi-TEM mode at ω_r. The possible definitions of characteristic impedance are in terms of the voltage and current (Z_{VI}), power and voltage (Z_{PV}), or power and current (Z_{PI}) [25]

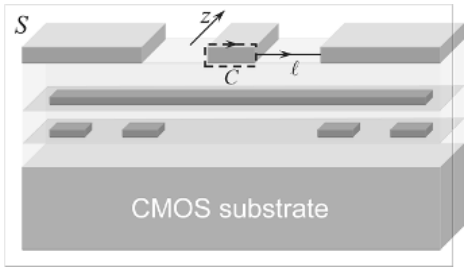

Fig. 2. Definition of integration paths for voltage (ℓ) and current (C) determination on CPW section.

$$Z_{VI} = \frac{V}{I} \quad Z_{PV} = \frac{|V|^2}{2P^*} \quad Z_{PI} = \frac{2P}{|I|^2} \tag{7}$$

where V, I have the usual meaning, P is the complex power and "*" denotes the complex conjugate. These quantities can be easily evaluated by using the Field Calculator of HFSS [26]:

$$\begin{aligned} V &= \int_{\ell} \vec{E}_r \cdot d\vec{l} \\ I &= \oint_{C} \vec{H}_r \cdot d\vec{c} \\ P &= \frac{1}{2}\int_{S} \vec{E}_r \times \vec{H}_r^* \cdot \hat{z}\, ds \end{aligned} \tag{8}$$

where ℓ and C, shown in Fig. 2, are suitable integration path defined on the surface S (which may coincide with either S_1 or S_2), and $\hat{z}$ is the normal to S. For MSs or CPWs the most used impedance definition is Z_{PI}, but all the definitions in (7) provide similar results, in the range of a few percent.

Note that, in finding the impedance of the periodic line, we use the resonant fields of the equivalent resonant-cavity model, instead of those of the true Floquet's mode, as it would be required by the theory of periodic structures. Actually, the two fields are slightly different, the former having the same magnitude at both ends of the unit cell [see (2)], the latter accounting also for the attenuation across the unit cell. Therefore, only approximated values of the impedance can be obtained by the equivalent resonant-cavity model. However, from a practical point of view, the accuracy in estimating the impedance is better than a few percent, provided the attenuation-per-unit cell is reasonably small, e.g., less than 0.01 dB per cell, a condition that applies in any line of practical use.

In order to validate this procedure, we have simulated a uniform 50 Ω MS transmission line, assuming the process parameters of a 65 nm CMOS process from STMicroelectronics, featuring 7 metal Cu layers plus an Al metal cover layer. Signal line is in Metal 7 and a solid ground is obtained shunting Metal 1 and 2 together. This structure, though not compliant with metal density design rules, has been selected since it can be analyzed

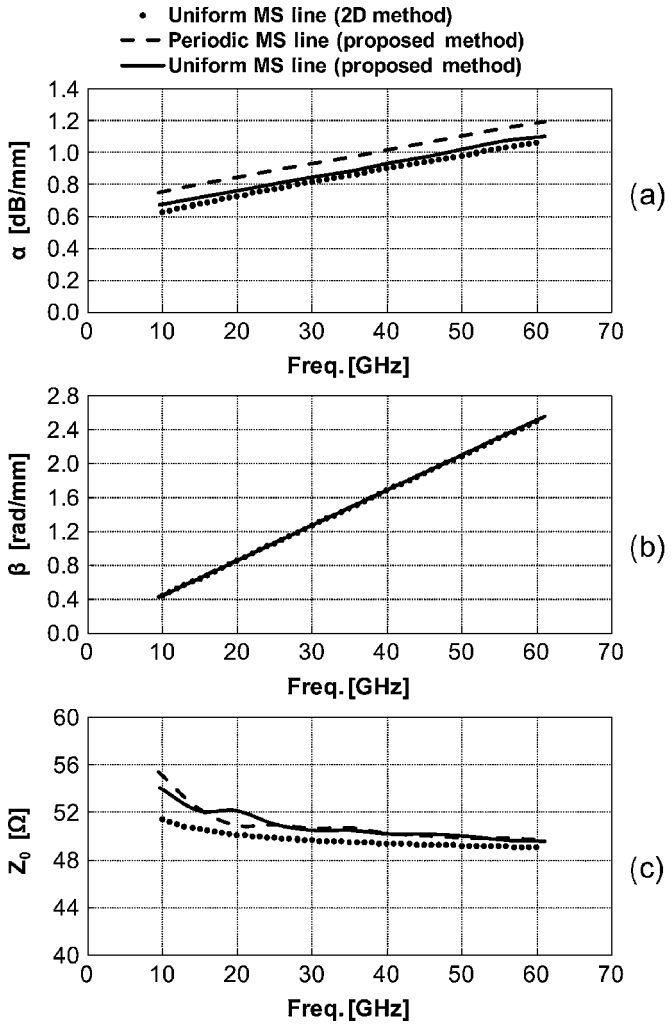

Fig. 3. (a) Attenuation, (b) phase constant, and (c) characteristic impedance versus frequency for a MS line. Simulations assuming a uniform line have been performed both by means of 2-D simulator (•) and proposed cavity-resonant model (—). Simulations of periodic structures (i.e., perforated ground plane) with proposed model are also reported (- -).

either by conventional 2-D method or by the equivalent resonant-cavity model, defining a fictitious periodicity ($d = 1\ \mu$m in this case). Fig. 3 shows the attenuation, the phase constant and the characteristic impedance as a function of frequency, comparing the results of our method versus the 2-D method of the commercial simulator HFSS. An excellent agreement emerges. To fulfill metal density rules for process planarity, we then introduced a periodically perforated ground plane, by using a configuration similar to the one introduced in [27] (metal strips of 0.55 μm in the longitudinal and transverse direction; square holes 0.45 μm $\times$ 0.45 μm). The MS line is not uniform anymore, but still periodic, with the same period of 1 μm as before. In this case, 2-D simulators *cannot* be adopted while our method *can*. Results for the periodic MS line are also reported in Fig. 3. At 60 GHz the design-rule compliant MS line features an attenuation constant of 1.2 dB/mm and a quality factor of 9.2. Note that the slots do not significantly influence the characteristic impedance, since they are much shorter than the wavelength, but they increase the attenuation constant of the MS. The simulation requires 212 s of CPU time and 84 MB of memory,

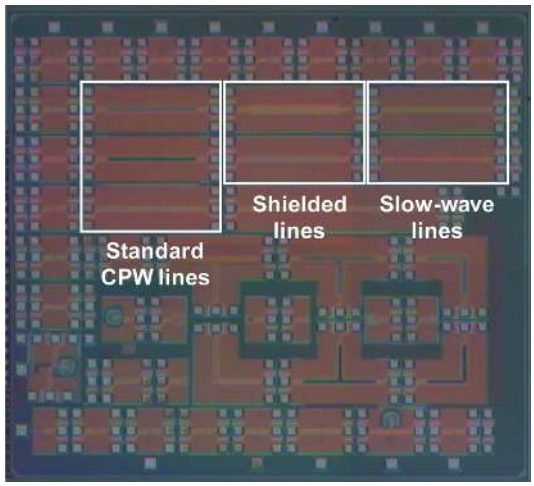

Fig. 4. Chip photomicrograph.

for each frequency point, on a PC using an Intel Core 2 Duo T7250 processor.

III. Design and Measurements

Although MS lines offer an intrinsic good isolation from the substrate, its field being almost confined in the low-loss oxide region between ground and signal conductors, we used MS lines as validation test case only, and we did not realize any MS prototype. In fact, in order to reduce MS line attenuation and improve its quality factor, larger line-to-ground distance and line width would be required, but the former is set given the used process, the latter determines the characteristic impedance. For this reason we considered CPW lines only, where more parameters are available, allowing the designer to optimize the line geometry for better performances.

All the lines were fabricated in the same 65 nm CMOS process used in the microstrip simulations. Fig. 4 shows the chip photomicrograph. The lines were designed using the proposed method, employing the commercial simulator HFSS from Ansoft, and its "eigenmode" EM simulator engine in particular [28]. All simulations were performed on a personal computer with an Intel Core 2 Duo T7250 processor. All the measurements were performed using Cascade Infinity Probes and an Anritsu VNA. Probe tips calibration was performed on a standard alumina substrate, and measurements were de-embedded by the Open-Short method [29].

A. Standard CPW Lines

Fig. 5 shows the geometry used to obtain a standard CPW. The two ground conductors and the signal one are realized on the top metal layer, which offers the lowest sheet resistance and highest distance from the substrate. To achieve a desired characteristic impedance two parameters are available, i.e., the signal conductor width W and the gap distance G between signal and ground conductors. The design is made more complicate and achievable performances are limited by the need for a specified metal density at each metal level. Dummies in metal levels where signal and ground are drawn can limit realizable impedances, while those at other levels can impair performances.

A set of lines, all with 50 Ω characteristic impedance, but with various signal conductor widths and gap distances has been

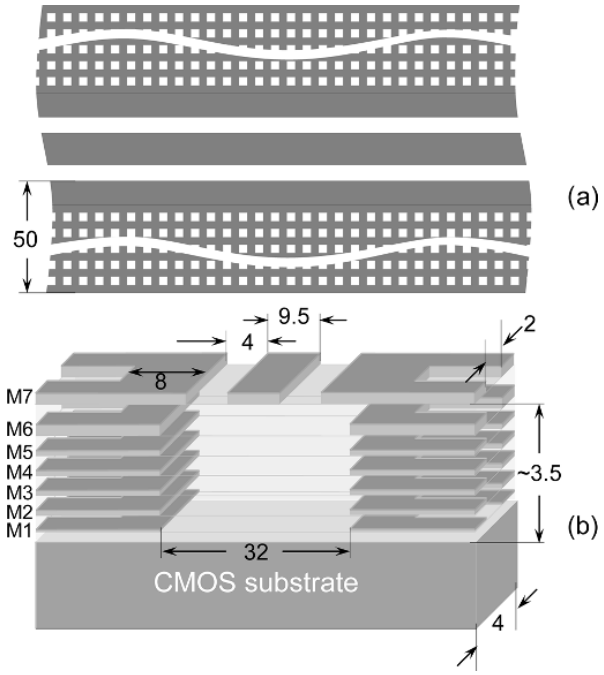

Fig. 5. Geometry of the proposed standard CPW transmission line: (a) top view; (b) detail of the cross section. Dimensions in μm (drawing not to scale).

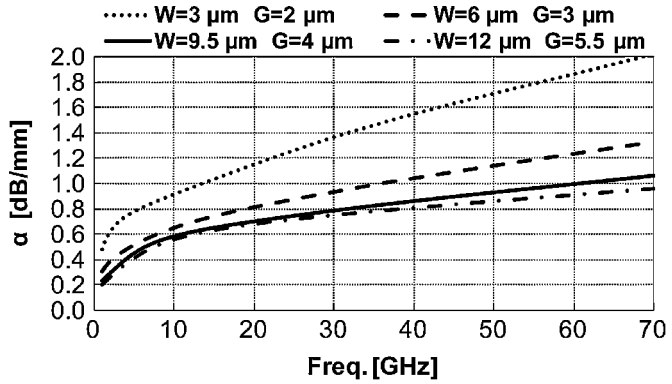

Fig. 6. Attenuation constant of standard CPW lines ($Z0 \approx 50\ \Omega$ @ 60 GHz) for different values of signal width W and gap G.

simulated. In principle, an optimum performance is expected as a compromise between metal and substrate losses. In fact, increasing the width of the signal conductor decreases metal losses, but larger gaps are needed to keep the impedance value constant, causing a reduction of field confinement in the low-loss oxide gap region and an increase of substrate losses. Fig. 6 plots simulated results. Attenuation reduction is monotonic with increasing W and G. The benefit is marginal for $W > 9.5$ μm and $G > 4$ μm, though. Moreover, larger line width and gap complicate the layout in order to respect density rules. Thus we chose $W = 9.5$ μm and $G = 4$ μm as optima values. Characterization of the unit cell at one frequency point requires about 330 s and 150 MB of memory.

To verify the impact of P^+ doped well on the surface of the CMOS substrate, introduced to prevent latch-up phenomena, two lines with the same geometry of Fig. 5 were realized, the

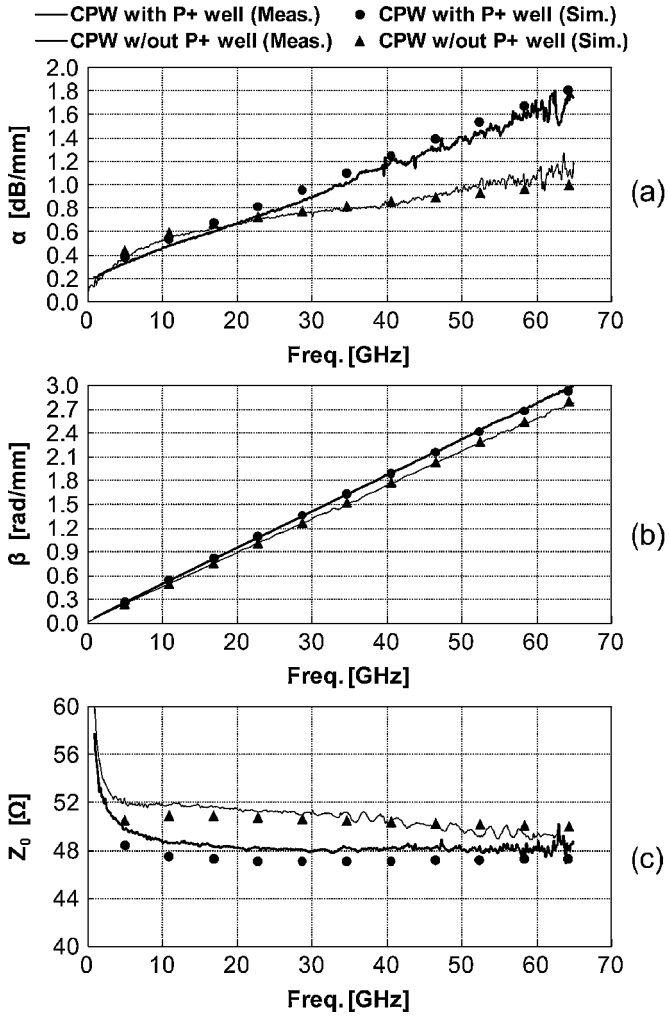

Fig. 7. (a) Attenuation, (b) phase constant, and (c) characteristic impedance versus frequency for the standard CPW shown in Fig. 5. Continuous lines show measurements of the CPW with P^+ well layer (—) and without P^+ well layer (—). Discrete points represent simulations.

only difference being a drawing layer which inhibits well diffusion. Fig. 7 shows measured and simulated results. Very good agreement can be observed in the whole frequency band. As expected, the P^+ well has a major impact on substrate losses, increasing attenuation from 1 dB/mm to 1.7 dB/mm at 60 GHz. Note that all dummy fills are connected to the ground planes through vias (not shown in Fig. 5), but no contacts are present between line ground-planes and substrate in proximity of the signal line: in fact, simulations show that in case of substrate contacts, the return currents would partially flow in the substrate due to the close spacing between top metals and substrate, producing a further increase in line attenuation.

B. Slow-Wave CPW Lines

Slow-wave CPWs are a result of a smart use of the dense stratification available in modern CMOS processes, to artificially increase the effective dielectric constant of the line. This is achieved, as shown in Fig. 8, by adding equally spaced floating metal strips underneath the transmission line, to locally increase

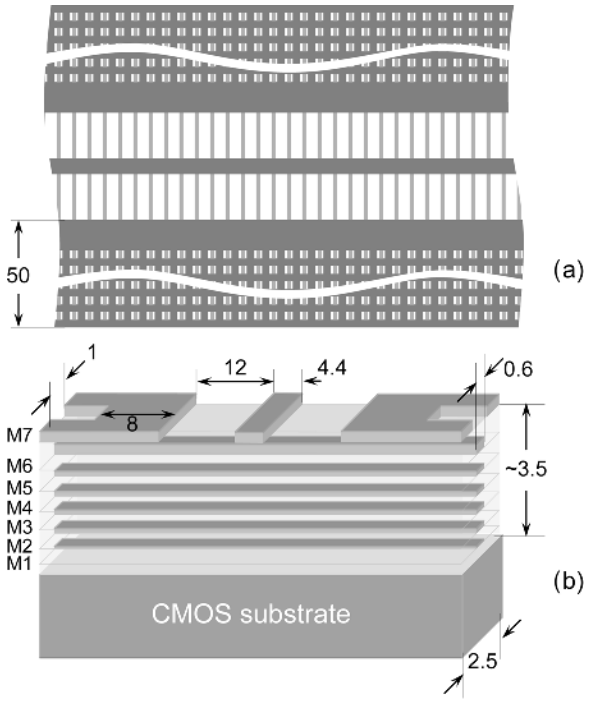

Fig. 8. Geometry of the proposed slow-wave CPW transmission line: (a) top view; (b) detail of the cross section. Dimensions in μm (drawing not to scale).

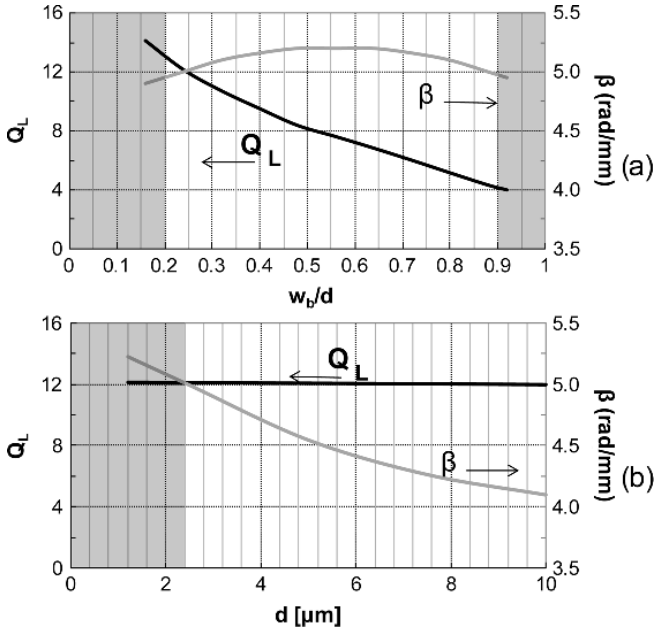

Fig. 9. Quality factor and phase constant of the slow-wave CPW transmission line at 60 GHz: (a) versus the ratio between strip width and unit cell period $\boldsymbol{w_b/d}$ for $\boldsymbol{d} = 2.5$ μm; (b) versus cell period $\boldsymbol{d}$ for $\boldsymbol{w_b/d} = 0.24$. Shadowed regions correspond to geometries forbidden by design rules.

the line capacitance: as a result, phase velocity of the line is decreased. In addition, these strips help fulfilling the metal density rules mitigating the problem of introducing metal dummies.

Besides W and G, a slow-wave CPW offers two additional degrees of freedom, i.e., the shield's metal strips width w_b and spacing s. These quantities define the period $d = w_b + s$ of the unit cell. W and G control the characteristic impedance, like in a standard CPW. On the other hand, the values of w_b and s can be optimized in order to maximize shield efficiency and phase constant. These effects, however, are not simple to analyze with common methods. Relying on an accurate and fast simulation method, we were able to perform many simulations in order to gain more insight into slow-wave CPW design intended for matching networks, where the goal is maximum quality factor Q_L, maintaining a large value of the phase constant β for minimum area occupation. In these simulations, carried out at 60 GHz, we considered fixed values of $W = 4.4$ μm and $G = 12$ μm, allowing characteristic impedances close to 50 Ω. These values are at the edge of the allowed range for density rules fulfillment, and were not changed even if the obtained characteristic impedance was less than 50 Ω, since larger gaps violate design rules, and narrower line widths increase conductor losses too much. Fig. 9(a) shows Q_L and β as a function of the ratio w_b/d for a fixed period $d = 2.5$ μm. It is evident that reducing w_b yields larger values of Q_L, without affecting β too much. Characteristic impedance varies between 45.6 Ω for $w_b/d = 0.16$ and 35.7 Ω for $w_b/d = 0.92$. Because the ratio w_b/d equals the metal density, not all values are possible (shaded regions in Fig. 9(a) correspond to metal densities forbidden by design rules), and the smallest feasible value should be used.

The effect of changing the unit cell period was also explored. Fig. 9(b) shows Q_L and β as a function of d, assuming a fixed ratio $w_b/d = 0.24$, i.e., a value close to the minimum allowed. In this case β increases for small values of d, while Q_L remains constant. Also in this case design rules set a limit to the minimum periodicity, due to the smallest feasible width of the strips ($w_b \geq 0.5$ μm). The shaded region in the plot corresponds to forbidden line widths. Characteristic impedance varies between 42.9 Ω for $d = 1.2$ μm and 51.9 Ω for $d = 10$ μm.

Based on these simulations, we designed the slow-wave CPW with the dimensions reported in Fig. 8. The resulting characteristic impedance is about 45 Ω. Measurements, performed on prototypes and reported in Fig. 10, show a very good agreement with simulations. Characterization of the unit cell at one frequency point requires about 320 s and 163 MB of memory. Note that α and β are almost doubled with respect to the standard CPW line, i.e., slow-wave CPW provide the same quality factor ($Q_L \cong 12$ at 60 GHz) as standard CPW, but they are suited to implement stubs and matching line sections using only half of the length, leading to a more compact circuit with unaltered performance. As a drawback, slow-wave lines usually require a larger cross-section for the same impedance as standard CPW line. Moreover, they allow increasing the capacitance per unit length, but the inductance is almost the same as for standard CPW lines: the range of feasible characteristic impedances is reduced with respect to standard CPW lines.

C. Shielded CPW Lines

As pointed out in Section III-A, in a standard CPW the EM field penetrates to some extent in the lossy CMOS substrate, contributing to the total attenuation factor. Using our method we could easily estimate this contribution, simulating a periodic cell with a fictitious loss-free CMOS substrate, and we found that in the CPW of Fig. 5 the substrate losses are about 40% of the total. The obvious remedy to reduce substrate losses would be to resort to an additional shielding metal layer, e.g., realized

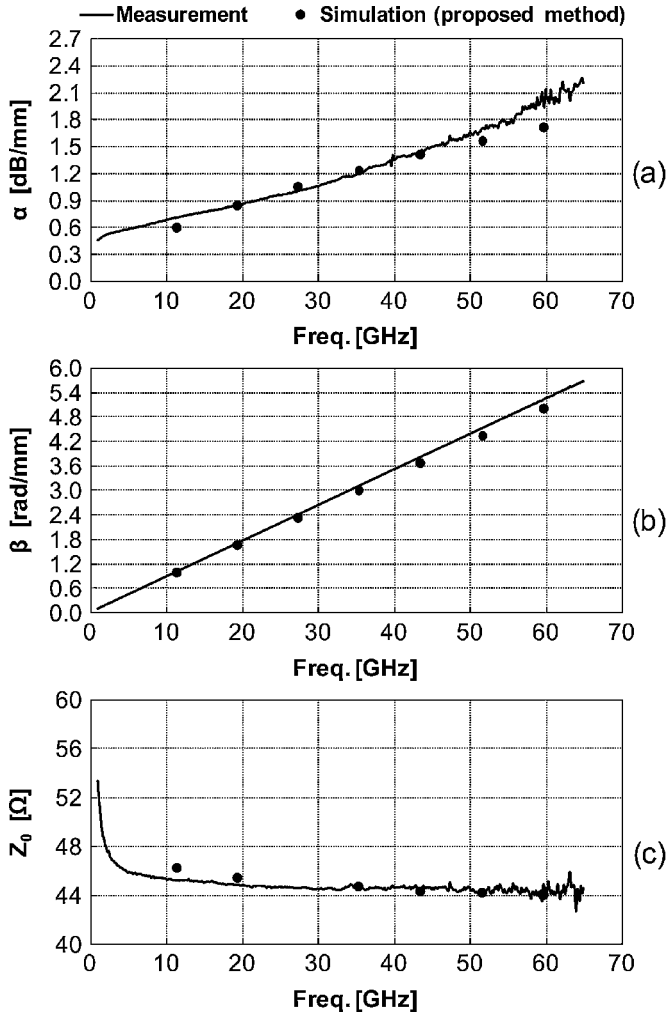

Fig. 10. (a) Attenuation, (b) phase constant, and (c) characteristic impedance versus frequency for the slow-wave CPW shown in Fig. 8; measurement (—) and simulation with the proposed method (•).

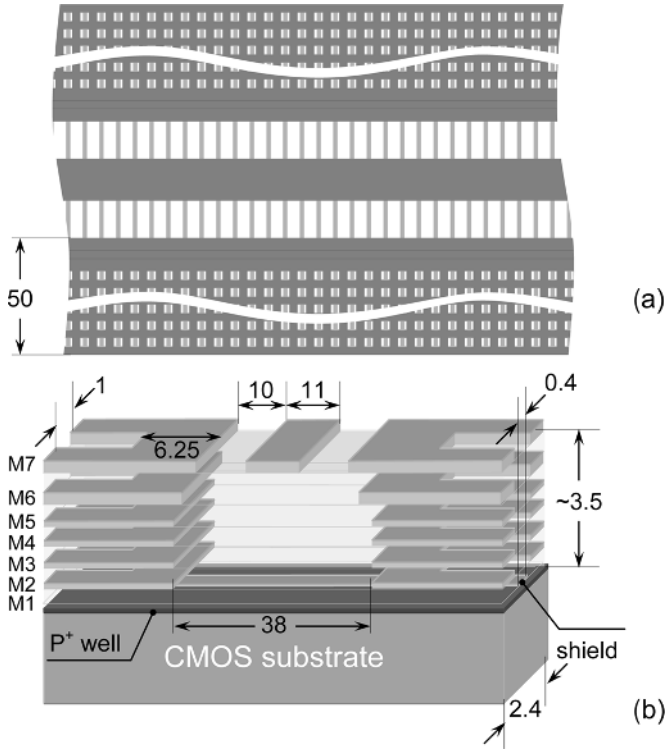

Fig. 11. Geometry of the proposed shielded CPW transmission line: (a) top view; (b) detail of the cross section. Dimensions in μm (drawing not to scale).

in Metal 1, thus obtaining a grounded CPW (G-CPW) [30]. Unfortunately, this solution is not practical in our case, due to the small thickness of the oxide layers between Metal 1 and Metal 7 set by the CMOS process. In fact, a 50 Ω G-CPW designed in our process would have a maximum signal-line width W not much different from that of a MS, and a gap distance much larger than W (the structure would resemble more a MS-line than a G-CPW). In such a structure, a significant amount of longitudinal current would flow in the thinner bottom ground plane (Metal 1) rather than on the thicker top grounds (Metal 7), and the increase in metal losses would completely overwhelm the improvement in attenuation obtained by substrate shielding.

With these limitations in mind we considered a different shielding structure, inspired—to some extent—by the patterned ground used in shielded inductors, consisting of an array of thin metal strips realized in Metal 1, as shown in Fig. 11, and connected to the top ground planes. Actually, this screen can be seen as an equivalent bottom ground-plane with anisotropic resistivity (very high resistivity in the propagation direction, relatively low resistivity in the orthogonal direction), which prevents the flow of longitudinal currents, still providing a good shielding of the substrate.

Metal strips geometry must be carefully optimized to obtain the maximum shielding efficiency, without introducing additional source of losses. As for the slow-wave CPW line, we carried out simulations at 60 GHz, to analyze the effects of metal strip width w_b and periodicity d for $W = 11$ μm, $G = 10$ μm. The results are reported in Fig. 12, which show Q_L and β as a function of the ratio w_b/d for a fixed $d = 2.4$ μm and of d for a fixed value of $w_b/d = 0.17$, respectively. Again, shaded regions correspond to geometries forbidden by design rules. Plots show that the narrower the strips and the shorter the period, the higher Q_L, β being less sensitive to the shield geometry. Characteristic impedance ranges from 49.3 Ω to 52.5 Ω for the geometries considered in the plots.

According to these considerations, we designed and realized a shielded-CPW (S-CPW) with the geometry shown in Fig. 11. After optimization, we chose $W = 11$ μm, $G = 10$ μm, $w_b = 0.4$ μm and $d = 2.4$ μm, in order to maximize Q_L, β and to obtain a 50 Ω characteristic impedance. Note that in this case we were able to design the line for 50 Ω, without violating design rules. The strips were connected to the top ground planes and to the other dummy fills by vias displaced by 27 μm from the structure centerline (for simplicity, vias are not shown in the figure). To better validate the effectiveness of the proposed S-CPW line, P^+ well was generated under the line in order to verify the shielding efficiency in the case where the substrate produces the worst impairment of attenuation.

Fig. 13 shows the good agreement between measured and simulated results. For comparison, also simulation results

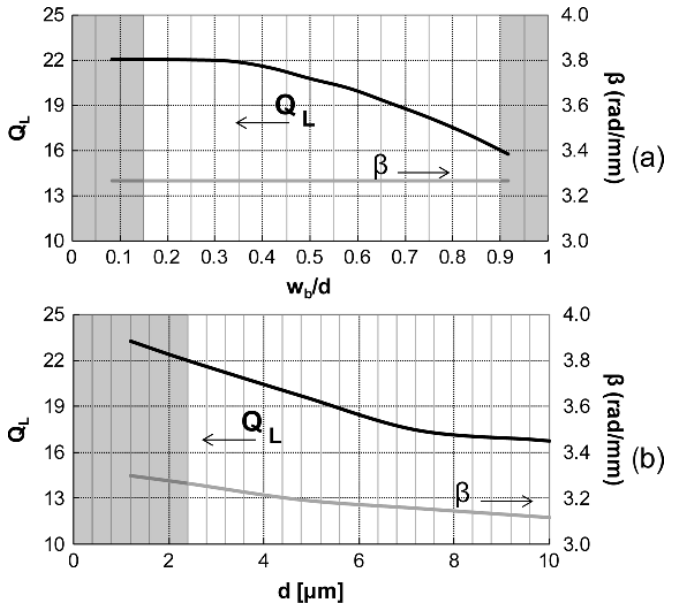

Fig. 12. Quality factor and phase constant of the shielded CPW transmission line at 60 GHz: (a) versus the ratio between strip width and unit cell period w_b/d for $d = 2.4\ \mu$m; (b) versus period d for $w_b/d = 0.17$. Shadowed regions correspond to geometries forbidden by design rules.

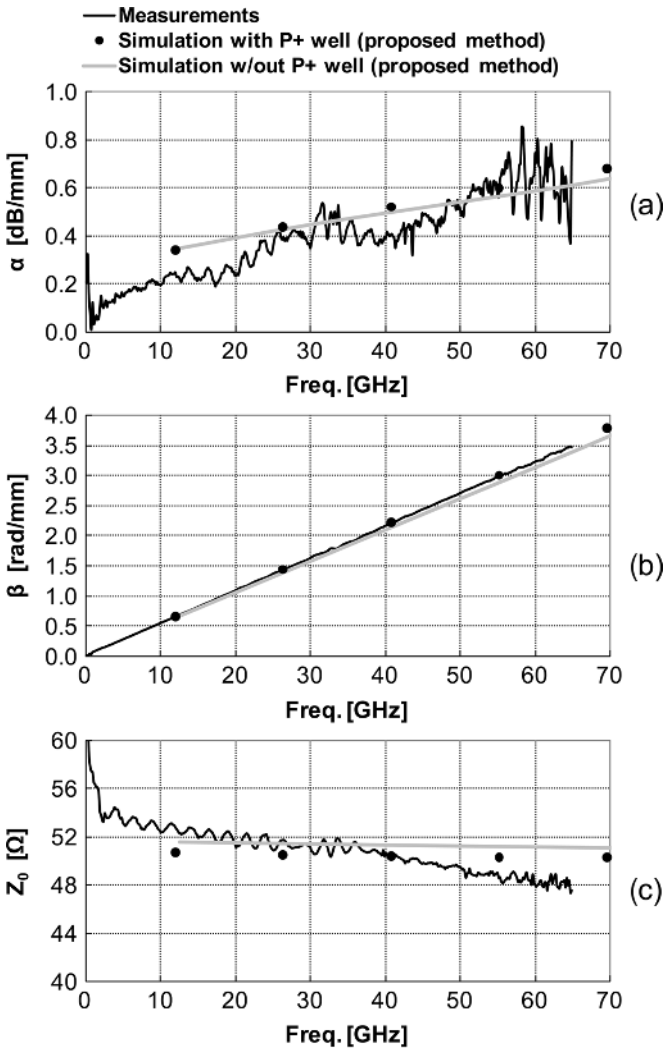

Fig. 13. (a) Attenuation, (b) phase constant, and (c) characteristic impedance versus frequency for the shielded CPW shown in Fig. 10; measurement (—) and simulation with the proposed method (•).

of the S-CPW on a substrate without P^+ well are reported, showing only a marginal improvement in attenuation (about 0.02 dB/mm), thus confirming the high shielding efficiency of the proposed structure). Simulation of the unit cell at one frequency point requires about 300 s and 148 MB of memory. The S-CPW shows an attenuation of 0.65 dB/mm at 60 GHz, i.e., a 30% improvement over standard CPW line. The shield affects also the phase constant of the S-CPW, which is increased by a 25% with respect to CPW. Consequently, the S-CPW features a quality factor $Q_L = 22$ at 60 GHz, a figure almost doubled with respect to the CPW ($Q_L = 12$ at 60 GHz). Note that, to the author's knowledge, the reported attenuation for S-CPW is the best performance ever obtained on a standard bulk 65 nm CMOS process. Additional simulations considering the same shielding structure with substrate contacts under the bottom metal bars show that also in this case line performance remains unaltered, confirming that no return currents flow in the lossy substrate.

IV. Comparison With State of the Art

The developed simulation method proves to be fast and accurate. As previously discussed, 2-D simulators are also accurate and fast, but they can be applied to uniform structures only. On the contrary, 3-D conventional methods not leveraging the periodicity of the line, require a huge amount of computational resources for an accurate result. As a final example, we have simulated the shielded CPW of Section III.C by means of a conventional 3-D simulator. In particular we considered line sections consisting of a variable number of unit cells. Increasing the number of cells, the results of the 3-D method tends to those of our method, of course at the expense of simulation time and required memory. Table I summarizes the results. Note that a conventional 3-D simulation of a line section consisting of 13 unit cells still provides results with an error of more than 6% in the characteristic impedance while requiring tens of minutes and some GB of memory. This suggests that an improved accuracy would require a prohibitive computational effort.

Finally, Table II compares performances of our realized CPW lines versus state of the art of integrated transmission lines of the same 50 Ω characteristic impedance. Noteworthy, although implemented in standard bulk CMOS, shielded CPW are comparable with lines realized in SiGe, SOI and high resistivity CMOS substrates [6], [7], [29]–[32].

V. Conclusion

We believe that the fast and accurate simulation method described in this paper can be very useful for the design of transmission lines for future industrial applications at mm-waves: not only to gain insight in the physical behaviour of complicated structures in order to optimize performances, but also to increase reliability of achieved results. Based on the proposed method, we have characterized several different CPW lines, either useful for a different function, e.g., slow-wave CPW for

TABLE I
COMPARISON BETWEEN 3-D MODAL ANALYSIS AND PROPOSED RESONANT CAVITY MODEL

Number of Unit Cells	Memory [MB]	CPU Time [s]	α @ 60 GHz [dB/mm]	β @ 60 GHz [rad/mm]	Z_0 @ 60 GHz [Ω]
3D Method					
1	85	36	4.00	3.87	40.60
4	830	257	2.83	3.73	42.69
7	1260	466	1.63	3.69	43.41
10	2410	1092	0.70	3.70	42.35
13	3040	1359	0.66	3.54	45.39
Proposed Method					
1	148	300	0.65	3.33	48.70

TABLE II
STATE OF THE ART OF 50 Ω INTEGRATED TRANSMISSION LINE

REF	Technology	Line type	α @ 60 GHz [dB/mm]
[6]	Intel CMOS 90nm High-Resistivity (HR) Substrate	MS	1.2
[6]	Intel CMOS 90nm HR	CPW	0.6
[7]	ST CMOS 90nm BULK	G-CPW	1.1
[31]	ST CMOS 130nm SOI	CPW	0.65
[32]	IBM SiGe 130nm	MS	0.8
[33]	ST CMOS 65nm SOI	CPW	0.7
[34]	ST SiGe 130nm - thick copper metal option	MS	0.5
This work	ST CMOS 65nm BULK	CPW	1
This work	ST CMOS 65nm BULK	Shielded-CPW	0.65

compact solutions, or shielded CPW when minimum attenuation, high Q is a key factor such as in resonators and low noise interconnects.

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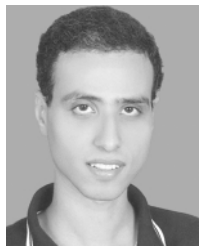

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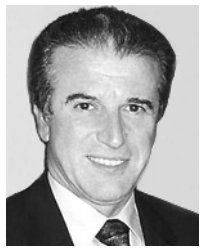
Since 2007 his interests have included CMOS RF design and modeling of passive and active components for millimeter-wave applications. Currently, he has a grant from IUSS–Institute for Advanced Studies–Pavia.



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