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Design of Low Power High Speed Adders Using Modified Self-Resetting Logic

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Abstract: Dynamic CMOS logic families are not an ideal option for low power circuits due to short circuit power dissipation, charge sharing and charge leakage. Self-Resetting Logic (SRL) has been widely preferred to overcome these issues; however it suffers from static power dissipation and low output voltage due to nMOS pull down network makes conductance overlap between nMOS and pMOS. This paper proposes a modified SRL technique which combines sleepy transistor and self-resetting logic to improve the performance of the high speed low power adder circuits. The proposed method is applied in different adder circuits and compared with existing SRL technique in terms of Average power dissipation, Power delay product and Energy delay product. Using modified SRL technique, carry lookahead adder and carry save adder are designed and implemented using 120nm CMOS processing technology. The obtained results show that the modified SRL technique is superior to existing techniques while considering speed and power dissipation of adder circuits.

Key words: CMOS logic · Low power design · Self-resetting logic (SRL) · Sleep Transistor Technique · High speed adders

INTRODUCTION

Static complementary metal oxide semiconductor (CMOS) technology has been the ideal choice of designers in the past years due to its robustness against voltage scaling and transistor sizing [1]. The main drawbacks of static CMOS are high power dissipation and large propagation delay. The high power dissipation is due to the fact that the larger number of pMOS transistors end up with high input loads. The high operating frequency also increases the power dissipation of these circuits. The Pass Transistor Logic (PTL) circuit provides better characteristics while comparing with static CMOS logic. PTL can implement most functions with less number of transistors, thus reducing the overall capacitance that provides faster switching times and low power dissipation [2]. The general issue pertaining to this PTL logic is voltage variation due to threshold drop owing to series resistance between input and output. These concerns motivate the need of dynamic CMOS logic circuits for high speed applications. It offers faster switching speed with reduced load capacitance and requires less number of transistors and occupies less area [3]. However this circuit suffers from charge sharing, charge leakage, loss of noise immunity, timing problem due to clock input and feed through. These issues can be suppressed using an asynchronous dynamic circuit [4] named Self Resetting logic (SRL).

SRL represents signals as short-duration pulses rather than as voltage levels. When a set of pulses are driven to the inputs to a logic gate, they must reach at the same time and they must overlap with one another for a minimum duration. After a logic gate has processed a set of input pulses, a reset signal is activated that restores the logic gate to a state in which it can receive another set of input pulses. Two types of reset structures have been proposed in the litearture. In global SRL [5], the reset signal for each stage is produced by a separate timing chain which yields a parallel worst-case delay path. Individual reset signals are obtained at various tap points along this timing chain in such a way that the reset pulse arrives at each stage only after the stage has completed its evaluation. Very careful device sizing based on extensive simulations over process-voltage-temperature corners are required in order to ensure correct operation. Moreover, any extra delay margin that is designed into the timing chain simply reduces the throughput by a corresponding amount. On the other hand, in locally

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self-resetting CMOS [6], reset signal is obtained by sending the stage's own output signal through a short delay chain. Again, this technique requires very careful simulations and device sizing in order to ensure that the reset signals do not arrive too early. As with the other technique, any timing margin that is built in will directly limit the achievable performance.

SRL circuit operation comprises of separate precharge and evaluation phase that discharges the dynamic storage nodes to evaluate the desired logic function. The nodes are reset back to their original charged state by a local timing. One of the benefits of self-resetting logic is that when the data present at the evaluation phase do not require dynamic node to discharge, which makes the precharge device inactive thereby reducing power [7]. However it suffers from static power dissipation and low output voltage due to nMOS pull down network makes conductance overlap between nMOS and pMOS. Sleep transistor logic along with Multi-threshold CMOS approach is applied to reduce the dynamic and leakage power issues [8].

Many different adder circuits' designs are proposed over last few years with different logic styles. In [9], low power Carry Look ahead Adder (CLA) is designed using domino logic of 150nm channel length is more optimized than other channel lengths. In [10], a sleepy technique or power gating technique is used to reduce the power consumption in the full adder circuit, 4-bit adder and 4-bit binary coded decimal (BCD) adder circuits. In [11], the high speed adder circuits designed in Self resetting logic are re-configured thereby the number of transistors in the modified design is reduced. Advantage of our modified combined SRL and Sleepy technique circuits compared to all the existing designs in self-resetting logic are that the Average power consumption is reduced. In this paper, we propose a modified SRL technique that combines SRL with ST Technique to design low power and high speed CLA and carry save adder circuits.

This paper is organized into six sections. Section 2 presents the existing SRL and ST techniques. Section 3 discusses the different adder circuits. Section 4 describes the proposed technique. Simulation results are discussed in section 5 and finally, section 6 concludes the paper.

Self Resetting Logic and Sleep Transistor Techniques: Self-resetting logic is a commonly used piece of circuitry that automatically precharge themselves (i.e., reset themselves) after a prescribed delay. They find applications where a small percentage of gates switch in a cycle, such as memory decoder circuits [12]. It is a form of logic in which the signal being propagated is buffered and used as the precharge or reset signal. By using a buffered form of the input, the input loading is kept almost as low as in normal dynamic logic while local generation of the reset assures that it is properly timed and only occurs when needed.

A generic view of a self-reset logic is shown in Fig 1. In the domino case, the clock is used to operate the circuit. In the self-resetting case, the output is fed back to the precharge control input and, after a specified time delay, the pull-up is reactivated. There is an NMOS sub block where the logic function performed by the gate is implemented which is represented as NMOS_LF through which the input data's are loaded. The output of the gate F provides a pulse if the logic function becomes true. This output is buffered and it is connected to PMOS structure to precharge. The delay line is implemented as a series of inverters.

The signals that propagate through these circuits are pulses. The width of the pulses must be controlled carefully or else there may be contention between NMOS and PMOS devices, or even worst, oscillations may occur.

One of the advantages of self-resetting logic is that when data present at evaluation does not require dynamic node to discharge, the precharge device is not active hence reduces power. In the circuit MP, MR and VSGR represent the precharge pull-up, reset pull-up and gate-source voltage of resetting transistor. During precharge phase clk=0, the transistor MP turns ON and the pull down network is OFF. Therefore the capacitor is charged to VDD. During evaluation phase clk=1, the transistor MP turns OFF and the pull down network is ON and evaluates the logic function. Therefore the capacitor is discharged making MR active which allows IDR to flow and recharge CX back up to a voltage of Vx=VDD.

The most natural way of lowering the leakage power dissipation of a VLSI circuit in the STANDBY state is to turn off its supply voltage. This can be done by using two PMOS transistor or two NMOS transistor in series with the transistors of each logic block to create a virtual ground and a virtual power supply as depicted in Fig 2. Notice that in practice only one transistor is necessary. The circuit operates in two different modes are Active and Sleep modes. In the sleep mode, the sleep transistors are turned OFF to reduce the leakage power. In the active mode, the sleep transistors are turned ON and can be treated as the functional redundant resistances, as circuit is in operation mode the power leakage should not be more than the basic full adder. When a sleepy transistor is placed at VDD, it is called as the "Header switch" and

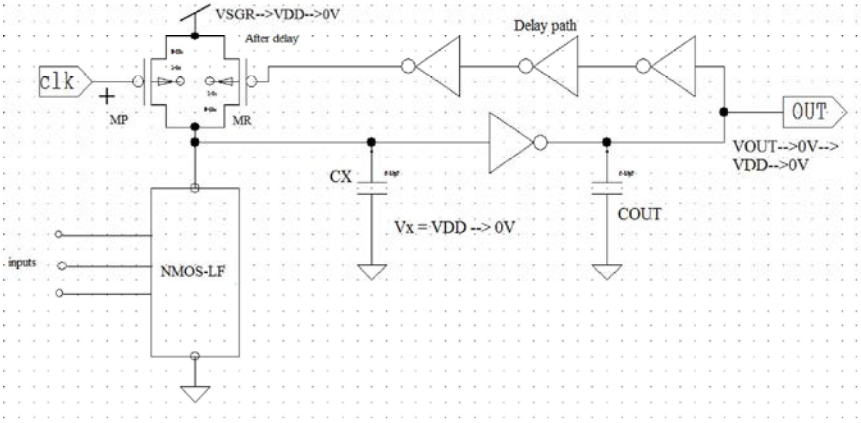

Fig. 1: Structure of Self Resetting Logic

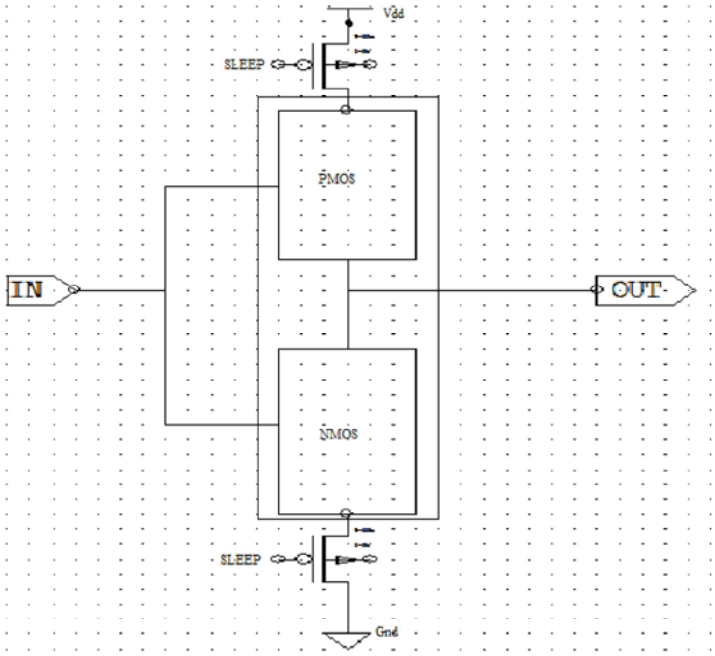

Fig. 2: Structure of Sleep Transistor Technique

while it is placed near the ground, it is called as "Footer switch". The Header and Footer transistor are used to disconnect the Vdd and Gnd connects to the main circuit which puts main circuit in sleep mode when the circuit in STANDBY state. SLEEP signal is used to turn ON the Header and footer and to put main circuit in Sleep mode. NMOS transistors are usually preferred, Because of their lower on-resistance, [8].

High Speed Adder Circuits

Carry Skip Adder: A carry-skip adder (CSkA) consists of a simple ripple carry-adder with a special speed up carry chain called a skip chain. Carry skip adder is a fast adder compared to ripple carry adder when addition of large number of bits take place; carry skip adder has very less delay provides a good compromise in terms of delay, along with a simple and regular layout This chain defines the distribution of ripple carry blocks, which compose the skip adder. A carry-skip adder is designed to speed up a wide adder by aiding the propagation of a carry bit around a portion of the entire adder. Actually the ripple carry adder is faster for small values of N. The crossover point between the ripple-carry adder and the carry skip adder is dependent on technology considerations and is normally situated 4 to 8 bits. The carry-skip circuitry consists of two logic gates. The AND gate accepts the carry-in bit and compares it to the group propagate signal.

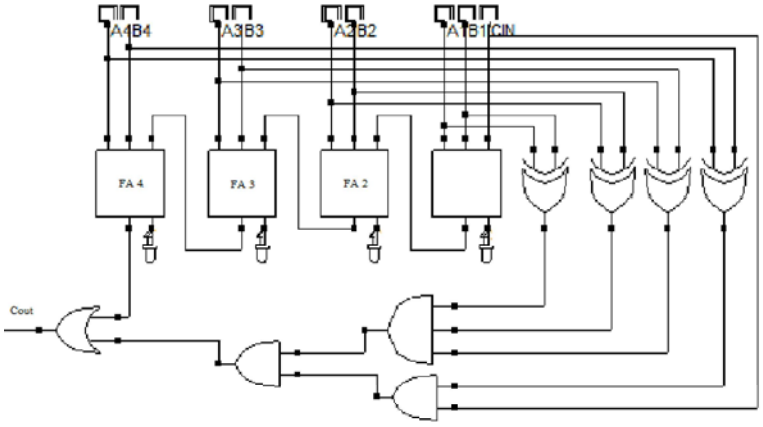

Fig. 3: Logic diagram of Carry Skip adder

$$P [i, i + 3] = (pi + 3)*(pi + 2)*(pi + 1)* pi \quad (1)$$

Using the individual propagate values. The output from the AND gate is ORed with Cout of RCA to produce a stage output of Carry.

$$Carry = ci + 4 + p [i, i + 3] * ci \quad (2)$$

If p [i, i + 3] =0, then the carry-out of the group is determined by the value of ci + 4.

However, if p[i, i + 3] =1 when the carry-in bit is ci =1, then the group carry-in is automatically sent to the next group of adders. The design schematic of Carry Skip Adder is shown in Fig 3.

Carry Look Ahead Adder: The propagation delay occurred in the parallel adders can be eliminated by CLA. This adder is based on the principle of looking at the lower order bits of the augends and addend if a higher order carry is generated. This adder reduces the carry delay by reducing the number of gates through which a carry signal must propagate. This adder consists of three stages: a propagate block/generate block, a sum generator and carry generator.

The generate block can be realized using the expression

$$Gi = Ai*Bi \quad \text{for i=0, 1, 2, 3} \quad (3)$$

Similarly the propagate block can be realized using the expression

$$Pi = A \text{ XOR } B \quad \text{for i=0, 1, 2, 3} \quad (4)$$

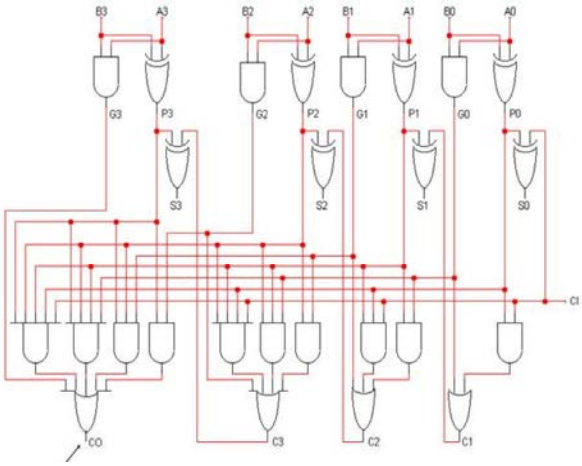

Fig. 4: Logic diagram of Carry Lookahead adder

The carry output of the (i-1) th stage is obtained from

$$Ci (Cout) = (Gi + Pi)*Ci-1 \quad \text{for i=0, 1, 2, 3} \quad (5)$$

The sum output is obtained using

$$S= (A \text{ XOR } B)*Ci-1 \quad \text{for i=0, 1, 2, 3} \quad (6)$$

The 4-bit modified carry look ahead adder with the primitive gates and output of the adder are processed with 120nm CMOS processing technology, with VDD = 5V are shown in Fig. 4.

Proposed Logic: Self-resetting circuitry automatically reset them after a specific delay by conditionally charging the dynamic nodes to assess the preferred logic function using a local feedback timing chain instead of a global clock. Even though this SRL

circuit exhibits lot of merits, it still suffers from static power dissipation due to the nMOS logic structure. As stated earlier, during precharge the nMOS stack is completely open and the output is fed back to the pMOS block to charge the capacitor. During this period the nMOS transistors operate in cut-off region shows sub-threshold current. In a complex circuitry we could be able to separate a part of circuit from main circuit by combining ST technique with SRL which will reduce the power consumption. The Header and Footer transistor are used to disconnect the V_{DD} and GND connects to the main circuit which puts main circuit in sleep mode. In this paper, we propose a modified SRL technique that combines SRL with ST Technique to design low power and high speed CLA and carry save adder circuits. Proposed adders using the modified SRL technique consumes less power and exhibits minimum power delay product while comparing with existing SRL designs.

RESULTS AND DISCUSSION

The simulation output, observed power consumption, Energy delay product (EDP) and Power delay product (PDP) are presented in this section. Using modified SRL technique, Carry lookahead adder and carry save adder are simulated using Tanner tool, designed and implemented using 120nm CMOS processing technology. Figures 5 and 6 show the simulation results of 4-bit CSkA and 4-bit CLA. The different parameters of high speed adders are compared in this paper. Table 1 compares the proposed CSkA with existing technique and Table 2 compares the proposed CLA with existing CLA. Power consumption of proposed Carry Skip adder is reduced by 51.7% when compared with SRL based Carry skip adder. The PDP and EDP are improved by 59.7% and 52.1% respectively. From Table 2, the proposed CLA in sleep mode reduces the power consumption, PDP and EDP by 54.9%, 59.3% and 62.9% respectively.

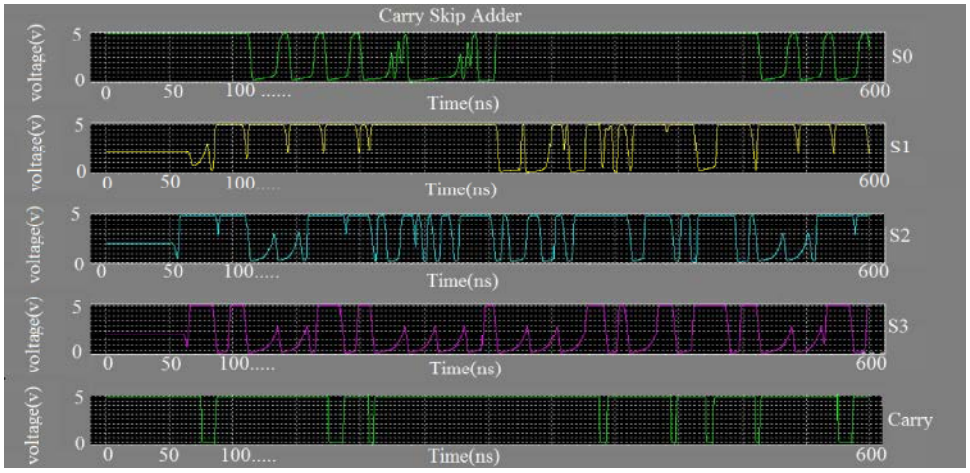

Fig. 5: Simulation of proposed Carry Skip adder

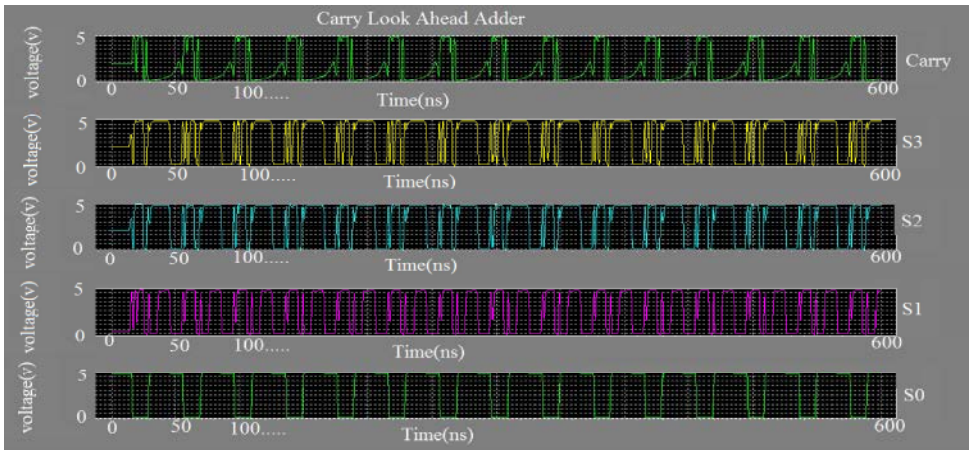

Fig. 6: Simulation of proposed Carry Look ahead adder

Table 1: Comparison of Different 4-bit CSkA

Parameter Technique	Power (mW)	PDP (pWS)	EDP (fWS^2)
CskA Adder	48.01	125.50	3.28
Proposed CSkA	41.01	119.02	3.17
Proposed CSkA (Disconnecting 1 FA)	32.69	99.43	3.03
Proposed CSkA (Disconnecting 2 FA)	23.88	72.56	2.21
Proposed CSkA (Disconnecting all FA)	16.97	51.50	1.57

Table 2: Comparison of Different 4-bit CLA

Parameter Technique	Power (mW)	PDP (pWS)	EDP (fWS^2)
CLA adder	51.42	118.57	3.54
Proposed CLA (Active Mode)	31.14	110.40	2.64
Proposed CLA (Sleep Mode)	23.29	48.85	1.31

CONCLUSION

The proposed method has been applied in different adder circuits and compared with existing SRL technique in terms of Average power dissipation, Power delay product and Energy delay product. Using modified SRL technique, carry lookahead adder and carry save adder are designed and implemented using 120nm CMOS processing technology. By combining the SRL with Sleepy technique, the power consumption of high speed adder circuits will reduce gradually. Hence it is concluded that the proposed design of combined Self resetting logic and Sleepy technique will provide effective way to reduce the power consumption in dynamic CMOS logic circuits. The obtained results show that the modified SRL technique reduces the power consumption of 51.7% and 54.9.3% in CSkA and CLA respectively.

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