Design of Low Power Multiplier With Less Area Using Quaternary Carry Increment Adder for New-Fangled Processors

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Research Article

Keywords: Quaternary Signed Digits, Carry Increment Adder, Multiplier and Low power.

Posted Date: August 10th, 2021

DOI: https://doi.org/10.21203/rs.3.rs-760248/v1

Abstract

Multiplication is one of the basic functions in Digital Signal Processing (DSP) applications. Multiplier plays an important role in Arithmetic and Logic Unit (ALU), which is a critical element in the processors. The efficiency of the multiplier takes part a crucial task in the execution of the processor. The performance of the multiplier depends on the adder circuit. The addition operation is the fundamental operation used in most of the digital circuits. Power, delay and area are the main issues in VLSI circuits. Efficiency of a VLSI circuit can be improved by rectifying any of these issues. Quaternary Signed Digits (QSD) placed on adders have better efficiency when compared to traditional binary logic. QSD based Carry Look Ahead (CLA) Adder is used to increase the efficiency with reference to power and delay. The proposed method uses Quaternary Carry Increment Adder in order to improve the power and reduce the delay of the existing Quaternary Carry Look Ahead Adder. Tanner EDA is the simulation tool used to design the circuits and the power, delay and power-delay product of the designed circuits are measured using it.

I. Introduction

Very Large Scale Integration (VLSI) summons the integration or embedding millions of transistors on a single silicon semiconductor microchip [1]. VLSI technology come up with the year 1970s when advanced level computer processor microchips were under development. The microprocessor is a VLSI device. A system on a chip is an Integrated Circuit (IC). Likewise, an electric circuit consists of CPU, RAM, ROM and other glue logic. In a single chip, VLSI let all the IC designs to be added. The theme that requires packing more and more logic devices into smaller and smaller areas [2].

The main factors affecting VLSI designs are power dissipation, delay and area. Power dissipation are often stated with the merchandise of total current supplied to the circuit and thus the entire voltage loss or leakage current [3]. When it involves portability of devices, power loss is that the main restriction. The total power dissipation can be expressed as the sum of three main components [4]. Hence, it is necessary to require the system's total electric power consumption. Minimizing the general power utilization in such devices is important since it is important to take lead of the run time with minimum feasible specifications on weight, battery life and size owed to batteries. As a result, in compact devices, the low power design is that the most determining factor to mediate while designing system on chip [5]. Conventionally, mobile users request supplementary attributes and extended battery life at an economical price.

Multipliers play a vital role in various digital signal processing and many other applications. Many researchers, with evolution in technology have already tried and are still endeavouring to design multipliers which furnishes either greater speed, less power consumption, regularity of layout and consequently with small area or even combination of them in one multiplier which makes them appropriate for several increased speed, decreased power and compact VLSI implementation [6]. Multiplication is the utmost working in at most all DSP applications. Multiplier speed defines the digital

signal processor speed in a processor. Multiplication is an important vital function in arithmetic operations. Multiplication related operations to the digital signal processing, such as filters, convolutions, Fast Fourier Transform (FFT) are implemented whereas in microprocessor, it is arithmetic and logic units. As multiplication subordinates the execution time for many DSP algorithms so there is a requirement of high-speed multiplier [7].

In digital combinational circuits, an array multiplier is used for multiplying two binary numbers by utilizing an array of full adder and half adder. This type is used for almost simultaneous addition of the several product terms concerned [8]. Array architecture is a prominent technology to execute these multipliers due to its regular compact structure. High power dissipation in these designs is mainly due to its shifting of a large numbers of forged transistors on internal nodes. In array multipliers, the basic building block is the timing analysis of a full adder that has been ensued in a discrete array connection pattern, which decreases power dissipation caused by the transition activity [9].

The objective of the proposed idea is to design a multiplier with quaternary carry increment adder by reducing the factors like power and area. In continuation of the paper, existing system is discussed in Sect. 2, followed by in Sect. 3 is about the proposed system, Sect. 4 is about the result as well as discussion, and finally Sect. 5 is about the conclusion of the work carried in this paper.

Ii. Existing Method

Higher radix number system like Quaternary Number System can be used to perform carry free addition. They can also be used to perform subtraction without borrow, multiplication and division [10]. Numbers that can be represented in QSD are -3, -2, -1, 0, 1, 2 and 3. The number 0, 1, 2, 3 are used to represent real numbers. The carry propagation and formation are increased when the number of bits are increased which leads to increase in delay, power and area [11]. This problem in the binary circuits can be overcome by using the number system having higher radix than binary number system. When compared with binary more states can be represented by quaternary because of its higher radix. With help of the higher radix, the number of interconnections in the circuits can be reduced [12]. As the interconnections are reduced, the complexity of the circuit is minimized. This leads to increase in speed of the circuits.

The most important task is to upturn the input signal applied. Whether the bidden input is low then the output becomes high and vice versa. Inverters can be forged using a one NMOS transistor or a one PMOS transistor combined hereby with a resistor. In different logic circuits, Quaternary inverter plays a major role. Input signal is enhanced utilizing inverter function. Totally six CMOS transistors are required for the designing the quaternary inverter [13].

The combination of inverter with AND gate forms NAND gate, or the AND gate is form by applying inverter at the output of NAND gate. The AND performance sets the output of the AND circuit to be the truncated value of several inputs. The execution of the NAND circuit with two quaternary inputs [14]. The circuit is actually created on the inverter circuit and a regular binary NAND circuit. An input set to zero will bring about the output of 3V in any case of the other input voltage level. The NMOS transistors

inclined in series construct the tracks to 1V, 2V, and ground to be opened only when both inputs are equal to or higher than the V_t of both transistors. PMOS transistors are at the helm of to close the path when both inputs are higher than their V_t values [15].

In case of OR gate the output sets to the highest of the input value. Opposite is the function of NOR gate i.e. NOR is the inversion of OR gate. So, the combination of inverter with OR gate forms NOR gate, or the OR gate is form by applying inverter at the output of NOR gate.

The normal Carry Look Ahead logic is used to design the Quaternary gates. The only difference is the instead of binary logic gates. Quaternary logic gates are used. The same propagate and generate logic of binary Carry Look Ahead. Carry Look Ahead generated in order to generate carry every other bit with the help of the input carry C_{in}. The output of the generate is given to carry look ahead generated for carry generation [16]. Then XOR gates are used the propagate and carry to generate the output as in figure 3.4. This quaternary adder can be used to perform fast addition than binary CLA due to lesser number of interconnections. The power consumption of the adder is also reduced. The formula are as follows

$$P_i = A_i \oplus B_i \quad (2.1)$$

$$G_i = A_i . B_i \quad (2.2)$$

$$C_i = P_i \oplus Gi \quad (2.3)$$

$$S_i = P_i \oplus Ci \quad (2.4)$$

The array multiplier is used here. The basic component of the multiplier is adder. An N bit array multiplier requires N-1 adder. Array Multiplier is a structured layout of a combinational multiplier. Since QSD multiplier can be handed down as a building block for all arithmetic operations, it can be implemented for building of a high performance multiprocessor [17]. So, it can be constructed easily. It relies on the preceding partial sum generated for the computation of the output device. There are typically two procedures for a multiplication operation that is parallel and iterative. QSD multiplication can be executed in duo ways requiring a QSD partial product generator and QSD adder as a primary component.

Iii. Proposed Work

In the proposed system, the quaternary CLA replaced with the 8-bit quaternary Carry Increment Adder in order to minimize the power consumption and area of the existing system. Two quaternary inputs X and Y are given as inputs and the output is obtained as Sum and Carry as shown in figure 3.1. The half adder consists of QSD XOR and QSD AND gates for generating sum and carry respectively.

The quaternary full adder is constructed utilizing quaternary half adders. The additional input Carry (C_{in}) is used for the completion of the full adder. The carry digit and two quaternary digits are sum up by this circuit. This circuit generates quaternary sum and quaternary carry as shown in the figure 3.2. In order to implement carry free addition, the carry in for the adder circuit restricted to values upto 1, that is, the carry can be either 0 or 1 as in binary number system. Execution of circuit is clarified by this assumption [18]. Two QSD Half adder circuits and one QSD OR gate are required for the design of the full adder circuit as shown in figure 3.2. It is same as that of designing the conventional full adder circuit. Three inputs X, Y and Carry in (C_{in}) are given as the input and the sum and carry are obtained as the outputs.

The Ripple Carry Adder (RCA) and an incrementor block form the traditional Carry Increment Adder (CIA), which is shown in the figure 3.3. Half adder circuits are used as incrementor circuit in the Carry Increment Adder sequentially. The total bits are divides into several 4 bits and then 4-bit Ripple Carry Adders perform the addition operation. The adders perform only one partial addition and the sum is increased if it is required, this eliminates the need for calculating two partial sums and choosing the exact one.

The 8-bit Quaternary CIA is made up of an incremental circuit block and two 4-bit Quaternary RCA as shown in figure 3.4. Four bits of LSB are added with the help 4 bit Quaternary RCA which produces sum and carry. The carry produced in the first block is used as C_{in} for the incrementor block. Similarly, the second four bits are added with the help of 4 bit Quaternary RCA. The partial sum that is produced by the second block is used as input for the incrementor circuit. The two 4 bit Quaternary RCAs adds the number in parallel manner since the C_{in} of the circuits are given as 0. The incremental block produces same output when the carry from the first Quaternary RCA block is 0 and increments the output by 1 when the carry from the first Quaternary RCA block is 1.

The same array multiplier, which is used in the existing method, is used. Only the adder part is changed. The Carry Look Ahead Adder is replaced with the Carry Increment Adder for the better performance of the multiplier. The 8X8 array multiplier have the ability of multiplying two 8-bit quaternary numbers. The power consumption of the circuit is reduced since ripple carry adder is used in place of carry look ahead adder. The number of transistors used in the circuit is also reduced. The efficiency if the design is increased. The Power Delay Product of the design is also improved.

Iv. Result And Discussion

The circuits that are designed with the help of Tanner EDA tool in S-Edit using 250nm technology are simulated. The output of the designed circuits is obtained in the W-Edit. The inputs that are given to both the designs are shown in the figures 4.1, 4.2, 4.3 and 4.4.

The design consists of 16 inputs, that is, 8-bit multiplicand and 8-bit multiplier in order to produce 16-bit output. Two different sets of the inputs are given to the circuits.

The first set of the input as follows

8 bit Multiplicand, A [7:0] = 00000000

8 bit Multiplier, B [7:0] = 00000000

The second set of the inputs are as follows

8 bit Multiplicand, A [7:0] = 11111111

8 bit Multiplier, B [7:0] = 11111111

The inputs shown in the figures 4.1, 4.2, 4.3 and 4.4 are given to quaternary CLA multiplier and the results are obtained as waveforms in W-Edit.

The outputs for the quaternary CLA multiplier are obtained and they are shown in the figures 4.5, 4.6 and 4.7.

The output for the first set of the input as follows

8 bit Multiplicand, A [7:0] = 00000000

8 bit Multiplier, B [7:0] = 00000000

16 bit Product, M [15:0] = 0000000000000000

The output for the second set of the inputs are as follows

8 bit Multiplicand, A [7:0] = 11111111

8 bit Multiplier, B [7:0] = 11111111

16 bit Product, M [15:0] = 1111111000000001

The glitches can be seen in the outputs, this is due to parallel inputs given to the adders in the circuit. Further works are need to be done in order to remove these glitches.

The inputs shown in the figures 4.1, 4.2, 4.3 and 4.4 are given to quaternary CIA multiplier and the results are obtained as waveforms in W-Edit.

The output for the quaternary CIA multiplier is obtained and it is shown in the figures 4.8, 4.9 and 4.10.

The output for the first set of the input is shown below

Inputs:

8 bit Multiplicand, A [7:0] = 00000000

8 bit Multiplier, B [7:0] = 00000000

Output:

16 bit Product, M [15:0] = 0000000000000000

The output for the second set of the inputs is shown below

Inputs:

8 bit Multiplicand, A [7:0] = 11111111

8 bit Multiplier, B [7:0] = 11111111

Output:

16 bit Product, M [15:0] = 1111111000000001

The glitches can be seen in the outputs, this is due to parallel inputs given to the adders in the circuit. Further works are need to be done in order to remove these glitches.

Table 4.1 Comparison table between Quaternary CLA and CIA multipliers

Performance metrics	Quaternary CLA multiplier	Quaternary CIA multiplier	Percentage
Power (milli watts)	104.18	89.76	13.84
Delay (nano second)	1.298	1.317	1.44
Power Delay Product (pico watt seconds)	135.22	118.21	12.57
No. of transistors	14616	11736	19.7

The table 4.1 compares the results of the Quaternary CLA Multiplier with Quaternary CIA Multiplier with reference to power, delay, Power Delay Product (PDP) and number of transistors used for the construction of the design. The transient analysis is done using the Tanner EDA with 250nm technology.

From the table 4.1, it is said that the proposed Quaternary CIA has low power consumption. The Quaternary CLA multiplier consumes power of about 104.18 mW whereas, the Quaternary CIA multiplier consumes 89.76 mW which 13.84% less than it consumes the former. This is due to the minimization of the number of gates used in the proposed method. As the number of transistors is reduced, the switching activity during the working of the design is reduced. Dynamic power of the circuit depends on the switching activity. Since the switching activity is reduced, the dynamic power dissipation of the circuit is reduced.

As per the table 4.1, the worst-case delay in obtaining for Quaternary CLA multiplier is 1.298 ns but the Quaternary CIA multiplier has a delay of 1.317ns, which is 1.44% higher when compared with the existing. This is due to the usage of Ripple carry adder in the Carry Increment Adder. However, the Ripple Carry Adder produce more delay due to carry propagation, the delay is reduced when compared to conventional RCA. This is due to the usage of RCA as parallel blocks in the Carry increment Adder so that, the carry propagation delay can be reduced.

The table 4.1 shows that the Power Delay Product of the proposed is 12.57% lesser then the existing method. Thus, the efficiency is improved in the Quaternary CIA multiplier. The number transistor count in the proposed is also 19.7% less than the existing method, which leads to the lesser area than the Quaternary CLA multiplier.

V. Conclusion

In this paper, we proposed a Carry Increment Adder by using QSD number system in order to replace Quaternary Carry Look Ahead Adder in array multiplier circuit. In VLSI, power consumption, delay and area are the factors determining the efficiency of the design. Tanner EDA tool with 250 nm technology is used for the simulation of the circuits and the above-mentioned analysis are done. These analyses are also done for the existing Quaternary Carry Look Ahead Adder multiplier and the results are compared. The QSD offers carry free addition, which minimizes the carry propagation delay that occur during binary arithmetic. This enhances the speed of the Quaternary Carry Increment Adder. Quaternary Carry Increment Adder has a lower power consumption and occupies lesser area than the existing method. This is because, the number of transistors present in the proposed method is lesser than the existing Quaternary Carry Look Ahead Adder multiplier. From the results, we come to know that the PDP of the proposed method is 12.57% reduced proving that the proposed is more efficient. In future works, the area of the designed circuits can ne improvised.

In future, the multiplier with Quaternary Carry Increment adder can be used to develop ALU, Processors, filters, etc. The delay of the Quaternary Carry Increment adder can be improvised.

Declarations

Funding – Not Applicable

Conflicts of interest/Competing interests

The authors whose names are listed immediately certify that they have NO affiliations with or involvement in any organization or entity with any financial interest or non-financial interest in the subject matter or materials discussed in this manuscript.

Availability of data and material – Not Applicable

Code availability – Not Applicable

Authors' contributions – All authors are equally contributed

Ethics approval - Agreed

Consent to participate – Yes

Consent for publication - Yes

DATA AVAILABILITY STATEMENT

Data sharing is not applicable to this article as no datasets were generated or analyzed during the current work.

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Figures

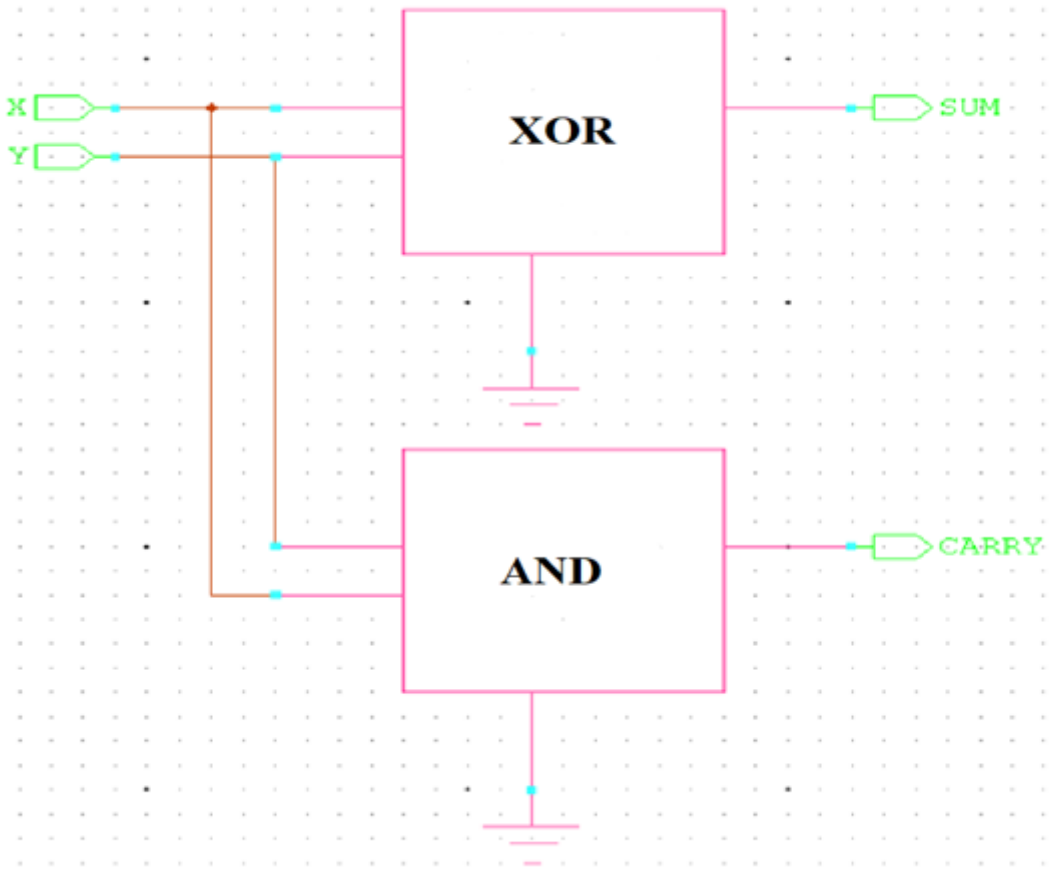

Figure 1

Tanner design of QSD half adder

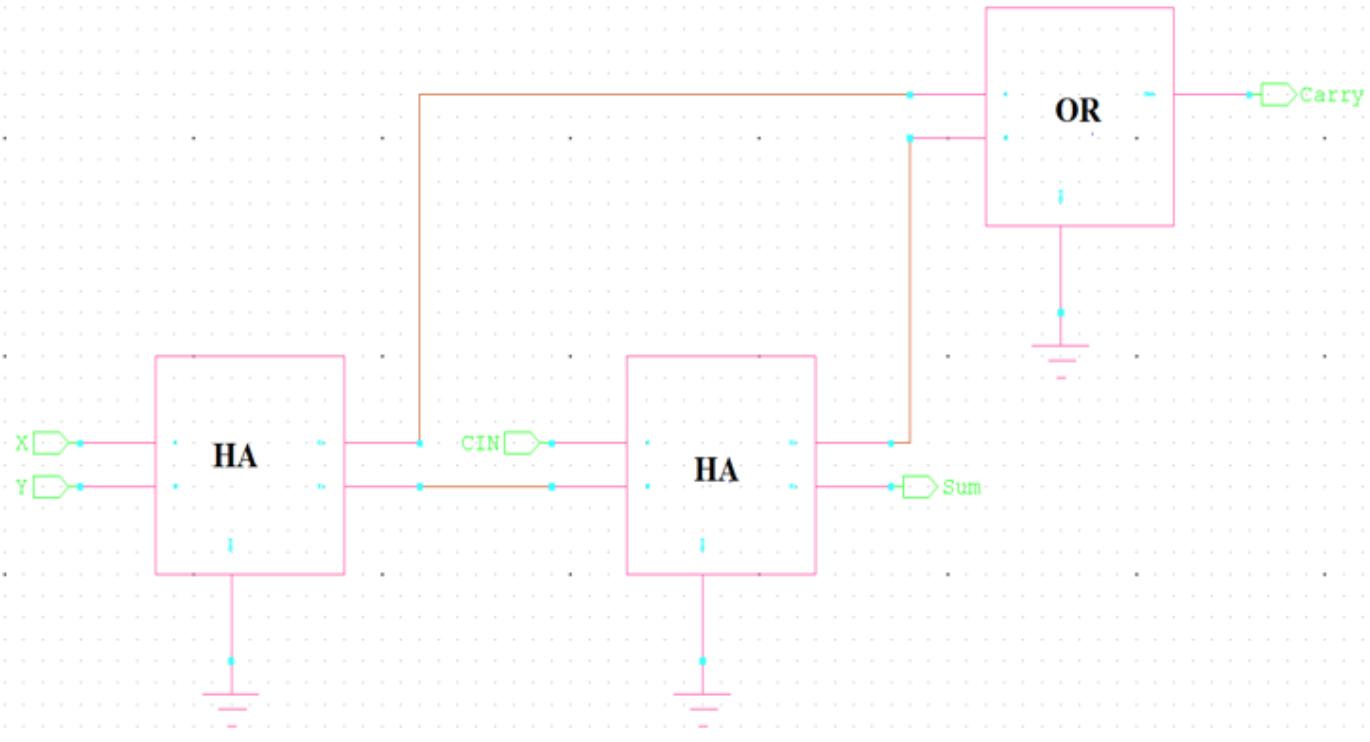

Figure 2

Schematic diagram of QSD full adder

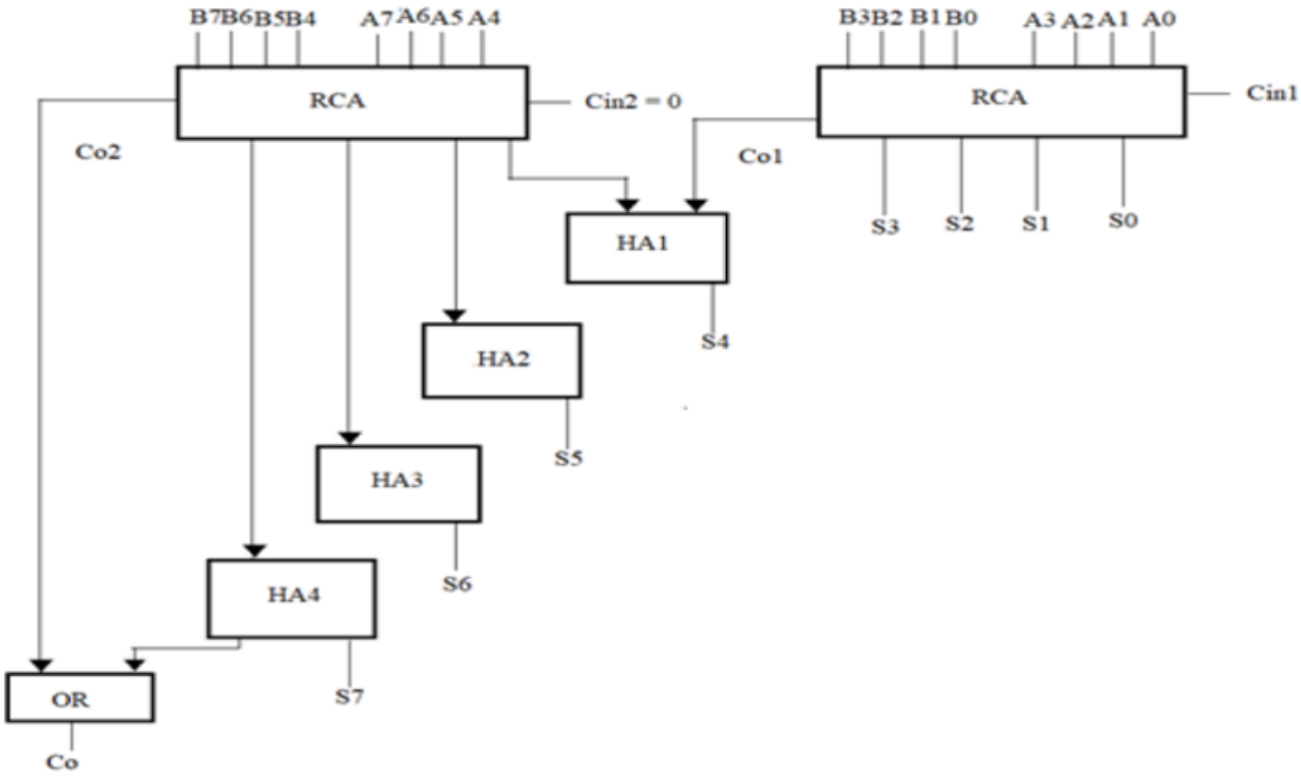

Figure 3

Block diagram of Quaternary CIA

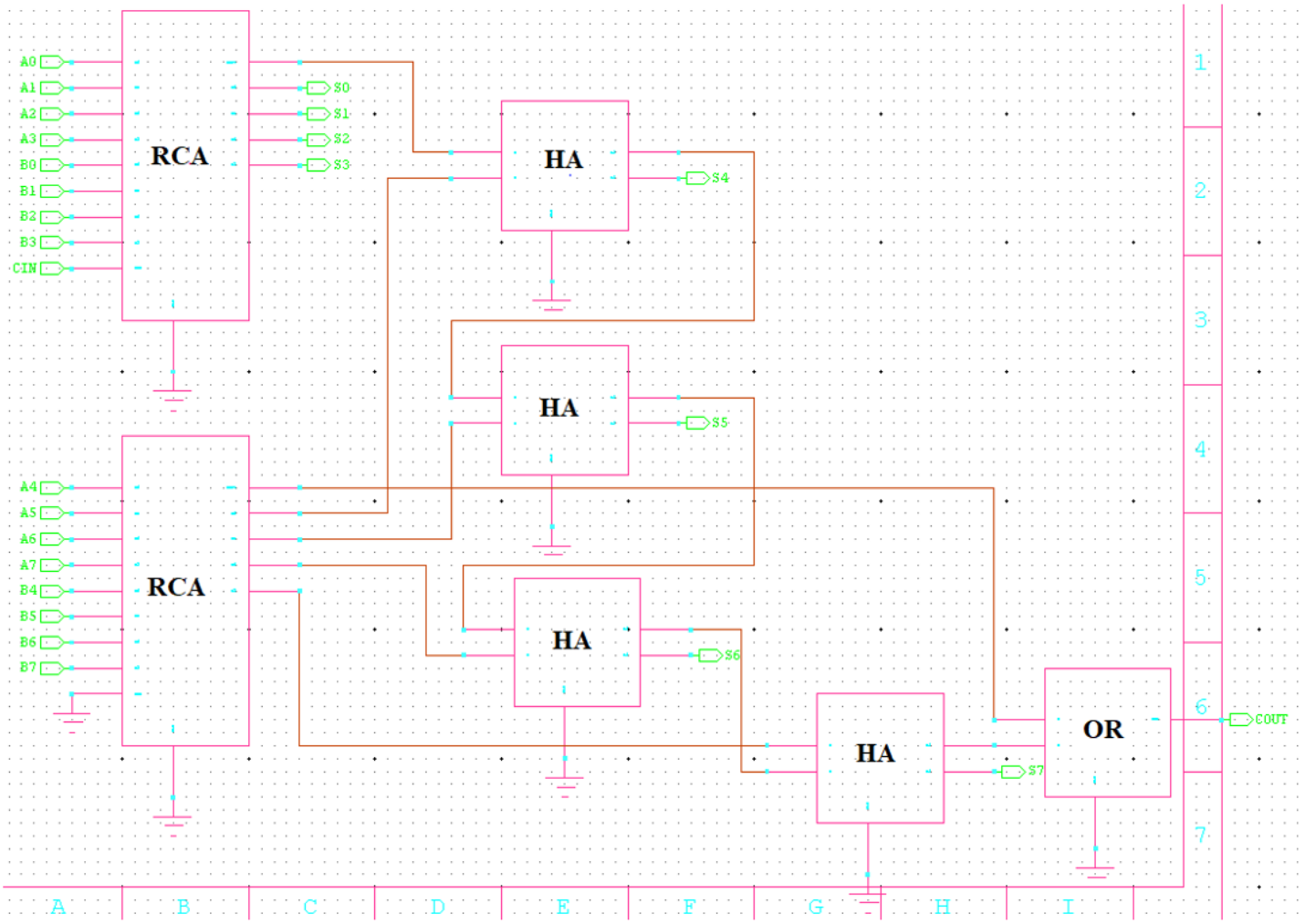

Figure 4

Schematic of 8 bit Quaternary CIA

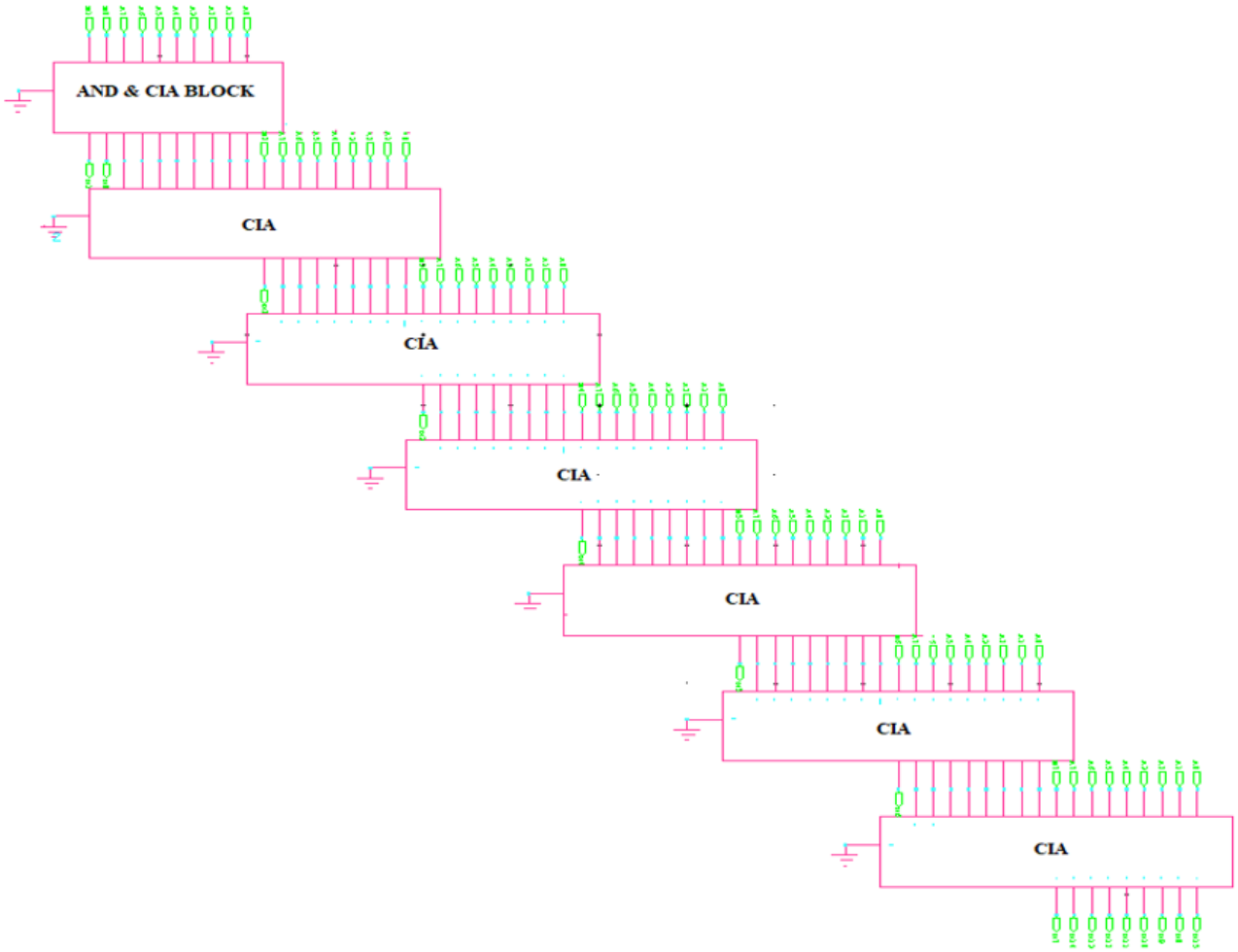

Figure 5

Tanner design for Quaternary CIA multiplier

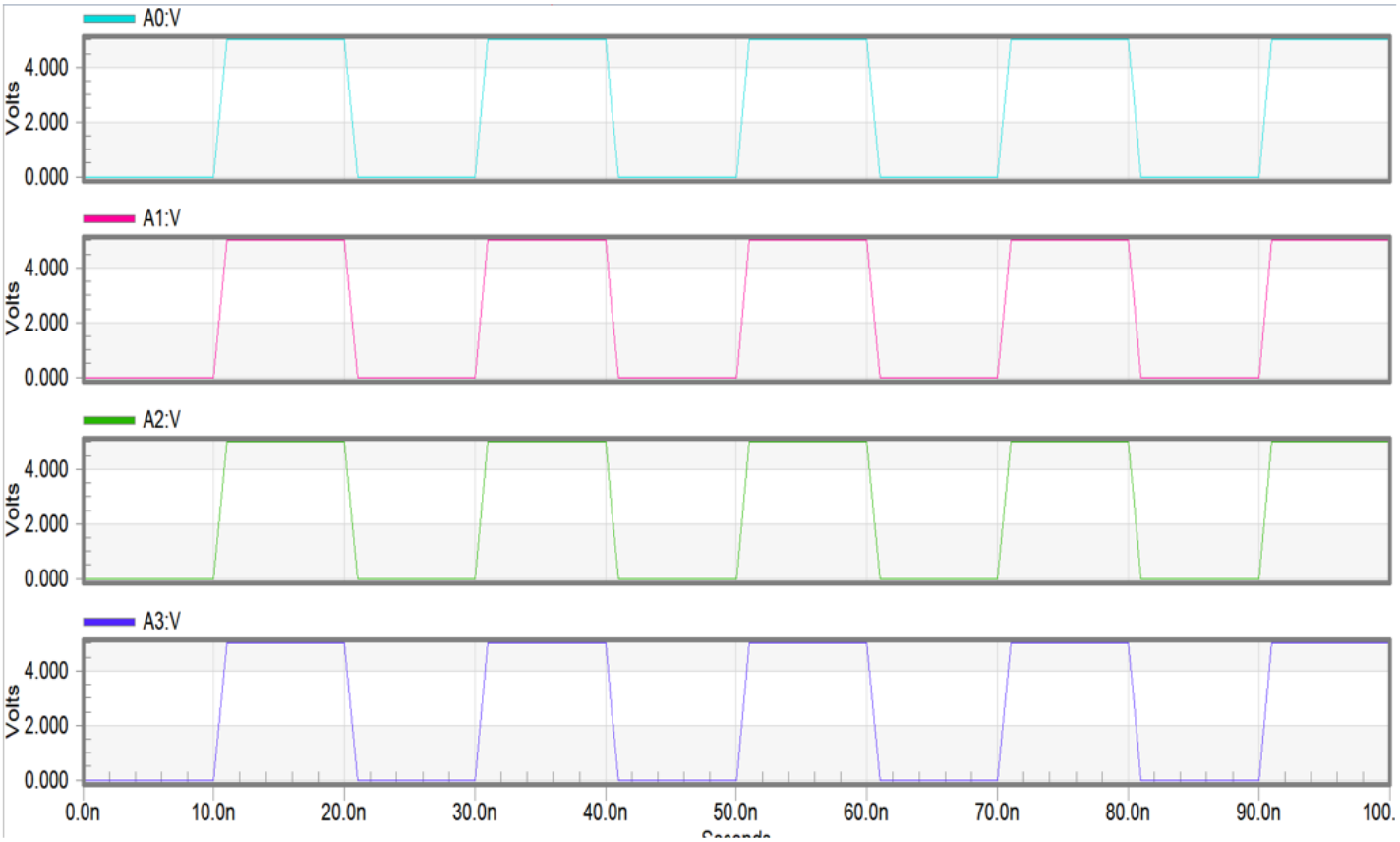

Figure 6

8-bit Input A0-A3

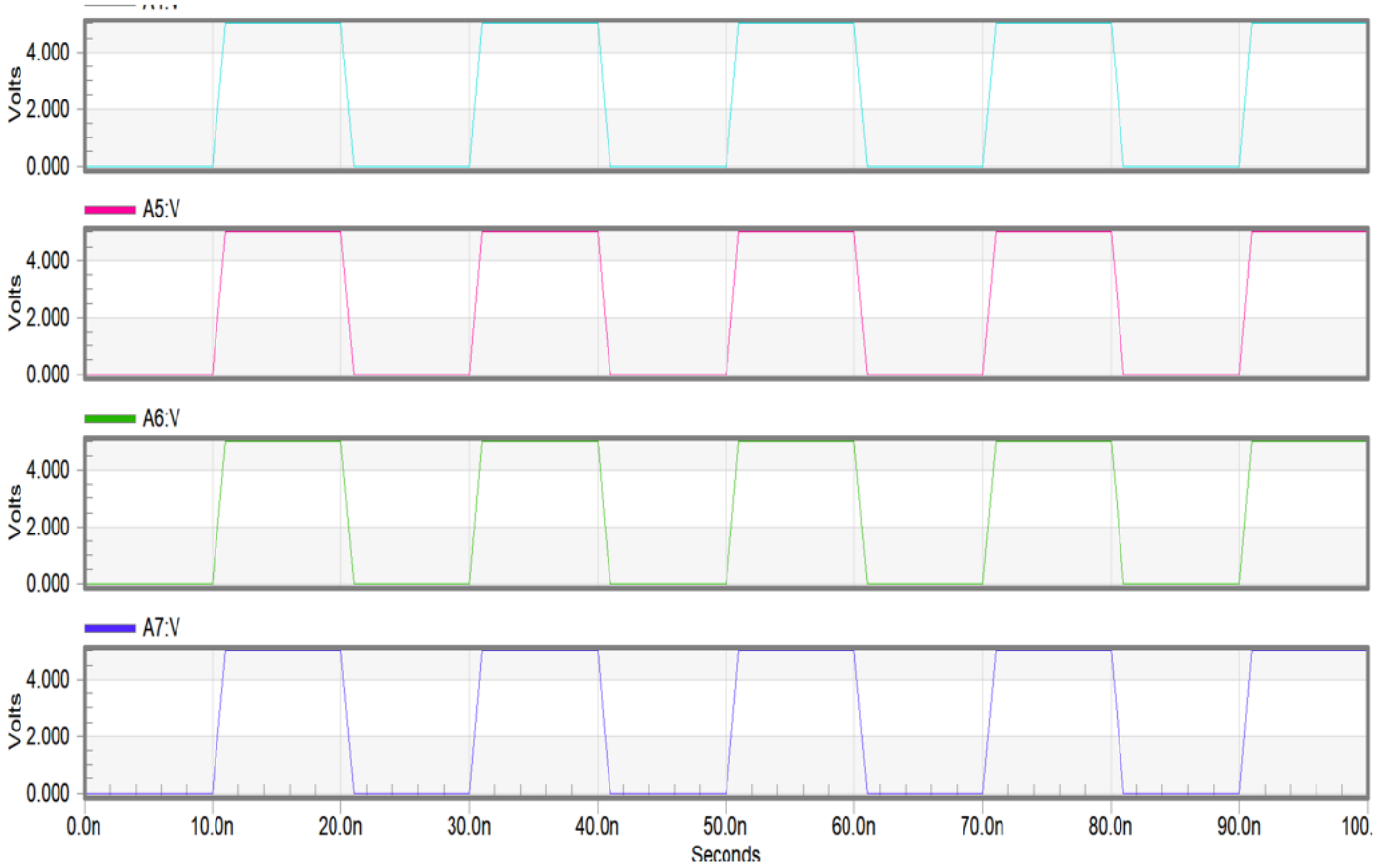

Figure 7

8-bit Input A4-A7

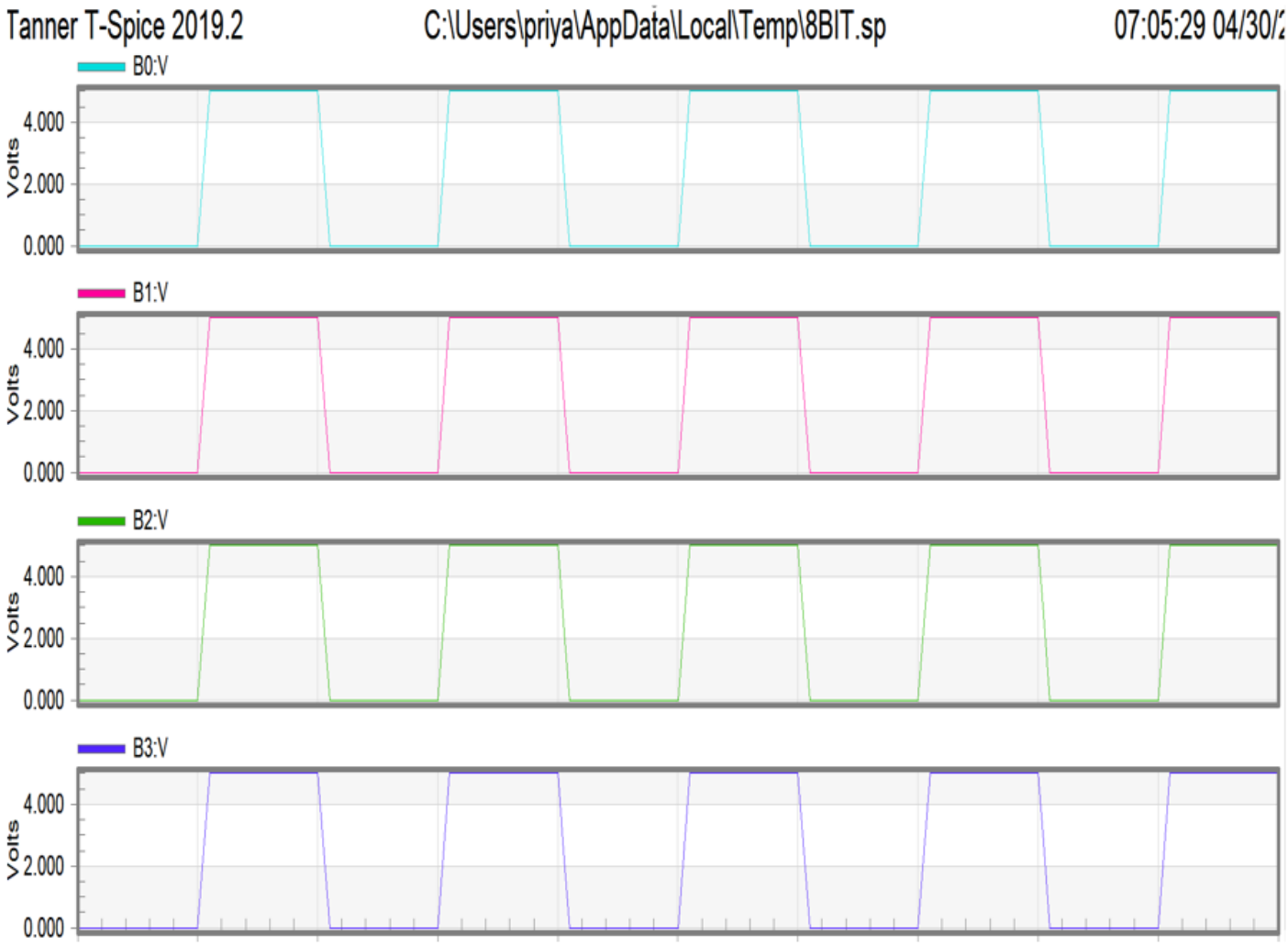

Figure 8

8-bit Input B0-B3

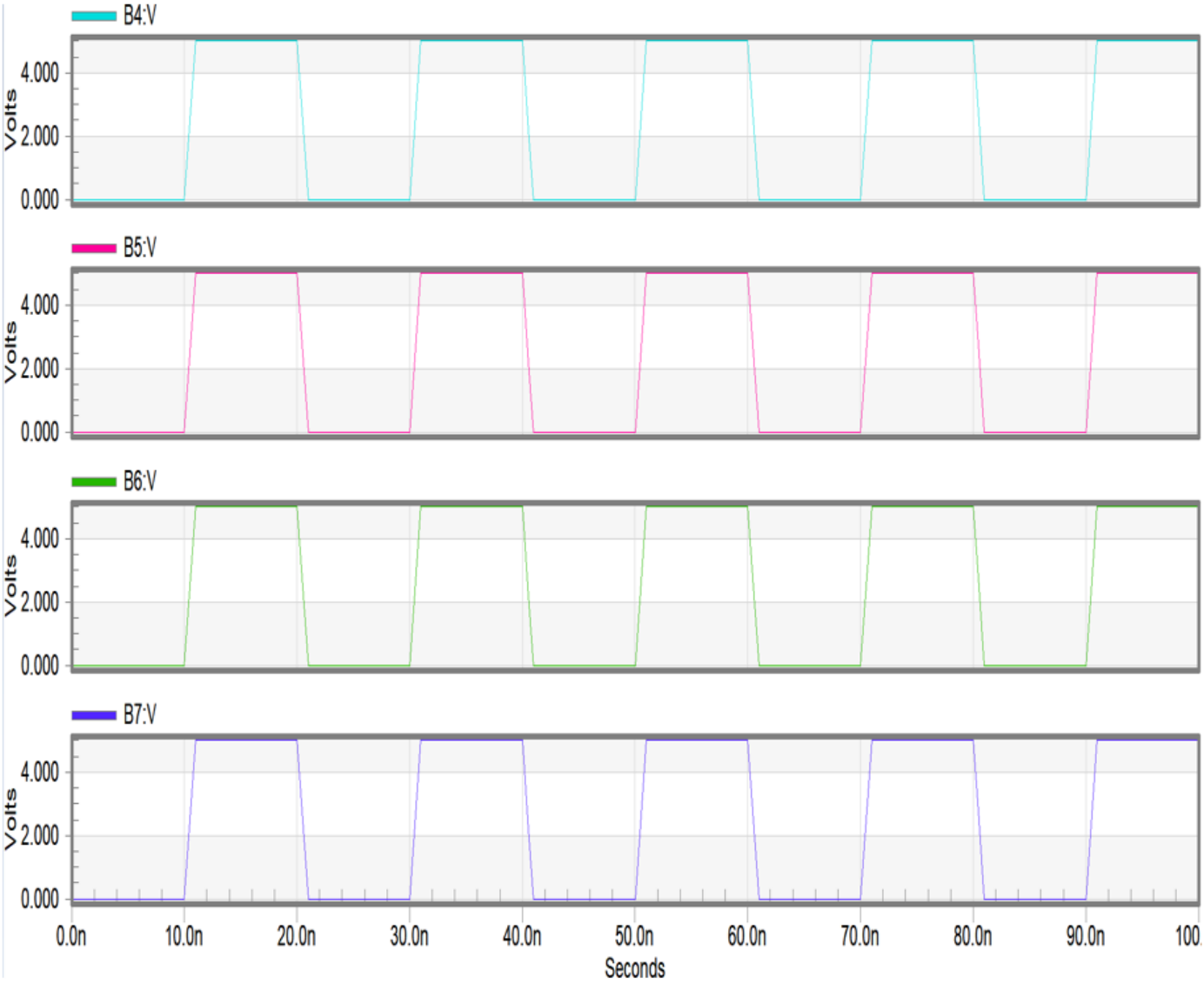

Figure 9

8-bit Input B4-B7

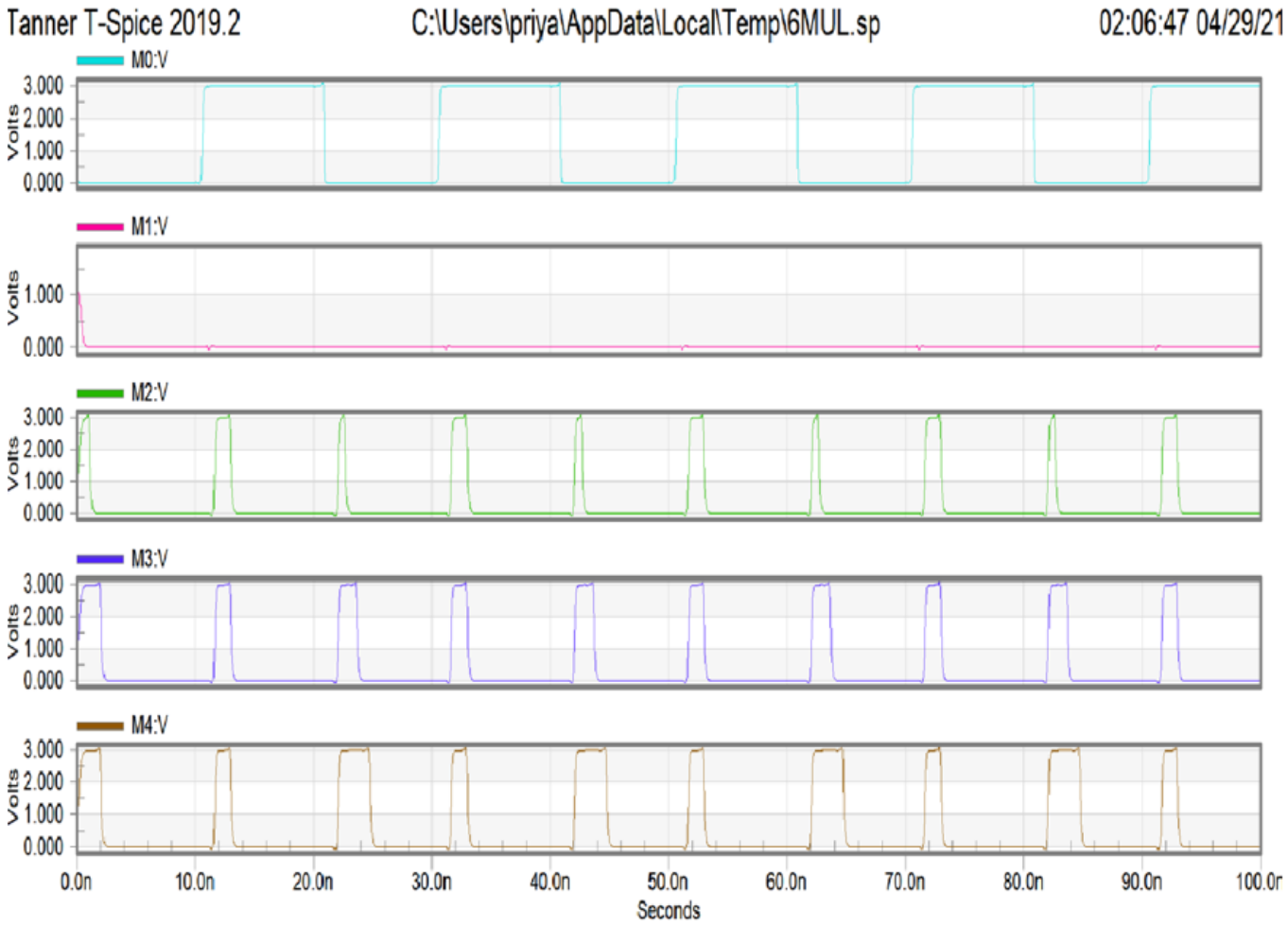

Figure 10

Output of CLA MULTIPLIER M0-M4

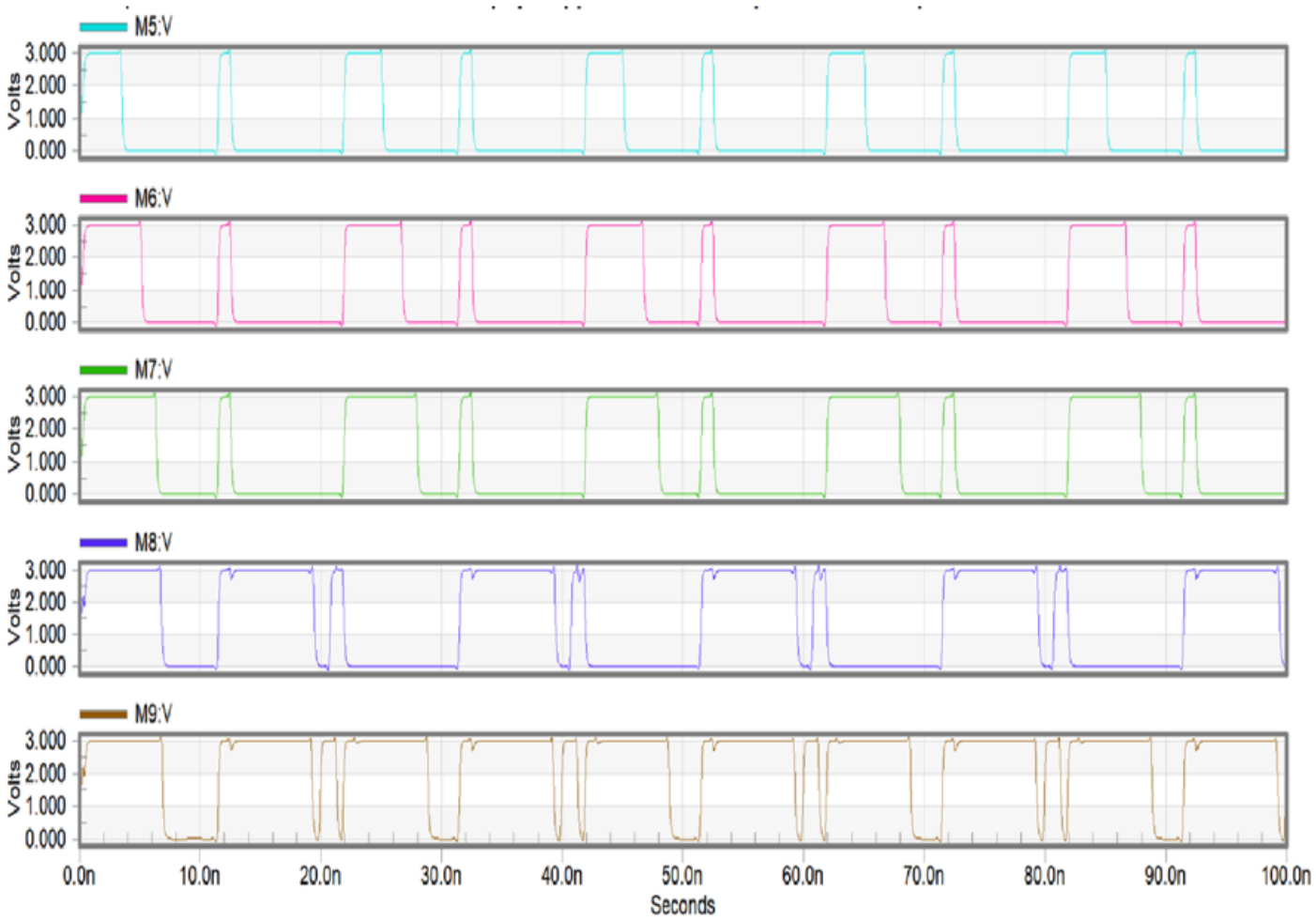

Figure 11

Output of CLA MULTIPLIER M5-M9

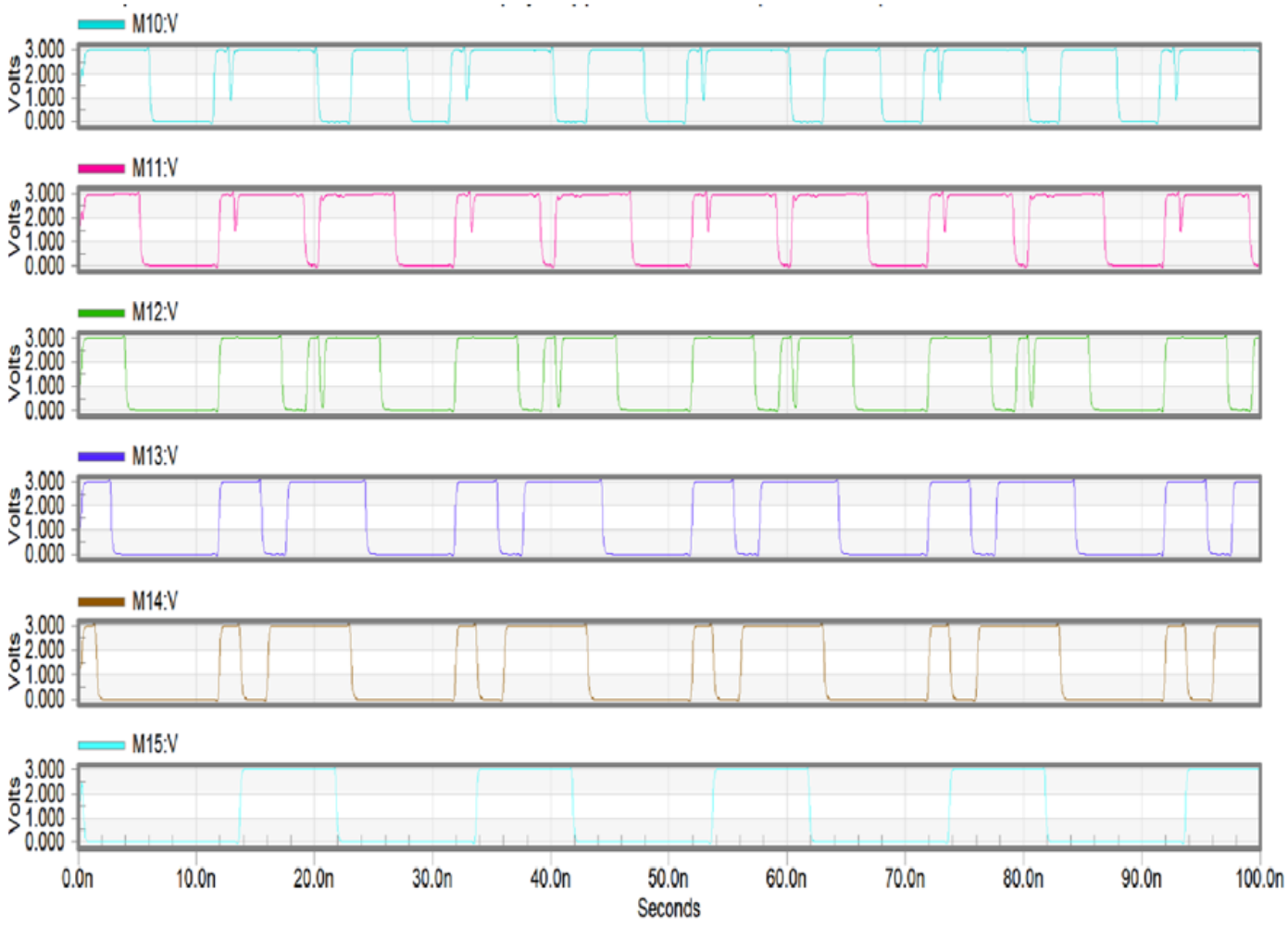

Figure 12

Output of CLA MULTIPLIER M10-M15

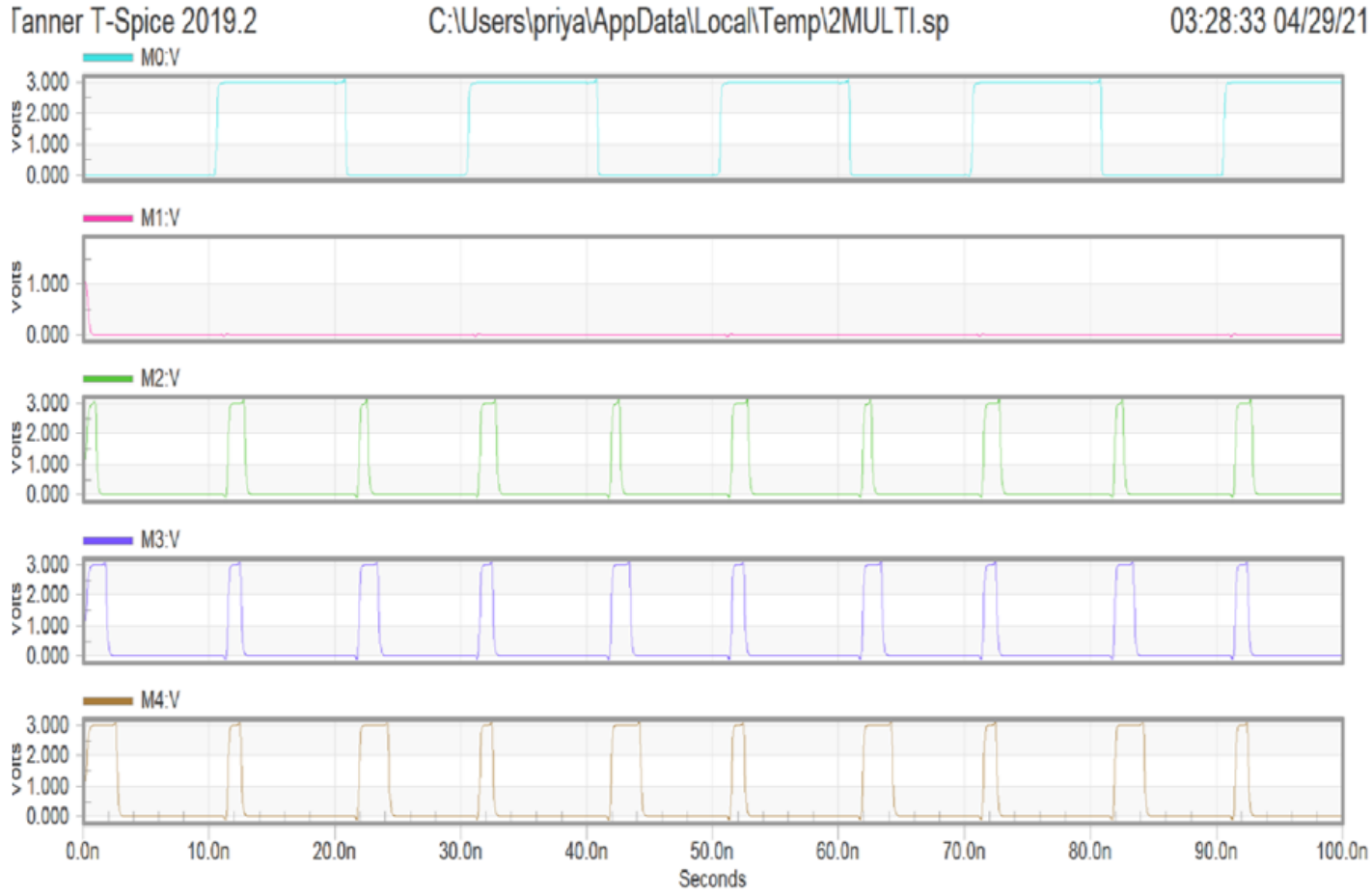

Figure 13

Output of CIA MULTIPLIER M0-M4

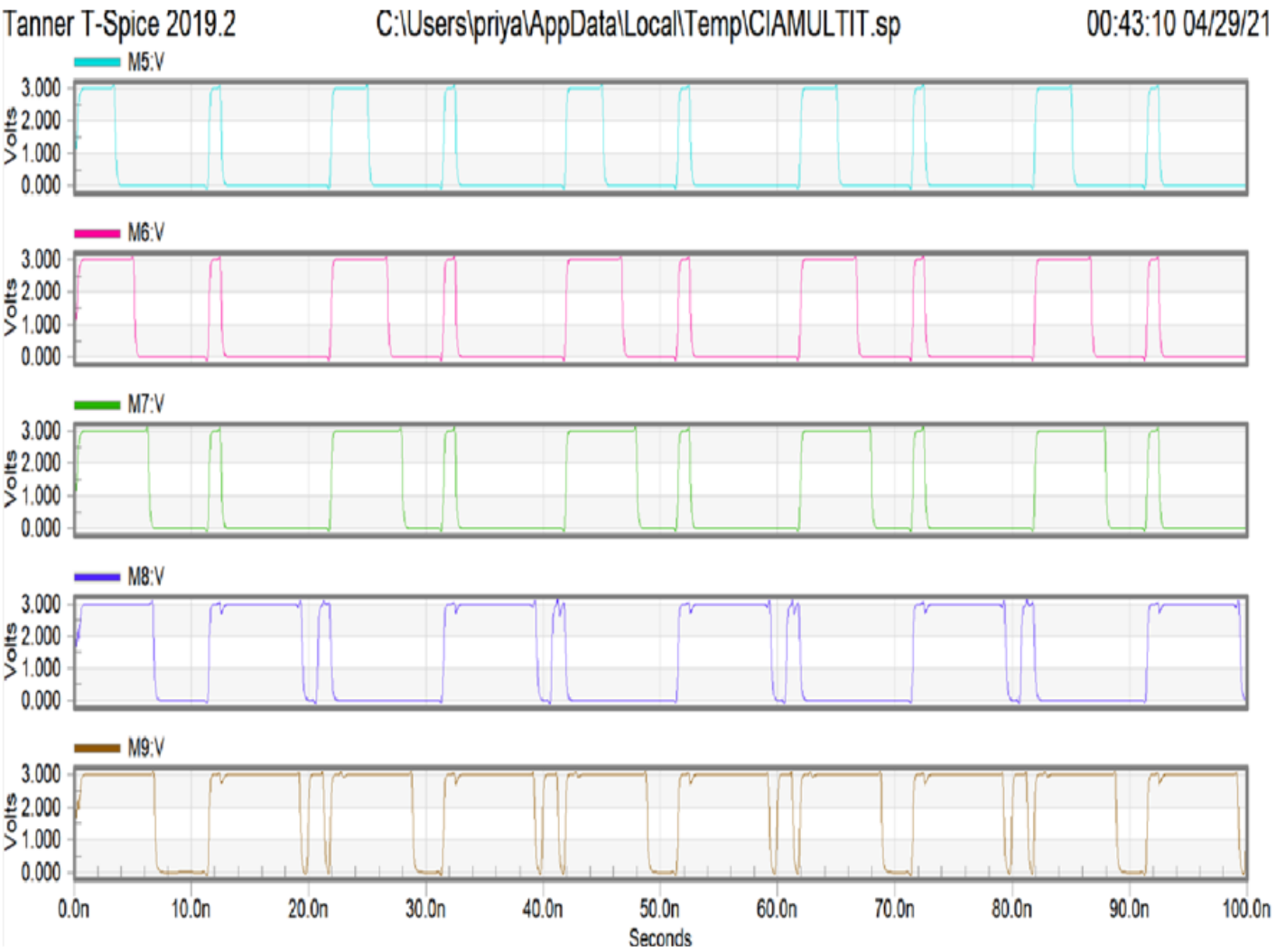

Figure 14

Output of CLA MULTIPLIER M5-M9

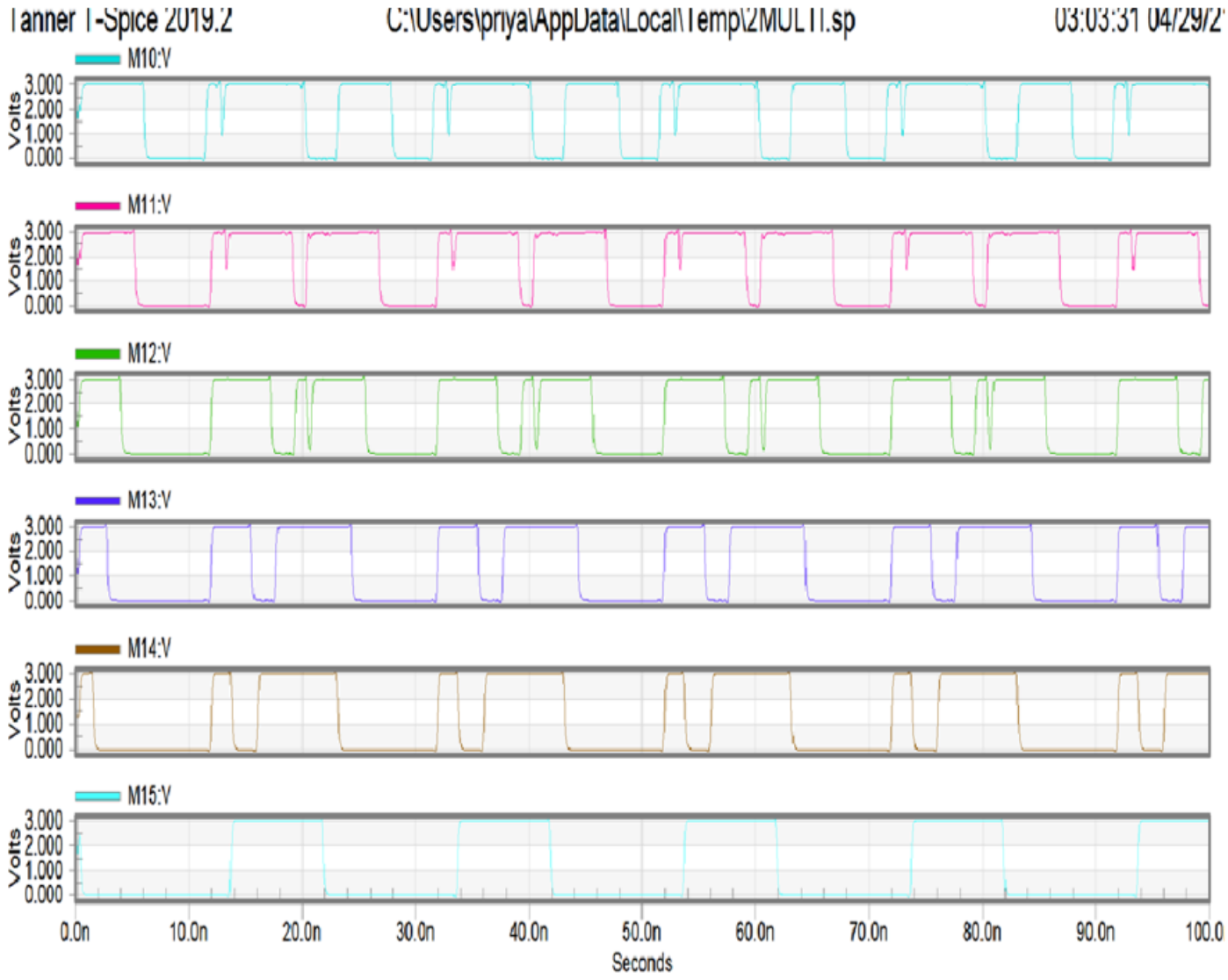

Figure 15

Output of CIA MULTIPLIER M10-M15