IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 7, Issue 4, Ver. I (Jul. - Aug. 2017), PP 09-14
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

Design of Low Voltage D-Flip Flop Using MOS Current Mode Logic (MCML) For High Frequency Applications with EDA Tool

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Abstract: *This paper presents a new topology to implement MOS current mod logic (MCML) tri-state buffers. In Mos current mode logic (MCML) current section is improves the performance and maintains low power of the circuit. MCML circuits contains true differential operation by which provides the feature of low noise level generation and static power dissipation. So the amount of current drawn from the power supply does not depends on the switching activity. Due to this MOS current mode logic (MCML) circuits have been useful for developing analog and mixed signal IC's. The implementing of MCML D-flip flop and Frequency divider done by using MCML D-latches. The proposed MCML D-latch consumes less power as it makes use of low power tri-state buffers. Which promotes power saving due to reduction in the overall current flow in the proposed D flip flop topology is verified though Cadence GPDK-180nM CMOS technology parameters.*
Keywords: *Mos current mode logic (MCML), Tri-state buffer, D-latch, D-flip flop, low power.*

I. Introduction

In recent years, the growing demand for portable electronic devices require low power building blocks that enable long lasting battery life of the system [1]. This has led to the development of low power digital circuits. D-latch is the basic circuit used for implementing many fundamental blocks whose performance strongly depends on the D-flip flop gate performance. This type of logic was first implemented using bipolar transistors [4] and extended for applications with MOS transistors. Conventional CMOS, however, has almost negligible static power dissipation but still the dynamic power dissipation during transition from one logic level to another has led to the development of a logic that reduced the dynamic power dissipation MOS Current-Mode Logic (MCML) is an alternative logic designing style that provides true differential operation, low noise level generation and noise immunity. While reduced voltage swing at the output helps to operate the circuit in very high frequencies with low noise generation. Ultra low-power logic circuits with the capability of operating at relatively high frequencies are very desirable in many modern applications such as portable equipment or implanted biomedical systems In addition to the benefits of low signal swing and fast switching speed, they also show a very low sensitivity to supply and substrate noise due to their differential topology. Low-power MCML circuits that can be applied to digital CMOS technologies ,MOS current mode logic (MCML) circuits with constant bias currents are intended for accurate high-speed mixed signal application. Compared to conventional CMOS logic. The constant supply currents, lower cross talk between the analog and the digital circuits of MCML improves the accuracy of mixed-mode systems D-latch acts as an integral part of various practical applications such as pre-scalars, frequency dividers, and sequential logic circuits. Spectre simulations where done in Cadence Analog Environment, The functionality of the proposed topology is verified through SPICE simulations by using 0.18 μm TSMC CMOS technology parameters.

II. MCML Circuits

A MOS Current Mode Logic (MCML) circuit consists of three main components, as shown in fig 1.which are load circuit and Pull down network and constant current source

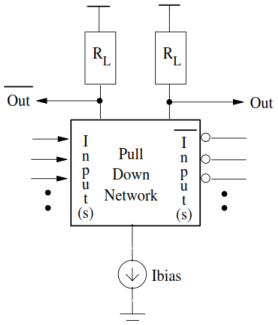


Fig 1: Basic MOS Current Mode Logic (MCML) Structure

The MCML circuits is a completely differential architecture i.e., all signals with their complements is needed in this MCML logic. All the current flows through one of the two branches of pull down network, providing complementary output signals. Voltage at the output of branch if no tail current is reaches then the output is VDD and other branch with some voltage drop across the load circuit, then the voltage becomes VDD-IssRL. The operation of MCML is performed in the current domain. The pull down network switches the constant current between two branches, and then the load converts the current to output voltage swings. MCML is does not provide a rail to rail output voltage swing due to its reduced swing. MCML circuits are faster than other logic families, because it uses NMOS transistors only.

2.1 MCML inverter:

MOS Current Mode Logic inverter/Buffer circuit is shown in figure 2.the basic MCML inverter /Buffer logical operation is performed based on current domain and source coupled transistor (M1 andM2) is true differential pair. The transistor switches constant current **Iss** between two branches. The current is converted again to voltage at output through the load resistors (R_L). Then the output voltage swing Vout is I_D R_L shown in fig.2.

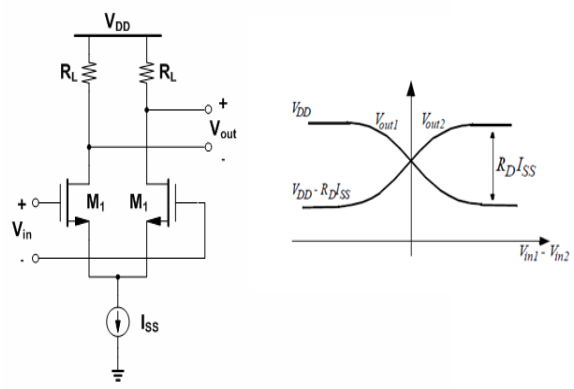
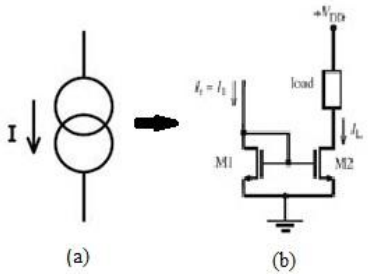


Fig 2: MCML Inverter/Buffer

2.2 CONSTANT CURRENT SOURCE DESIGN:

The constant current sources are designed by using different current mirrors. So the constant current source is simply designed by using the single NMOS transistor shown in Fig.3(c). The NMOS transistor should be in saturation region to flow constant current I_D through drain of transistor.



The load resistor is modelled by using PMOS transistor and the PMOS transistors should be in triode region, then it act as a resistor shown in Fig.3(C).

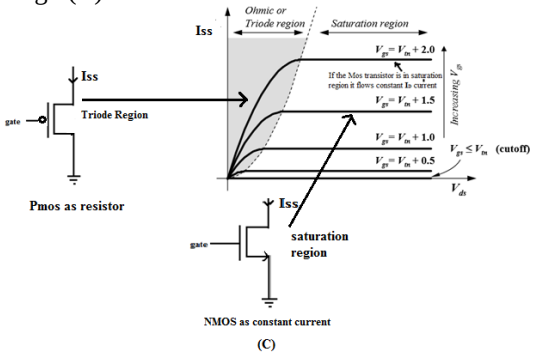


Fig 3:(a)constant current source (b)current mirror (c)Transistor as a constant current source

2.3 TRI STATE BUFFER:

The tri state buffer has two inputs they are data input and control input. The tri state buffer is used to controls the input data to output side, so if control input is active then same input present at output and its act like a buffer. Tri state buffer controls with high and low control inputs shown in Fig 4.

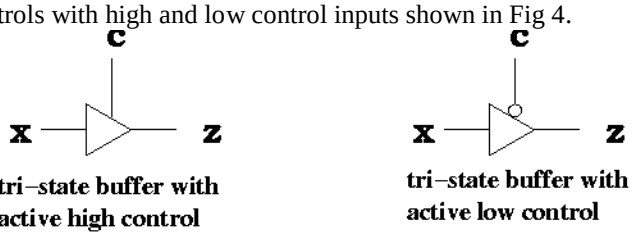


Fig 4: Tri state buffers with active high and low controls

2.4 D-LATCH DESIGN

In CMOS logic the D-latch is designed by using tri state inverters as shown in Fig 5.

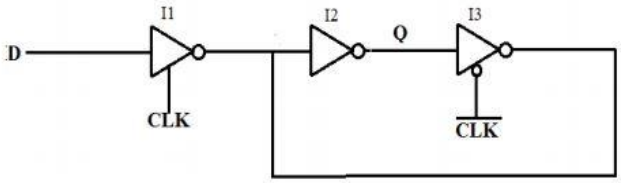


Fig 5: D-Latch design

the D-latch design is make use of two tri state inverters and one inverter is based on CMOS logic as shown in fig 5.The clock signal is used to alternately enable and disable the two tri-state inverters (I1 and I3),so if the inverter is in normal mode and other tri state inverter is in high impedance mode. When the clock signal is active then the input is transferred to the output of tri state inverter and the clock is low then the output is preserved by back to back inverters.

The proposed D-Latch design using MOS Current Mode Logic(MCML) tri-state buffers, the D-latch design require two MCML tri-state buffers and MCML is a true differential logic that is signals and there complements needed. The D-latch design based on tri –state buffers is shown in Fig 6.the clock signal is used to enable buffers alternately. When the clock

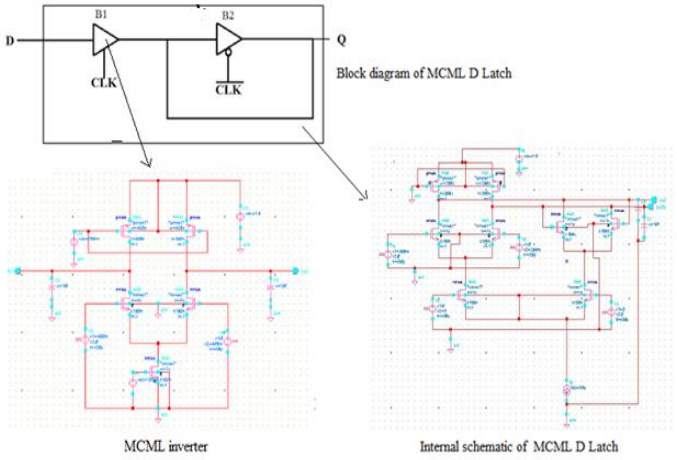


Fig 6: D Latch design using tri-state buffer

Signal is high, the MCML tri-state buffer (B1) is active/normal state and then input transferred to output. The buffer (B2) is in high impedance mode and the loop brakes. When the clock signal is low buffer (B1) is in high impedance mode then there is no path between input and output, so the buffer (B2) is activated thus completing the loop and last output state is passed till the next clock transition. The output wave forms for clock and data signals are shown in Fig 6.

2.5 D flip flop implementation using MCML D-latch:

The structure of the MCML D flip-flop is shown in the Fig 7. The most common approach for constructing D flip-flop is to use a master-slave configuration. The MCML D flip-flop is realized by cascading a negative latch (master stage) with a positive one (slave stage), as shown in Fig 7.

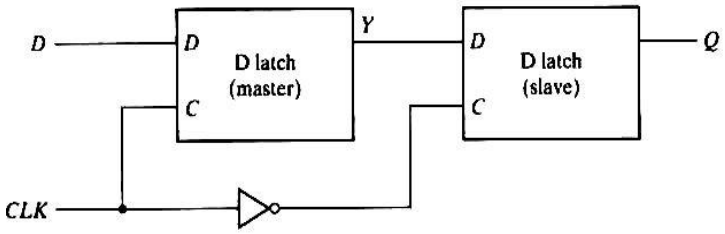


Fig 7: Basic D-Flip flop

The current switching between the pairs takes place by the complementary signals of the clock. The sample pair works as a buffer. When it is activated by the clock signal, it keeps track of the input data and transforms it to the outputs. This is known as the sampling mode of the latch.

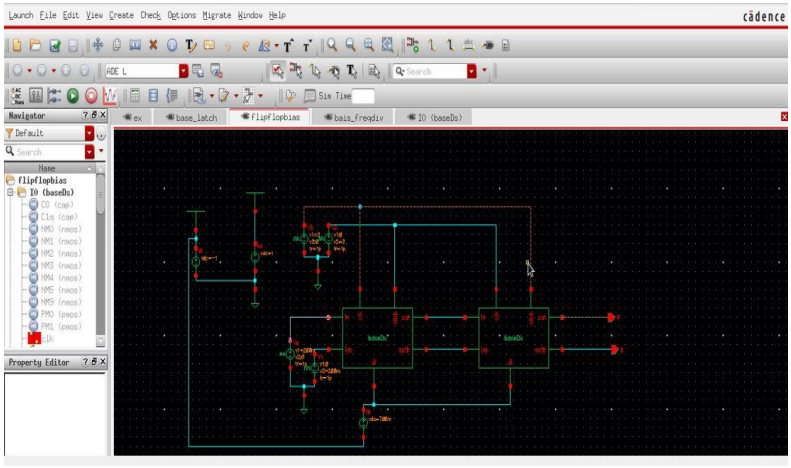


Fig 8: D flip flop design using MCML D-Latches

2.6 Frequency divider using MCML D-Latches:

Frequency dividers are fundamental building blocks in a number of applications, such as frequency synthesis in mobile and satellite communication systems, clock generation, data recovery, synchronization and multiple-Gb/s optic fibre systems. In these applications, the frequency divider is often the speed-limiting block, thus a high speed is required.

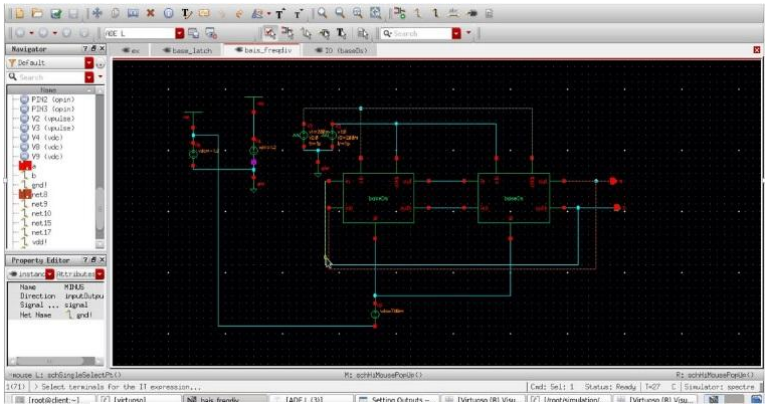


Fig 9: Block diagram MCML based Frequency divider

This architecture is primarily a master-slave flip-flop with a negative feedback. This circuit works by continually toggling the output state after every clock cycle. The mechanism effectively causes the output to toggle between one and zero at a rate half that of the input clock.

III. Simulation Results

The schematics of low voltage MCML D-Latch, MCML D Flip Flop are simulated and the transient responses are analysed using Cadence analog design environment.

Fig 10: Transient response of of proposed D-latch

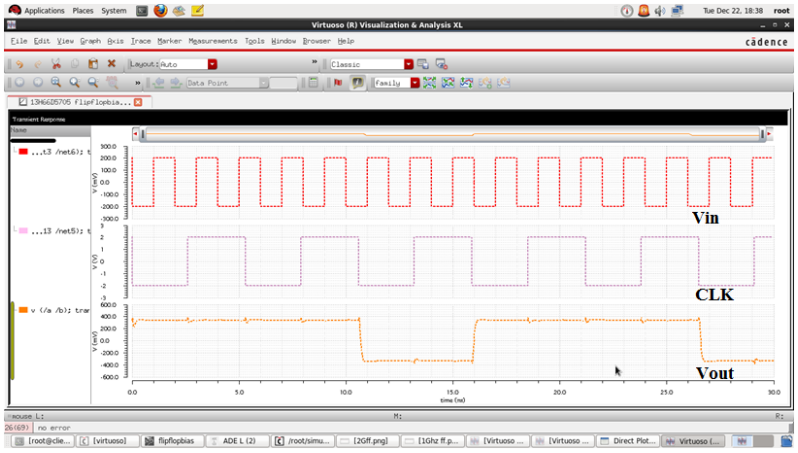


Fig 11: Transient response of D-flip flop

Fig 12: Transient response of frequency divider

IV. Conclusion

In this paper, Low voltage Mos current mode logic (MCML) circuits has been implemented, simulated and analysed. The performance of the MCML D-Latch, D-Flip-flop and Frequency divider is assessed in terms of supply voltage, delay and power consumption. The main goal to reduce the power dissipation at variable frequencies and optimize overall power consumption by using tri-state MCML Inverter/Buffers. The transient response analysed by Cadence EDA Tool.

The power consumption of Mos current mode logic (MCML) circuit is shown in table 2.

Table 1: Simulation environment

Technology	180 nm
Temperature	27 ^{o}c
Supply Voltage	1V
Output Load Capacitor Bias	10 ff
Current	50 µA
Input Data Frequency Clock	100 Mhz-3Ghz
Frequency	500 Mhz

Table 2: Power dissipation at different supply voltages

MCML LOGIC	**Source current(Iss)**	**Power dissipation (µW) VDD=1.8V**	**Power dissipation(µW) VDD=1.0V (Proposed MCML)**
MCML based D-latch	50µW	112µW	**51 µW**
MCML based D-flip flop	50µW	243 µW	**107 µW**
MCML based frequency divider	50µW	203 µW	**119 µW**

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