applied sciences

MDPI

Article

Design of Novel HG-SIQBC-Fed Multilevel Inverter for Standalone Microgrid Applications

Suvetha Poyyamani Sunddararaj [1], Shriram S. Rangarajan [2,3,*], Subashini Nallusamy [1], Umashankar Subramaniam [4], E. Randolph Collins [3,5] and Tomonobu Senjyu [6]

1 School of Electrical and Electronics Engineering, SASTRA Deemed University, Thanjavur 613401, Tamil Nadu, India
2 Department of Electrical and Electronics Engineering, SR University, Warangal 506371, Telangana, India
3 Department of Electrical and Computer Engineering, Clemson University, Clemson, SC 29634, USA
4 Renewable Energy Laboratory, College of Engineering, Prince Sultan University, Riyadh 11586, Saudi Arabia
5 College of Engineering and Technology, Western Carolina University, Cullowhee, NC 28723, USA
6 Department of Electrical and Electronics Engineering, University of the Ryukyus, Okinawa 903-0213, Japan
* Correspondence: shriras@g.clemson.edu

Abstract: The growth of distributed power generation using renewable energy sources has led to the development of new-generation power electronic converters. This is because DC–DC converters and inverters form the fundamental building blocks in numerous applications, which include renewable integrations, energy harvesting, and transportation. Additionally, they play a vital role in microgrid applications. The deployment of distributed energy resources (DERs) with renewable sources such as solar has paved the way for microgrid support systems, thus forming an efficient electric grid. To enhance the voltage of such sources and to integrate them into the grid, high-gain DC–DC converters and inverter circuits are required. In this paper, a novel single-switch high-gain converter (HG-SIQBC) with quadratic voltage gain and wide controllable range of load is proposed, the output of which is fed to a modified multilevel inverter for conversion of voltage. The overall performance of the newly designed converter and inverter is analyzed and compared with the existing topologies. A prototype of the investigated multilevel inverter is designed and tested in the laboratory. Development and testing of such novel topologies have become the need of the hour as the grid becomes smarter with increased penetration of distributed resources.

Keywords: DC–DC converters; multilevel inverter; microgrid; distributed energy resources (DERs)

Citation: Sunddararaj, S.P.; Rangarajan, S.S.; Nallusamy, S.; Subramaniam, U.; Collins, E.R.; Senjyu, T. Design of Novel HG-SIQBC-Fed Multilevel Inverter for Standalone Microgrid Applications. *Appl. Sci.* **2022**, *12*, 9347. https://doi.org/10.3390/app12189347

Academic Editor: Andreas Sumper

Received: 22 July 2022
Accepted: 14 September 2022
Published: 18 September 2022

1. Introduction

Conventional power systems are getting degraded due to the gradual reduction in fossil fuels, poor energy efficiency, and low reliability. This leads to the development of new power generation systems at the distribution level using various nonconventional and renewable energy sources such as solar energy, wind power, fuel cells, and biogas [1]. These energy sources are integrated into a utility distribution network; the power generated using this network is termed as distributed power generation, and the energy sources incorporated in this network are known as distributed energy resources (DERs). The penetration of DERs in the worldwide electrical distribution leads to the formation of power clusters which are known as microgrids. This provides an opportunity to utilize renewable energy sources for a green and clean environment [2,3]. Furthermore, the DC microgrid has advantages such as high reliability, uninterruptible power supply, no reactive power, reduced losses, higher efficiency, simpler connection with DC bus, no need of synchronization, and no frequency aspects. Despite advantages over alternating current microgrids, the output voltage of these DC power generators is low. Therefore, high-gain DC–DC converters are needed for a DC microgrid [4]. Moreover, the use of multilevel inverters has become predominant in the fields of power systems, solid-state transformers,

power quality conditioning, renewable energy applications, and many more industrial applications. Among these, PV-based power generation systems are gaining popularity and are widely used in distribution-side networks. The process of power generation is classified into on-grid and off-grid systems, and the role of inverters is inevitable in all grid-connected networks. Initially, two-level inverters are employed in grid operation for the conversion of voltage from PV arrays to the grid network. However, the efficiency and conversion gain of these conventional inverters is much lower, which results in poor power quality issues and harmonics. To overcome these problems, multilevel converters have been introduced for combining PV arrays with the distribution grid [5,6]. Multilevel inverters possess better characteristics when compared to conventional two-level inverters [7–9]. The merits of MLI topologies include a better harmonic profile, reduced filter size, modular structure, improved load sharing capabilities, and reduction in voltage stress levels across the switches [10]. Many researchers working in this domain are trying to contribute a novel configuration with improved efficiency, power density, and reliability at a low cost. The studies published by many researchers working in this field have proven that the modifications of NPC (neutral point clamped), cascaded H-bridge topologies give greater efficiency with reduced harmonic content [11].

The types of multilevel inverter are illustrated as a schematic in Figure 1.

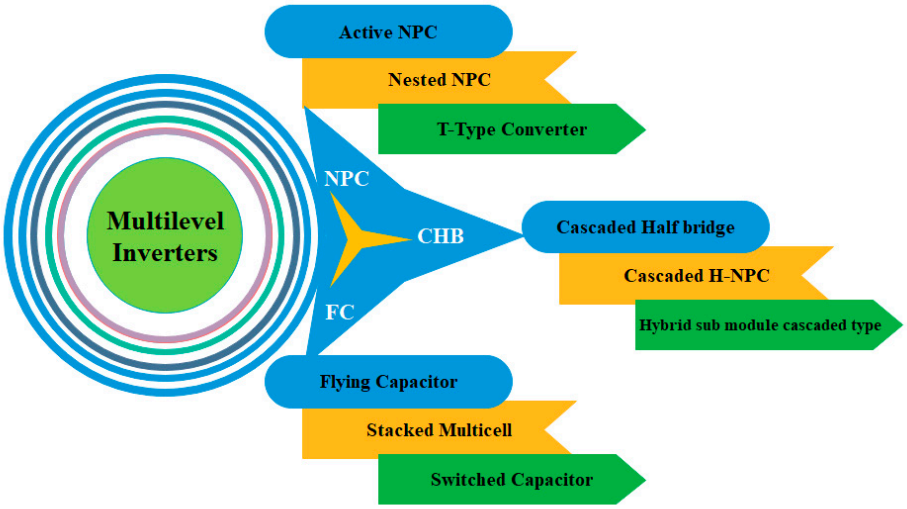


Figure 1. Multilevel inverter classifications.

Overall, this work focuses on power electronic converters such as DC–DC converters and inverters for applications associated with the DC microgrid. An illustration of the proposed system is shown in Figure 2. The input is fed from a PV array and is given to a novel single-switch non-isolated high-gain DC–DC converter to match with the DC bus voltage level. It can also supply AC loads via the modified 11-level inverter proposed in this work. The switching logic of the proposed multilevel inverter can also be extended to higher-level configurations and is verified in the simulation environment. To match the output voltage of this converter with the DC bus voltage, a suitable PI controller is designed, providing a better control operation. The analysis is performed and the results are obtained with the help of MATLAB simulations. To validate the simulation results of the multilevel inverter, a prototype for five-level configuration is developed and tested in the laboratory.

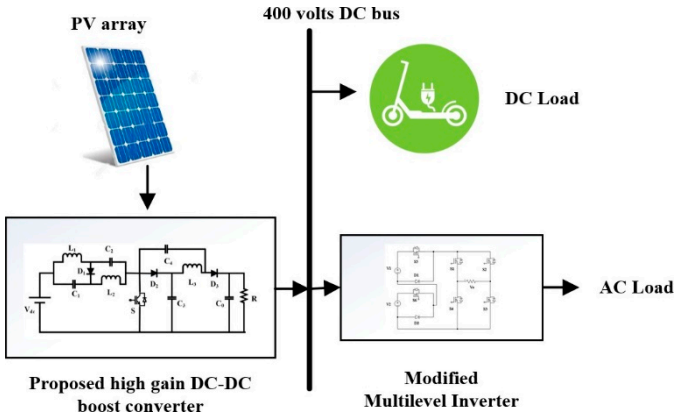


Figure 2. Layout of the proposed system.

2. Proposed Converter—I: Novel Non-Isolated High-Gain Switched Inductor Quadratic Boost Converter with High Voltage Conversion Ratio (HG-SIQBC)

The proposed HG-SIQBC comprises a switched inductor cell and a quadratic converter configuration. The first part of the converter comprises a switched inductor cell formed with the combination of inductors L_1 and L_2, as well as diodes D_{11}, D_{12}, and D_1. The latter part of the circuit comprises a switch 'S', as well as combinations of inductor L_3 and capacitors C_1, C_2, C_3, and C_0, along with the diodes D_2–D_6. The circuit diagram of the proposed HG-SIQBC topology is displayed in Figure 3.

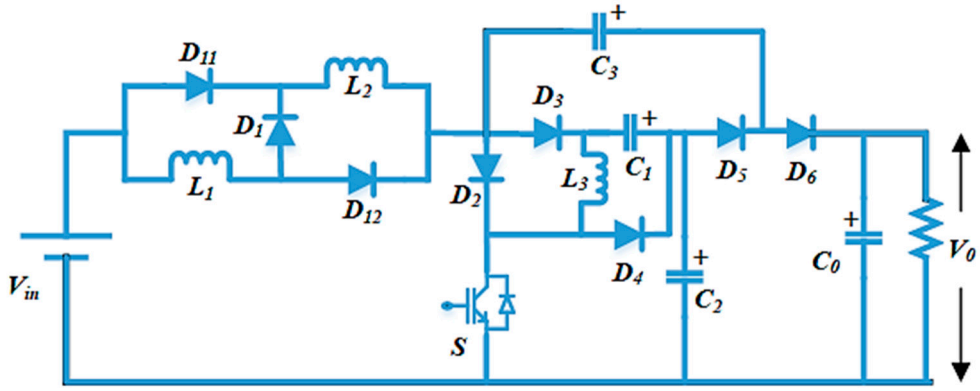


Figure 3. Circuit diagram of proposed HG-SIQBC.

The circuit operates in two modes as a function of the switching sequence of the active switch present in the converter. According to the relationships between current and voltage in the different operating modes, the theoretical waveforms of the proposed topology are illustrated in Figure 4. The waveforms drawn from top to bottom correspond to the gate pulse of the switch, currents of L_1, L_2, and L_3, and voltages of C_1, C_2, C_3, and C_0.

2.1. HG-SIQC—Mode I: Switch 'S' in ON State

During this switching interval, the switch 'S' is kept in the ON state, and the diodes D_1, D_2, and D_5 are simultaneously forward-biased, as presented in Figure 5.

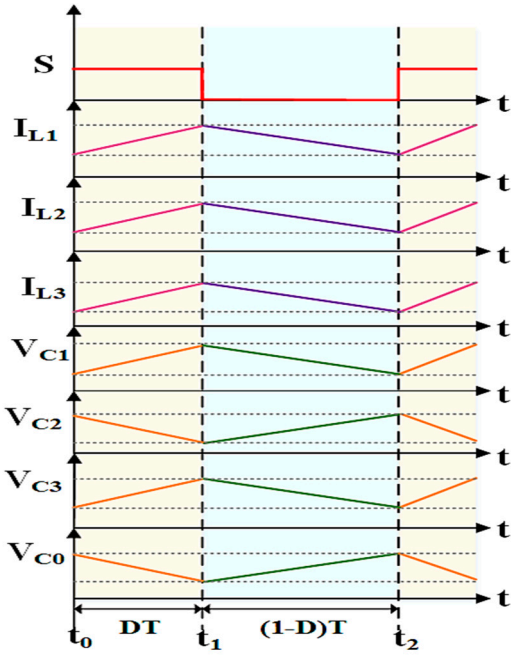


Figure 4. Theoretical waveforms of the proposed HG-SIQBC. (Ton and Toff are differentiated with dotted lines with pink and blue backgrounds respectively).

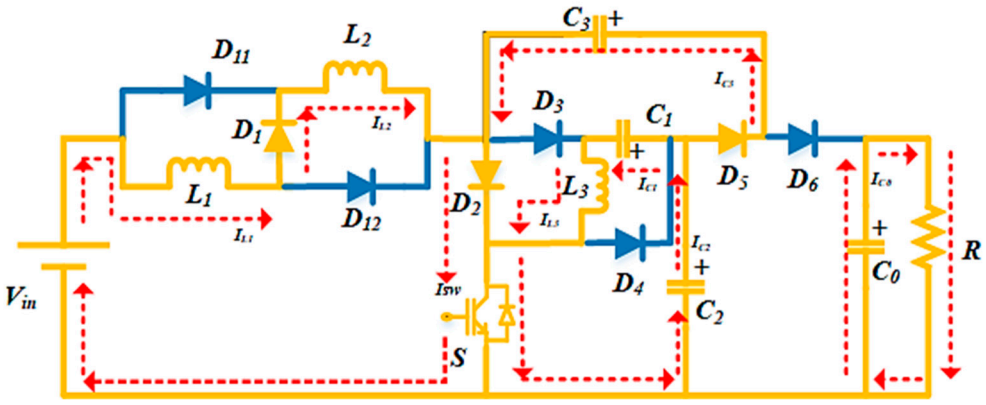


Figure 5. HG-SIQBC—equivalent circuit for Mode I. (The conducting portion of the circuit is shown in Yellow color with the current flow in dotted lines).

The voltage across the inductor L_1 and L_2 becomes equal to $V_{in}/2$, and the voltage across L_3 is equal to the difference between the voltage in C_1 and C_2. The capacitor C_2 is discharged, and it charges C_1 and C_3. Similarly, the capacitor C_0 is discharged to the load. The following equations are obtained when Kirchhoff's voltage law (KVL) is applied to Figure 5:

$$\begin{cases} V_{in} - V_{L_1} - V_{L_2} = 0 \\ V_{C_2} - V_{C_1} - V_{L_3} = 0 \\ V_{C_2} - V_{C_3} = 0 \end{cases}. \quad (1)$$

From Equation (1), the voltage across the inductors L_1, L_2, and L_3 can be written as

$$\begin{cases} L_1 \frac{di_{L_1}}{dt} = \frac{V_{in}}{2} \\ L_2 \frac{di_{L_2}}{dt} = \frac{V_{in}}{2} \\ L_3 \frac{di_{L_3}}{dt} = V_{C_2} - V_{C_1} \end{cases}, \quad (2)$$

where V_{in} is the input voltage, and V_{C1} and V_{C2} are the voltages across the capacitors C_1 and C_2, respectively.

Similarly, Kirchhoff's current law (KCL) is applied to the circuit shown in Figure 5 to obtain the current flowing through the capacitors.

$$\begin{cases} I_{C_1} = I_{L_3} \\ I_{C_2} = -\left[I_{C_3} + I_{C_1}\right] \\ I_{C_3} = I_{C_2} - I_{C_1} \\ I_{C_0} = -I_0 \end{cases} . \tag{3}$$

2.2. HG-SIQC—Mode II: Switch 'S' in OFF State

During this switching interval, the switch 'S' is kept in the OFF state, as shown in Figure 6.

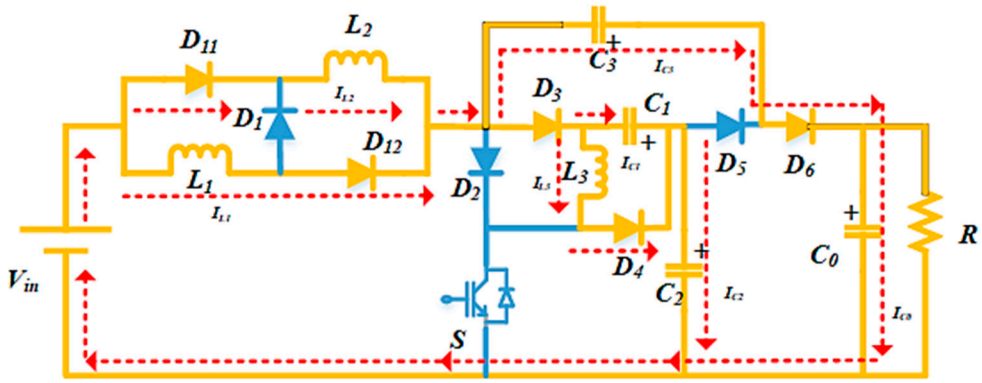


Figure 6. HG-SIQBC—equivalent circuit for Mode II. (The conducting portion of the circuit is shown in Yellow color with the current flow in dotted lines).

The inductors connected at the input side discharge and transfer energy to capacitor C_2. Meanwhile, capacitor C_3 is discharged and supplies output capacitor C_0. The voltage equations of the proposed converter during the OFF state of the switch can be obtained by applying the KVL to Figure 6.

$$\begin{cases} V_{in} - V_{L_2} + V_{C_3} - V_{C_0} = 0 \\ V_{in} - V_{L_1} + V_{C_1} - V_{C_2} = 0 \\ V_{in} - V_{L_2} - V_{L_3} - V_{C_2} = 0 \end{cases} . \tag{4}$$

From Equation (4), the voltage across the inductors L_1, L_2, and L_3 can be written as

$$\begin{cases} L_1 \frac{di_{L_1}}{dt} = V_{in} + V_{C_1} - V_{C_2} \\ L_2 \frac{di_{L_2}}{dt} = V_{in} + V_{C_3} - V_0 \\ L_3 \frac{di_{L_3}}{dt} = -V_{C_1} \end{cases} , \tag{5}$$

where V_{in} is the input voltage, V_0 is the output voltage, and V_{C1} and V_{C3} are the voltages across the capacitors C_1 and C_3, respectively.

Similarly, KCL is applied to the circuit shown in Figure 6 to yield the current equations.

$$\begin{cases} I_{C_1} = -\left[I_{C_2} - I_{L_3}\right] \\ I_{C_2} = I_{C_1} + I_{L_3} \\ I_{C_3} = I_{C_0} = I_0 \end{cases} . \tag{6}$$

The total volt-seconds applied to the inductor L_3 over one switching period are as follows [12]:

$$\int_0^T V_{L_3}(t)dt = (V_{C_2} - V_{C_1})DT + (-V_{C_1})(1-D)T, \tag{7}$$

where D is the duty cycle, and T is the switching period.

The following equation can be obtained by equating Equation (7) to zero:

$$(V_{C_2}D) - (V_{C_1}D) - V_{C_1} + (V_{C_1}D) = 0. \tag{8}$$

Therefore,

$$V_{C_2} = \frac{V_{C_1}}{D}. \tag{9}$$

The total volt-seconds applied to inductor L_1 over one switching period are calculated as

$$\int_0^T V_{L_1}(t)dt = \left(\frac{V_{in}}{2}\right)DT + (V_{in} + V_{C_1} - V_{C_2})(1-D)T. \tag{10}$$

By equating Equation (10) to zero, the following equations can be obtained:

Substituting $V_{C_2} = \frac{V_{C_1}}{D}$,

$$\left(\frac{V_{in}}{2}\right)D + \left(V_{in} + V_{C_1} - \frac{V_{C_1}}{D}\right)(1-D) = 0, \tag{11}$$

$$\left(\frac{V_{in}D + 2V_{in} - 2V_{in}D}{2}\right) + \left(\frac{2V_{C_1}D - V_{C_1}D^2 - V_{C_1}}{2}\right), \tag{12}$$

$$V_{C_1}\left(\frac{2D - D^2 - 1}{D}\right) = \frac{V_{in}(D-2)}{2}. \tag{13}$$

Therefore,

$$V_{C_1} = \frac{V_{in}D(D-2)}{2(1-D)^2}. \tag{14}$$

Substituting the value of V_{C1} into Equation (9) yields

$$V_{C_2} = \frac{V_{C_1}}{D} = \frac{V_{in}(D-2)}{2(1-D)^2}. \tag{15}$$

Similarly, V_{C3} is calculated using the following equation:

$$V_{C_3} = \frac{V_{in}(D-2)}{2(1-D)^2}. \tag{16}$$

Subsequently, the voltage gain of the proposed converter can be obtained by applying the volt-sec principle to inductor L_2.

$$\int_0^T V_{L_2}(t)dt = \left(\frac{V_{in}}{2}\right)DT + (V_{in} + V_{C_3} - V_0)(1-D)T. \tag{17}$$

By equating Equation (17) to zero, the following equations can be obtained:

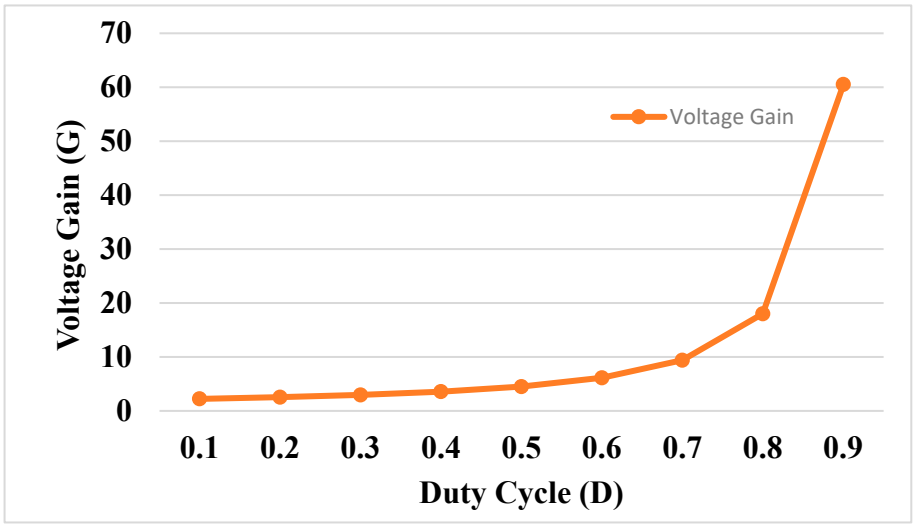
$$\left(\frac{V_{in}}{2}\right) * D + V_{in} - V_{in}D + V_{C_3}(1-D) = V_0(1-D), \tag{18}$$

$$\frac{V_{in}(2-D)(D-1)+V_{in}(D-2)}{2(D-1)} = V_0(1-D), \tag{19}$$

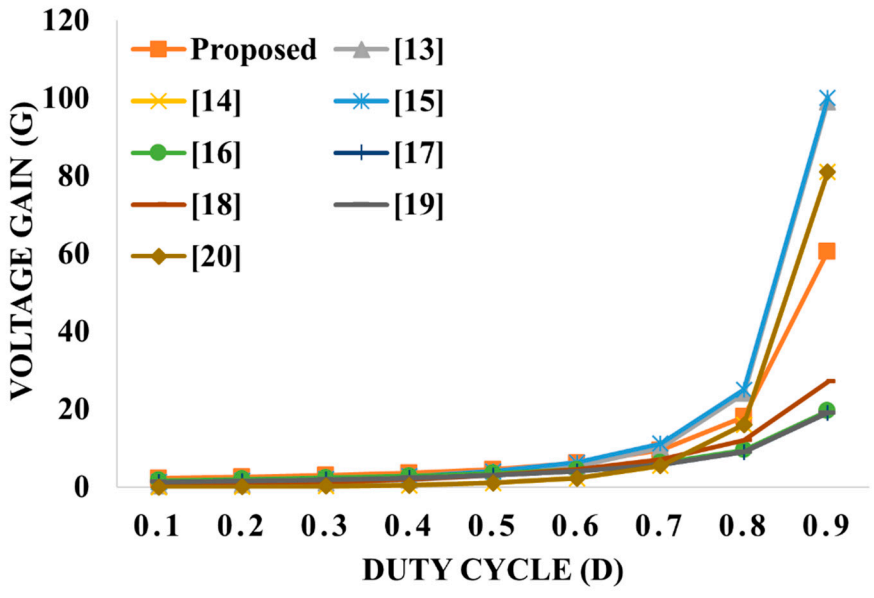
$$\therefore G = \frac{V_0}{V_{in}} = \frac{(D-2)^2}{2(1-D)^2}, \tag{20}$$

where G is the voltage gain of the proposed HG-SIQBC converter, and D is the duty cycle of the converter switch.

The plot between the voltage gain vs. duty cycle of the proposed topology and a comparison of proposed HG-SIQBC converter with other quadratic converters are shown in Figure 7a,b, respectively. The graph between voltage gain (G) and duty cycle (D) is drawn according to Equation (20).



(**a**)



(**b**)

Figure 7. Voltage gain vs. duty cycle: (**a**) proposed HG-SIQBC Topology; (**b**) HG-SIQBC vs. other topologies—comparison of voltage gain with duty cycle [13–20].

The input and output voltages for the proposed HG-SIQBC were considered as 75 V and 400 V, respectively. The converter should be operated at a duty cycle of 55.8% to achieve the required output voltage. The following expression can determine this:

$$\frac{400}{75} = \frac{(D-2)^2}{2(1-D)^2}. \tag{21}$$

Therefore, $D = 0.558 = 55.8\%$.

Other existing quadratic boost topologies with high voltage gain [13–20] were compared to the proposed HG-SIQBC topology. The proposed topology had better results in terms of voltage stress and voltage gain. A comparison of topologies is shown in Table 1.

Table 1. Comparison of proposed HG-SIQBC converter with other quadratic converters.

Topology	No. of Switches	No. of Diodes	No. of Inductors	No. of Capacitors	Voltage Gain (*G*)	Voltage Stress
[13]	1	3	2	2	$\frac{D(2-D)}{(1-D)^2}$	$\frac{1}{(1-D)^2}$
[14]	1	3	2	2	$\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)^2}$
[15]	1	4	2	4	$\frac{3+D}{2(1-D)}$	$\frac{1}{(1-D)}$
[16]	1	3	1	3	$\frac{1+D}{1-D}$	$\frac{1+D}{1-D}$
[17]	1	3	4	6	$\frac{3D}{1-D}$	$\frac{1}{1-D}$
[18]	1	2	2	3	$\frac{1+D}{1-D}$	$\frac{1}{1-D}$
[19]	1	3	2	3	$\left(\frac{D}{1-D}\right)^2$	$\left(\frac{1}{D}\right)^2$
[20]	1	3	3	3	$\frac{D}{(1-D)^2}$	$\frac{D}{(1-D)^2}$
Proposed HG-SIQBC	1	8	3	4	$\frac{(D-2)^2}{2(1-D)^2}$	$\frac{(D-2)}{2(1-D)^2}$

To determine the power loss of each component connected in the converter circuit, it is necessary to determine the current flowing through it. Therefore, by applying the ampere-seconds balance on capacitor C_0, the current flowing through the capacitor C_3 can be determined as follows:

$$(I_{C_0})D + (I_{C_0})(1-D) = 0, \tag{22}$$

$$-I_0 D + (I_{C_3})(1-D) = 0. \tag{23}$$

Therefore,

$$I_{C_3} = \frac{I_0 D}{(1-D)}. \tag{24}$$

Similarly, by applying the ampere-seconds balance, the current flowing through the capacitors can be determined as follows:

$$\begin{cases} I_{C_1} = \left(\frac{D(4D^2+D-6)+4}{2(D-1)^2(2D-1)}\right)\frac{V_0}{R} \\ I_{C_2} = \left(\frac{7D-6}{4(D-1)^3} - 1\right)\frac{V_0}{R} \end{cases}. \tag{25}$$

2.3. Voltage Stress of Switches and Diodes for HG-SIQBC

The voltage and current stress calculations of the power semiconductor switch are essential for ensuring proper component selection and reduced power loss of the converter [21]. The voltage stress across the power switch can be determined as shown in Figure 8.

$$V_{sw} - V_{C_2} = 0. \tag{26}$$

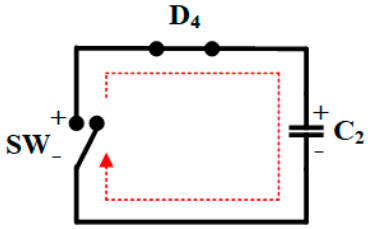


Figure 8. HG-SIQBC—equivalent circuit to find the voltage stress across the switch. (The current flow is given in dotted lines).

Substituting, the value of V_{C2} from Equation (15) into Equation (26) yields

$$V_{sw} = \frac{V_{in}(D-2)}{2(1-D)^2}. \tag{27}$$

Applying KVL to Figures 5 and 6, the voltage stress across the diodes can be obtained. For example, the voltage stress across the diode D_1 can be determined from the equivalent circuit shown in Figure 9.

$$V_{D_1} = V_{L_1} = V_{in} + V_{C_1} - V_{C_2} \tag{28}$$

$$= V_{in} + \frac{V_{in}D(D-2)}{2(1-D)^2} - \frac{V_{in}(D-2)}{2(1-D)^2} \tag{29}$$

$$= V_{in} + V_{in}\frac{D(D-2)}{2(1-D)^2}[D-1]. \tag{30}$$

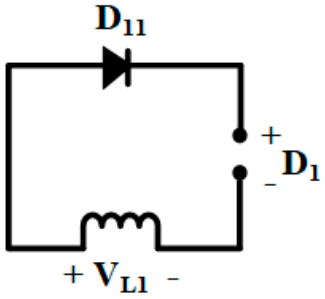


Figure 9. HG-SIQBC—equivalent circuit to find the voltage stress across diode D_1.

Therefore,

$$V_{D1} = V_{in}\left[\frac{3D-4}{2(D-1)}\right]. \tag{31}$$

Similarly, the voltage stress across other diodes is determined using the following expressions:

$$\begin{cases} V_{D_{11}} = \frac{V_{in}}{2} \\ V_{D_{12}} = \frac{V_{in}}{2} \\ V_{D_2} = \left(\frac{D(D-2)}{2(1-D)^2}\right)V_{in} \\ V_{D_3} = \left(\frac{D-2}{2(1-D)}\right)V_{in} \end{cases} \quad \begin{cases} V_{D_4} = \left(\frac{(D-2)}{2(1-D)^2}\right)V_{in} \\ V_{D_5} = \left(\frac{D-2}{2(1-D)}\right)V_{in} \\ V_{D_6} = \left(\frac{(D-2)(D-3)}{2(1-D)^2}\right)V_{in} \end{cases}. \tag{32}$$

2.4. Current Stress of Switches and Diodes for HG-SIQBC

The current of the switch is given by the following equation [18]:

$$I_{sw} = (I_{in} + I_{C_2})D. \tag{33}$$

Similarly, the current stress of the diodes can be calculated by applying KCL to Figures 5 and 6. For example, the current stress of the diode D_1 is given as

$$I_{D_1} = I_{in} = D\left(\frac{(D-2)^2}{2(1-D)^2}\right)\frac{V_0}{R}. \tag{34}$$

Similarly,

$$I_{D_2} = I_{in} + I_{C_3} \tag{35}$$

$$= \left(\frac{(D-2)^2}{2(1-D)^2}\right)\frac{V_0}{R} + \left(\frac{D}{1-D}\right)\frac{V_0}{R}. \tag{36}$$

Therefore,

$$I_{D_2} = \left(\frac{4-D(D+2)}{2(D-1)^2}\right)\left(\frac{V_0}{R}\right). \tag{37}$$

In the same manner, the current stress on other diodes is determined as given below.

$$\begin{cases} I_{D_{11}} = \frac{(D-2)^2}{4(1-D)^2}\left(\frac{V_0}{R}\right) \\ I_{D_{12}} = \frac{(D-2)^2}{4(1-D)^2}\left(\frac{V_0}{R}\right) \\ I_{D_3} = \left(\frac{D(-7D^2+8D-4)}{4D^2-6D+2}\right)\frac{V_0}{R} \end{cases}, \begin{cases} I_{D_4} = \left(\frac{3(D-2)D+4}{2-4D}\right)\frac{V_0}{R} \\ I_{D_5} = \left(\frac{D^2}{1-D}\right)\frac{V_0}{R} \\ I_{D_6} = D\frac{V_0}{R} \end{cases}. \tag{38}$$

2.5. Design Consideration of HG-SIQBC Configuration

2.5.1. Current Ripple of Inductors for HG-SIQBC

The current of all inductors increases as the input voltage is applied. The peak-to-peak ripple in the current of inductors L_1, L_2, and L_3 can be derived as follows:

$$\begin{cases} \Delta I_{L_1} = \frac{V_{L_1}}{L_1}DT_s = \frac{DV_{in}}{2L_1f_s} \\ \Delta I_{L_2} = \frac{V_{L_2}}{L_2}DT_s = \frac{DV_{in}}{2L_2f_s} \\ \Delta I_{L_3} = \frac{V_{L_3}}{L_3}(1-D)T_s = \frac{D(D-2)V_{in}}{2(1-D)L_3f_s} \end{cases}, \tag{39}$$

where f_s is the switching frequency of the power switches.

The design values of inductors are calculated with the known values of D, V_{in}, and f_s.

2.5.2. Voltage Ripple of Capacitors for HG-SIQBC

The voltage ripple of the capacitors C_1, C_2, C_3, and C_0 is calculated using the current given in Equations (3) and (6); substituting the values of I_{C1}, I_{C2}, I_{C3}, and I_{C0}, we get

$$\begin{cases} \Delta V_{C_1} = \frac{I_{C_1}}{C_1}(1-D)T_s = \frac{V_0(3D^2+6D-4)}{R*2(1-2D)^2C_1f_s} \\ \Delta V_{C_2} = \frac{I_{C_2}}{C_2}DT_s = \frac{V_0D(3D^2+6D-4)}{R*2(1-2D)^2(D-1)C_2f_s} \\ \Delta V_{C_3} = \frac{I_{C_3}}{C_3}(1-D)T_s = \frac{V_0D^2}{RC_3f_s} \\ \Delta V_{C_0} = \frac{I_{C_0}}{C_0}DT_s = \frac{V_0D}{RC_0f_s} \end{cases}. \tag{40}$$

2.6. Efficiency Analysis of HG-SIQBC Configuration

To determine the efficiency of the proposed HG-SIQBC converter, the power losses due to the inductors, capacitors, diodes, and switch are calculated as described below.

The power losses of the inductor can be derived as

$$\sum_{i=1}^{3} P_{L_i} = R_{L_1} * I^2{}_{L_i,rms}. \tag{41}$$

The power losses of the capacitor can be derived as

$$\sum_{i=0}^{3} P_{C_i} = R_{C_1} * I^2{}_{C_i,rms}. \tag{42}$$

The power losses of the capacitor can be derived as

$$\sum_{i=1}^{6} P_{D_i} = \sum R_{FD_1} * I^2{}_{D_i,rms} + \sum V_{FD_1} * I_{D_i}. \tag{43}$$

The total power loss of the converter is given by

$$P_{Total} = P_{R_{DS}} + P_{SW}, \tag{44}$$

$$P_{R_{DS}} = I^2{}_{sw} * R_{DS}, \tag{45}$$

$$P_{SW} = V^2{}_{sw} * C_s * f_s, \tag{46}$$

where P_{RDS} is the conduction loss, P_{SW} is the switching loss, V_{sw} is the voltage stress of the switch, I_{sw} is the current stress of the switch, f_s is the switching frequency, R_{DS} is the ON state resistance of the switch, and C_s is the parasitic switch capacitance.

Then, the efficiency of the proposed HG-SIQBC converter can be calculated as follows:

$$\eta_{\text{Proposed HG-SIQBC}} = \frac{P_0}{P_0 + P_L + P_C + P_D + P_{Total}}. \tag{47}$$

The converter loss breakdown chart for the HG-SIQBC topology is shown in Figure 10.

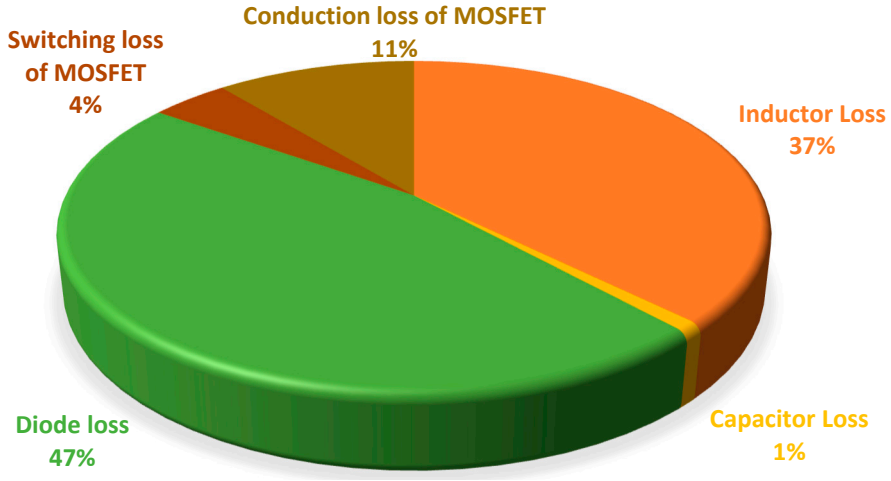


Figure 10. Converter loss breakdown chart for HG-SIQBC topology.

2.7. Simulation Results of Proposed HG-SIQBC

To observe the performance of the converter, simulations were performed using the MATLAB/SIMULINK tool. The following parameters were considered for the simulation: for a 1 kW system, DC input voltage = 75 V, output voltage = 400 V, inductor $L_1 = L_2 = 2.8$ mH, $L_3 = 50$ µH, capacitor $C_1 = 100$ µF, $C_2 = C_3 = 50$ µF, $C_0 = 470$ µF, load resistance $R_L = 160$ Ω, and switching frequency $f_s = 10$ kHz.

The closed-loop control system for the proposed HG-SIQBC with a PI-based voltage controller is presented in Figure 11. The PI controller parameters K_p and K_i were chosen as 0.001 and 0.1 respectively. The output voltage (V_0) was compared with the reference voltage, generating an error signal. This error (e_1) was processed in the PI controller. The output of this controller was compared with a high-frequency repeating sequence signal, and the required PWM signal for the switch was generated. To match with the rating of the

DC bus voltage, the reference voltage (V_{ref}) was considered as 400 V. The performance of the converter was analyzed in terms of rise time, settling time, overshoot (%), and regulation (%), corresponding to the load variation for three different values of input voltages. The plot for output voltage response and load current of the converter concerning variations in load resistance is shown in Figure 12.

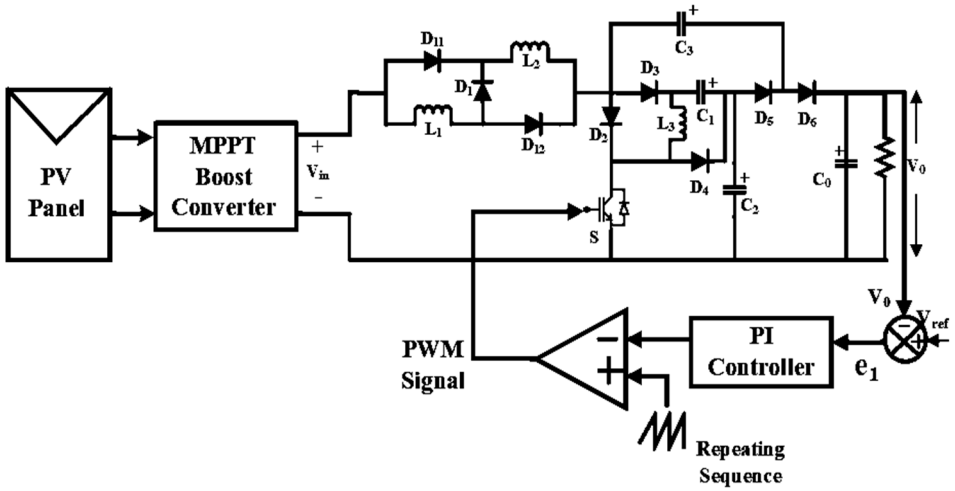


Figure 11. Block diagram of closed-loop control for proposed HG-SIQBC.

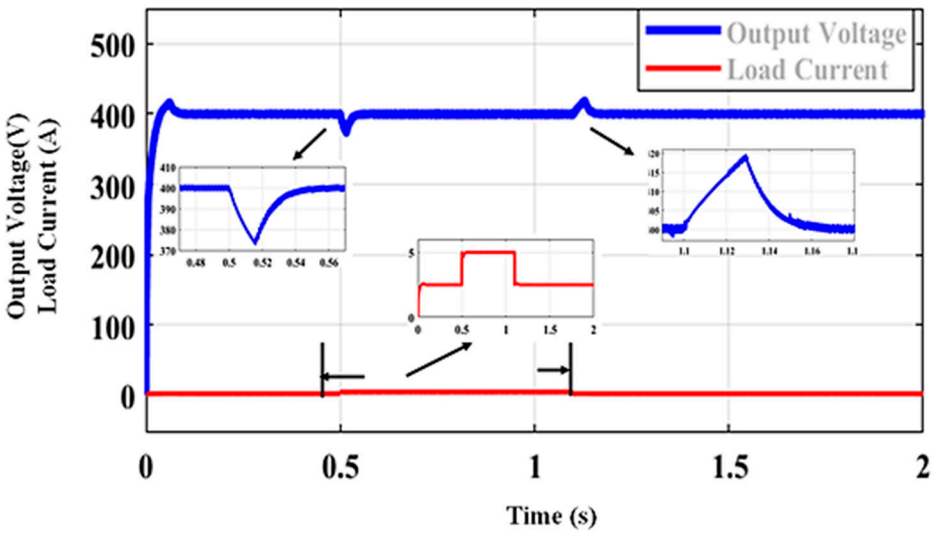


Figure 12. HG-SIQBC-output voltage and current when subjected to a load change for V_{in} = 75 V.

At t = 0.5 s, an undershoot of 7.5% of V_0 occurred with a step increase in load from 2.5 A to 5 A. The output voltage returned to the steady state within 0.04 s. Similarly, an overshoot of 5% of V_0 occurred at t = 1.2 s with a step decrease in load from 5 A to 2.5 A. The output voltage returned to the steady state within 0.06 s. Thus, the proposed converter is well suited for integrating PV with the DC grid. Hence, the performance was analyzed by considering the change in input voltage due to a change in irradiance. For each input voltage range, the load was varied from 160 Ω to 320 Ω with a step increase of 20 Ω. The performance parameters for the proposed HG-SIQBC are calculated and presented in Tables 2–4.

Table 2. Performance parameters of proposed HG-SIQBC for V_{in} = 75 V.

V_{in} = 75 V				V_{ref} = 400 V	
R (Ω)	**Rise Time (s)**	**Setting Time (s)**	**Overshoot (%)**	**Regulation (%)**	**Measured Output (V)**
160	0.035	0.15	10	0.05	399.8
180	0.035	0.15	10.5	0	400
200	0.035	0.155	10.875	0.025	399.9
220	0.035	0.16	11.125	0.25	399
240	0.034	0.17	11.45	0.25	399
260	0.032	0.175	11.625	0	401.3
280	0.032	0.175	11.95	0.175	399.3
300	0.032	0.178	12.075	0	401.6
320	0.033	0.178	12.2	0.05	399.8
80	0.04	0.13	5.5	0.1	399.6

Table 3. Performance parameters of proposed HG-SIQBC for V_{in} = 150 V.

V_{in} = 150 V				V_{ref} = 400 V	
R (Ω)	**Rise Time (s)**	**Setting Time (s)**	**Overshoot (%)**	**Regulation (%)**	**Measured Output (V)**
80	0.004	0.03	1.375	0.075	399.7
160	0.00346	0.05	3.4	0.05	399.8
180	0.00346	0.0535	3.5	0	400
200	0.00346	0.006	3.575	0.025	399.9
220	0.00335	0.066	3.75	0.05	399.8
240	0.00334	0.0662	4.2	0.05	399.8
260	0.00335	0.07	4.375	0.05	399.8
280	0.0034	0.08	4.55	0.05	399.8
300	0.0035	0.085	4.55	0.05	399.8
320	0.0033	0.085	4.75	0	400

Table 4. Performance parameters of proposed HG-SIQBC for V_{in} = 250 V.

V_{in} = 250 V				V_{ref} = 400 V	
R (Ω)	**Rise Time (s)**	**Setting Time (s)**	**Overshoot (%)**	**Regulation (%)**	**Measured Output (V)**
160	0.0012	0.008	6.25	0.275	398.9
180	0.00119	0.009	6.35	0.2	399.2
200	0.0011	0.016	6.4375	0	400
220	0.00116	0.018	6.5	0.075	399.7
240	0.00112	0.12	6.56	0.175	399.3
260	0.00115	0.12	6.56	0.175	399.3
280	0.00119	0.125	6.625	0.175	399.3
300	0.00119	0.125	6.6875	0.2	399.2
320	0.0012	0.125	6.725	0.2	399.2
80	0.00115	0.1	5.35	0.2	399.2

From the above tables, it can be observed that the output voltage of the converter is well regulated, becoming settled earlier for wide range of load variations. The output voltage response corresponding to input voltage variation is shown in Figure 13.

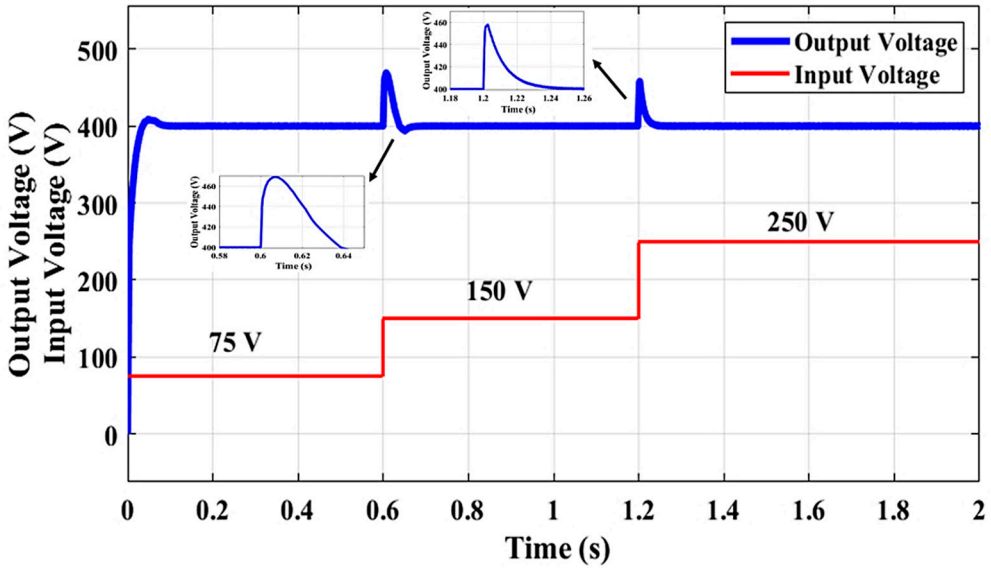


Figure 13. Output voltage response with input voltage variation for proposed HG-SIQBC.

During the time interval of t = 0 to 0.6 s, the input voltage was maintained at 75 V. At t = 0.6 s, an overshoot of 17.5% of V_0 occurred with a step increase in input voltage from 75 V to 150 V, and it settled down to 400 V within 0.04 s. Similarly, an overshoot of 14% of V_0 occurred with a step increase in input voltage from 150 V to 250 V, and the output voltage returned to the steady state within 0.04 s. The respective changes are depicted in Figure 13. Despite the input voltage variation, the output voltage became regulated and returned to the desired level within a fraction of seconds. The output voltage response for a step change in load resistance is given in Figure 14.

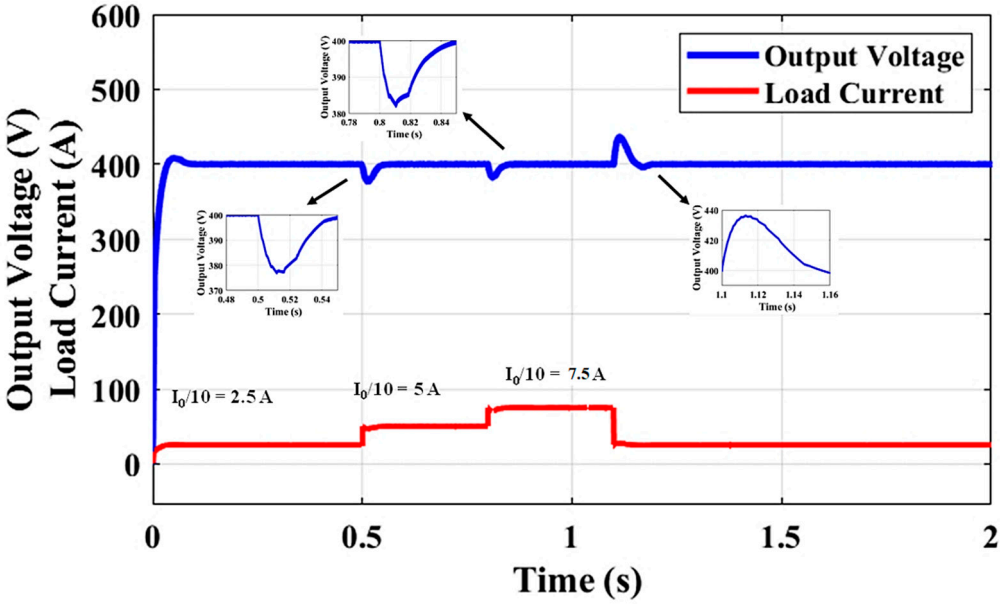


Figure 14. Output voltage response with step change in load resistance for proposed HG-SIQBC for V_{in} = 75 V.

During the time interval of t = 0 to 0.5 s, the output voltage V_0 was in the range of 400 V for a rated load current of 2.5 A. When the load was changed from the rated value, there was a step increase in load current from 2.5 A to 5 A at t = 0.5 s. An undershoot occurred for a minimum duration of 0.04 s before returning to the steady-state value. Again, at t = 0.8 s, the load current increased to 7.5 A with an undershoot of 4.5% of V_0 for 0.045 s.

Finally, the load decreased from 7.5 A to 2.5 A at t = 1.1 s. There was an overshoot of 9.5% of V_0 for a duration of 0.06 s. For the step increase/decrease in load current, V_0 quickly settled down to nominal value. The respective changes are depicted in Figure 14.

From Tables 2–4, it is evident that the proposed converter can operate for a wide range of load variations. It can also operate at the desired conditions for input voltage variations. The parameters such as rise time, settling time, overshoot, and regulation were analyzed. A graphical representation of these parameters with respect to load resistance change is given in Figure 15a–c.

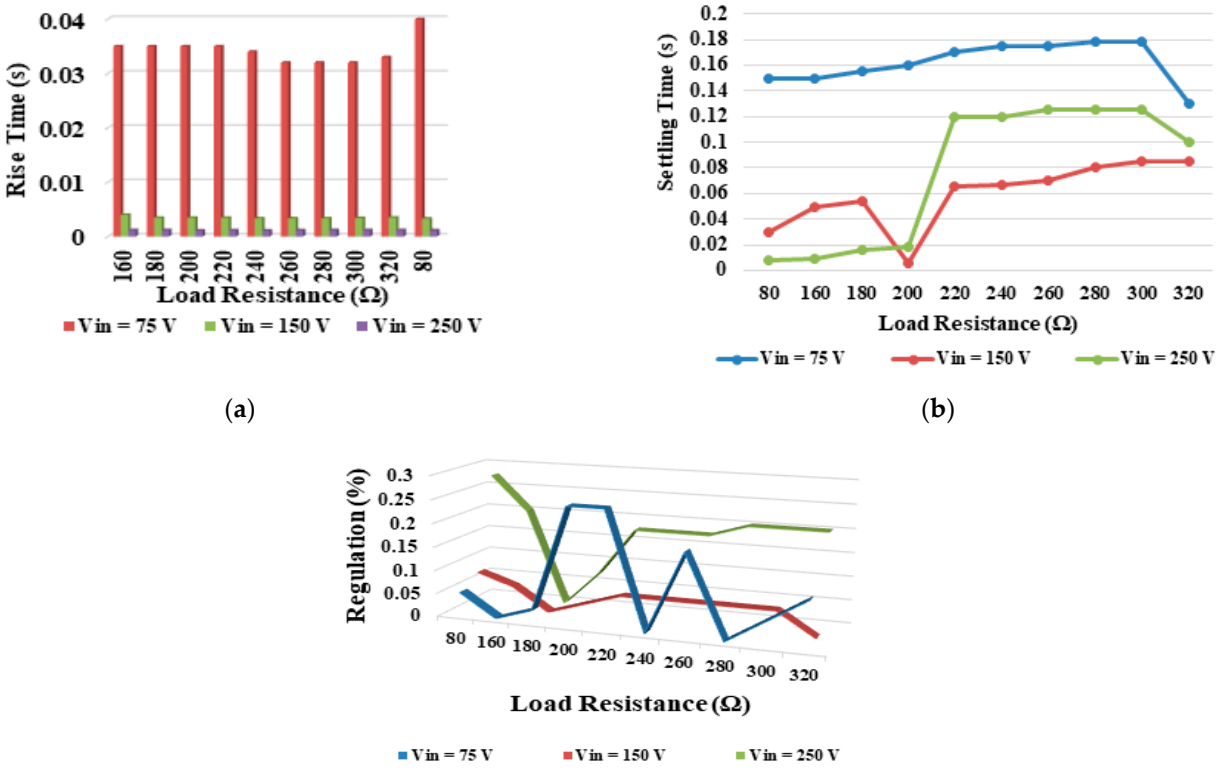


Figure 15. Performance analysis of HG-SIQBC: (**a**) rise time; (**b**) settling time; (**c**) regulation.

3. Modified Multilevel Inverter

The proposed inverter is a combination of a cascaded H-bridge inverter and symmetrical semiconducting switches. The switches in the H-bridge topology operate with a frequency of 50 Hz, while other switches operate with a frequency of 100 Hz. Two different frequencies are used, and the stepped voltage waveform is obtained. Thus, it can also be called a hybrid switching inverter. The circuit configuration is shown in Figure 16.

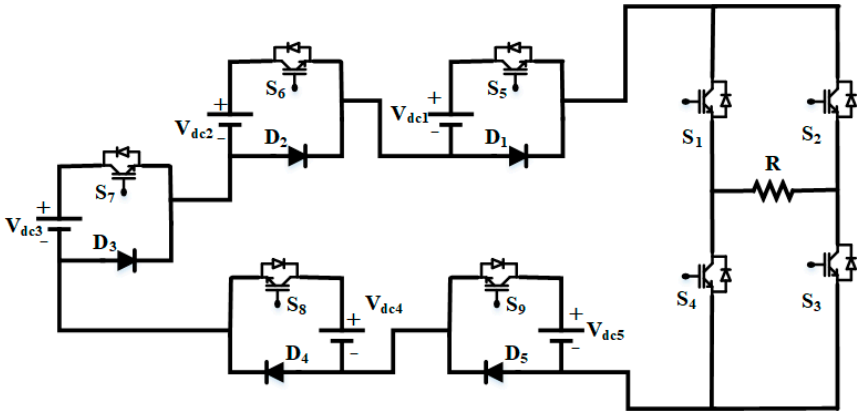


Figure 16. Circuit configuration of proposed multilevel inverter.

The switching sequence for the proposed MLI is given in Table 5.

Table 5. Switching sequence for proposed MLI.

Voltage Levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
$5\ V_{dc}$	1	0	1	0	1	1	1	1	1
$4\ V_{dc}$	1	0	1	0	1	1	1	1	0
$3\ V_{dc}$	1	0	1	0	1	1	1	0	0
$2\ V_{dc}$	1	0	1	0	1	1	0	0	0
V_{dc}	1	0	1	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	0
$-V_{dc}$	0	1	0	1	1	0	0	0	0
$-2\ V_{dc}$	0	1	0	1	1	1	0	0	0
$-3\ V_{dc}$	0	1	0	1	1	1	1	0	0
$-4\ V_{dc}$	0	1	0	1	1	1	1	1	0
$-5\ V_{dc}$	0	1	0	1	1	1	1	1	1

Modes of Operation

For the positive cycle, to obtain a voltage level of 5 V_{dc}, the switches S_1 and S_3 of the H-bridge are kept in the ON state, and the switches S_5–S_9 are also turned on to produce the positive level of the output voltage. The equivalent circuit for this mode is shown in Figure 17a. Figure 17b shows the equivalent circuit of stage II operation of a multilevel inverter. In this stage, to obtain the voltage level of 4 V_{dc}, the switches S_1 and S_3 of the H-bridge are kept in the ON state, and the switches S_5–S_8 are also turned ON. Here, the diode connected in an antiparallel manner with S_9 is forward-biased, and the current flows through it. From Figure 17c, a voltage of 3 V_{dc} is obtained by turning ON the switches S_1 and S_3 of the H-bridge and the switches S_5–S_7. The current flows through the diodes associated with S_8 and S_9 switches. To obtain the voltage of 2 V_{dc}, the switches S_1 and S_3 of the H-bridge are in the ON state, and the bidirectional switches S_5–S_6 are also turned ON. The diodes connected in antiparallel with S_7, S_8, and S_9 become forward-biased due to the flow of current passing through it. The equivalent circuit for this mode is shown in Figure 17d. To obtain a positive level voltage V_{dc}, the switches S_1 and S_3 of the H-bridge are in the ON state and the bidirectional switch S_5 is also turned on to produce a positive level of the output voltage. The diodes connected with the switches S_6, S_7, S_8, and S_9 are in conduction mode due to the flow of current through them. The equivalent circuit for this mode is shown in Figure 17e.

Similarly, the negative cycle operation occurs with S_2 and S_4 in the ON condition. The equivalent circuit for this mode is shown in Figure 18a–e.

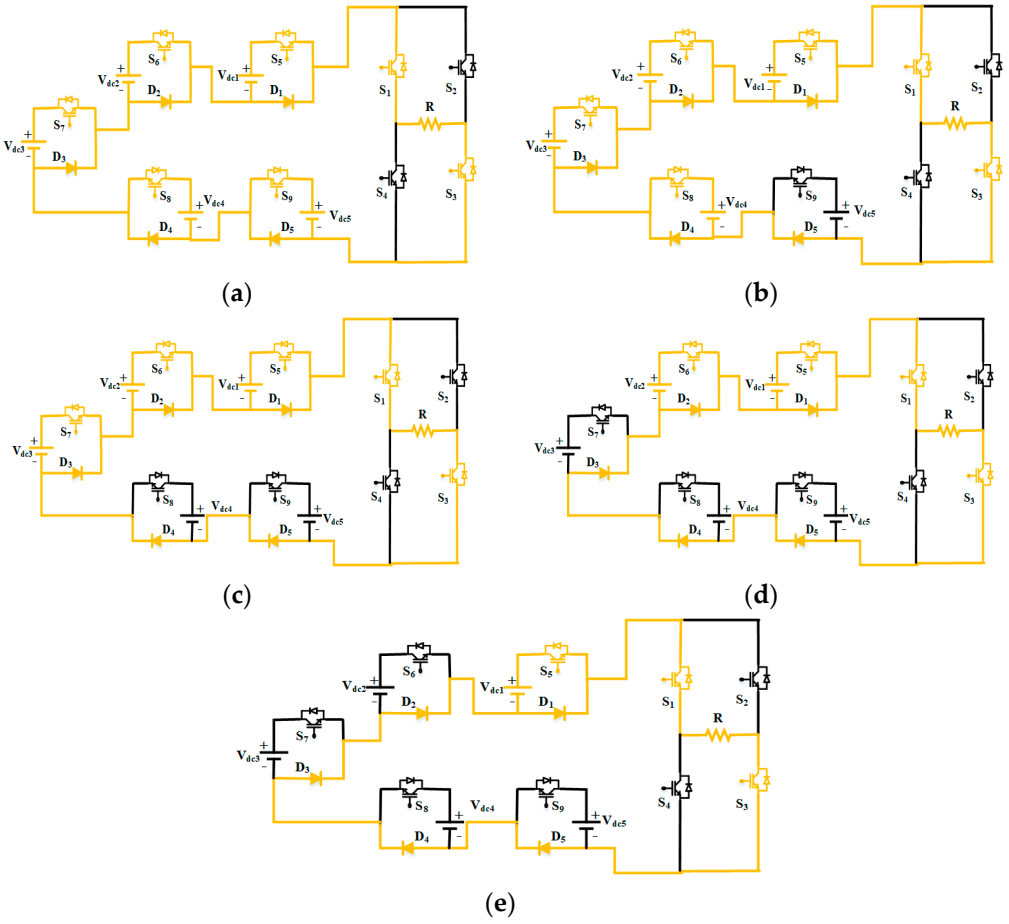


Figure 17. (**a**–**e**) Equivalent circuit for different modes during positive cycle of output voltage.

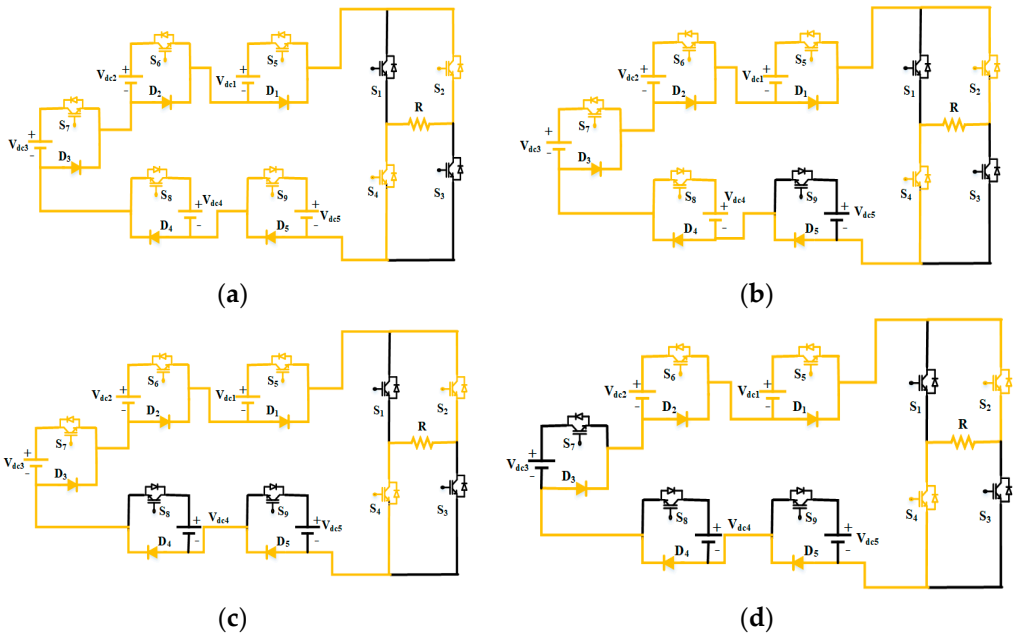
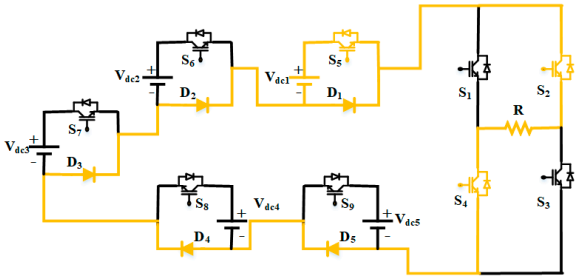


Figure 18. *Cont.*



(**e**)

Figure 18. (**a**–**e**) Equivalent circuit for different modes during negative cycle of output voltage.

The pulse pattern waveform and the output voltage waveform simulated in MATLAB/SIMULINK are given in Figure 19.

The pulse pattern for switches S_1–S_4 is shown on the first four axes of the figure, followed by the pulse patterns of switches S_5–S_9. The waveform shown on the last axis describes the output voltage of the 11-level inverter.

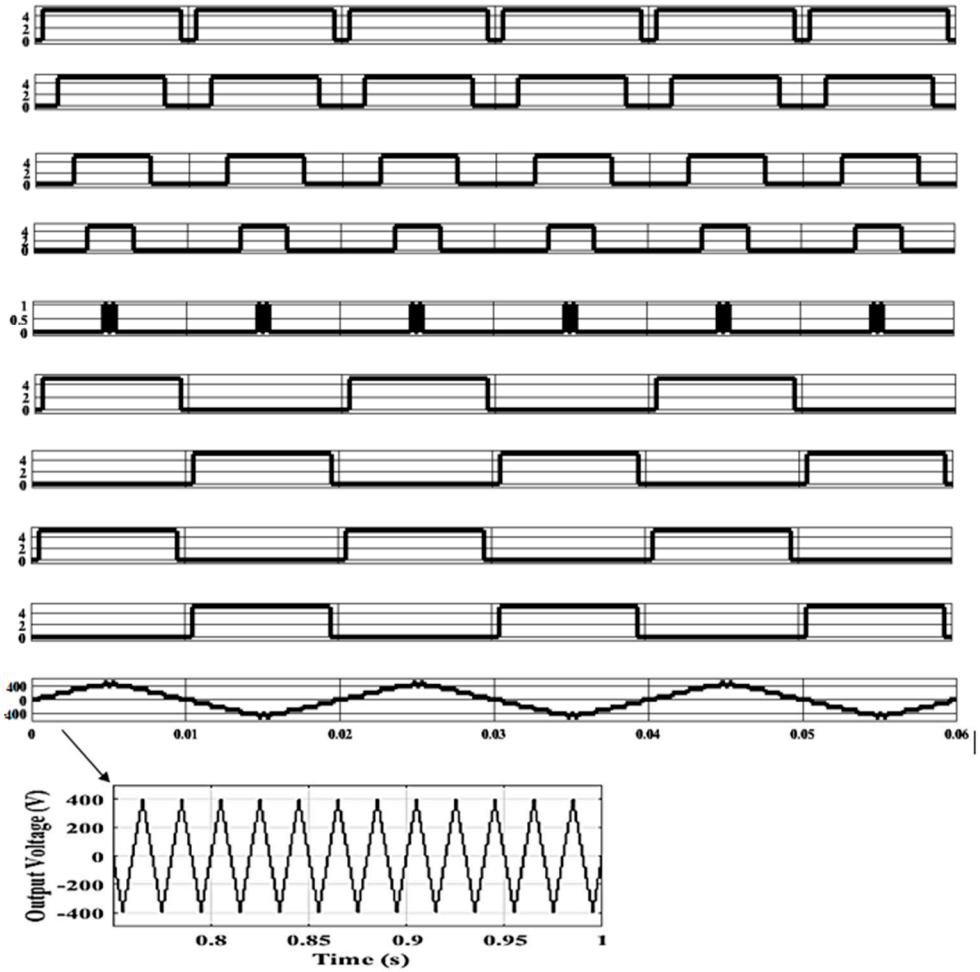


Figure 19. Pulse waveforms and output voltage waveform of the proposed inverter.

4. Hardware Results of Five-Level Modified Multilevel Inverter

The design of a modified multilevel inverter with a single source was carried out for delivering five levels of output voltage. To generate the required output voltage level, the circuit diagram shown in Figure 16 was modified with a single DC source with an H- bridge comprising switches S_1–S_4 and power semiconductor switches S_5 and S_6. To verify the

theoretical results and to analyze the performance of the system, the proposed inverter was tested experimentally for the following input and output data specifications: V_{dc} = 60 V, V_{ac} = 60 V, with a fundamental switching frequency of 50 Hz for H-bridge and 100 Hz for the switches S_5 and S_6. The value of the capacitors C1, C_2, and C_3 was 0.1 F. The hardware setup of the multilevel inverter with five levels is shown in Figure 20. The proposed design was fed with a DC supply voltage of 60 V using a regulated power supply (RPS), and an output of 60 V AC was generated. The SPARTAN FPGA controller provided the necessary gating signals for the MOSFETs connected to the inverter circuit. The gate pulse waveforms of different switches are shown in Figure 21. The output values were also measured and analyzed with the help of a digital storage oscilloscope.

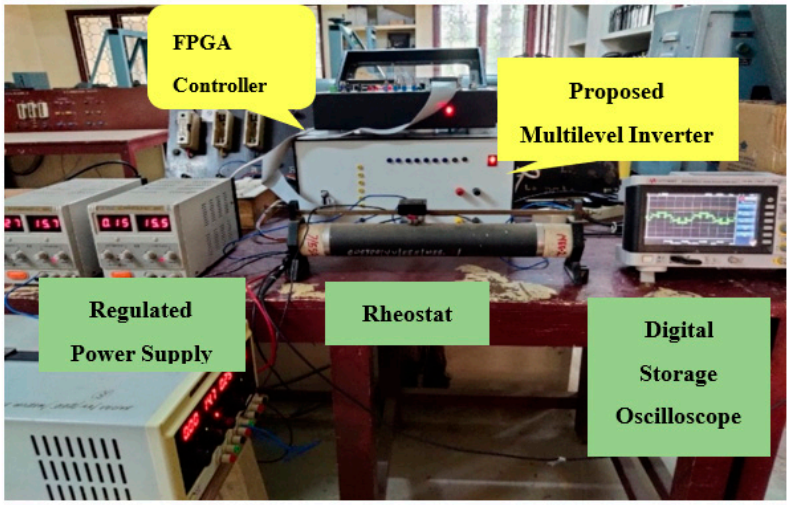


Figure 20. Hardware setup for proposed multilevel inverter.

Figure 21. Gate pulses for switches S_1–S_6.

Figure 22 shows that the proposed inverter produced an output voltage two times greater than the given input. This reduced switch multilevel inverter is highly recommended for PV, grid-connected, and EV applications.

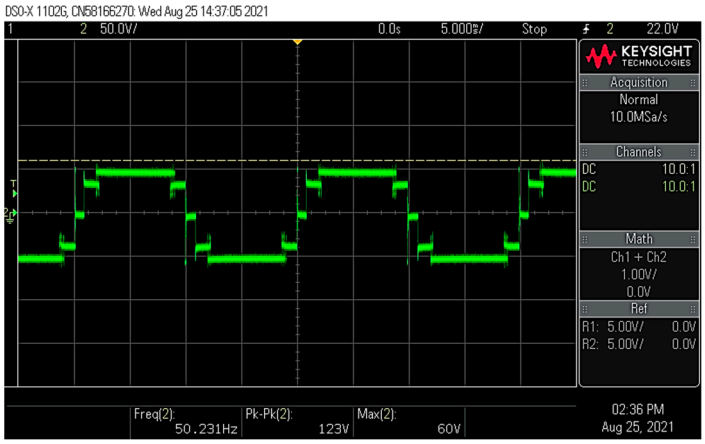


Figure 22. Output voltage waveform (five levels).

5. Conclusions

In this paper, different configurations of power electronic converters were proposed and analyzed with the controllers. A novel HG-SIQBC topology was designed and developed in a MATLAB/SIMULINK environment. The voltage stress across the main switch was low and found to be 4.25% of the total losses. The efficiency calculation of the proposed topology shows that the proposed converter had a better efficiency of 91.31%. The HG-SIQBC topology investigated in this paper was tested for a change in input voltage, as well as for a change in load conditions. The controller performance was also analyzed for a wide range of loads. The equivalent output level of the novel converter topology was fed to a modified five-level inverter using a regulated power supply and tested experimentally. It can be extended for higher-level configurations. Thus, suitable configurations for microgrid applications were designed and tested under different conditions.

Author Contributions: Conceptualization, S.P.S. and S.S.R.; Data curation, S.P.S., S.N. and E.R.C.; Formal analysis, S.P.S., S.S.R. and U.S.; Investigation, S.P.S., S.S.R. and E.R.C.; Methodology, S.P.S. and U.S.; Project administration, S.S.R., S.N., U.S. and T.S.; Resources, S.S.R.; Supervision, S.S.R., S.N., E.R.C. and T.S.; Validation, S.P.S., S.N. and E.R.C.; Visualization, S.P.S., S.S.R., S.N. and U.S.; Writing—original draft, S.P.S.; Writing—review & editing, S.P.S., S.S.R., S.N., U.S., E.R.C., T.S. and S.P.S. performed the experiment and carried out the research under the supervision and direction of S.S.R., S.N., U.S., E.R.C. and T.S. All authors have contributed equally in terms of validation, verification, research, and writing. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Hartono, B.S.; Budiyanto, Y.; Setiabudy, R. Review of microgrid technology. In Proceedings of the 2013 International Conference on Quality in Research, QiR 2013—In Conjunction with ICCS 2013: The 2nd International Conference on Civic Space, Yogyakarta, Indonesia, 25–28 June 2013; pp. 127–132.
2. Anand, S.; Fernandes, B.G. Optimal voltage level for DC microgrids. In Proceedings of the IECON Proceedings (Industrial Electronics Conference), Glendale, AZ, USA, 7–10 November 2010; pp. 3034–3039.

3. Iskender, I.; Genc, N. Power Electronic Converters in DC Microgrid. In *Microgrid Architectures, Control and Protection Methods*; Springer: Cham, Switzerland, 2020; pp. 115–137.
4. Bose, S.; Liu, Y.; Bahei-Eldin, K.; de Bedout, J.; Adamiak, M. Tieline controls in microgrid applications. In Proceedings of the 2007 iREP Symposium-Bulk Power System Dynamics and Control—VII, Revitalizing Operational Reliability, Charleston, SC, USA, 19–24 August 2007.
5. Hamed, H.; Mohammad, M. An integrated interleaved dual-mode time-sharing inverter for single-phase grid-tied applications. *IEEE Trans. Ind. Electron.* **2019**, *66*, 286–296.
6. Liu, L.; Li, H.; Xue, Y.; Liu, W. Decoupled Active and Reactive Power Control for Large-Scale Grid-Connected Photovoltaic Systems Using Cascaded Modular Multilevel Converters. *IEEE Trans. Power Electron.* **2015**, *30*, 176–187. [CrossRef]
7. Sunddararaj, S.P.; Srinivasarangan Rangarajan, S. An Extensive Review of Multilevel Inverters Based on Their Multifaceted Structural Configuration, Triggering Methods and Applications. *Electronics* **2020**, *9*, 433. [CrossRef]
8. Vijeh, M.; Rezanejad, M.; Samadaei, E.; Bertilsson, K. A General Review of Multilevel Inverters Based on Main Submodules: Structural Point of View. *IEEE Trans. Power Electron.* **2019**, *34*, 9479–9502. [CrossRef]
9. Lai, J.S.; Peng, F.Z. Multilevel converters—A new breed of power converters. *IEEE Trans. Ind. Appl.* **1996**, *32*, 509–517.
10. Tolbert, L.; Peng, F. Multilevel converters for large electric drives. *IEEE Trans. Ind. Appl.* **1999**, *35*, 36–44. [CrossRef]
11. Kouro, S.; Malinowski, M.; Gopakumar, K.; Pou, J.; Franquelo, L.G.; Wu, B.; Rodriguez, J.; Perez, M.A.; Leon, J.I. Recent Advances and Industrial Applications of Multilevel Converters. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2553–2580. [CrossRef]
12. Erickson, R.W.; Maksimovic, D. *Fundamentals of Power Electronics*, 3rd ed.; Springer: New York, NY, USA, 2014.
13. Gorji, S.A.; Mostaan, A.; Tran My, H.; Ektesabi, M. Non-isolated buck–boost dc–dc converter with quadratic voltage gain ratio. *IET Power Electron.* **2019**, *12*, 1425–1433. [CrossRef]
14. Leyva-Ramos, J.; Ortiz-Lopez, M.G.; Diaz-Saldierna, L.H.; Morales-Saldana, J.A. Switching regulator using a quadratic boost converter for wide DC conversion ratios. *IET Power Electron.* **2009**, *2*, 605–613. [CrossRef]
15. Saravanan, S.; Babu, N.R. Design and Development of Single Switch High Step-Up DC–DC Converter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2018**, *6*, 855–863. [CrossRef]
16. Wu, G.; Ruan, X.; Ye, Z. Nonisolated High Step-Up DC–DC Converters Adopting Switched-Capacitor Cell. *IEEE Trans. Ind. Electron.* **2015**, *62*, 383–393. [CrossRef]
17. Banaei, M.R.; Ghabeli Sani, S. Analysis and Implementation of a New SEPIC-Based Single-Switch Buck–Boost DC–DC Converter with Continuous Input Current. *IEEE Trans. Power Electron.* **2018**, *33*, 10317–10325. [CrossRef]
18. Qin, L.; Zhou, L.; Hassan, W.; Soon, J.L.; Tian, M.; Shen, J. A Family of Transformer-Less Single-Switch Dual-Inductor High Voltage Gain Boost Converters with Reduced Voltage and Current Stresses. *IEEE Trans. Power Electron.* **2021**, *36*, 5674–5685. [CrossRef]
19. Zhang, N.; Zhang, G.; See, K.W.; Zhang, B. A Single-Switch Quadratic Buck–Boost Converter with Continuous Input Port Current and Continuous Output Port Current. *IEEE Trans. Power Electron.* **2018**, *33*, 4157–4166. [CrossRef]
20. Maroti, P.K.; Padmanaban, S.; Holm-Nielsen, J.B.; Bhaskar, M.S.; Meraj, M.; Iqbal, A. A New Structure of High Voltage Gain SEPIC Converter for Renewable Energy Applications. *IEEE Access* **2019**, *7*, 89857–89868. [CrossRef]
21. Nguyen, M.H.; Kwak, S. Enhance Reliability of Semiconductor Devices in Power Converters. *Electronics* **2020**, *9*, 2068. [CrossRef]