Design of Parasitic-Insensitive Bilinear-Transformed Admittance-Scaled (BITAS) SC Ladder Filters

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Abstract—**A new method for the design of parasitic-insensitive switched-capacitor (SC) ladder filters is described. The filters are derived from analog *LC* prototypes utilizing the bilinear *z*-transform. The method is based on the signal-flowgraph (SFG) concept in the discrete-time domain. The resulting networks preserve the frequency response and low sensitivity properties of the equivalent continuous-time *LC* filters.**

I. INTRODUCTION

RECENT developments in MOS technology and the resulting feasibility of sampled-data networks using this technology are setting new horizons for the design of active filters based on the switched-capacitor (SC) concept. Numerous procedures for the design of SC filters have been proposed so far [1]–[14]. In most cases, the design is based on the simulation of an analog filter by converting it into the discrete-time domain utilizing a sampled-data transformation. In one approach, *LC* filters are simulated either by replacing inductors and capacitors by SC integrators using the corresponding signal flowgraph (SFG) (active ladder or leapfrog design) [1]–[3], or by converting the series and shunt branches of analog filter models into the corresponding voltage-controlled current sources (VCS's) and integrators [4]. Other methods use either capacitors and voltage inverter switches (i.e., they are based on the resonant-transfer principle [5]) or FDNR and gyrator simulations [6], [7]. In another important class of design techniques, the transfer functions are realized either by cascading second-order building blocks or coupled-biquad structures [8]–[11].

A comparison of these design methods has shown that the active ladder structures, realized in SC form using the bilinear *z*-transform, are a particularly good choice for the realization of high-quality filters. Unfortunately, however, such filters are generally not insensitive to stray capacitances and therefore not useable in MOS IC form.

In this paper, a new technique for the design of SC ladder filters is introduced that combines the advantages of the bilinear *z*-transform with the characteristics of stray-insensitive circuit configurations. In particular, the method takes the following two important design considerations into account:

i) The filter circuits are completely stray-insensitive. This is achieved by using either stray-insensitive biquads or first-order low-pass building blocks of the kind shown in Fig. 1. The transfer function of this circuit can readily be derived (e.g., by indefinite-admittance matrix (IAM) [15]), and is given by

$$V_4^e = \frac{C_1(C_5+C_7)z^{-2}}{\Delta} V_1^e - \frac{C_2(C_4+C_5)(1-z^{-2})}{\Delta} V_2^e - \frac{C_3(C_4+C_5)}{\Delta} V_3^e \quad (1)$$

where

$$\Delta = (C_4+C_5)(C_5+C_6) - C_5(C_5+C_7)z^{-2}.$$

The individual terms in this expression can be interpreted as ratios of discrete-time impedances. Integrator-summer building blocks (lossy or lossless) such as those suggested in [3] can be realized using the circuit in Fig. 1. Its SFG representation is shown in Fig. 2.

ii) The SC circuits can be derived from passive *RLC* ladder filters, by applying the bilinear *s*- to *z*-transform:

$$s \rightarrow \frac{1}{\tau}\frac{1-z^{-2}}{1+z^{-2}} \quad (2)$$

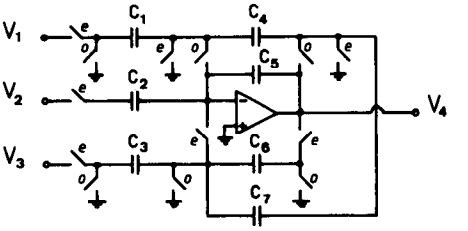

Fig. 1. First-order low-pass building block.

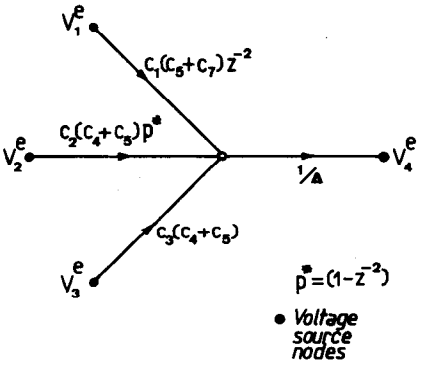

Fig. 2. The SFG representation of Fig. 1.

Manuscript received October 6, 1982; revised February 4, 1983.
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0098-4094/83/1200-0873$01.00

where $z=\exp(s\tau)$ and $\tau=1/2f_s$ (f_s is the sampling frequency).

As is well known, ladder structures are generally preferred for high-quality filters because of their low sensitivity to component variations. Being derived from passive *RLC* ladder filters, the bilinear z-transformed SC filters retain this important property.

II. A Frequency-Dependent Immittance Transformation

In the design procedure to be described in the next section, starting from an analog *LCR* prototype ladder filter, each branch admittance is transformed from the s- to the z-plane by applying the bilinear z-transform, i.e., (2). The resulting SC integrators are susceptible to stray-capacitive effects, which is in contradiction with our stipulation i) above. In order to overcome this drawback we now apply a frequency-dependent scaling factor S to each bilinearly transformed branch of the filter. The resulting branches are realizable by so-called backward- and forward-difference integrators, both of which are realizable in stray-insensitive form [3].

The use of scaling techniques, e.g., using a scaling factor S, is well known in classical network theory. If all branch admittances y_i of a network are replaced by the uniformly scaled admittances y_i/S, then all network functions will be scaled accordingly; in particular, transfer admittances Y (or transfer impedances Z) will become Y/S (or SZ), while voltage and current transfer functions will remain unaltered. The problem at hand was to find a scaling factor S, i.e., a frequency-dependent admittance transformation, which, when applied to the bilinearly transformed reactances obtained from the *LCR* prototype filter, would result in reactances corresponding to backward- and forward-difference transformations. A scaling factor satisfying this requirement is [20]

$$S=1/\tau(1+z^{-2}). \tag{3}$$

Note that S has the dimension of frequency.

In Table I the corresponding admittance transformation, converting bilinearly transformed reactances into a combination of reactances obtained by the backward and forward-difference transformations, is given. Note that capacitors are converted into discrete-time admittances obtainable by the backward-difference transformation, while inductors are transformed into parallel connections of reactances obtainable by backward- and forward-difference transformations. Consequently, the branch transmittances of the resulting discrete-time SFG consist of *stray-insensitive difference integrators* which are realizable by the general building block depicted in Fig. 1.

One disadvantage of this transformation would seem to be that resistors in the continuous-time filter are converted into frequency-dependent impedances in the discrete-time domain, i.e., that resistively terminated filters in the s-domain are transformed into generally terminated filters in the z-domain. Fortunately, as will be shown, these general terminations can be realized, requiring neither supplementary predistortion (beside $\tanh(sT)$ prewarping, due to the bilinear transformation) nor additional active devices.

The scaling factor given by (3) is not unique, i.e., others exist, each of which results in a different combination of discrete-time reactances. Although the one given by (3) appears to be ideal for the problem at hand, some of the others may be useful, either to compare the resulting circuits with the solutions of other methods, or to obtain some favorable properties in a given design example. Some of them will be discussed in section VII.

III. The General Design Procedure

The conventional procedure for the design of an SC ladder filter involves the transformation of a continuous-time prototype filter into an equivalent discrete-time filter meeting prescribed specifications. Since the approximation methods of analog filter design are highly advanced, yielding useful results in the form of classical filter tables or other numerical design data, it is advantageous to start out using the design techniques already developed for analog *LC* filters. Such filters have a very low sensitivity to component variations. Having obtained an appropriate analog *LC* filter, the bilinear z-transform permits an accurate mapping of the analog filter specifications into the z-domain.

Thus the purpose of our design technique is to combine the favorable properties of passive *LCR* ladder filters with those of the bilinear transformation, while permitting the resulting SC ladder structure to be realized in a stray-insensitive form. This is achieved by carrying out the following design steps.

Step 1:

Solve the approximation problem in the continuous frequency domain and obtain the corresponding *prototype LCR ladder filter* (e.g., from filter tables, computer programs).

Step 2:

Perform the bilinear s- to z-transformation on each branch reactance of the prototype *LCR* filter obtained in Step 1. After subsequently admittance scaling each branch reactance by $S=1/\tau(1+z^{-2})$, the *discrete-time equivalent network* is obtained. This transformation can also be carried out directly by converting the continuous-time reactances into discrete-time reactances according to Table I. The system of equations associated with the transfer characteristics of the equivalent network obtained in this step can be derived using Kirchoff's laws. Consequently, the resulting network equations can be represented graphically by a *discrete-time SFG*. Note that this SFG contains only branch transmittances consisting of backward- and forward-difference integrators (damped or undamped), which, as we have pointed out above, can be realized by parasitic-insensitive circuits.

Step 3:

The *SC ladder equivalent* of the SFG obtained in Step 2 can readily be derived by replacing the branch transmittances by the corresponding integrator-summer circuits.

TABLE I
ADMITTANCE TRANSFORMATION

element	admittance s-domain	admittance z-domain $s \to \frac{1}{\tau}\frac{1-z^{-2}}{1+z^{-2}}$	scaled admittance $Y \to Y/S$	definitions $S=\frac{1}{\tau(1+z^{-2})}$, S = scaling frequency
R	G = 1/R	G	$C_G(1+z^{-2})$	$C_G = \tau G$
C	s C	$\frac{C}{\tau}\frac{1-z^{-2}}{1+z^{-2}}$	$C_C(1-z^{-2})$	$C_C = C$
L	1/s L	$\frac{\tau}{L}\frac{1+z^{-2}}{1-z^{-2}}$	$\frac{\tau^2}{L}\frac{(1+z^{-2})^2}{1-z^{-2}} = C_L\frac{z^{-2}}{1-z^{-2}} + C_{C_L}(1-z^{-2})$	$C_L = \frac{4\tau^2}{L}$ & $C_{C_L} = \frac{\tau^2}{L}$
D	s^2 D	$\frac{D}{\tau^2}\frac{(1-z^{-2})^2}{(1+z^{-2})^2}$	$\frac{D}{\tau}\frac{(1-z^{-2})^2}{1+z^{-2}} = C_D(1-z^{-2}) - 2C_D\frac{z^{-2}(1-z^{-2})}{1+z^{-2}}$ $= C_D(1+z^{-2}) - 4C_D\frac{z^{-2}}{1+z^{-2}}$	$C_D = \frac{D}{\tau}$

The reader may have noticed that this design procedure resembles the so-called leapfrog design method [1]–[3]. Nevertheless, there are some important differences. In the leapfrog synthesis, the SFG of the *continuous-time* prototype filter is derived first. The integrators in this SFG are then replaced by SC integrators applying the LDI transformation. By contrast, in this new technique, the *bilinear z-transform* is carried out first. The SFG and SC equivalent of the discrete-time filter are then derived using the admittance scaling summarized in Table I. Thus this design procedure is based on a *reactance transformation* which converts the reactances in the s-plane into reactances in the z-plane. This leads to a conceptually easy design procedure for active ladder structures: (i) design a prototype filter, (ii) make element substitutions as in Table I and derive the SFG of the transformed filter, (iii) realize the SC equivalent of the SFG.

It should be noted that this design procedure can be applied to any kind of continuous-time *LCR* structures or their FDNR-transformed equivalents. *In fact, any discrete-time network, whose branch impedances have been obtained by the bilinear s- to z-transformation, can be realized with parasitic-insensitive (forward- and backward-difference) integrators by first applying the impedance-scaling factor given by* (3).

In the following three sections, the design procedure outlined above will be illustrated for low-pass, bandpass, and high-pass filters. The general properties of filters obtained by our proposed design technique will then be given in Section VII, followed by some explicit design examples in Section VIII.

IV. Design of Low-Pass Filters

In this section, the synthesis of a fifth-order elliptic low-pass filter is given using the proposed design procedure.

Step 1:

Without loss of generality, we suppose that the desired specifications are fulfilled by the doubly terminated elliptic low-pass filter shown in Fig. 3(a). Note that singly terminated and all-pole networks can also be included as special cases of such filters in that one of the termination resistors, or the feedforward capacitors (C_2 and C_4), will be zero, respectively.

Step 2:

After admittance scaling each branch reactance according to Table I the discrete-time equivalent circuit shown in Fig. 3(b) is obtained. The particular transformation of each component results in "backward"- and "forward-difference" admittances. Note that the structure of the transformed filter remains unchanged.

Applying Kirchhoff's current law to nodes, 1, 3, and 5, the network equations associated with the transfer characteristics are obtained as follows:

$$V_1 = \frac{\alpha_1}{\Delta_1}V_0 + \frac{\alpha_1 z^{-2}}{\Delta_1}V_0 - \frac{\alpha_2(1-z^{-2})}{\Delta_1}V_3' - \frac{\alpha_5 z^{-2}}{\Delta_1\Delta_2}(V_1 + V_3') \tag{4}$$

$$V_3' = -\frac{\alpha_2(1-z^{-2})}{\Delta_3}V_1 - \frac{\alpha_5 z^{-2}}{\Delta_2\Delta_3}(V_1 + V_3') - \frac{\alpha_4(1-z^{-2})}{\Delta_3}V_5 - \frac{\alpha_7 z^{-2}}{\Delta_3\Delta_4}(V_3' + V_5) \tag{5}$$

$$V_5 = -\frac{\alpha_4(1-z^{-2})}{\Delta_5}V_3' - \frac{\alpha_7 z^{-2}}{\Delta_4\Delta_5}(V_3' + V_5) \tag{6}$$

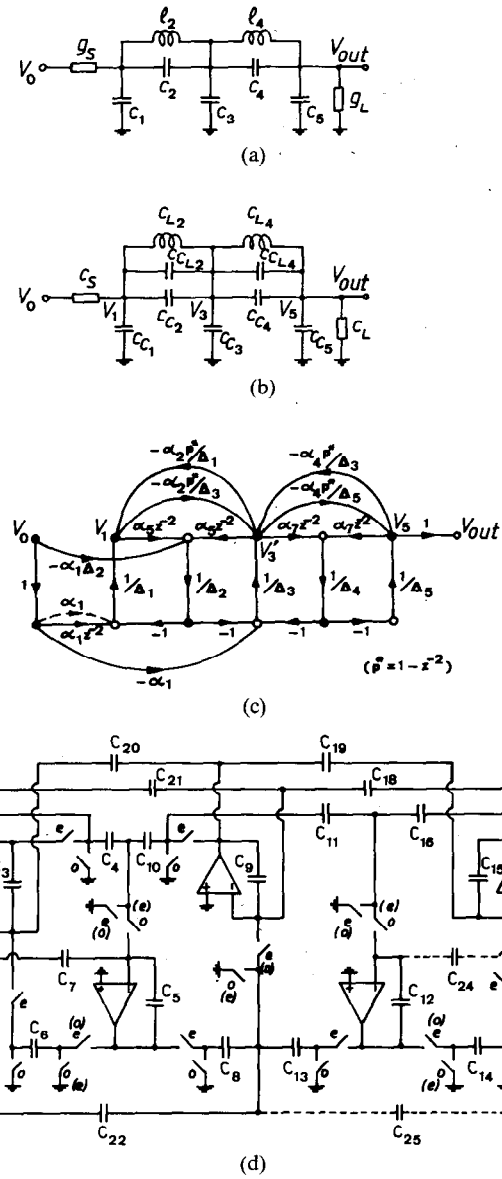

Fig. 3. (a) The doubly terminated elliptic low-pass filter. (b) The bilinear-transformed discrete-time equivalent of Fig. 3(a). (c) SFG of Fig. 3(b). (d) The SC ladder filter.

where

$V_3' = -V_3$

$\Delta_1 = \alpha_3(1-z^{-2})+2\alpha_1 \qquad \Delta_2 = (1-z^{-2})$

$\Delta_3 = \alpha_6(1-z^{-2})$

$\Delta_4 = (1-z^{-2}) \qquad \Delta_5 = \alpha_8(1-z^{-2})+2\alpha_9$

$\alpha_1 = C_s/C_r \qquad \alpha_2 = (C_2 + C_{C_{L2}})/C_r \qquad \alpha_3 = C_1'/C_r$

$\alpha_4 = (C_4 + C_{C_{L4}})/C_r \qquad \alpha_5 = C_{L2}/C_r \qquad \alpha_6 = C_3'/C_r$

$\alpha_7 = C_{L4}/C_r \qquad \alpha_8 = C_5'/C_r \qquad \alpha_9 = C_l/C_r$

$C_1' = C_1 + C_2 + C_{C_{L2}} - C_s$

$C_3' = C_2 + C_{C_{L2}} + C_3 + C_4 + C_{C_{L4}}$

$C_5' = C_4 + C_{C_{L4}} + C_5 - C_l$

$C_i = C_{Ci}$ $(i = 1, \cdots, 5)$, and C_r the normalization capacitor. (7)

In (5), V_3' must be introduced because the feedback and feedforward paths between V_1 and V_3', V_3' and V_5 can be performed only with a sign inversion [1]. The resulting network equations can be represented by the discrete-time SFG of Fig. 3(c). As pointed out in the preceding section, this SFG contains only branch transmittances consisting of backward- and forward-difference integrators (damped or undamped). Another modification associated with the implementation of the frequency-dependent source terminator C_s should be noted. The branch transmittance α_1 shown by the dotted line in the SFG is carried out by the product-transmittance of $(-\alpha_1\Delta_2)$. Consequently, an additional signal, which depends on the input voltage V_0 will be introduced to the input node of the branch transmittance $1/\Delta_3$. This additional signal must also be taken into account and removed by the equal and opposite signal of the transmittance $(-\alpha_1)$. This modification permits the entire SC circuit to be designed insensitive to parasitics.

Step 3:

The SC ladder equivalent of Fig. 3(c) can now be obtained as shown in Fig. 3(d). Note that the circuit given in Fig. 1 is used to obtain the branch transmittances given in (7). The circuit of Fig. 3(d) provides the desired transfer function for "even" input and output, i.e., $H^{ee}(z)$.

Depending on the choice of the scaling factor S, there exists one-to-one relationship between the analog prototype filter (Step 1) and its discrete-time equivalent (Step 2) and between the SFG structure (Step 2) and its SC realization (Step 3). The graphical representation of a discrete-time equivalent, however, is ambiguous, i.e., a number of SFG configurations can be derived by modifying the network equations in Step 2. The actual realization obtained is flexible and can be selected to provide further improvements with regard to the design requirements. Some modified SFG's and SC equivalents of the analog prototype (see Fig. 3(a)), which are of practical interest, will be illustrated here.

First we consider (4)–(6). Multiplying each equation with (-1) we obtain

$$V_1' = -\frac{\alpha_1}{\Delta_1}V_0 - \frac{\alpha_1 z^{-2}}{\Delta_1}V_0 - \frac{\alpha_2(1-z^{-2})}{\Delta_1}V_3 - \frac{\alpha_5 z^{-2}}{\Delta_1\Delta_2}(V_1'+V_3) \tag{8}$$

$$V_3 = -\frac{\alpha_2(1-z^{-2})}{\Delta_3}V_1' - \frac{\alpha_5 z^{-2}}{\Delta_2\Delta_3}(V_1'+V_3) - \frac{\alpha_4(1-z^{-2})}{\Delta_3}V_5' - \frac{\alpha_7 z^{-2}}{\Delta_3\Delta_4}(V_3+V_5') \tag{9}$$

$$V_5' = -\frac{\alpha_4(1-z^{-2})}{\Delta_5}V_3 - \frac{\alpha_7 z^{-2}}{\Delta_4\Delta_5}(V_3+V_5'). \tag{10}$$

The modified network equations require a sign inversion of the input voltage V_0. This sign inversion is accomplished by the SFG in Fig. 4. The resulting representation is a modified version of the SFG in Fig. 3(c) in that some internal transmittance gains are exchanged. The structure of the SFG, however, remains unaltered. This implies changing only some switching phases of the initial SC circuit, as depicted in parantheses in Fig. 3(d).

The frequency-dependent termination impedances of SC networks presented so far have been implemented by damping the input and output integrators. Note that, in the case of singly terminated *LCR* prototype filters, the capacitor C_{17} which simulates a load resistor, will be zero. These terminators can, however, be simulated in various ways. To illustrate an alternative realization, the network equations are modified by adding and subtracting new terms associated with the input and output signals so that all internal integration transmittances $1/\Delta_i$ are undamped. We consider now (8)–(10). Adding the terms $(-2\alpha_1 z^{-2}/\Delta_1)V_1'$ and $(-2\alpha_9 z^{-2}/\Delta_5)V_5'$ to (8) and (10), respectively, the

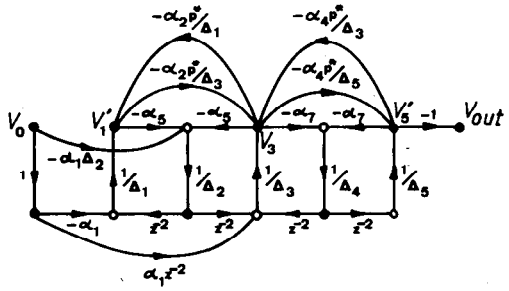

Fig. 4. The modified SFG for the sign inversion of the input voltage V_0.

network equations become

$$V_1' = -\frac{\alpha_1}{\Delta_1^*}V_0 - \frac{\alpha_1 z^{-2}}{\Delta_1^*}V_0 - \frac{\alpha_2(1-z^{-2})}{\Delta_1^*}V_3 - \frac{\alpha_5 z^{-2}}{\Delta_1^*\Delta_2}(V_1'+V_3) - \frac{2\alpha_1 z^{-2}}{\Delta_1^*}V_1' \tag{11}$$

$$V_3 = -\frac{\alpha_2(1-z^{-2})}{\Delta_3}V_1' - \frac{\alpha_5 z^{-2}}{\Delta_2\Delta_3}(V_1'+V_3) - \frac{\alpha_4(1-z^{-2})}{\Delta_3}V_5' - \frac{\alpha_7 z^{-2}}{\Delta_3\Delta_4}(V_3+V_5') \tag{12}$$

$$V_5' = -\frac{\alpha_4(1-z^{-2})}{\Delta_5^*}V_3 - \frac{\alpha_7 z^{-2}}{\Delta_4\Delta_5^*}(V_3+V_5') - \frac{2\alpha_9 z^{-2}}{\Delta_5^*}V_5' \tag{13}$$

where

$$\Delta_1^* = (\alpha_3+2\alpha_1)(1-z^{-2}) \text{ and } \Delta_5^* = (\alpha_8+2\alpha_9)(1-z^{-2}).$$

The other values remain unchanged, i.e., as given in (7).

The SFG representation of the network (11)–(13) and the equivalent SC network is shown in Fig. 5(a) and Fig. 5(b), respectively. As a result of the modifications in (11)–(13), the SFG topology of the network is changed by the additional product-transmittances $(-2\alpha_1\Delta_2, -2\alpha_9\Delta_4, 2\alpha_1 z^{-2}, 2\alpha_9 z^{-2})$ so that the termination impedances are implemented inherently. Note that the compensation transmittances $2\alpha_1 z^{-2}$ and $2\alpha_9 z^{-2}$ are necessary in order to eliminate the supplementary signals introduced by the product-transmittances $(-2\alpha_1\Delta_2, -2\alpha_9\Delta_4)$.

V. Design of Bandpass Filters

The design of bandpass filters is carried out following essentially the same design procedure as that outlined in the preceding sections. It is summarized here for the design of a sixth-order elliptic bandpass filter.

Step 1:

As above, it is assumed that an *LCR* prototype satisfying the analog frequency specifications is obtained using either filter tables or synthesis programs. Note that the resulting configuration should contain as few nodes as possible. This is because the output voltages of integrators correspond to the node voltages of the analog prototype. Consequently, the number of required active devices is directly proportional to the number of nodes in the analog prototype. For

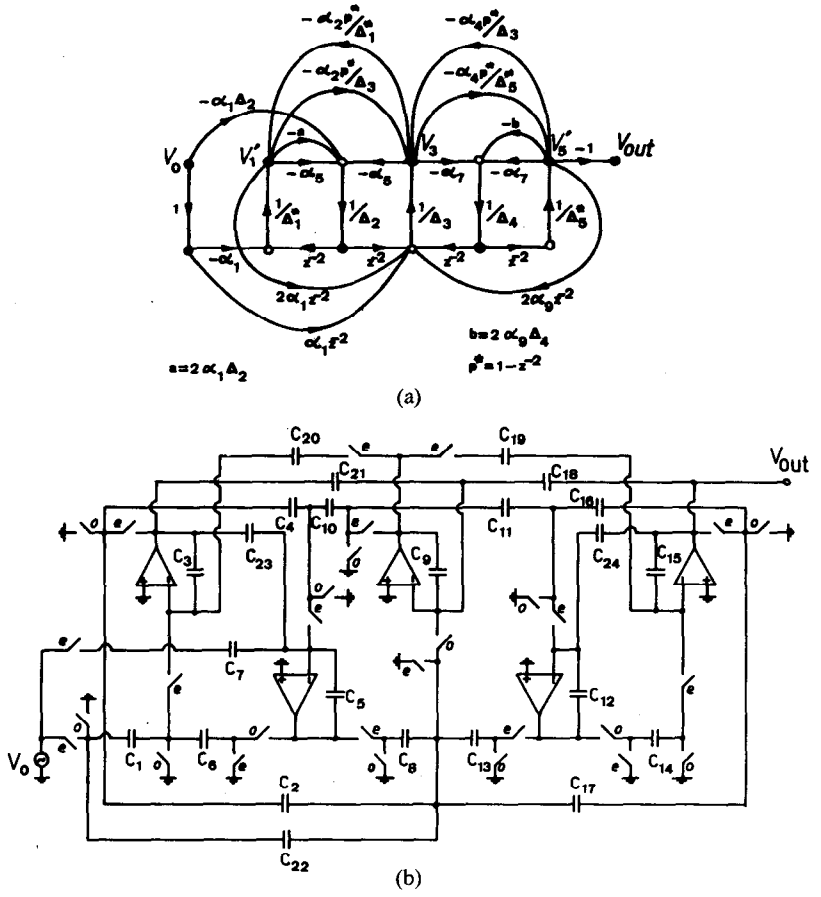

Fig. 5. (a) New SFG topology with the undamped integration transmittances. (b) The SC ladder equivalent of Fig. 5(a).

our design example we consider the bandpass filter of Fig. 6(a), derived by the LP → BP transformation of a third-order low-pass filter.

Step 2:

Applying admittance scaling as in Table I, the bilinear transformed and S-scaled bandpass filter can be obtained as shown in Fig. 6(b). The Kirchhoff node equations of this network are

$$V_1 = \frac{\alpha_1(1+z^{-2})}{\Delta_1}V_0 - \frac{\alpha_8 z^{-2}}{\Delta_1\Delta_2}V_1 - \frac{\alpha_3 z^{-2}}{\Delta_1\Delta_2}V_3' - \frac{\alpha_2(1-z^{-2})}{\Delta_1}V_3' \tag{14}$$

$$V_3' = -\frac{\alpha_4 z^{-2}}{\Delta_3\Delta_4}V_1 - \frac{\alpha_9 z^{-2}}{\Delta_3\Delta_4}V_3' - \frac{\alpha_2(1-z^{-2})}{\Delta_4}V_1 - \frac{\alpha_5(1-z^{-2})}{\Delta_4}V_5 - \frac{\alpha_6 z^{-2}}{\Delta_3\Delta_4}V_5 \tag{15}$$

$$V_5 = -\frac{\alpha_{14} z^{-2}}{\Delta_5\Delta_6}V_3' - \frac{\alpha_{11} z^{-2}}{\Delta_5\Delta_6}V_5 - \frac{\alpha_5(1-z^{-2})}{\Delta_6}V_3' \tag{16}$$

where

$$V_3' = -V_3$$

$$\Delta_1 = \alpha_7(1-z^{-2})+2\alpha_1 \qquad \Delta_2 = (1-z^{-2})$$

$$\Delta_3 = (1-z^{-2})$$

$$\Delta_4 = \alpha_{10}(1-z^{-2}) \qquad \Delta_5 = (1-z^{-2})$$

$$\Delta_6 = \alpha_{12}(1-z^{-2})+2\alpha_{13}$$

$$\alpha_1 = C_s/C_r \qquad \alpha_2 = (C_2 + C_{C_{L2}})/C_r \qquad \alpha_3 = C_{L2}/C_r = \alpha_4$$

$$\alpha_5 = (C_4 + C_{C_{L4}})/C_r \qquad \alpha_6 = C_{L4}/C_r \qquad \alpha_7 = C_1'/C_r$$

$$\alpha_8 = C_{L1//L2}/C_r \qquad \alpha_9 = C_{L2//L4}/C_r \qquad \alpha_{10} = C_3'/C_r$$

$$\alpha_{11} = C_{L4//L5}/C_r \qquad \alpha_{12} = C_5'/C_r$$

$$\alpha_{13} = C_l/C_r \qquad \alpha_{14} = \alpha_6$$

$$C_1' = C_1 + C_{C_{L1}} + C_2 + C_{C_{L2}} - C_s$$

$$C_3' = C_2 + C_{C_{L2}} + C_4 + C_{C_{L4}}$$

$$C_5' = C_4 + C_{C_{L4}} + C_5 + C_{C_{L5}} - C_l$$

$C_i = C_{Ci}$ $(i = 1,2,4,5)$, and C_r the normalization capacitor. (17)

The SFG representation is shown in Fig. 6(c).

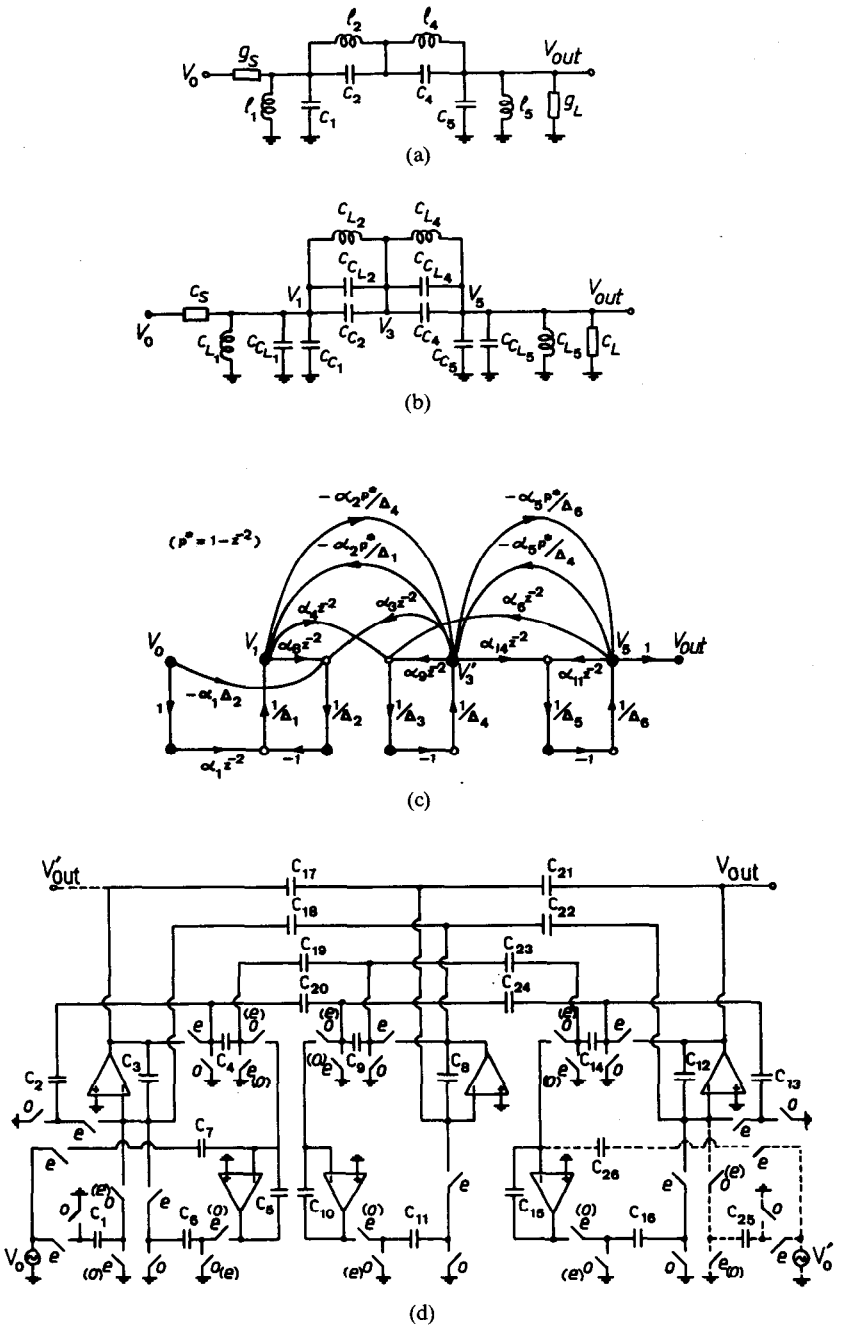

Fig. 6. (a) The *LCR* bandpass prototype. (b) The BITAS equivalent of Fig. 6(a). (c) SFG of Fig. 6(b). (d) SC bandpass network.

Step 3:

The corresponding SC network can be obtained as shown in Fig. 6(d).

The network equations (14)–(16) can be modified to obtain other possible SC structures that may be superior for certain design requirements. For example, the modified SC version with the sign-inverted input voltage, as illustrated in the low-pass case, is shown in Fig. 6(d) with the corresponding switching phases given in parentheses. Furthermore, a new family of bandpass SC configurations can be derived, starting out with the FDNR-transformed version of the *LCR* prototype filter in Step 1. More will be said about this possibility in connection with high-pass filter design in the next section.

It should be pointed out that our design technique is not restricted only to integrators; it can be applied to any other building blocks such as, for instance, SC biquads. Interestingly enough, the resulting SC bandpass filters link coupled-biquad structures [11] to the bandpass circuits obtained by leapfrog design [1]. In fact, by modifying the z-domain network equations, one can derive several SC bandpass equivalents, including coupled-biquad filters. To

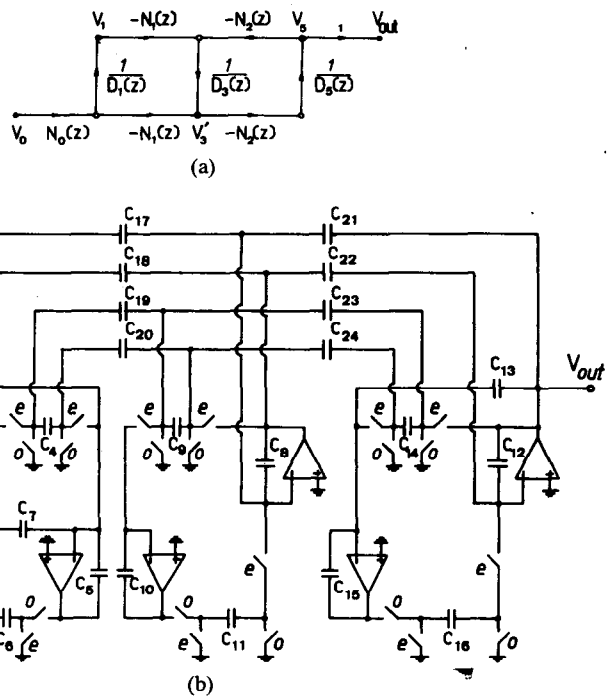

Fig. 7. (a) The SFG representation of Fig. 6(b) using the second-order network (18)–(20). (b) SC bandpass filter using the coupled-biquad structures.

do so, we rewrite the system of (14)–(16) as follows:

$$V_1 = \frac{N_0(z)}{D_1(z)} V_0 - \frac{N_1(z)}{D_1(z)} V_3' \tag{18}$$

$$V_3' = -\frac{N_1(z)}{D_3(z)} V_1 - \frac{N_2(z)}{D_3(z)} V_5 \tag{19}$$

$$V_5 = -\frac{N_2(z)}{D_5(z)} V_3' \tag{20}$$

where

$$\begin{aligned} N_0(z) &= \alpha_1(1 - z^{-4}) \\ N_1(z) &= \alpha_2 z^{-4} + (\alpha_3 - 2\alpha_2) z^{-2} + \alpha_2 \\ N_2(z) &= \alpha_5 z^{-4} + (\alpha_6 - 2\alpha_5) z^{-2} + \alpha_5 \\ D_1(z) &= \alpha_7 z^{-4} + (\alpha_8 - 2\alpha_7 - 2\alpha_1) z^{-2} + (\alpha_7 + 2\alpha_1) \\ D_3(z) &= \alpha_{10} z^{-4} + (\alpha_9 - 2\alpha_{10}) z^{-2} + \alpha_{10} \\ D_5(z) &= \alpha_{12} z^{-4} + (\alpha_{11} - 2\alpha_{13} - 2\alpha_{12}) z^{-2} + (\alpha_{12} + 2\alpha_{13}). \end{aligned} \tag{21}$$

The α_i values are the same as defined in (17).

The corresponding SFG is shown in Fig. 7(a). The advantage of this procedure, which can be regarded as a discrete-time application of the method proposed by Yoshihiro *et al.* [19], is that the individual transfer functions of the SFG can be derived directly from the converted ladder filters in terms of the normalized inductor and capacitor values. Each pair of transfer functions have the same denominator, i.e., *they can be realized by one and the same biquad circuit.* It should be noted that the individual transfer functions in (18)–(20) are of second-order, since the definition of the discrete-time variable z is given by

$$z = \exp(s\tau) = \exp(sT/2). \tag{22}$$

In the implementation of the equivalent SC circuits, any one of the biquad circuits whose transfer functions correspond to the expressions in (21) can be applied. For example, using the second-order building blocks presented in [11] we obtain the SC circuit shown in Fig. 7(b).

VI. Design of High-Pass Filters

Before going into the actual design of high-pass filters, a stability problem, due to the application of the frequency-dependent admittance scaling of Table I, is briefly discussed.

Consider the third-order elliptic high-pass filter shown in Fig. 8(a). Applying the admittance transformation of Table I to the analog prototype directly yields the bilinear-transformed and admittance scaled high-pass filter shown in Fig. 8(b). This filter suffers from the instability phenomenon described in [4]. With reference to our example, this phenomenon can be explained as follows. Carrying out the frequency-dependent admittance scaling, the source and load resistors in Fig. 8(a) have been converted into the frequency-dependent terminations in Fig. 8(b). Since the impedance of the series branches of a ladder filter determines the transmission zeros of the transfer function, the presence of the source termination C_s in Fig. 8(b) leads to a supplementary transmission zero at half the sampling frequency. For the passband gain of a high-pass transfer function, however, the following condition must be fulfilled:

$$|H_h(z)|_{\omega=\omega_s/2} \neq 0. \tag{23}$$

(Usually it is equal to unity or 0.5.)

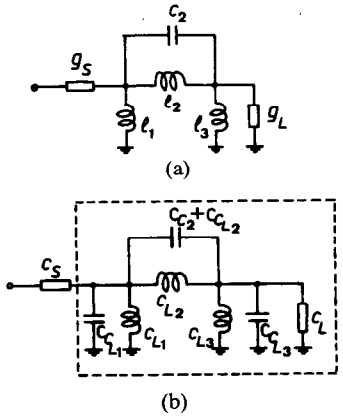

Fig. 8. (a) The third-order elliptic high-pass filter. (b) The directly converted discrete-time equivalent.

This condition requires an additional pole at the frequency $\omega_s/2$ so that the transfer function obtained can attain the required passband gain. Thus we obtain

$$H_h'(z) = \frac{1+z^{-2}}{1+z^{-2}} H_h(z) \tag{24}$$

$H_h(z)$ high-pass transfer function to be realized
$H_h'(z)$ high-pass transfer function obtained.

Note that the order of the transfer function is increased by adding a pole–zero pair (for our example from third to fourth order). The resulting transfer function appears to be stable due to the pole–zero cancellation. But this transmission pole–zero pair is, by nature, implemented independently of each other: the transmission zero by the frequency-dependent source termination C_s on the forward path of the equivalent SC circuit, and the pole by the remaining part of the SC circuit which corresponds to the network framed by dotted lines in Fig. 8(b). However, this latter network has an eigenvalue on the unit circle. Thus the network is unstable and oscillates with half the sampling frequency.

A solution to overcoming this problem is to start out from the *FDNR-transformed version* of an *LCR* high-pass filter. If the FDNR-transformation is carried out first, the additional pole–zero cancellation in the transfer function, resulting from the admittance transformation, is eliminated. In what follows, this procedure is described by the following design steps:

Step 1:

Consider the FDNR-transformed third-order elliptic high-pass prototype filter shown in Fig. 9(a).

Step 2:

The bilinear-transformed network is shown in Fig. 9(b). As a consequence of the FDNR-transformation, the frequency-dependent terminations are converted into discrete-time reactances obtained by backward-difference transformation. The transmission zero of the high-pass filter function at $\omega = 0$ is realized by the source termination C_{G1}; other zeros are realized by the series branch impedances of the ladder equivalent. The passband gain at $\omega_s/2$ is determined by the ratio of two termination impedances with a finite value. Thus the order of the transfer function remains unchanged and the resulting network is stable.

Applying Kirchhoff's current law to the internal and output nodes of the converted network, the following system of network equations is obtained:

$$V_1' = -\frac{\alpha_1(1-z^{-2})}{\Delta_1} V_0 - \frac{\alpha_2}{\Delta_1} V_3 + \frac{\alpha_4 z^{-2}}{\Delta_1} V_3 + \frac{2\alpha_5 z^{-2}(1-z^{-2})}{\Delta_1\Delta_2}(V_1' + V_3) \tag{25}$$

$$V_3 = -\frac{\alpha_6}{\Delta_3} V_1' + \frac{\alpha_7 z^{-2}}{\Delta_3} V_1' + \frac{2\alpha_8 z^{-2}(1-z^{-2})}{\Delta_2\Delta_3}(V_1' + V_3) \tag{26}$$

where

$$\begin{aligned}
&V_1' = -V_1 \\
&\alpha_1 = C_{G1}/C_1 \qquad \alpha_2 = (C_{D2} - C_{G_{L2}})/C_1 \\
&\alpha_3 = (C_{G_{L1}} + C_{G_{L2}})/C_1 \\
&\alpha_4 = (C_{D2} + C_{G_{L2}})/C_1 \qquad \alpha_5 = C_{D2}/C_1 \\
&\alpha_6 = (C_{D2} - C_{G_{L2}})/C_3 \\
&\alpha_7 = (C_{D2} + C_{G_{L2}})/C_3 \qquad \alpha_8 = C_{D2}/C_3 \\
&\alpha_9 = (C_{G_{L2}} + C_{G_{L3}})/C_3 \\
&C_1 = C_{G1} + C_{D2} - C_{G_{L1}} - C_{G_{L2}} \\
&C_3 = C_{G2} + C_{D2} - C_{G_{L2}} - C_{G_{L3}} \\
&\Delta_1 = 1 - z^{-2} + 2\alpha_3 \qquad \Delta_2 = 1 + z^{-2} \\
&\Delta_3 = 1 - z^{-2} + 2\alpha_9.
\end{aligned} \tag{27}$$

In this case, the coefficients (α_k) are given as ratios of capacitor values of the bilinear-transformed equivalent filter, without considering any other reference capacitors. Thus the calculated capacitor ratios yield the gain constants of the integrator-summer building blocks directly. The corresponding SFG can be obtained as shown in Fig. 9(c).

Step 3:

One possible implementation of the SC equivalent is shown in Fig. 9(d). Note that four amplifiers are required in order to realize all internal transmittances (including Δ_2) in a fully strays-insensitive form. Without modification, the transmittance Δ_2 cannot be implemented by the first-order building block in Fig. 1. To realize it by a completely parasitic-insensitive circuit, an inverter must be introduced into the feedback path as depicted in Fig. 9(d).

It should be noted that the design procedure outlined above has yielded stable SC high-pass equivalents in all cases considered so far.

VII. Properties of Bilinear-Transformed Admittance-Scaled (BITAS) Filters

In the preceding sections, a new design technique based on the bilinear z-transform and subsequent frequency-dependent admittance scaling (see Table I) has been pre-

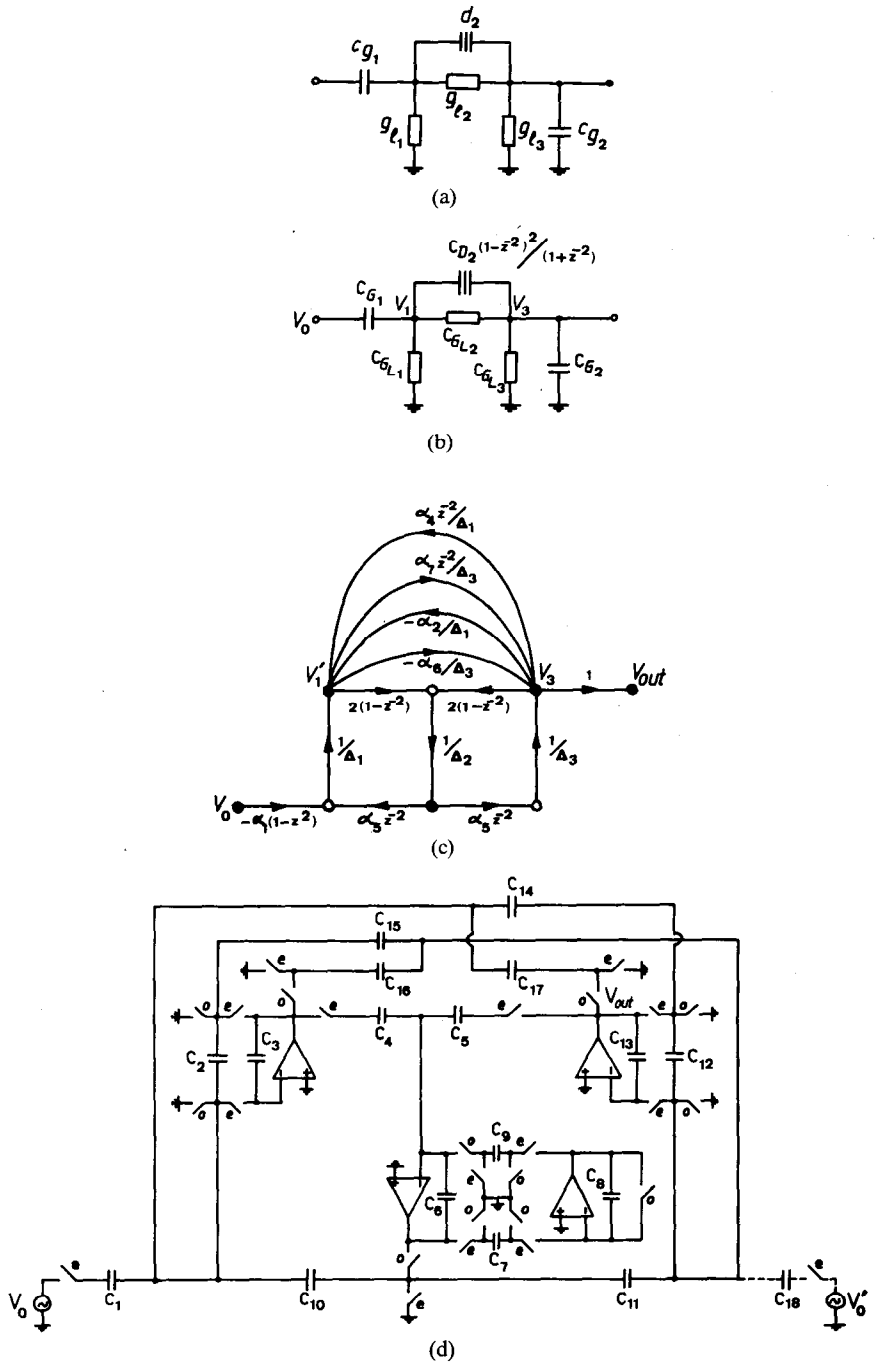

Fig. 9. (a) The FDNR-transformed high-pass prototype filter. (b) The BITAS equivalent of Fig. (9a). (c) SFG of Fig. (9b). (d) The resulting SC high-pass realization.

sented. With this method, SC ladder filters are realizable using well-known parasitic-free differential integrator loops and coupled-biquad structures. In what follows, the main properties of such filters are summarized.

One interesting feature of BITAS filters is that, like the *LCR* prototype filters, they are symmetrical, i.e., their input and output terminals can be interchanged. These interchanged feed-in terminals are shown with dotted lines for the low-pass, bandpass, high-pass case in Figs. 3(d), 6(d), 9(d), respectively. As will be shown in the next section, a comparison, with respect to the capacitor areas, of the original, and the input–output interchanged version after optimization with respect to dynamic-range, indicates that the choice of the feed-in terminal is very important with regard to the total required capacitor area.

Another feature of BITAS filters is that the conversion of an elliptic to an all-pole ladder filter of the same order (low-pass, bandpass, or high-pass) can be carried out simply by changing the gain constants of the integrator-summer blocks of a given SC filter structure.

To illustrate other properties of BITAS filters, consider the analog low-pass prototype filter shown in Fig. 10(a)

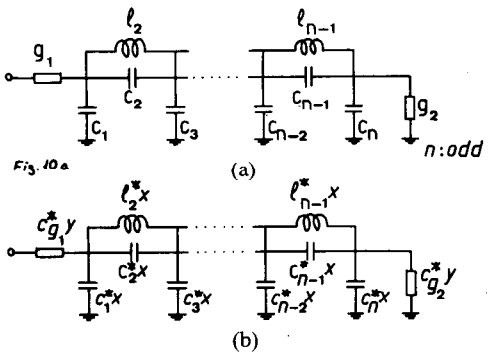

Fig. 10. (a) The analog low-pass prototype filter. (b) The discrete-time equivalent of Fig. 10(a) using (28).

and its BITAS equivalent in Fig. 10(b). Note that the admittance scaling factor has in this case been chosen as

$$S_1 = z^{-1}/(1+z^{-2}) \tag{28}$$

and is dimensionless.

This modified scaling factor is used in order to illustrate the similarity between leapfrog synthesis and our design procedure. The branch reactances of the network in Fig. 10(b) become the same reactances as those obtained by LDI transformation, namely,

$$1/l_i s \to 1/l_i^* x \qquad l_i^* = l_i/2,\ i\text{: even} \tag{29}$$

$$c_i s \to c_i^* x \qquad c_i^* = 2(c_i + c_{l_i}),\ c_{l_i} = \tau^2/l_i,\ i\text{: even} \tag{30}$$

$$c_j s \to c_j^* x \qquad c_j^* = 2c_j,\ j\text{: odd} \tag{31}$$

where

$$x = \frac{1}{T_s}\frac{1-z^{-2}}{z^{-1}}$$

$T_s = 2\tau = 1/f_s$, $\quad f_s$ is sampling frequency.

The termination admittances are given by

$$g_k \to c_k^* y, \qquad c_k^* = 2\tau g_k,\ k = 1,2 \tag{32}$$

where

$$y = \frac{1}{T_s}\frac{1+z^{-2}}{z^{-1}}.$$

In the case of all-pole filters ($c_i = 0$, i: even), inductors in the analog prototype filter are converted into equivalent discrete-time parallel resonance circuits. These realize the transmission zeros of the low-pass transfer function at half the sampling frequency ($\omega = \omega_s/2$). Substituting $s = j\omega$, we obtain

$$1/j\omega l_i \to 1/j\sin(\omega T_s/2) l_i^* \tag{33}$$

$$j\omega c_j \to j\sin(\omega T_s/2) c_j^* \tag{34}$$

$$g_k \to \cos(\omega T_s/2) c_k^*. \tag{35}$$

Recall that the relationship between the continuous- and discrete-time frequency is

$$j\omega \to j\frac{2}{T_s}\tan(\omega T_s/2). \tag{36}$$

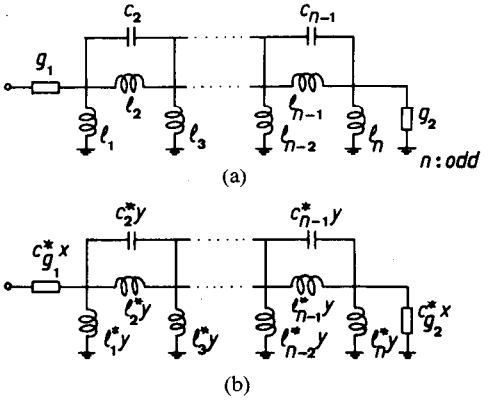

Fig. 11. (a) The analog high-pass prototype filter. (b) The discrete-time equivalent of Fig. 11(a) using (37).

Thus the BITAS low-pass networks can be regarded as LDI-transformed leapfrog filters, terminated by frequency-dependent admittances, which are inherently determined by (36). As is well known from leapfrog design, a high clock-to-cutoff frequency ratio is required in order for the sampling effects on the frequency response, due to the extra half delay in the termination loops, to be negligible. Various methods have been published in order to eliminate this terminating error. One of these [12] is to terminate SC ladder equivalents with frequency-dependent impedances corresponding to (36).

Another [13] is to redesign the all-pole low-pass filters comprising such terminations. In this case, the transmission zeros at half the sampling frequency due to the bilinear z-transform are removed. In doing so, the network poles must be relocated such that the resulting frequency response satisfies the design specifications. This amounts to a prewarping of the network function and entails a modification of the entire design process. Similar observations apply to the high-pass case. Consider, for example, the analog high-pass prototype depicted in Fig. 11(a) and its BITAS equivalent in Fig. 11(b). Note that this time the dimensionless admittance scaling factor is chosen to be

$$S_2 = z^{-1}/(1-z^{-2}). \tag{37}$$

By splitting up the resulting reactances as follows:

$$\frac{c_i}{\tau}\frac{(1-z^{-2})^2}{z^{-1}(1+z^{-2})} = \frac{c_i}{\tau}\frac{(1+z^{-2})}{z^{-1}} - \frac{4c_i}{\tau}\frac{z^{-1}}{(1+z^{-2})} \tag{38}$$

we obtain the branch reactances:

$$c_i s \to 1/l_i^* y \qquad l_i^* = -\tau^2/2c_i,\ i\text{: even} \tag{39}$$

$$1/l_i s \to c_i^* y \qquad c_i^* = 2(c_i + c_{l_i}),\ c_{l_i} = \tau^2/l_i,\ i\text{: even} \tag{40}$$

$$1/l_j s \to c_j^* y \qquad c_j^* = 2c_{l_j},\ j\text{: odd} \tag{41}$$

and terminators

$$g_k \to c_k^* x \qquad c_k^* = 2\tau g_k,\ k = 1,2. \tag{42}$$

The branch reactances of the BITAS high-pass ladder equivalents have the form of the terminations in the low-pass case, and the terminations the from of the branch

TABLE II
COMPLEMENTARY ADMITTANCE TRANSFORMATION

element	admittance s - domain	admittance z - domain $s \to \frac{1}{\tau}\frac{1-z^{-2}}{1+z^{-2}}$	scaled admittance $Y \to Y/S^*$	definitions $S^* = \frac{1}{\tau(1-z^{-2})}$ S* = scaling frequency
R	$G = 1/R$	G	$C_G(1-z^{-2})$	$C_G = \tau G$
C	sC	$\frac{C}{\tau}\frac{1-z^{-2}}{1+z^{-2}}$	$C\frac{(1-z^{-2})^2}{1+z^{-2}} = C(1+z^{-2}) - 4C\frac{z^{-2}}{1+z^{-2}}$	
L	$1/sL$	$\frac{\tau}{L}\frac{1+z^{-2}}{1-z^{-2}}$	$C_L(1+z^{-2})$	$C_L = \tau^2/L$
M	$1/s^2 M$	$\frac{\tau^2}{M}\frac{(1+z^{-2})^2}{(1-z^{-2})^2}$	$\frac{\tau^3}{M}\frac{(1+z^{-2})^2}{1-z^{-2}} = C_M(1-z^{-2}) + 4C_M\frac{z^{-2}}{1-z^{-2}}$	$C_M = \tau^3/M$

reactances, respectively. In other words, x (LDI variable) and y (termination variable) are exchanged. Notice that the value of l_i^* in (39) is negative.

Another result of this observation is that the scaling frequency

$$S^* = 1/\tau(1-z^{-2}) \tag{43}$$

yields the same discrete-time equivalent filter as would be obtained by applying the original admittance transformation (see (3) and Table I) to the corresponding FDNR-transformed high-pass prototype filter. A complementary admittance scaling factor can, therefore, be defined as shown in Table II. To summarize: the scaling factor in (43) represents an alternative method of obtaining a BITAS filter from a prototype *LCR* filter. The two methods of reactance scaling are complementary. In the first case (i.e., the admittance transformation according to Table I) the source termination of the resulting network causes the transmission zero to be at half the sampling frequency ($\omega = \omega_s/2$). In the second case (i.e., the admittance transformation according to Table II) the corresponding transmission zero is at $\omega = 0$.

Finally, assuming $\tau = 1$, i.e., $\omega_s = \pi$, a comparison of Tables I and II suggest a simple method of converting a low-pass into a high-pass filter, which is similar to the continuous-time case. As can be seen, the admittances in Table II can readily be derived form those in Table I by letting

$$z^{-2} \to -z^{-2}. \tag{44}$$

Consequently, we obtain the following relationship between the high-pass and low-pass transfer functions:

$$H_h(z) = H_l(z)|_{z^{-2} = -z^{-2}}. \tag{45}$$

Note that except for some distortion of the frequency scale, this transformation provides a high-pass frequency response which appears as if the low-pass response had been shifted in frequency by π. A similar set of simple transformations can be derived for the conversion of a low-pass filter into a bandpass or bandstop filter.

VIII. EXPLICIT DESIGN EXAMPLES

The design technique outlined in the preceding sections will be illustrated by several detailed examples. First, however, a brief digression. Normally, design specifications must be prewarped in order to take the nonlinear frequency relationship between the analog- and discrete-frequency domain into account (see (36)). This prewarping can be introduced directly into the denormalized elements which are given by

$$C_i = \frac{1}{\omega_c R_r} c_i \quad \text{and} \quad L_j = \frac{R_r}{\omega_c} l_j \tag{46}$$

where ω_c is the specified angular cutoff frequency and R_r a reference resistor (usually equal to the termination resistors).

Taking the frequency prewarping (36) into account and with $C_r = \tau/R_r$ as an arbitrary reference capacitor, the required capacitor ratios can then be derived as

$$\frac{C_{G_i}}{C_r} = 1 \qquad \frac{C_{c_i}}{C_r} = \frac{c_i}{\tan(\omega_c \tau)}$$
$$\frac{C_{l_j}}{C_r} = \frac{4\tan(\omega_c\tau)}{l_j} \qquad \frac{C_{C_{l_j}}}{C_r} = \frac{\tan(\omega_c\tau)}{l_j}. \tag{47}$$

Thus the gain constants (α_k) of the internal integrators are obtained in terms of the normalized element values of the analog prototype filter and the cutoff/sampling frequency ratio. This is an alternative approach to the conventional one of designing the analog prototype filter using an approximation and synthesis program *after* prewarping the critical frequencies according to (36). In this case, of course, the correction term $\tan(\omega_c\tau)$ is equal to unity.

Consider, now, the normalized element values of the elliptic low-pass filter CC 052548 given in Table III. As pointed out in Section IV, numerous SC realizations can be derived for an analog low-pass prototype filter. The capacitor values in Table III are given for the version shown in Fig. 3(d) with the switching phases in parentheses. They are obtained by substituting (47) in (7) for the cutoff

TABLE III

LCR LOWPASS-PROTOTYPE VALUES

$g_s = 1.$ $\ell_2 = 1.11477$ $\ell_4 = 0.80597$ $g_L = 1.$

$c_2 = 0.21771$ $c_4 = 0.64069$

$c_1 = 1.28329$ $c_3 = 1.77253$ $c_5 = 0.99832$

CAPACITOR VALUES

initial values SBLP1		dynamic-range optimized SODLP1		input-output interchanged SBLP2		dynamic-range optimized SODLP2	
C1	2.1299	C1	1.2259	C1	------	C1	------
C2	2.1299	C2	2.116	C2	2.1299	C2	1.1623
C3	3.8760	C3	3.8507	C3	3.876	C3	2.1176
C4	1.2442	C4	1.0738	C4	1.2442	C4	1.
C5	1.	C5	2.7859	C5	1.	C5	3.5363
C6	1.065	C6	3.4154	C6	1.065	C6	2.56
C7	2.	C7	1.	C7	------	C7	------
C8	1.065	C8	3.438	C8	1.065	C8	4.6858
C9	8.869	C9	8.9276	C9	8.869	C9	16.2338
C10	1.2442	C10	1.0809	C10	1.2442	C10	1.8304
C11	1.7209	C11	1.7374	C11	1.7209	C11	1.575
C12	1.	C12	3.4814	C12	1.	C12	3.5155
C13	1.065	C13	3.6965	C13	1.065	C13	7.4877
C14	1.	C14	2.9955	C14	1.	C14	3.5155
C15	4.157	C15	2.0785	C15	4.157	C15	3.4774
C16	1.7209	C16	1.	C16	1.7209	C16	1.44
C17	2.	C17	1.	C17	2.	C17	1.673
C18	2.426	C18	1.4056	C18	2.426	C18	4.0587
C19	2.278	C19	1.9789	C19	2.278	C19	2.0849
C20	1.	C20	1.	C20	1.	C20	1.
C21	1.	C21	1.	C21	1.	C21	1.
C22	2.1299	C22	1.2340	C22	------	C22	------
C23	------	C23	------	C23	2.	C23	1.
C24	------	C24	------	C24	2.	C24	1.
C25	------	C25	------	C25	2.1299	C25	2.13

SBLP: Stray-Insensitive Bilinear Transformed Lowpass Filter

SODLP: Stray-Insensitive Optimum Dynamic-Range Lowpass Filter

frequency $f_c = 3.4$ kHz and sampling frequency $f_s = 32$ kHz. The SC equivalents, i.e., the original- (SBLP1) and the interchanged input–output (SBLP2) versions, have been scaled for an optimum dynamic-range resulting in filters SODLP1 and SODLP2, respectively. A comparison of the resulting filters (SODLP1 and SODLP2) with respect to the required capacitor area shows a considerable difference (approximately 30 percent), although both circuits were designed for minimum total capacitance and, of course, for the same design specifications. Note that the minimum scaled capacitor values in both cases are equal to one, i.e., the capacitor area obtained is directly proportional to the sum of the scaled capacitor values. As a result, the choice of the feed-in terminals in the filters optimized for dynamic-range is very important with regard to the optimum capacitor area. Note that the nonoptimized SC equivalents SBLP1 and SBLP2 have equal capacitance area.

For the design of a geometrically symmetric bandpass filter, the normalized element values derived from the low-pass prototype CC 032026 (passband ripple 0.177 dB and stopband loss 30.41 dB) are shown in Table IV. The capacitor values are also given for the version depicted in Fig. 6(d) with the switching phases in parentheses. They are obtained for a passband between 1.4–3.4 kHz and a sampling frequency $f_s = 32$ kHz.

Finally, our design procedure is illustrated for a third-order elliptic high-pass SC filter. The element values of the RCD prototype filter are derived from the same low-pass filter used in the bandpass case. With the same design procedure as above, and with (27), the capacitor values of the initial- (SBHP1) and dynamic-range optimized (SODHP1) SC networks are obtained as given in Table V. The measured amplitude responses of the low-pass (see Fig. 3(d)), bandpass- (Fig. 6(d)), and high-pass- (Fig. 9(d)) SC filters using discrete components (opamps LF 356, switches MC 14016, and capacitors with 0.5-percent accuracy) are shown in Figs. 12, 13, and 14, respectively. In all three cases the passband sensitivity with respect to a 1-percent change remained below 0.12 dB. This is the kind of insensitivity to be expected from the classical ladder structure, also when it has been converted into an SC filter according to the BITAS procedure.

IX. Conclusions

A fundamental approach for the accurate design of precision monolithic SC networks has been described. The design is carried out by converting a conventional continuous-time filter into a discrete-time filter utilizing the bilinear z-transform. Since the design procedure is based on the network equations and the corresponding SFG in the

TABLE IV

LCR BANDPASS PROTOTYPE VALUES

$g_s = 1.$ $g_L = 1.$

$\ell_1 = 0.8768$	$\ell_2 = 0.7215$	$\ell_4 = 5.7711$	$\ell_5 = 0.8768$
$c_1 = 1.1404$	$c_2 = 0.1733$	$c_4 = 1.3861$	$c_5 = 1.1404$

CAPACITOR VALUES

initial values SBBP1		dynamic-range optimized SODBP1	
C1	2.	C1	1.
C2	2.	C2	1.468
C3	5.552	C3	4.075
C4	2.213	C4	1.6246
C5	1.	C5	3.1365
C6	1.	C6	3.1365
C7	2.	C7	1.
C8	7.461	C8	9.2944
C9	8.999	C9	18.015
C10	6.588	C10	31.173
C11	1.	C11	2.944
C12	10.824	C12	5.412
C13	2.	C13	1.
C14	7.582	C14	3.787
C15	6.588	C15	15.482
C16	1.	C16	2.3525
C17	1.095	C17	1.
C18	1.095	C18	1.096
C19	1.214	C19	1.2155
C20	7.999	C20	11.7425
C21	6.367	C21	3.9614
C22	6.367	C22	6.373
C23	1.	C23	1.
C24	1.	C24	1.

SBBP: Stray-Insensitive Bilinear Transformed Bandpass Filter

SODBP: Stray-Insensitive Optimum Dynamic-Range Bandpass Filter

TABLE V

RCD HIGHPASS-PROTOTYPE VALUES

$C_{g_s} = 1.$ $g_{\ell_1} = g_{\ell_3} = 0.921$ $g_{\ell_2} = 6.821$ $d_2 = 0.991$ $C_{g_\ell} = 1.$

CAPACITOR VALUES

initial values SBHP1		dynamic-range optimized SODHP1	
C1	2.3406	C1	1.5955
C2	1.	C2	1.
C3	4.015	C3	4.015
C4	2.	C4	1.467
C5	2.	C5	1.
C6	1.	C6	2.0605
C7	1.	C7	1.
C8	1.	C8	1.
C9	2.	C9	4.121
C10	3.3447	C10	9.3956
C11	3.3447	C11	13.7833
C12	1.	C12	1.
C13	4.015	C13	4.015
C14	3.4042	C14	2.3205
C15	3.4042	C15	4.994
C16	3.2852	C16	4.8194
C17	3.2852	C17	2.2394

SBHP: Stray-Insensitive Bilinear Transformed Highpass Filter

SODHP: Stray-Insensitive Optimum Dynamic-Range Highpass Filter

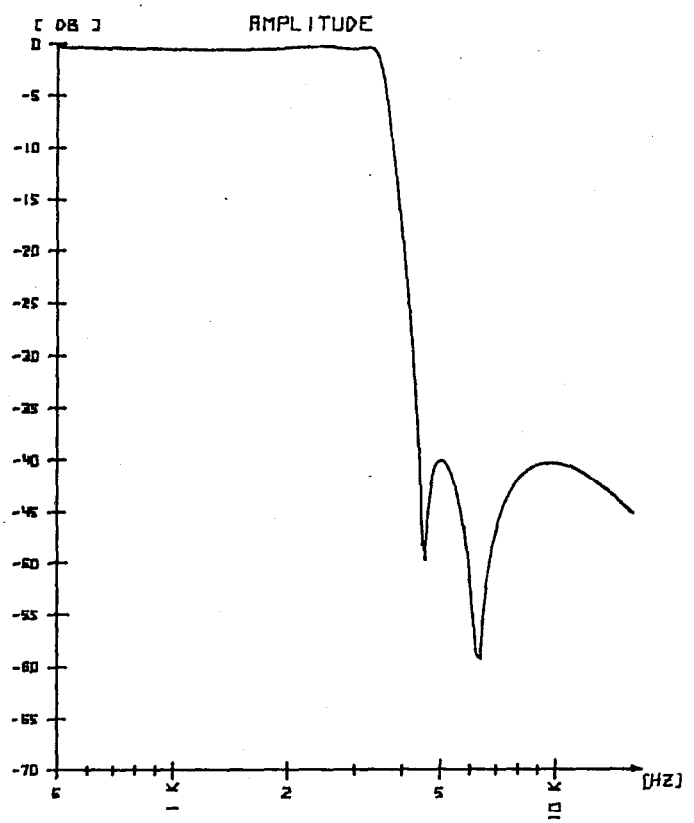

Fig. 12. Measured frequency responses of the elliptic low-pass filter.

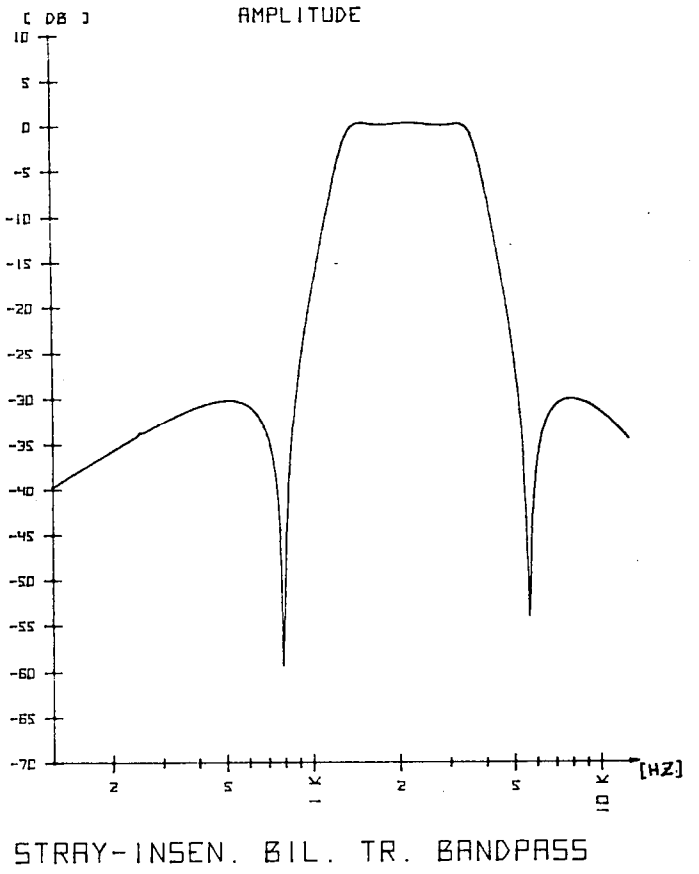

Fig. 13. Measured frequency response of the SC bandpass filter in Fig. 6(d).

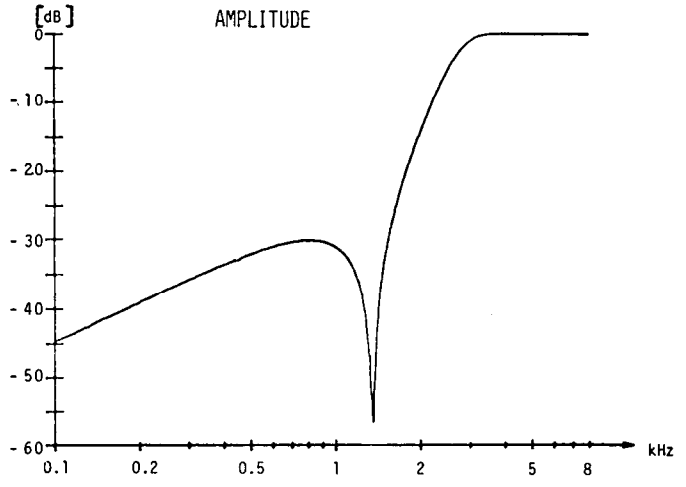

Fig. 14. Measured frequency response of the SC high-pass implementation in Fig. 9(d).

z-domain, the equations can be modified to generate a number of SC filter versions, all derived from one and the same analog filter prototype. The different versions obtained make it possible to choose an optimum solution with respect to tradeoffs between the sampling frequency, the element-spread, the chip area, the dynamic-range and other technological problems of integration. The resulting SC circuits are fully stray-insensitive, allowing the designer to use small capacitors, and hence a small chip area.

References

[1] D. J. Allstot, R. W. Brodersen, and P. R. Gray, "MOS switched-capacitor ladder filters," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 806–814, 1978.

[2] G. M. Jacobs, D. J. Allstot, R. W. Brodersen, and P. R. Gray, "Design techniques for MOS switched-capacitor ladder filters," *IEEE Trans. Circuits Syst.*, vol. CAS-25, pp. 1014–1021, 1978.

[3] K. Martin, "Improved circuits for the realization of switched-capacitor filters," *IEEE Trans. Circuits Syst.*, vol. CAS-27, pp. 237–244, 1980.

[4] M. S. Lee, G. C. Temes, C. Chang, and M. B. Ghaderi, "Bilinear switched-capacitor ladder filters," *IEEE Trans. Circuits Syst.*, vol. CAS-28, pp. 811–822, 1981.

[5] A. Fettweis, "Basic principles of switched-capacitor filters using voltage-inverter switches," *Arch. Elek. Übertragung*, vol. 33, pp. 13–19, 1979.

[6] B. J. Hosticka and G. S. Moschytz, "Switched-capacitor simulation of grounded inductors and gyrators," *Electron. Lett.*, vol. 14, pp. 788–790, 1978.

[7] G. S. Temes, H. J. Orchard, and M. Jahanbegloo, "Switched-capacitor filter design using the bilinear z-transform," *IEEE Trans. Circuits Syst.*, vol. CAS-25, pp. 1039–1044, 1978.

[8] U. W. Brugger, D. C. von Grünigen, and G. S. Moschytz, "A comprehensive procedure for the design of cascaded SC filters," *IEEE Trans. Circuits Syst.*, vol. CAS-27, pp. 803–810, Aug. 1981.

[9] P. E. Fleischer and K. R. Laker, "A family of active switched-capacitor biquad building blocks," *Bell System Tech. J.*, vol. 58, pp. 2235–2269, 1979.

[10] G. Szentirmai and G. C. Temes, "Switched-capacitor building blocks," *IEEE Trans. Circuits Syst.*, vol. CAS-27, pp. 492–501, 1980.

[11] K. Martin and A. S. Sedra, "Exact design of SC bandpass filters using coupled-biquad structures," *IEEE Trans. Circuits Syst.*, vol. CAS-27, pp. 469–475, 1980.

[12] T. C. Choi and R. W. Brodersen, "Considerations for high-frequency SC ladder filters," *IEEE Trans. Circuits Syst.*, vol. CAS-27, pp. 545–552, 1980.

[13] S. O. Scanlan: "Analysis and synthesis of SC state-variable filters," *IEEE Trans. Circuits Syst.*, vol. CAS-28, pp. 85–93, 1981.

[14] E. Hökenek, U. W. Brugger, and G. S. Moschytz, "New frequency transformation for the accurate design of SC ladder fitlers", *Electron. Lett.*, vol. 18, pp. 276–278, 1982.

[15] E. Hökenek and G. S. Moschytz, "The analysis of general switched-capacitor networks using the indefinite admittance matrix (IAM)," *Proc. IEE*, -G, vol. 127, pp. 21–33, 1980.

[16] L. T. Bruton, "Network transfer functions using the concept of frequency-dependent negative resistance," *IEEE Trans. Circuits Theory*, vol. CT-16, pp. 406–408, 1969.

[17] G. S. Moschytz, *Linear Integrated Networks: Fundamentals*. New York: Van Nostrand-Reinhold, 1974.

[18] A. I. Zverev, *Handbook of Filter Synthesis*, New York: Wiley, 1967.

[19] M. Yoshihiro, A. Nishihara, and T. Yanagisawa, "Low-sensitivity active and digital filters based on the node-voltage simulation of *LC* ladder structures," *IEEE Int. Symp. on Circuits and Syst.*, (Phoenix, AZ), 1977.

[20] S. Signell and K. Mossberg, "Parasitics-insensitive state-variable SC-filters derived from general *LC*-prototype filtes via the bilinear transform," in *Proc. Journées d'Electronique*, (Lausanne, Switzerland), Oct. 6–8, 1981, pp. 295–303.

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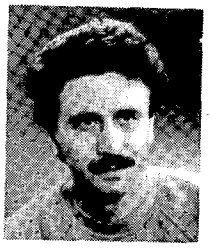

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Exact Design of Strays-Insensitive Switched-Capacitor Ladder Filters

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Abstract—**This paper presents a systematic solution to the problem of designing a stray-insensitive switched-capacitor filter based on the exact simulation of the operation of an *LC* ladder prototype. A complete procedure is given for the design of low-pass and bandpass filters with and without transmission zeros.**

I. INTRODUCTION

THE problem of designing a strays-insensitive switched-capacitor (SC) filter based on the *exact* simulation of the operation of an *LC* ladder prototype has recently been of considerable interest [1]–[9]. In this paper we present yet another solution to this problem. The proposed method has the advantages of being simple, systematic and applicable to filters having finite transmission zeros as well as to all-pole filters. Furthermore, the method should prove useful in connecting previous contributions to this topic, specifically, [5], [15], [3], [7], [8]. In fact in some cases the resulting circuits are identical to those obtainable by these other techniques.

Our SC networks will be realized using the standard strays-insensitive building blocks [10]–[14] shown in Fig. 1.

Manuscript received October 13, 1982. This work was supported by the Natural Sciences and Engineering Research Council of Canada under Grant A7394. R. B. Datar gratefully acknowledges the support of the Indian Government Scholarship.

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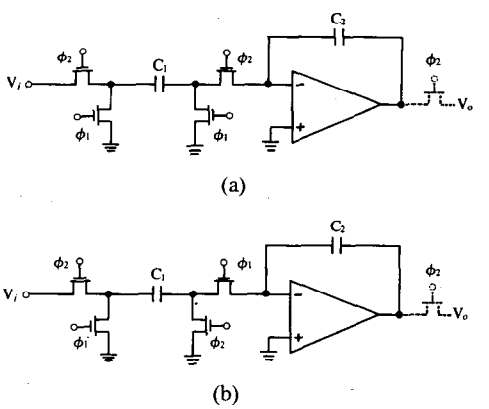

Fig. 1. Strays-insensitive SC building blocks. (a) inverting. (b) noninverting.

Their transfer functions are as follows:

Inverting circuit (Fig. 1(a)):

$$\frac{V_0(z)}{V_i(z)} = -\frac{C_1}{C_2}\frac{z^{1/2}}{z^{1/2}-z^{-1/2}}. \tag{1}$$

Noninverting circuit (Fig. 1(b)):

$$\frac{V_0(z)}{V_i(z)} = \frac{C_1}{C_2}\frac{z^{-1/2}}{z^{1/2}-z^{-1/2}}. \tag{2}$$

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