

DESIGN OF REVERSIBLE MULTIPLIERS FOR LINEAR FILTERING APPLICATIONS IN DSP

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ABSTRACT

Multipliers in DSP computations are crucial. Thus modern DSP systems need to develop low power multipliers to reduce the power dissipation. One of the efficient ways to reduce power dissipation is by the use of bypassing technique. If a bit in the multiplier and/or multiplicand is zero the whole array of row and/or diagonal will be bypassed and hence the name bypass multipliers. This paper presents the column Bypass multiplier and 2-D bypass multiplier using reversible logic; Reversible logic is a more prominent technology, having its applications in Low Power CMOS and quantum computations. The switching activity of any component in the bypass multiplier depends only on the input bit coefficients. These multipliers find application in linear filtering FFT computational units, particularly during zero padding where there will be umpteen numbers of zeros. A bypass multiplier reduces the number of switching activities as well as the power consumption, above which reversible logic design acts to further almost nullify the dissipations.

KEYWORDS

Reversible logic, Low power Multipliers, Column Bypass multiplier, 2-D Bypass Multiplier ,Reduced Switching Activity, Fast Fourier Transform, Zero Padding.

1. INTRODUCTION

Multiplication is an essential arithmetic operation for common DSP applications such as Filtering, computation of FFTs etc. High end DSP processors also need to cater to the execution speed, accuracy of the results and also keep an eye on the power consumption. To achieve this, parallel array multipliers are used, where there is a need to check the power efficiency. The dynamic power consumption (i.e., power loss due to switching activity) can be reduced by bypassing technique. The switching activity of the component used in the design depends on the input bit coefficient. This means that if the input bit coefficient is zero corresponding rows or column of the adders need not be activated. If the multiplicand (or the multiplier) contains more zeros, then higher power reduction can be achieved, which is the case in FFT computation.

Conventional combinational logic circuits are known to dissipate heat for every bit of information that is lost. This is also evident from the second law of thermodynamics which states that any irreversible process leads to loss of energy. R.Landauer [1] showed that any gate that is irreversible necessarily dissipates energy, and each irreversible bit generates $k \cdot T \ln 2$ joules of heat where k is Boltzmann's constant (1.38×10^{-23} joules/Kelvin) and T is temperature in Kelvin. C.H.Bennett in 1973 [2] showed that an irreversible computer can always be made reversible. Reversible logic circuits naturally take care of heating since in a reversible logic every

input vector can be uniquely recovered from its output vectors and therefore no information is lost.

A reversible logic gate is an N input, N output logic device with one to one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Extra inputs or outputs are added so that the number of inputs is made equal to the number of outputs whenever it is necessary. An important constraint present on the design of a reversible logic circuit using reversible logic gate is that fan-out is not allowed. A reversible circuit should be designed using minimum number of reversible gates. One key requirement to achieve optimization is that the designed circuit must produce minimum number of garbage outputs. They must use minimum number of constant inputs. The gate count should also be minimum in a given reversible logic design.

This paper presents an archetypical design of multipliers using Row Bypassing and 2D Bypassing circuits using reversible logic in the literature. This paper is organized as follows; Section 2 discusses the prior work on both reversible logic and bypass multipliers. Section 3 shows the importance of bypass multipliers in linear filtering, Section 4 gives the proposed design of the column bypass and 2-Dimensional Row and column bypass techniques using reversible logic. Section 5 gives the comparison of performance parameters of the two multipliers and simulation results. Conclusions and references follow.

2. PRIOR WORK

2.1. Parallel Multiplier V/s Bypass Multiplier

Consider the multiplication of two unsigned n-bit numbers, $A=a_{n-1}a_{n-2}\dots a_0$ and $B=b_{n-1} b_{n-2}\dots b_0$ to produce the product $P=p_{2n-1} p_{2n}\dots p_0$. The product can be written as:

$$P = \sum_{i=0}^{n-1} a_i \sum_{j=0}^{n-1} b_j 2^{(i+j)}$$

The multiplicand a_i is added to the incoming partial product bit based on the value of the multiplier bit b_j and each row now adds the multiplicand to the incoming partial product (PP) PP_i to generate the outgoing partial product $PP_{(i+1)}$ if b_j is 1, else passed unchanged vertically downwards. Conventional 4X4 Braun Multiplier array consists of 3 rows of carry save adders (CSAs) in which each row contain 3 full adders (FAs). Each FA in turn has 3 inputs and 2 outputs- the sum and the carry.

To design a low power multiplier is to reduce the switching activity [12] and literature supports this statement by providing a direct approach of designing a low power full adder. This can be achieved through architectural modifications such as row, column or 2 dimensional bypassing. The technique of bypassing the columns of the adders has an upper hand on the technique of bypassing the rows of the adders in two aspects: Firstly it eliminates the extra correcting circuits that may be needed [7]. Secondly, the modified full adder in column bypassing multiplier is much simpler than that used in row bypassing multiplier [7].

Since all the partial products $a_i b_j$, $0 \leq j \leq n-1$ are zeroes, if bit a_i in the multiplicand is zero, the addition operation in the $(i+j)$ th column can be bypassed. In column bypass multiplier the modified full adder is simpler than that in the row bypass multiplier. In the carry save array, the full adder is replaced by a modified full adder which consists of a full adder attached to a 2:1 multiplexer. If the bit, a_i in the multiplicand is 0, the inputs in the $(i+1)$ th column will be disabled and the carry output in the column must be set to 0 to produce the correct output. This protecting process can be done by adding an AND gate at the output of the last row of the CSA.

There can be Power reduction in a multiplier if bit a_i , in the multiplicand is 0 or bit b_j , in the multiplier is 0. The addition operations in the $(i + 1)$ th or the j th row can be bypassed if the above conditions are satisfied. Normally, the extra correcting circuits in the row bypassing multiplier are used to add the bypassed carry results to the multiplication result. [6] Proposed two dimensional bypassing multiplier circuit designs in order to eliminate the extra correcting circuits. Here, the carry result in the previous row is integrated in the 2 dimensional bypassing process, which in turn causes the addition operations in the $(i+1, j)$ Full Adders (FA) to be by passed, if the product, $a_i b_j$, is 0 and carry bit $c_{i,j-1}$, is 0. This in turn implies that the addition operation in the $(i+1, j)$ FA will be executed if the product $a_i b_j$, is 1, or bit $c_{i,j-1}$, is 1.

2.2. Reversible Logic

A Boolean function is reversible if each of the values in the input set can be mapped with a unique value in the output set. A number of reversible logic gates have been proposed till date. The most important and fundamental ones are the Feynman Gate, Fredkin Gate, Peres Gate, Toffoli Gate to name a few. Other gates related to the discussion are the Double Peres Gate [10] and Modified Toffoli Gate [11]. The symbols of all the gates are as shown in the figure1. The inputs and the outputs are named on the respective I/O lines. The quantum cost of Feynman Gate is 1, Fredkin Gate is 5[4], Peres Gate is 4[5], Toffoli Gate is 4[3], Double Peres Gate is 6[10] and that of the Modified Toffoli Gate is 6[11].

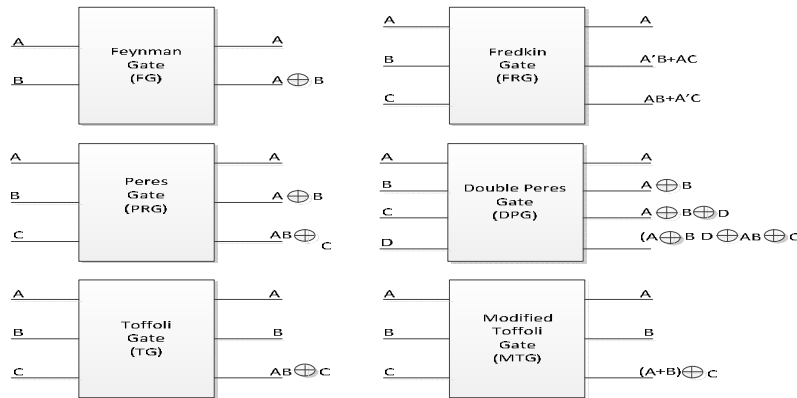


Figure 1: Basic Reversible Gates

3. FFT AND BYPASS MULTIPLIERS

Vital operation of any Digital signal processor is the FFT computation. When the input sequence length does not match with the filter coefficient size while performing circular convolution, zero padding becomes inevitable. In case of linear filtering using overlap-add or overlap-save methods, it becomes mandatory to pad zeroes to the input sequence as well as the impulse response sequence, so that their block sizes match. Zero padding in time domain is used extensively in practice to compute a heavily interpolated spectra; aliter, when we take DFT of a zero padded signal we get a smoother looking frequency resolution. As already stated in the previous section, the bypass multiplier reduces the power dissipation by avoiding those carry save adders which are unnecessarily being used when the input bit coefficient is zero.

To appreciate the bypass technique in the proposed multiplier, consider the following scenario. When linear convolution is performed digitally by fast convolution, a practical difficulty often arises. If the signal has several hundred of samples but an impulse response has less than 50 samples, it would be uneconomical in terms of computing time, storage and above all the power,

to use same length of transform for both input sequence and impulse response sequence. In addition, most of the real time applications use very long transforms lengths for input sequence which may give rise to unacceptable processing delays. This is overcome by segmenting the input sequence into sections of manageable lengths and then performing fast convolution on each section and finally combining the outputs. During processing, the input sequence as well as the impulse response should be zero padded. Since multiplication is performed on these zero padded sequences the normal multipliers dissipate more heat. The bypass technique limits this type of extraneous power dissipations.

4. DESIGN OF BYPASS MULTIPLIERS USING REVERSIBLE LOGIC

4.1 Design of Reversible Column Bypass Multiplier

The reversible column bypass multiplier has three computational blocks namely the product unit, the full adder unit and the column bypass unit. The three units are as shown in figure 2.

1. Product Unit (PU): This unit is used to compute the partial products. It has two inputs and one output. It consists of a single Peres Gate that gives the product term as one of its output. Peres Gate has been used since it has minimum quantum cost in comparison with other gates which give a product term. Thus, the number of gates used is 1 (NG=1), with 2 garbage outputs (GO=2), and one constant input (CI=1), with quantum cost of 4 (QC=4).
2. Full Adder Unit (FAU): This unit is used to compute the sum and the carry. It has three inputs and two outputs. It consists of a single Double Peres gate which alone computes the sum and the carry. This block is used in the last row of the multiplier as a ripple carry adder. The number of gates used is 1 (NG=1), number of garbage outputs is 2 (GO=2), Number of constant inputs is 1 (CI=1), and the quantum cost of the block is 6 (QC=6).
3. Column Bypass Unit (CBU): This unit is used in the carry save adder stages of the column bypass multiplier. It has four inputs and two outputs. Three of the inputs are applied to the Double Peres Gate and the other input is the column bypass control input (CBCI) which is used to control the multiplexer. The multiplexer is realized using a Fredkin Gate which chooses the sum term when CBCI is 1 and the partial product if CBCI is 0. The carry out is passed on unaltered. The unit thus has two gates (NG=2) with four garbage outputs (GO=4), and the number of constant inputs is 1 (NC=1). The quantum cost of the unit is 11 (QC=11).

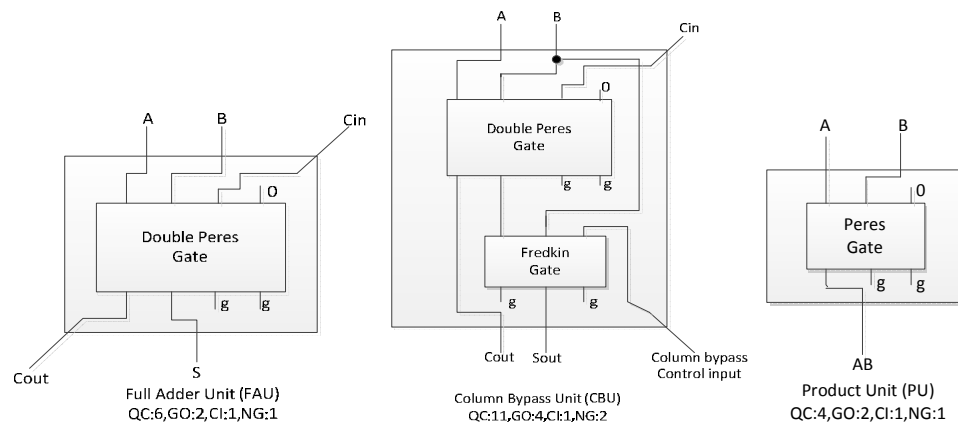


Figure 2: Computational Blocks for Constructing Column Bypass Multiplier

The circuit of a 4X4 Reversible Column Bypass Multiplier is as seen in the figure 3. The Fan-outs are not considered.

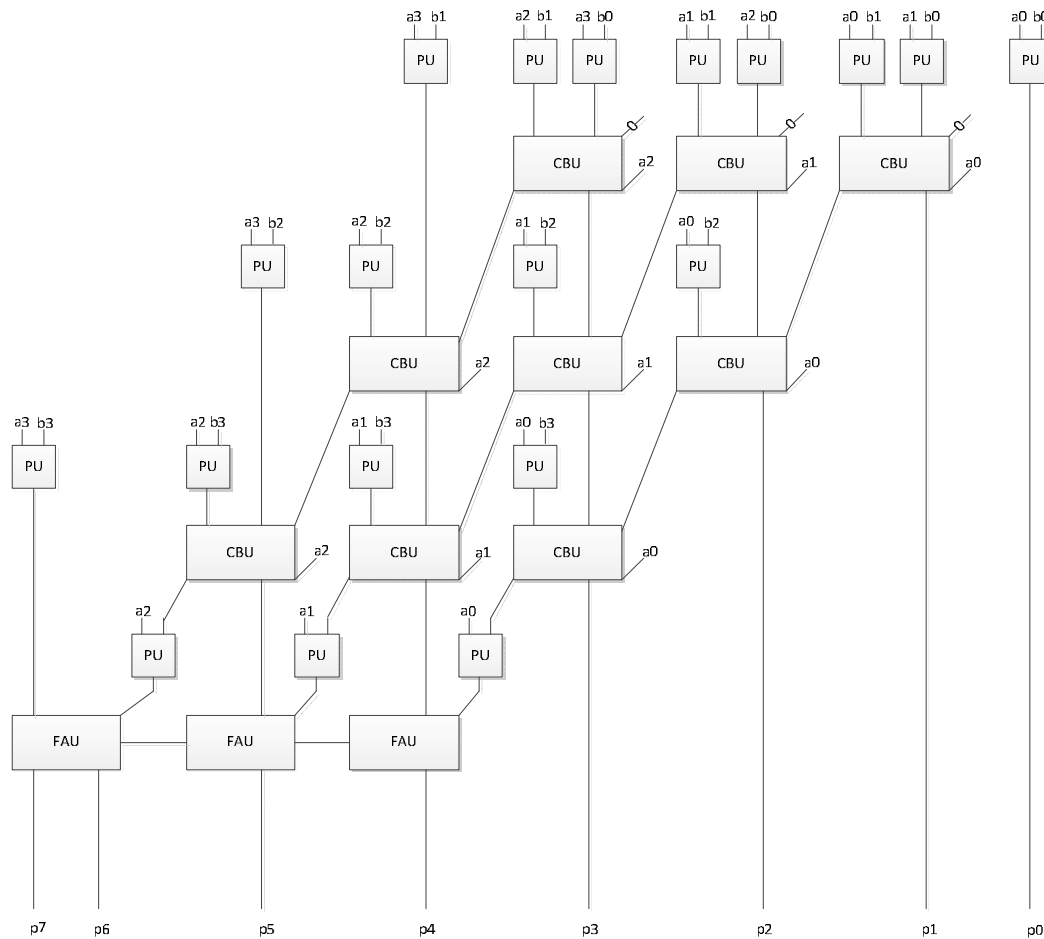


Figure 3: Proposed Design of Reversible Column Bypass Multiplier

4.2 Reversible 2-Dimensional bypass multiplier

The two dimensional bypassing multiplier consists of the following Units which is illustrated in figure.

1. A+1 Adder: It is realized using a single Feynman Gate. The Quantum Cost of this unit is 1 (QC=1), number of gates is 1 (NG=1), Number of constant inputs is 1 (NC=1), and Garbage is 1 (GO=1). This unit is used to increment the partial product 1 in the first row of CSA of multiplier.
2. A+B Half Adder: This unit is used to find the Sum and Carry and realized using a Peres Gate. The Quantum Cost of this unit is 4(QC=4), number of gates is 1 (NC=1), Number of constant inputs is 1 (NC=1), and Garbage is 1 (GO=1). This unit is used to determine the sum in last stage of the multiplier.

3. **A+B+1 Half Adder:** This unit is constructed using two Feynman Gates and a single Modified Toffoli Gate. The Quantum Cost of this unit is 8(QC=8), number of gates is 3 (NC=3), Number of constant inputs is 2 (NC=2), and Garbage is 4 (GO=4). It replaces the functional full adder.
4. **Full Adder:** This unit uses a single Double Peres Gate. The Quantum cost of the unit is 6 (QC=6), number of gates is 1(NC=1), Number of constant inputs is 1 (NC=1), and Garbage is 2 (GO=2). Used in the last row of CSA to incorporate ripple carry addition.
5. **Multiplexer:** It is one of the major components of the bypass multiplier which decides the switching activity of adder cells. It is realized using a single Fredkin Gate. The Quantum Cost of this unit is 5(QC=5), number of gates is 1 (NG=1), Number of constant inputs is 1 (NC=0), and Garbage is 2 (GO=2).

The design of the 4X4 reversible multiplier employing the two dimensional bypassing scheme is as shown in figure Fan-outs are not considered in this design.

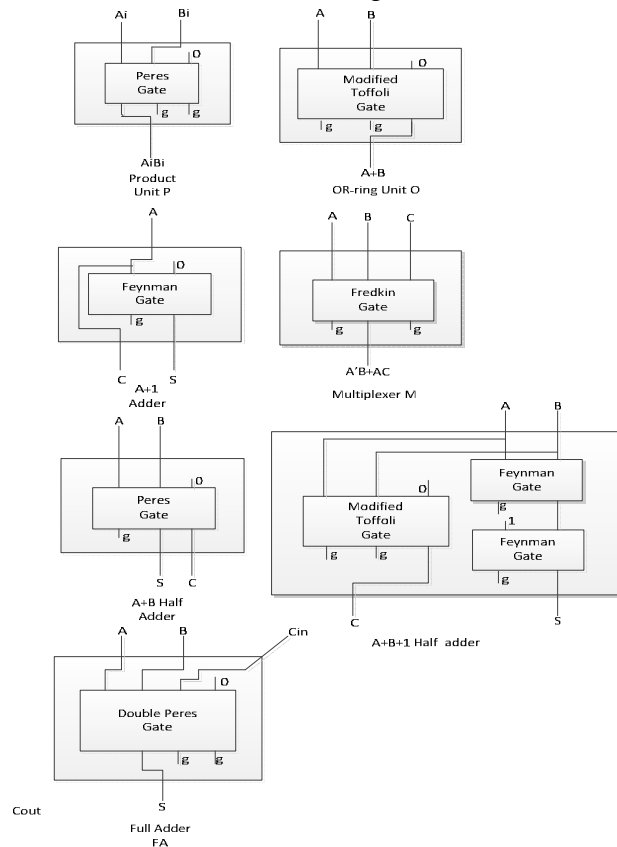
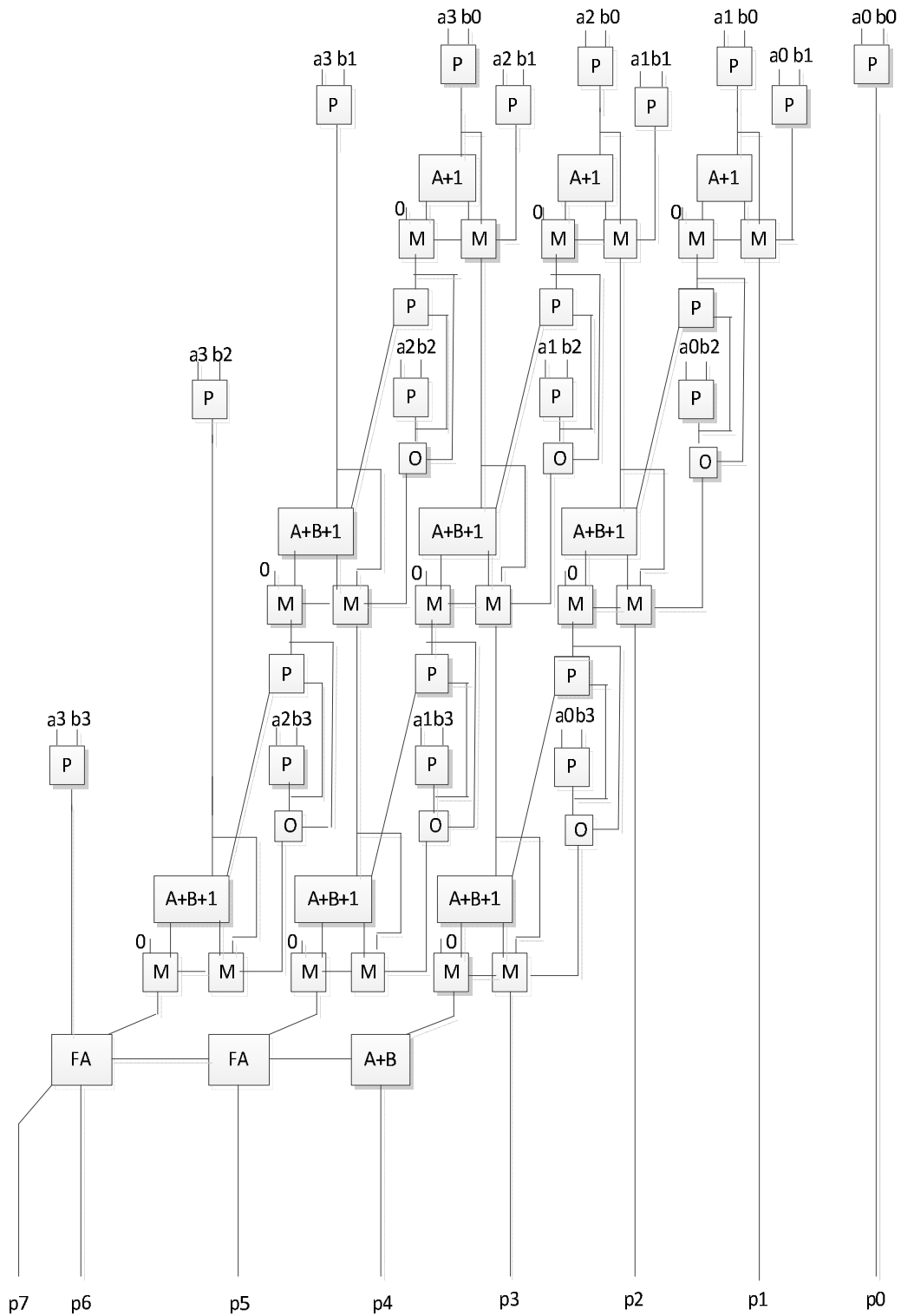


Figure 4: Units for constructing 2-D bypass Multiplier



M=Mux; P=Product Unit; O=OR-ring Unit;

Figure 5: Proposed Design of Two Dimensional Bypass Multiplier

5. RESULTS AND ANALYSIS

The reversible column bypass multiplier and the reversible 2 dimensional bypass multiplier are both simulated to test their functionality using XILINX in conjunction with MODELSIM. The simulation results for a 4X4 reversible column bypass multiplier and 4X4 reversible 2 D bypass multiplier are shown in the figure 6 and 7 respectively. The performance parameters of the two bypass multipliers are compared and tabulated in table 1. This includes comparison of quantum cost, number of garbage outputs, number of constant inputs and number of gates (or the gate cost) of the two circuits.

Table 1: Comparison of the bypass multipliers

Multiplier	Quantum Cost	Garbage outputs	No. Of Gates	Constant Inputs
Column Bypass Multiplier	193	80	40	31
2D Bypass multiplier	271	127	70	62

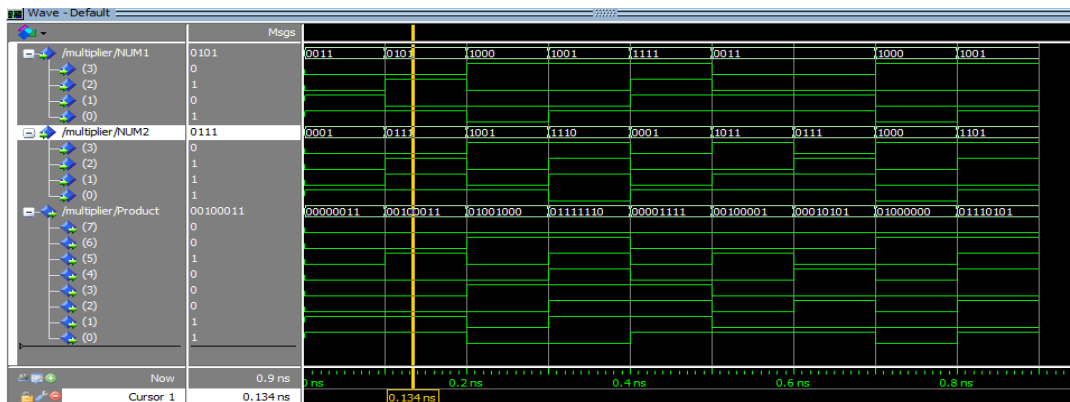


Figure 6: Simulation Results for Column Bypass Multiplier

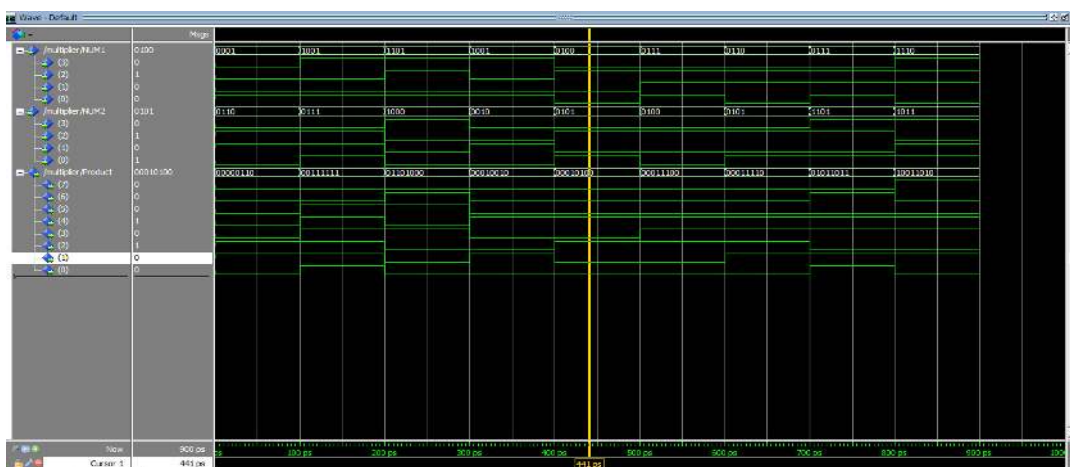


Figure 7: Simulation Results for 2 Dimensional Bypass Multiplier

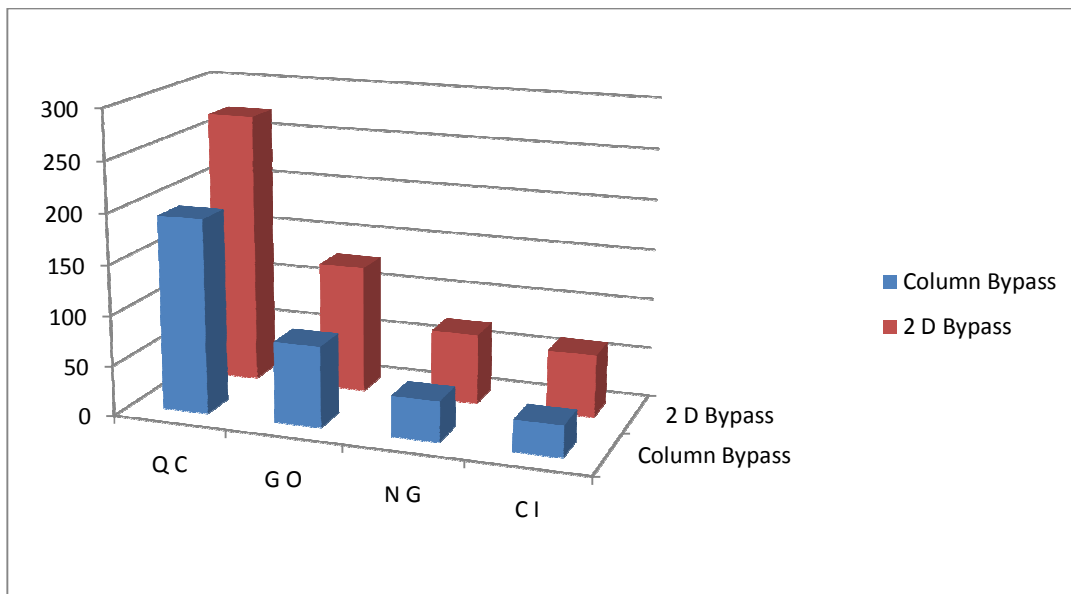


Figure 8: Comparison of Column Bypass and 2 Dimensional Bypass Multipliers' Parameters

The proposed design of column multiplier is compared with other reversible multipliers available in the literature. Table 2 shows the comparison of column bypass multiplier with multipliers in [9], [13],[14], [15], [16] and [17].It is evident from the table that the proposed bypass multiplier design is better or at most comparable to those in the literature besides having bypass units overhead. A graph showing the comparison of quantum cost of bypass multiplier and other multipliers listed above is as shown in figure 9.

Table 2: Comparison of column bypass multiplier with other multipliers

Design	Quantum Cost	Percentage change
Proposed design of Column Bypass Multiplier	193	-
Design [9]	286	-48.18%
Design [13]	244	-26.42%
Design [14]	244	-26.42%
Design [15]	236	-22.27%
Design [16]	234	-21.24%
Design [17]	208	-7.77%

6. CONCLUSIONS

On the concluding lines, this paper boasts to present the first reversible multiplier in the literature that employs a bypassing scheme. Firstly the column bypassing scheme is taken for discussion as it has the advantage that it eliminates the extra correction circuits [7] needed and has a simpler modified full adder as compared to the row bypass multiplier.

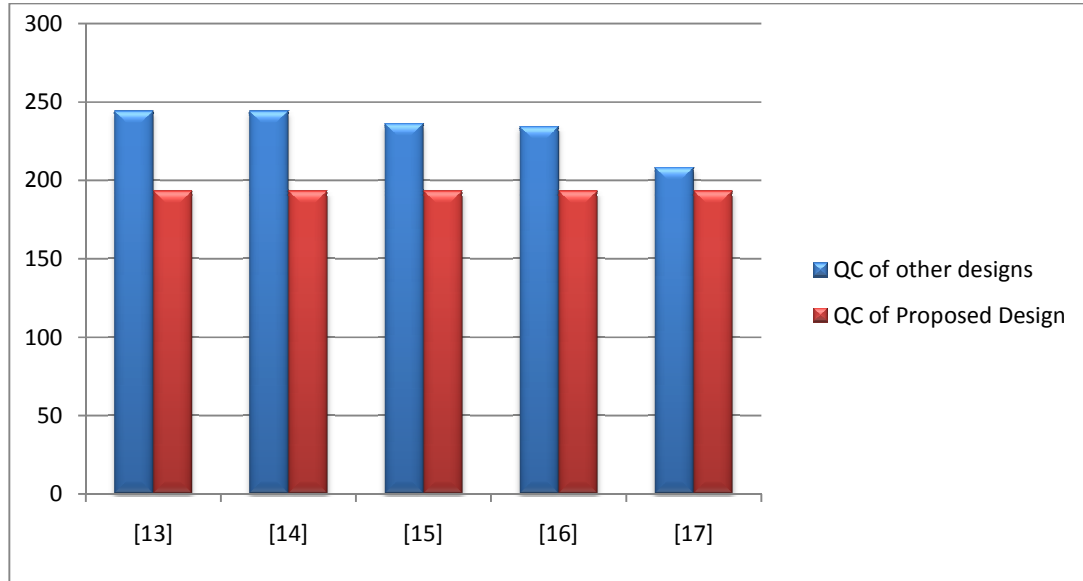


Figure 9: Comparison of Quantum Cost of Column Bypass with other multipliers

The key variation of the proposed multiplier is the presence of Column Bypassing unit. This unit minimizes the switching activity of the multiplier when the binary word has zeros in it. This reduced switching activity in turn yields two more appreciable results i.e. power reduction and delay reduction. The power reduction is already accomplished using reversible logic gates. The delay in this multiplier gets reduced which thereby produces the products faster than the normal multipliers. The design has more quantum cost and garbage outputs than some of the already proposed designs which is mainly due to the presence of bypass units that is not present in other multipliers. Next the 2-D bypass multiplier is considered. The 2-dimensional bypass multiplier includes both row bypassing as well as column bypassing. Thus when the multiplicand has more number of zeros the column bypass unit efficiently reduces the switching activity. Mean while if the multiplier has more number of zeros the row bypass unit takes the charge of reducing the switching activity, combining effectiveness of both systems.

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