{tag}

Authors:

Md. Selim Al Mamun

Syed Monowar Hossain

{bibtex}pxc3883182.bib{/bibtex}

Abstract

Reversible logic has become immensely popular research area and its applications have spread in various technologies for their low power consumption. In this paper we proposed an efficient design of random access memory using reversible logic. In the way of designing the reversible random access memory we proposed a reversible decoder and a write enable reversible master slave D flip-flop. All the reversible designs are superior in terms of quantum cost, delay and garbage outputs compared to the designs existing in literature.

References

-    Rolf Landauer, "Irreversibility and Heat Generation in the Computing Process", IBM Journal of Research and Development, vol. 5, pp. 183-191, 1961.
-    Charles H. Bennett, "Logical Reversibility of computation", IBM Journal of Research and Development, vol. 17, no. 6, pp. 525-532, 1973.
-    Perkowski, M. , A. Al-Rabadi, P. Kerntopf, A. Buller, M. Chrzanowska-Jeske, A. Mishchenko, M. Azad Khan, A. Coppola, S. Yanushkevich, V. Shmerko and L. Jozwiak, "A general decomposition for reversible logic", Proc. RM'2001, Starkville, pp:

119-138, 2001

- J. E Rice, "A New Look at Reversible Memory Elements", Proceedings International Symposium on Circuits and Systems(ISCAS) 2006, Kos, Greece, May 21-24 ,2006, pp. 243-246.

- Dmitri Maslov and D. Michael Miller, "Comparison of the cost metrics for reversible and quantum logic synthesis", http://arxiv. org/abs/quant-ph/0511008, 2006

- Hafiz Md. Hasan Babu, Md. Rafiqul Islam, Ahsan Raja Chowdhury, and Syed Mostahed Ali Chowdhury, "Synthesis of full-adder circuit using reversible logic," International Conference on VLSI Design, vol. 17, pp. 757-760, 2004.

- Richard P. Feynman, "Quantum mechanical computers," Foundations of Physics, vol. 16, no. 6, pp. 507-531, 1986.

- Mohammadi,M. and Mshghi,M, On ?gures ofmerit in reversible and quantumlogic designs, Quantum Inform. Process. 8, 4, 297–318, 2009.

- D. Michael Miller, Dmitri Maslov, GerhardW. Dueck, A Transformation Based Algorithm for Reversible Logic Synthesis, Annual ACM IEEE Design Automation Conference,Proceedings of the 40th annual Design Automation Conference, Anaheim, CA, USA Pages: 318 – 323.

- Perkowski, M. , "A hierarchical approach to computer-aided design of quantum circuits", 6th International Symposium on Representations and Methodology of Future Computing Technology, 201-209, 2003.

- Tommaso Toffoli, "Reversible Computing," Automata, Languages and Programming, 7th Colloquium of Lecture Notes in Computer Science, vol. 85, pp. 632-644, 1980.

- Edward Fredkin and Tommaso Toffoli, "Conservative Logic," International Journal of Theoretical Physics, vol. 21, pp. 219-253, 1982.

- A. Peres, "Reversible Logic and Quantum Computers," Physical Review A, vol. 32, pp. 3266-3276, 1985.

- Sk. Noor Mahammad and Kamakoti Veezhinathan, "Constructing Online Testable Circuits Using Reversible Logic", Ieee transactions on instrumentation and measurement, vol. 59, no. 1, January 2010.

- Himanshu Thapliyal and Nagarajan Ranganathan, Design of Reversible Sequential Circuits Optimizing Quantum Cost, Delay, and Garbage Outputs, ACMJournal onEmerging Technologies inComputer Systems,Vol. 6,No. 4,Article 14, Pub. date:December 2010.

- Lafifa Jamal, Farah Sharmin, Md. Abdul Mottalib and Hafiz Md. Hasan Babu, Design and Minimization of Reversible Circuits for a Data Acquisition and Storage System, International Journal of Engineering and Technology Volume 2 No. 1, January, 2012

- H. Thapliyal and A. P. Vinod, "Design of reversible sequential elements with feasibility of transistor implementation" In Proc. the 2007 IEEE Intl. Symp. On Cir. and Sys. , pages 625–628, New Orleans, USA, May 2007.

- M. -L. Chuang and C. -Y. Wang, "Synthesis of reversible sequential elements," ACM journal of Engineering Technologies in Computing Systems (JETC). Vol. 3, No. 4, 1–19, 2008.

- Matthew Morrison, Matthew Lewandowski, Richard Meana and Nagarajan Ranganathan, "Design of Static and Dynamic RAM Arrays using a Novel Reversible Logic Gate and Decoder" 11th IEEE International Conference on Nanotechnology, Portland, Oregon, USA, August 15-18, 2011

Index Terms

Computer Science   Circuit And Systems

Keywords

Flip-flops   Garbage Output   Random Access Memory   Reversible Logic   Quantum Cost