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Design of Sigma-Delta Modulators for Analog-to-Digital Conversion Intensively Using Passive Circuits

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ABSTRACT

This thesis presents the analysis, design implementation and experimental evaluation of passive-active discrete-time and continuous-time Sigma-Delta (ΣΔ) modulators (ΣΔMs) analog-to-digital converters (ADCs).

Two prototype circuits were manufactured. The first one, a discrete-time 2nd-order ΣΔM, was designed in a 130 nm CMOS technology. This prototype confirmed the validity of the ultra incomplete settling (UIS) concept used for implementing the passive integrators. This circuit, clocked at 100 MHz and consuming 298 μW, achieves DR/SNR/SNDR of 78.2/73.9/72.8 dB, respectively, for a signal bandwidth of 300 kHz. This results in a Walden FoM_W of 139.3 fJ/conv.-step and Schreier FoM_S of 168 dB.

The final prototype circuit is a highly area and power efficient ΣΔM using a combination of a cascaded topology, a continuous-time *RC* loop filter and switched-capacitor feedback paths. The modulator requires only two low gain stages that are based on differential pairs. A systematic design methodology based on genetic algorithm, was used, which allowed decreasing the circuit's sensitivity to the circuit components' variations. This continuous-time, 2-1 MASH ΣΔM has been designed in a 65 nm CMOS technology and it occupies an area of just 0.027 mm^2. Measurement results show that this modulator achieves a peak SNR/SNDR of 76/72.2 dB and DR of 77dB for an input signal bandwidth of 10 MHz, while dissipating 1.57 mW from a 1 V power supply voltage. The ΣΔM achieves a Walden FoM_W of 23.6 fJ/level and a Schreier FoM_S of 175 dB. The innovations proposed in this circuit result, both, in the reduction of the power consumption and of the chip size. To the best of the author's knowledge the circuit achieves the lowest Walden FOM_W for ΣΔMs operating at signal bandwidth from 5 MHz to 50 MHz reported to date.

RESUMO

Esta tese de investigação apresenta a análise, projecto e avaliação experimental de conversores analógico-digital (ADCs) usando moduladores Sigma-Delta (ΣΔM) baseados em amplificadores de baixo ganho e utilizando tempo discreto e contínuo.

Dois circuitos protótipos foram fabricados. O primeiro, um ΣΔM em tempo discreto de segunda ordem, foi implementando numa tecnologia CMOS 130 nm. Este protótipo validou o conceito de circuitos de condensadores comutados com tempo de estabelecimento ultra incompleto (UIS) usado para realizar integradores passivos. Este circuito opera a uma frequência de 100 MHz, tem uma dissipação de potência de 298 μW, apresenta uma DR/SNR/SNDR de 78.2/73.9/77.8 dB, respetivamente, e uma largura de banda de 300 kHz. Estes resultados apresentam uma figura de mérito medido experimentalmente de 139.3 fJ/conv.-step (Walden FoM_W) e de 168 dB (Schreier FoM_S).

O segundo protótipo, consiste num ΣΔM altamente eficiente em temos de área e de potência dissipada, utiliza uma combinação de topologias em cascata, através de filtros *RC* contínuos no tempo, necessitando apenas de dois andares de amplificação com baixo ganho implementados através de pares diferenciais. A malha de realimentação utiliza condensadores comutadores. Foi utilizada uma metodologia de projeto sistemática baseada em algoritmo genético que permite diminuir a sensibilidade do circuito face a variações nos seus components constituíntes. Este 2-1 MASH ΣΔM contínuo foi implementado numa tecnologia CMOS 65 nm e ocupa uma área de apenas 0.027 mm^2. Os resultados medidos mostraram que este modulador atinge uma SNR/SNDR de 76/72.2 dB, e uma DR de 77 dB para um sinal de entrada com uma largura de banda de 10 MHz. Nesta configuração a dissipação de potência é de 1,57 mW para uma tensão de alimentação de 1 V. O ΣΔM apresenta, respectivamente, figuras de mérito de 23.6 fJ/level (Walden FoM_W) e de 175 dB (Schreier FoM_S). A inovação presente neste circuito resulta numa redução na potência dissipada e na área do chip. Este circuito, tanto quanto os autores têm conhecimento, apresenta a mais baixa figura de mérito de Walden para ΣΔMs que operam com sinais cuja largura de banda esta entre os 5 MHz e os 50 MHz, reportada na literatura à date deste documento.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS AND ACRONYMS

Φ	Clock Phase
dB_{FS}	dB Full Scale
F_{in}	Input Signal Frequency
F_S	Sampling Frequency
gm	Transconductance
$mV_{pp,diff}$	mV peak-to-peak, differential
AC	Alternating Current
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
BW	Bandwidth
CMOS	Complementary Metal-Oxide-Semiconductor
CT	Continuous-Time
DAC	Digital-to-Analog Converter
DC	Direct Current
DCL	Digital Cancellation Logic
DFF	D-Type Flip-Flop
DR	Dynamic Range
DRC	Design Rule Check
DT	Discrete-Time
DUT	Device Under Test
ENOB	Effective-Number-Of-Bits
FoM	Figure of Merit
FPGA	Field Programmable Gate Array
GA	Genetic Algorithm
GBW	Gain-Bandwidth Product
IC	Integrated Circuit
LVS	Layout Versus Schematic
MASH	Multistage Noise-Shaping
MiM	Metal-insulator-Metal
MOS	Metal-Oxide-Semiconductor
NTF	Noise Transfer Function

Op-amp	Operational Amplifier
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PECL	Positive Emitter Coupled Logic
PSD	Power Spectral Density
PWM	Pulse-Width Modulation
S/H	Sample and Hold
SC	Switched-Capacitor
ΣΔ	Sigma-Delta
ΣΔM	Sigma-Delta Modulator
SMASH	Sturdy MASH
SNDR	Signal-to-Noise-plus-Distortion Ratio
SNR	Signal-to-Noise Ratio
STF	Signal Transfer Function
UIS	Ultra Incomplete Settling
VCO	Voltage-Controlled Oscillator

1. INTRODUCTION AND MOTIVATION

Analog-to-digital converters (ADCs) are important building blocks in all of today's electronic circuits. They are used in a wide range of devices in medical, consumer, instrumentation and communication applications, just to name a few. Many different ADC architectures are available for a vast selection of resolution and bandwidth requirements. ADCs' performance affects the efficiency and speed at which analog information can be converted into digital signals. Since an energy efficient operation is required by modern electronic systems, there has been a great push to reduce energy consumption in all relevant system building blocks, including ADCs [1]. The constant size reduction of CMOS technologies has resulted in an increase of the transition frequency of CMOS transistors, but it has also resulted in the reduction of the intrinsic gain of these devices [2]. As a consequence, it has become more difficult to design high gain and high bandwidth amplifiers with reduced power dissipation, making the design of ADCs that require such amplifiers, including ΣΔMs, more challenging.

There are several possible implementation choices for ΣΔM architectures [3]. Continuous-time (CT) modulators are becoming more popular than discrete time (DT) modulators, since they can operate at higher clock rates [4, ch. 6]. Recent ΣΔM design trends include higher order loop filters (integrators) [5], digitally assisted digital-to-analog converter (DAC) correction [6, 7], and reduced number of operational amplifiers (op-amps) [5, 8]. These trends have contributed to an improvement of the figures of merit (FoMs) and to the decrease of the circuit active area. In the case of high order ΣΔMs, MASH and SMASH structures reveal better stability and allow for more aggressive noise-shaping than their single-loop counterparts. Therefore, implementations of various MASH-like architectures can be found in recent publications [9-12]. In order to achieve reasonable cancellation of the quantization noise, a high gain in the integrators' amplifiers is desired. The amplifiers can improve the circuit linearity, parasitic insensitivity and robustness in exchange for the power they dissipate. Moreover, gain provided by the amplifiers in the active integrators, reduce the input-referred noise. On the other hand, even with the use of the techniques mentioned previously, the power consumption of the amplifiers is still a significant part of the total modulator's power consumption. In the case of increasing signal bandwidths, together with moderate-high resolutions and with diminishing supply voltage headroom, these amplifiers become difficult to design (since they must achieve a large enough gain-bandwidth product (GBW) to guaranty a small settling error during the limited clock period) and result in an increase of the power dissipation of ΣΔMs.

One solution to deal with an issue of designing high gain amplifiers is to select passive or mixed active-passive ΣΔM architectures, where the processing gain of the comparator is used in the feedback loop of the modulator's filter [13]. This solution is very appealing for deep nanometer CMOS technologies, because a comparator can achieve large gain through positive feedback, which improves with faster transistors. This approach has been used in [13-20]. Passive integrators provide signal attenuation and therefore, are more sensitive to noise coupling than active integrators that use amplifiers. On the other hand, passive ΣΔMs are simpler (have less hardware complexity) compared to their active counterparts, do not require complex amplifiers and allow for significant power reduction.

The research question of this thesis is: how can one take advantage of the passive or hybrid active-passive structures in order to design ΣΔMs achieving competitive power efficiency? Therefore, this thesis intends to investigate the passive and hybrid passive-active ΣΔM architectures and to define the most suitable area of application for these types of modulators.

This work focuses on the design of the integrated circuits (ICs). Therefore, a validation methodology ensuring proper operation of the IC is an important issue. Designing a circuit involves process of building and validating of: behavioral, high-level model of the system; transistor-based circuit schematic; layout and fabricated IC. High-level model, build in order to optimize circuit coefficients, is validated on the basis of its estimated performance. The schematic validation is based on electrical simulations (with process and temperature variations). At this point, one can verify if the system is working properly, according to the desired specifications. After the layout design the validation additionally includes post-layout simulations (including parasitics of the circuit) of the whole system, letting the designer to obtain the closest results to real behavior of the circuit. The most important and final is the validation of the IC prototype. The IC is soldered on the specially designed, fabricated testing board. Then meaningful data is collected and processed, following good measurement practices. If the obtained results meet the specification, the prototype can be considered as validated.

The first proposed implementation for a passive-active ΣΔM is based on ultra-incomplete settling (UIS). In this approach, a single switched-capacitor branch can implement a discrete-time (DT) lossy-integrator. As a proof of this concept, a 2^{nd} order ΣΔM, has been built in a 130 nm CMOS technology and experimentally evaluated [21].

The second proposed implementation of a passive-active modulator is a continuous-time cascaded ΣΔM based on passive *RC* integrators (derived from the UIS structure [21]) and using low gain stages (~20 dB) instead of high gain amplifiers. Like in all circuit techniques, there are limits to the maximum achievable performance and the passive modulator structure requires a higher clock frequency (higher oversampling ratio) than other techniques used to design ΣΔMs. This means that, that if the signal bandwidth is increased, the clock frequency would have to increase as well, in order to maintain the same signal-to-noise-plus-distortion ratio (SNDR).

Therefore, it would be very difficult to design the passive or passive-active modulator for high bandwidth applications. The analysis of various higher order ΣΔM topologies, supported by the optimization methodology, revealed that the passive-active modulator structures are suitable for moderate resolution (62 dB < SNDR ≤ 74 dB) and a medium signal bandwidth (5 MHz < BW ≤ 20 MHz) applications. Therefore, it was decided to design, fabricate and measure a moderate resolution ΣΔM achieving SNDR larger than 70 dB for a signal bandwidth of 10 MHz that occupies a small active area.

The final prototype developed in this thesis is a continuous-time 2-1 MASH ΣΔM based on passive *RC* integrators and low gain stages (~20 dB). The circuit has been designed in a 65 nm CMOS technology and occupies an active area of only 0.027 mm^2. Measurement results show that the modulator achieves a peak SNR/SNDR/DR of 76/72.2 dB/77dB for an input signal bandwidth of 10 MHz, while dissipating 1.57 mW from a 1 V power supply voltage. The proposed ΣΔM achieves a Walden FOM of 23.6 fJ/level and a Schreier FOM of 175 dB. The innovations proposed in this circuit result, both, in the reduction of the power consumption and of the chip size. To the best of the author's knowledge the modulator achieves the lowest Walden FOM_W for ΣΔMs with signal bandwidth from 5 MHz to 50 MHz reported to date.

1.1. Contributions

The main contributions of this research thesis are concentrated in the development and improvement of ΣΔM circuits using passive integrators. In this thesis we study and compare the behavior of passive and active ΣΔM architectures. This work also provides theoretical analysis of the proposed discrete-time and continuous-time passive integrators. These contributions have led to various publications. The main contributions of this work are summarized next:

- The derivation of the discrete-time transfer function and *Z* transfer function of the passive switched-capacitor integrator, using ultra incomplete settling (UIS), was shown in [22]. It also presented the thermal noise analysis of this passive integrator and studied the behavior of the 1st-order passive ΣΔM. Moreover, [23] analyzed the non-ideal effects present in the passive integrator, which become more significant for higher clock frequencies. It also presented two examples of 1st-order passive ΣΔMs operating with 100 MHz and 300 MHz sampling frequencies together with the results of the transient-noise electrical simulations of these two circuits.

- A 2nd-order ΣΔM circuit based on the discrete-time switched-capacitor integrators using ultra incomplete settling and implemented in 130 nm CMOS technology was proposed and described in [24]. The measured key performance parameters of three prototype circuit samples were presented in [21]. This approach allowed building a ΣΔM with mostly dynamic elements thus reducing the power dissipation. The ΣΔM architecture using this technique was presented and analyzed in detail. The validity of ultra

incomplete settling concept was confirmed by high-level simulations, transient noise electrical simulations and measurement results. The 2nd-order ΣΔM circuit, clocked at 100 MHz and consuming 298 μW, achieved a peak DR/SNR/SNDR of 78.2/73.9/72.8 dB, respectively, for a signal bandwidth of 300 kHz. This resulted in a FoM_W of 139.3 fJ/conv.-step and FoM_S of 168 dB.

- A discrete-time, switched-capacitor, 2-2 MASH ΣΔM, clocked with frequency of 1 GHz, designed in a 65 nm CMOS technology was proposed in [25]. This modulator, similarly to the previous examples, was based on the passive integrators using the ultra-incomplete settling concept. Its high-level model and transistor-level implementation were discussed as well as modulator sensitivity to components variation. The work presented in [25] shown that it is possible to design MASH ΣΔM, using UIS integrators, operating in a 10 MHz bandwidth with a moderate resolution.

- A design methodology for ΣΔMs based on optimization using a genetic algorithm, was proposed in [26]. In order to obtain more accurate and faster performance predictions of a given ΣΔM architecture, the evaluation process is divided into a coarse (fast, equation based) and fine (slow, recursive simulation based) evaluations. It uses a high-level model of a given design, together with its theoretically estimated thermal noise, quantization noise, voltage swing variations and stability of the modulator. Furthermore, by taking into account mismatch errors between the circuit's components, it also selects the most insensitive design solution to components' variations. As a proof of validity of the methodology presented in [26], two case studies of continuous-time and a discrete-time ΣΔMs were carefully discussed.

- A passive-active 2-1 MASH modulator, using *RC* integrators and simple low gain stages (~20 dB) was presented in [27]. In this work, a continuous-time implementation of the passive integrator with switched-capacitor feedback DAC has been proposed. A MASH modulator structure requires a digital cancellation logic that combines and filters its digital output signals (coming from the MASH stages). Therefore, simplified digital cancellation logic was proposed, which allowed for reduction in power and in number of components (avoiding multipliers, adders and multiplexers). The 2-1 MASH ΣΔM was implemented in a 65 nm CMOS technology and it occupied an active area of only 0.027 mm^2. Measurement results showed that the circuit clocked at 1 GHz achieved a peak DR/SNR/SNDR of 77/76/72.2 dB for an input signal bandwidth of 10 MHz, while dissipating 1.57 mW from a 1 V power supply voltage. This modulator achieved a measured Walden FoM of 23.6 fJ/level and a Schreier FoM of 175 dB.

1.2. Thesis Layout

The thesis is composed of seven chapters (including the present introduction). It is structured as follows:

- **Chapter 2** presents principles of ΣΔ modulation and basic definitions about ΣΔMs. It also describes performance metrics used for evaluating ADCs, techniques of reducing the feedback DAC nonlinearities and methods to further improve modulator's figure of merit.

- **Chapter 3** gives a brief literature review regarding architectures and techniques used in designing recent single-loop and cascaded ΣΔMs. It also presents a comparison between selected state-of-the-art ΣΔMs.

- **Chapter 4** compares active and passive ΣΔMs structures and gives insight into discrete-time and continuous-time implementations of passive integrators. In the last section it presents a general ΣΔM design methodology based on a genetic algorithm.

- **Chapter 5** provides the high level and transistor level analyzes of the passive and hybrid passive-active ΣΔMs. It discusses several modulators' case studies that include 1st, 3rd-order single-loop ΣΔMs and cascaded ΣΔMs. It also presents implementation details of two integrated prototypes, namely a discrete-time 2nd-order ΣΔM and a continuous-time 2-1 MASH ΣΔM.

- **Chapter 6** presents the chip floor-planning, layout design, evaluation printed-circuit-board (PCB) design, testing setup and measured data obtained from the experimental evaluation of the two ΣΔMs prototypes: 1) a discrete-time 2nd-order ΣΔM; 2) a continuous-time 2-1 MASH ΣΔM.

- **Chapter 7** discusses the results obtained by the evaluated circuits, comparing them to other state-of-the-art ΣΔMs and it presents conclusions concerning this work as well as suggests topics for future work.

2. BASICS OF SIGMA-DELTA MODULATORS

This chapter presents some basic definitions about ΣΔM including description of different architectures and their analytical stability issues as well as performance metrics, techniques of DAC linearization and methods to improve modulators' figure of merits.

2.1. Principles of Sigma-Delta Modulation

Sigma-delta (ΣΔ) modulation consists of two main operations, namely, oversampling and noise shaping, which are described in this chapter. Below we start by presenting basic principles of analog to digital (A/D) conversion, which apply directly to sigma-delta modulator (ΣΔM).
A general analog to digital converter (ADC) (Fig. 2.1) is composed of:

- An anti-aliasing filter, which prevents folding or aliasing (interference between signal spectrum and its repeated versions) of high frequency components falling into the signal bandwidth;
- A sample and hold (S/H), that samples the continuous signal $x_1(t)$ at sampling frequency F_s producing discrete signal $x_1(n)$ (time discretization);
- A quantizer, which provides non-invertible process of mapping of continuous range of amplitudes of its input signal to finite number of discrete levels (amplitude discretization);
- A binary encoder, that transforms each level of the quantizer output signal into a unique binary code.

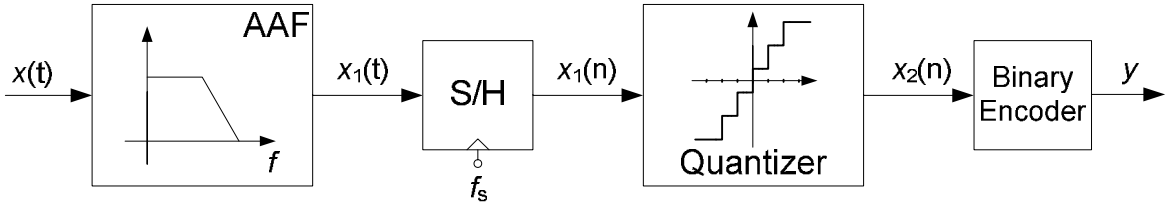

Fig. 2.1 Conceptual scheme of an ADC system

One of the main categories of data converters are the Nyquist-rate converters. In this type of

ADCs the sampling process is performed with a frequency of, at least, twice the signal bandwidth (BW) $fs = 2 \cdot \mathrm{BW}$ (usually somewhat higher because of practical reasons). This is the minimum F_s, which can be used according to the Nyquist theorem. This category of ADCs has one-to-one correspondence between their input and output signals. The converter has no memory and the samples are processed separately [4]. Each sequence (of given length) of the ADC input samples corresponds to its processed digital output word (of the same length).

The accuracy of a Nyquist-rate converter is mainly determined by the matching of its analog components. Therefore, it is difficult to achieve high resolutions for this type of ADCs [28]. Moreover the conversion resolution depends on the resolution of the quantizer. Concluding, one can claim that quantization and sampling operations limit the performance of Nyquist-rate converters.

The second category of A/D data converters are the oversampled converters. Their sampling rate is higher than the Nyquist rate, $fs \gg 2 \cdot \mathrm{BW}$, (typically by factor 8 to 512 [4, p. 3]). The oversampling ratio (OSR) is defined as:

$$\mathrm{OSR} = fs / (2 \cdot \mathrm{BW}) \tag{2.1}$$

In a sigma delta modulator (ΣΔM), which is an example of an oversampling converter, there is no one-to-one correspondence between input and output signals, because the converter uses all the preceding input samples to generate a valid output. This feature requires memory elements in the ADC structure.

The oversampled converter, in contrary to the Nyquist-rate converter, does not require a sharp cut-off in the anti-aliasing filter, which could introduce phase distortion for signal components close to the cut-off frequency [29]. This means that, the requirements for anti-aliasing filter are relaxed as one can notice in Fig. 2.2.

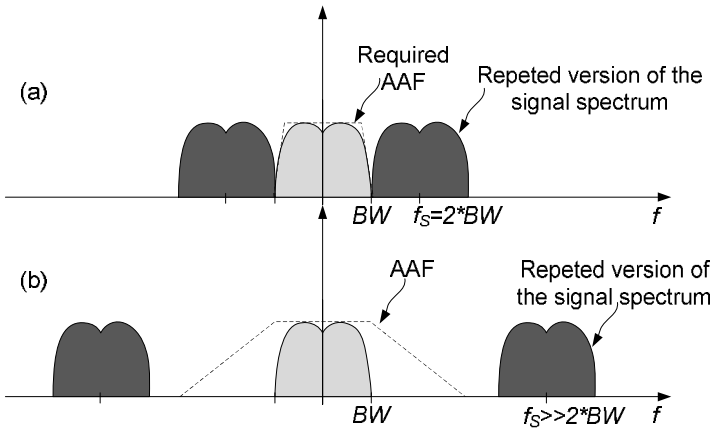

Fig. 2.2 Representation of anti-aliasing filter (a) for Nyquist-rate (b) for oversampling ADC

The ideal staircase characteristic of a quantizer is depicted in Fig. 2.3a. The digital output has 2^B discrete levels. This number depends on resolution of the B-bit quantizer. The difference between two adjacent levels is called the quantization step, Δ, and can be calculated as

$\Delta = Y_{MAX} / (2^B - 1)$. For all input signals, in the range of X_{MAX}, the quantization error e_Q is limited to ±Δ/2, as depicted in Fig. 2.3b and its average value is zero. The quantization error, conceptually, can be defined as the difference between the analog version of its output and input signals. For inputs exceeding X_{MAX} the quantizer becomes overloaded and its e_Q grows beyond ±Δ/2.

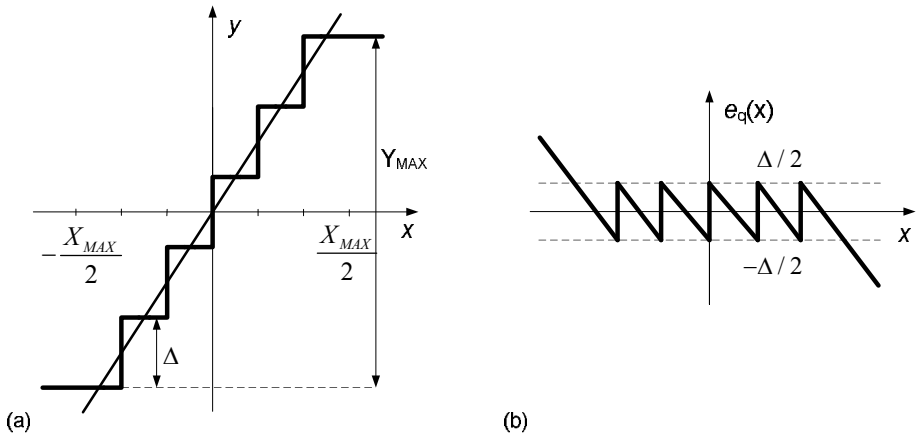

Fig. 2.3 (a) Ideal characteristic of quantizer. (b) Quantization error

Assuming a rapidly varying input signal, the quantization error becomes uniformly distributed between ±Δ/2 [30, p. 450]. This allows the quantizer, which is a nonlinear element, to be linearized and its e_Q modeled as, non-correlated with input signal, white quantization noise. The power spectral density (PSD) of the total quantization noise power equals:

$$S_Q(f) = \frac{1}{F_S}\left[\frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e_q^2 de_q\right] = \frac{\Delta^2}{12F_S} \tag{2.2}$$

and the in-band quantization noise power is given by:

$$P_Q = \int_{-\mathrm{BW}}^{\mathrm{BW}} S_E(f)df = \frac{\Delta^2}{12 \cdot \mathrm{OSR}} \tag{2.3}$$

One can notice that, theoretically, doubling OSR decreases the P_Q by 3 dB. The fixed quantization noise power spreads over the sampling frequency range F_S, which is greater in case of an oversampled ADC than in case of a Nyquist-rate ADC. This means that, the P_Q of the former is much smaller comparing to the latter ADC (Fig. 2.4).

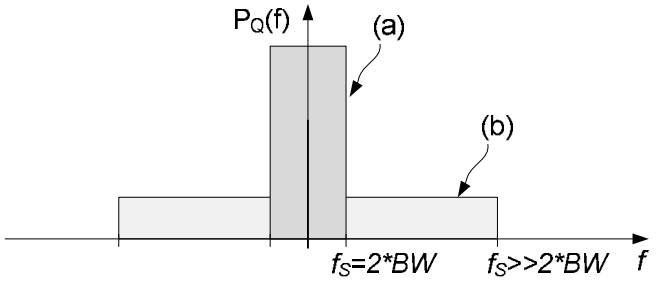

Fig. 2.4 Spectral density of quantization noise power for: (a) Nyquist-rate and (b) oversampling converter

Two main types of oversampling converters are delta (Δ) and ΣΔ modulators. A Δ modulator has the disadvantage of amplifying the nonlinear DAC distortion in the signal band. The ΣΔM, which has a loop filter in a forward path (instead of feedback path, like in case of a Δ modulator) avoids this shortcoming [4, ch. 1]. This modulator, shown in Fig. 2.5a, contains an internal ADC, a DAC and a loop filter (here, an integrator). Fig. 2.5b depicts a linear sampled-data system with a quantizer represented by a linear, additive white noise model.

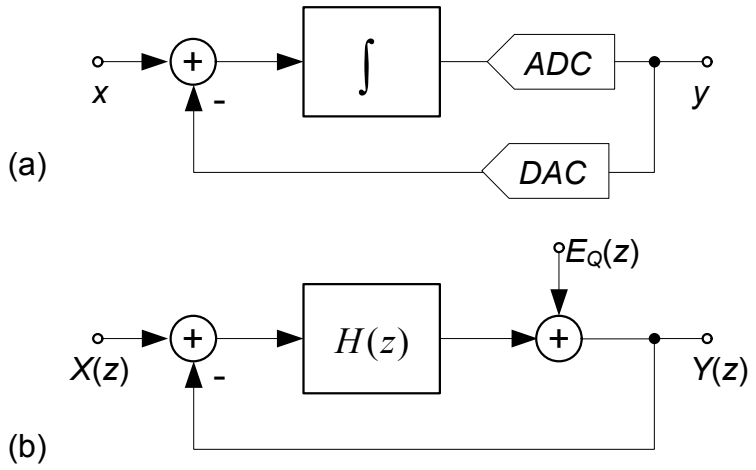

Fig. 2.5 (a) ΣΔM ADC and (b) its linear z-domain model.

The Z-domain output of the above system (having two independent inputs) can be represented by:

$$Y(z) = X(z)\cdot \mathrm{STF}(z) + E_{\mathrm{q}}(z)\cdot \mathrm{NTF}(z) \tag{2.4}$$

where $X(z)$ and $E_Q(z)$ are the Z-transforms of x and e_Q respectively, and STF(z) and NTF(z) are the signal- and noise transfer functions, respectively given by:

$$\mathrm{STF}(z) = \frac{H(z)}{1+H(z)}; \quad \mathrm{NTF}(z) = \frac{1}{1+H(z)} \tag{2.5}$$

In general, if in signal band $H(z)$ has a high gain, resulting in STF(z) being close to one and very small NTF(z) (the zeros of the NTF(z) are the equal to poles of $H(z)$). This means that, the input signal is largely unaffected, whereas the quantization noise is strongly attenuated. In the ideal situation, the quantization noise would be completely cancelled for a DC signal (if $H(z{=}1) \rightarrow \infty$). The NTF($z$), in the ideal case, can be defined as:

$$\mathrm{NTF}(z) = (1-z^{-1})^{L} \tag{2.6}$$

where L denotes the filter order, P_Q can be recalculated as (assuming that $z{=}e^{j2\pi/Fs}$, OSR>>1 and that the quantization error can be modeled as an additive white noise source):

$$P_Q \equiv \int_{-\mathrm{BW}}^{\mathrm{BW}} \frac{\Delta^2}{12\cdot F_S}\left|\mathrm{NTF}(f)\right|^2 df \simeq \frac{\Delta^2}{12}\cdot\frac{\pi^{2L}}{(2\cdot L+1)\cdot \mathrm{OSR}^{2\cdot L+1}} \tag{2.7}$$

One can notice that, in the case of noise shaping, doubling the OSR decreases the P_Q by $6L$ dB more than in case of using just oversampling (which is 3 dB - (2.3)). Fig. 2.6, illustrates the general noise shaping curves for different NTFs, and it confirms this conclusion. Noise shaping causes less in-band (f_0) noise than in case of a Nyquist-rate converter.

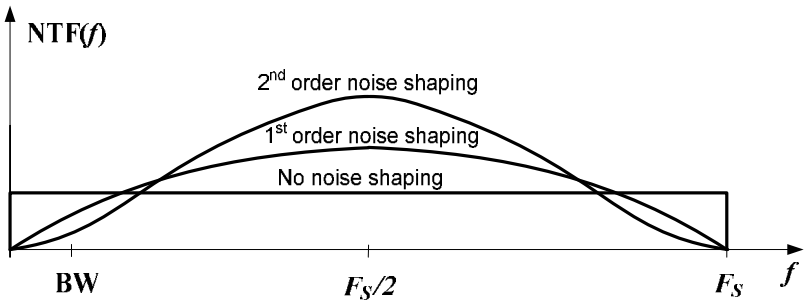

Fig. 2.6 Examples of noise shaping transfer functions

A ΣΔM converter incorporates, both, oversampling and quantization noise shaping, which allow improving performance of an ADC. These two operations allow relaxing the complexity of the analog circuitry. The anti-aliasing filter does not need sharp transition band and the quantizer resolution can be lower than in the case of Nyquist-rate converter. The price to pay for these improvements is mainly the required faster system operation for the same signal bandwidth and additional digital circuitry for the output filter. As mentioned before, the noise filtering "pushes" the quantization noise to higher than signal bandwidth frequencies. This noise power has to be strongly attenuated by employing a digital low-pass filter after the ADC. After digital filtering, the signal is usually downsampled to Nyquist rate without affecting the signal-to-noise ratio. The operation of filtering and downsampling is known as decimation.

2.2. Performance Metrics

The accuracy of ΣΔM converters is degraded by their internal thermal noise (inherent to the circuit) and by their quantization noise (generated during the modulation process). The performance of a ΣΔM is evaluated by metrics, which are described below.

The signal-to-noise ratio (SNR) is the ratio of the output signal power at the frequency of an input sinusoid (with amplitude A) to the in-band noise power. For simplicity reasons, in the expression below, the quantization noise power P_Q is considered.

$$\mathrm{SNR} \equiv \frac{A^2}{2P_Q} \tag{2.8}$$

The dynamic range (DR) is the ratio of the output signal power at the frequency of an input sinusoid (with maximum amplitude A_{MAX}) to the output power for a small input for which one has SNR = 0 dB.

$$\mathrm{DR} \equiv \frac{A_{MAX}{}^2}{2P_Q} \tag{2.9}$$

Taking into consideration (2.7) the ideal DR is expressed as:

$$\mathrm{DR}\,|_{dB} = 10 \cdot \log\left[\frac{3 \cdot (2^B - 1)^2 \cdot (2 \cdot L + 1) \cdot \mathrm{OSR}^{2 \cdot L + 1}}{2 \cdot \pi^{2 \cdot L}}\right] \tag{2.10}$$

In order to take into consideration the aforementioned noises and distortions affecting the output signal, the signal-to-noise-plus-distortion ratio (SNDR) is used. A typical graph of the SNDR, of the SNR and of the DR is illustrated in Fig. 2.7. The values SNR_{peak} and SNDR_{peak} refer to the maximum values of SNR and SNDR. One can notice that, the SNR increases with A_X until A_X reaches the overload value X_{OL}. Beyond this level the quantizer often starts to be overloaded and, hence the SNR curve drops abruptly. The SNDR_{peak} value is lower than SNR_{peak} because the distortion is taken into consideration.

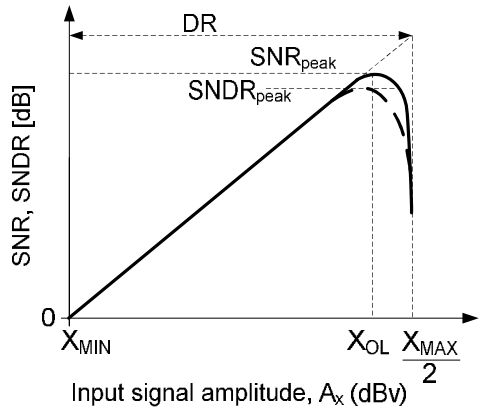

Fig. 2.7 Basic performance metrics: SNR, SNDR, DR

The effective-number-of-bits (ENOB) of ΣΔM is given by the equation:

$$\mathrm{ENOB}\,|_{bits} \simeq \frac{\mathrm{SNDR}_{peak} - 1.76}{6.02} \tag{2.11}$$

In order to compare different modulator circuits and classify them, several figure of merits (FoM) can be defined. The Walden FoM ($\mathrm{FoM_W}$) takes into consideration the main specification metrics like: ENOB, signal bandwidth, and power consumption of a given ΣΔM [31]. The smaller the $\mathrm{FoM_W}$, a given ADC can achieve, the better is its energy efficiency.

$$\mathrm{FoM_W}\,|_{\mathrm{fJ}/conv-step} = \frac{P_C}{2^{\mathrm{ENOB}} \cdot 2 \cdot \mathrm{BW}} \cdot 10^{15} \tag{2.12}$$

Another well-known FoM used to rank circuits is the Schreier $\mathrm{FoM_S}$. In this case, better circuits (i.e. more energy efficient) reach larger $\mathrm{FoM_S}$.

$$\mathrm{FoM_S}\,|_{dB} = \mathrm{DR} + 10\log\left(\frac{\mathrm{BW}}{P_C}\right) \tag{2.13}$$

2.3. Basic Architectures of ΣΔMs

ΣΔM architectures can be mainly classified into few different categories:

- Discrete-time, continuous-time and hybrid continuous-time/discrete-time modulators (category classified according to type of loop filter);
- Single-bit/multi-bit modulators (category classified according to number of bits of the internal quantizer);
- Single-loop and cascade - multistage noise-shaping (MASH) modulators (category classified according to the number of quantizers used in a complete modulator).

Moreover, ΣΔMs can also be categorized according to input signal bandwidth being processed, resulting in low-pass and band-pass ΣΔMs.

2.3.1. Low-Pass Single-Loop ΣΔM

The first presented architecture of the considered modulators is first order discrete-time ΣΔM, illustrated in Fig. 2.8.

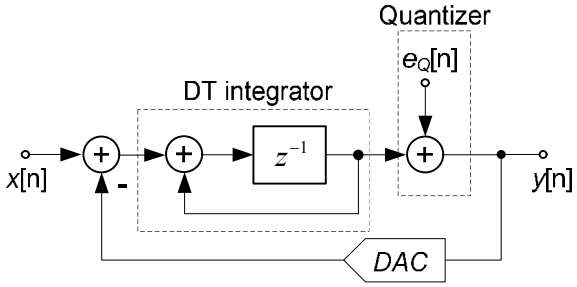

Fig. 2.8 Example of a 1st-order discrete-time ΣΔM

The loop filter is a discrete-time integrator, whose Z transfer function given by $H(z)=z^{-1}/(1-z^{-1})$, results in $\mathrm{STF}(z)=z^{-1}$ and $\mathrm{NTF}(z)=1-z^{-1}$. The 1st-order ΣΔM shapes quantization noise with 20 dB/decade slope (Fig. 2.9).

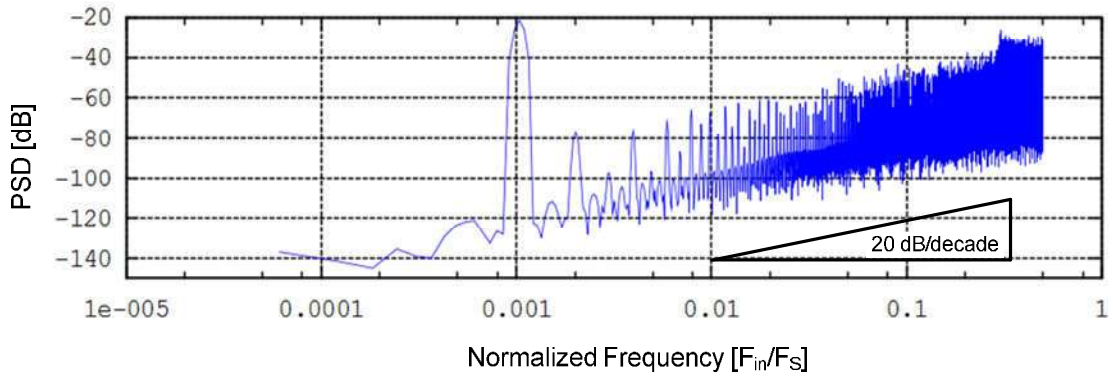

Fig. 2.9 Example of spectral density of the 1st-order ΣΔM output signal power

An example of the output spectrum of the 1st-order ΣΔM is shown in Fig. 2.9. A disadvantage of the 1st-order ΣΔM is the quantization error power that is not uniformly distributed over the

entire spectrum and it contains strong tone distortion components. The reason is that the quantization error is strongly correlated with input signal, which leads to a colored quantization error instead of white noise and it raises and accumulates the in-band error power. The second disadvantage of this type of modulator is that doubling the OSR theoretically only improves SNR by 9 dB (1.5 bit) (in reality this assumption is often not accurate because of the above mentioned correlation between input signal and quantization error). This is because, 1st-order ΣΔM requires large OSR for accurate A/D data conversion. In practice 1st-order ΣΔM are not widely used [28].

The problems described above can be mostly avoided by adding to the previous system one additional integrator and an extra feedback branch, which translates in using a second-order modulator (Fig. 2.10).

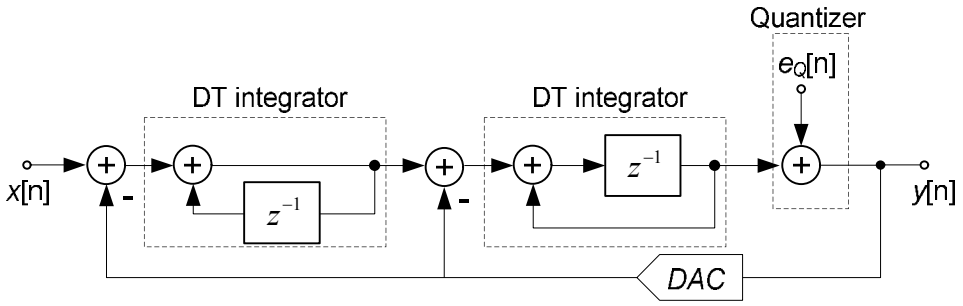

Fig. 2.10 Example of second-order ΣΔM

In this case $\mathrm{STF}(z)=z^{-1}$ and $\mathrm{NTF}(z)=(1-z^{-1})^2$. The 2nd-order ΣΔM shapes the quantization noise with 40 dB/decade slope. It provides additional in-band quantization noise suppression and it amplifies more efficiently the noise outside the signal bandwidth. Moreover the use of two integrators also helps to decorrelate the quantization error from input signal (less idle tones in output spectrum). The SNR of a 2nd-order ΣΔM improves by 15 dB (2.5 bits) each time the OSR is doubled.

By adding more integrators and feedback branches, higher order modulators can be created. Their $NTF(z)=(1-z^{-1})^L$ and the quantization noise is shaped with $20\cdot L$ dB/decade. Fig. 2.11 shows the theoretical relationship between the order of the ΣΔ modulator versus the OSR value that allows achieving a particular SNR.

Doubling the OSR improves the SNR by $6L+3$ dB ($L+0.5$ bit) and it results in less in-band noise and extra noise pushed into higher frequencies. However, in reality it is hard to achieve the theoretical performance because of some limitations of higher order structures. The main difficulty is that a high order ΣΔM is only conditionally stable when single-bit quantizer is utilized. The stability can depend either on precise circuit coefficient matching or limited range of input signal amplitudes. In particular, large input amplitudes can cause instability of the modulator, which may never return to stability, even when the input signal decreases [30, p. 556].

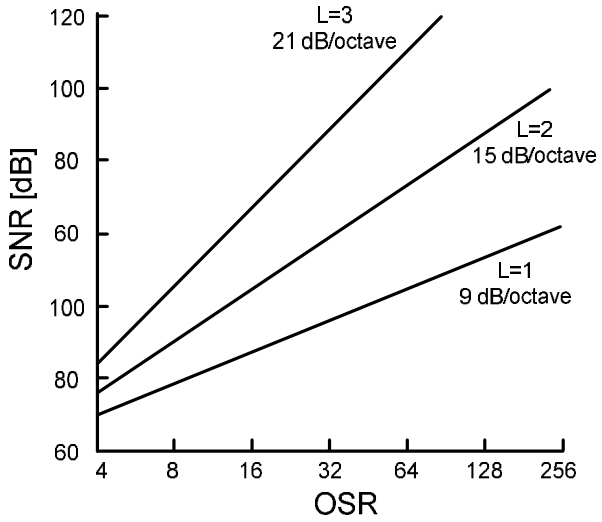

Fig. 2.11 Theoretical SNR vs. OSR and modulator order [32].

2.3.2. Discrete-Time and Continuous-Time ΣΔM

The previously presented low-pass structures are discrete-time ΣΔMs. The conceptual diagram of a discrete-time modulator is illustrated in Fig. 2.12a. Usually, it is necessary that the modulator is preceded by an anti-aliasing filter. The filtered input is sampled and held by the S/H block and then made available to remaining part of the completely discrete-time modulator. It should be mentioned that in a switched-capacitor (SC) implementation the S/H block is not required because the switched-capacitor integrators already perform, inherently, the sampling operation.

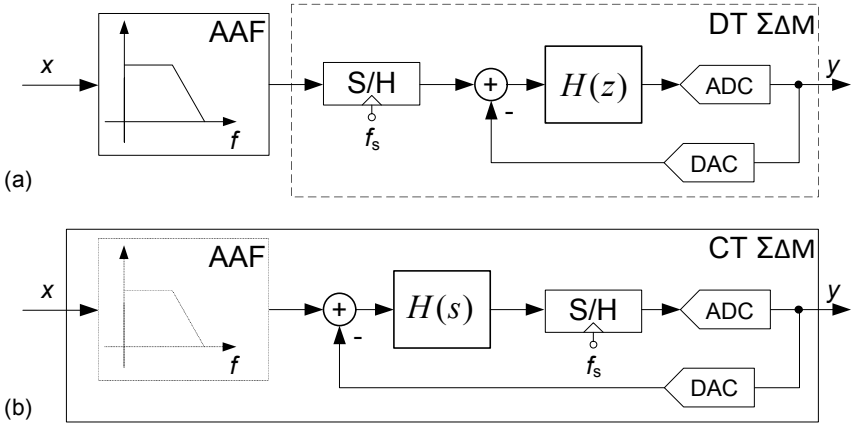

Fig. 2.12 (a) Discrete-time and (b) continuous-time modulators

The block diagram of a continuous-time modulator is depicted in Fig. 2.12b, using a continuous-time integrator while the rest of the circuit operates in the discrete-time domain. Therefore, the output signal of a continuous-time ΣΔM is discrete-time. One can notice that, the sampling operation occurs at the output of the loop filter. This node is less sensitive than input of the modulator and, moreover, it is already in a shaping loop of the ΣΔM. This is because the S/H imperfections and the wideband noise folding do not affect the circuit as much as in the

case of discrete-time ΣΔM. In this architecture the anti-aliasing filter usually is not required because both, sampling and quantization, occur at the same point in the loop [4, ch. 6.6.2]. Since quantization is usually modeled as addition of noise, the sampling can be regarded as addition of aliases. Therefore, the alias signals are usually attenuated by the same amount as the quantization noise.

Continuous-time ΣΔMs allow designers using two to four times larger F_S and consequently achieve larger signal bandwidth than switched-capacitor discrete-time modulators. In the former ones, F_S is limited by the quantizer regeneration time and by the update rate of the feedback DAC, while in the latter ones, F_S is limited by settling requirements of operational amplifier (op-amp) to about 20% of its unity gain frequency [4, p. 206].

Despite of the previously mentioned advantages of the continuous-time ΣΔM architecture, it should be mentioned that the continuous-time signals have to be processed with high linearity and, on the other hand, that the system is sensitive to DAC memory effects [33, p. 297]. Moreover a continuous-time ΣΔM is more sensitive to the clock jitter noise than its discrete-time counterpart. This noise affects mainly the S/H and DAC, blocks working with discrete-time signals (Fig. 2.13a). The jitter noise is not critical for the S/H because, as mentioned before, in continuous-time architecture the errors added by the S/H are attenuated, in band, by the noise shaping. However, in the DAC, the jitter error is introduced at the input of the ΣΔM without any attenuation. Fig. 2.13b shows that in a switched-capacitor implementation, because of the complete settling of the charge in the capacitor, the charge loss caused by jitter is relatively small. In the case of the continuous-time circuit the rate of charge transferred during the whole period is constant. This means that, the charge loss due to jitter is, in this situation, more significant.

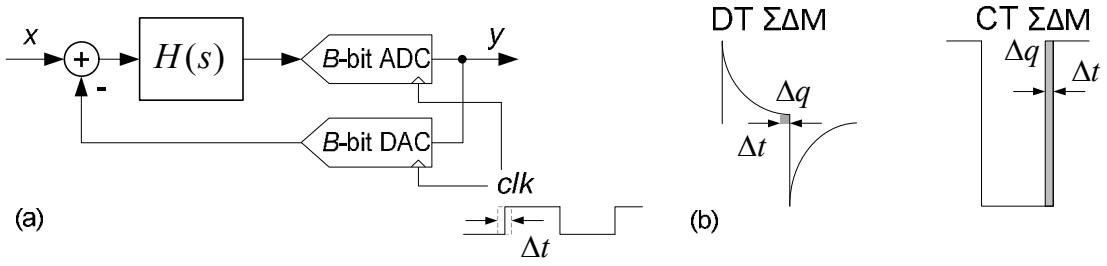

Fig. 2.13 Clock jitter effect in CT ΣΔM (a) main error sources (b) DT vs. CT waveforms of feedback DAC

Another important issue is related with the time delay in the response of the quantizer and DAC, which results in a delay in the ΣΔM loop filter response. This delay is called excess-loop-delay and usually it is a fraction of a sampling period, which can introduce additional poles, thus increasing the STF and NTF orders. This often leads to worse performance or even to an unstable behavior of continuous-time ΣΔMs.

Because of these reasons, although continuous-time ΣΔMs can achieve wide signal bandwidth, its linearity and accuracy is often reduced and compromised in comparison with discrete-time modulators.

2.3.3. Single-bit and Multi-bit ΣΔM

Depending on the number of bits of the quantizer used in the ΣΔM, one can distinguish between single-bit and multi-bit modulators. Usage of *B*-bit quantizer implies that the *B*-bit DAC is used in the feedback path of the converter. The examples of quantization characteristics of single- and multi-bit quantizers are illustrated in Fig. 2.14.

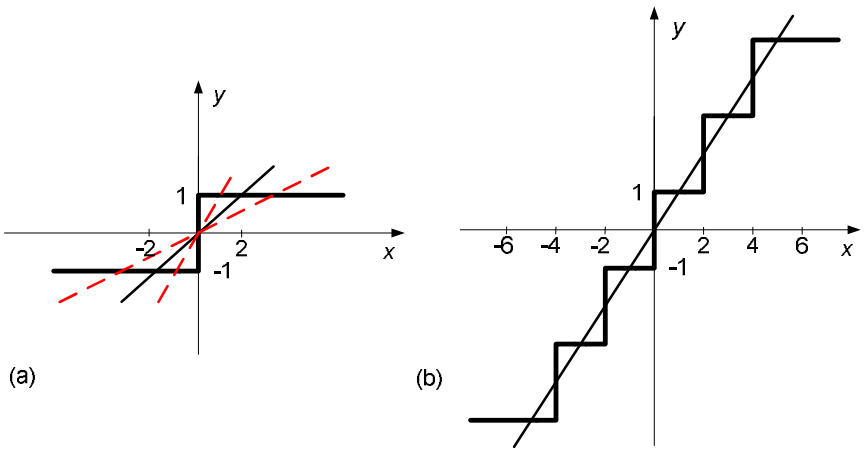

Fig. 2.14 Quantization characteristics of (a) single-bit and (b) multi-bit quantizers.

The output signal of the internal DAC is directly fed back into the ΣΔM input. Its non-linearity can be represented as an error source that adds directly to the input and which cannot be attenuated by the noise shaping loop of modulator. Therefore, the DAC linearity strongly influences the overall linearity of the ΣΔM, resulting in using single-bit quantizer (comparator) and a corresponding 1-bit DAC, which is inherently linear (there are only two output levels defining a straight line between two points $\pm V_{ref}$) and it does not require neither trimming, calibration nor other precision component matching [30, p. 537]. On the other hand, the gain of the single-bit quantizer cannot be easily determined because it depends on its input signal amplitude as illustrated by the red dashed lines in Fig. 2.14a. When the input signal amplitude decreases, the gain increases and vice versa. This means that, a single-bit ΣΔM has to remain stable over a wide range of loop gains and that the maximum input signal amplitude is reduced as well as the achievable SNR [4, p. 15].

By using a single-bit ΣΔM with a large enough OSR, it is possible to achieve a high overall resolution. However, the multi-bit architecture has the advantage of improving the modulator's SNR by 6 dB per each bit added to the quantizer. This means that, by using a multi-bit ΣΔM, the target performance can be achieved with lower F_S, which helps to decrease the power consumption of the whole circuit. The gain of the multi-bit quantizer is well defined which can be noticed in Fig. 2.14b. The behavior of a multi-bit ΣΔM can be quite closely modeled by its linearized model. Consequently, the system stability can be more accurately predicted for the given range of input signals than the stability of a single-bit ΣΔM. Moreover this architecture reveals less tone problems in 1st and 2nd-order modulators than single-bit [28].

Although multi-bit architectures theoretically allow improving the performance of the modulator, the DAC nonlinearity problems can cause harmonic distortions and increase baseband noise because of inter-modulation of high frequency noise.

As mentioned before, ΣΔM's linearity strongly depends on the linearity of the DAC. The components' mismatch in the multi-bit DAC causes, that its input-output characteristic becomes non-linear, which degrades the overall ΣΔM performance. In order to reduce the distortion added by the mismatch errors, dynamic element matching techniques are often used [4, ch. 6.4].

2.3.4. Multi Feedback and Multi Feed-Forward ΣΔM

In order to improve performance of ΣΔM, different circuit architectures can be employed. In [4, ch. 3.4] a few architectures utilizing additional feedbacks and feed-forward paths are presented. The generalized structure of a 2nd-order modulator, with arbitrary feed-forward and feedback coefficients, is shown in Fig. 2.15.

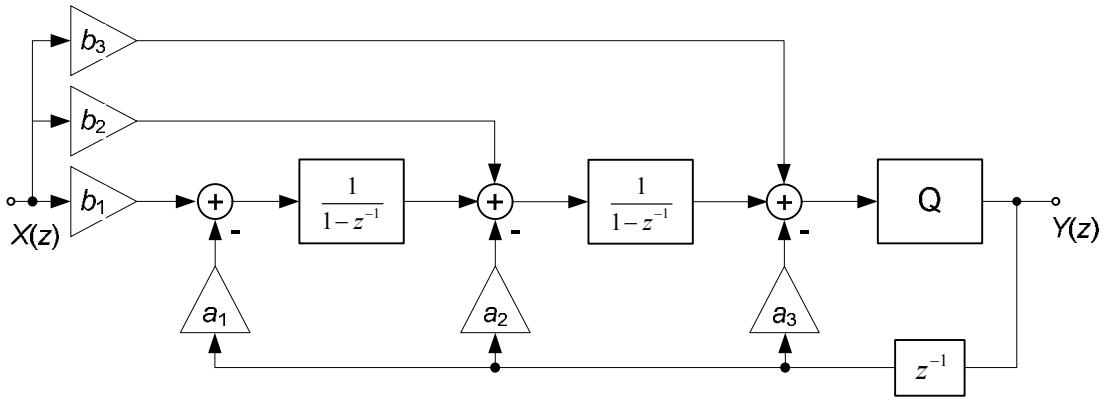

Fig. 2.15 General structure of a 2nd-order ΣΔM

One can notice that, the input and the output signals are fed forward and fed back, respectively, to all integrators and quantizer inputs. The general equations for STF(z) and NTF(z) are:

$$\mathrm{STF}(z)=\frac{B(z)}{A(z)};\quad \mathrm{NTF}(z)=\frac{(1-z^{-1})^2}{A(z)} \tag{2.14}$$

where

$$B(z)=b_1+b_2\cdot(1-z^{-1})+b_3\cdot(1-z^{-1})^2 \tag{2.15}$$

and

$$A(z)=1+(a_1+a_2+a_3-2)\cdot z^{-1}+(1-a_2-2\cdot a_3)\cdot z^{-2}+a_3\cdot z^{-3} \tag{2.16}$$

From the above equations one can observe that the NTF is no longer a simple differentiator. The coefficients a and b determine the poles and zeros of the STF, respectively. The feedback coefficient a_3 is rarely used because it increases order of the NTF to 3 but it does not introduce additional in-band NTF zero (it can be useful in case of a continuous-time ΣΔM [4]).

The concept of multiple feed-forward and feedback paths can be applied to higher order ΣΔMs. It gives the designer more flexibility to improve the performance and enhance stability of a given modulator. This last feature is especially important for orders $L>2$ of ΣΔMs, where in case of using a pure differentiating NTF, the stability is conditionally ensured for a limited range of input amplitudes.
In [4, ch. 4.4] a few loop filter architectures are presented, like:

- Cascade of integrators with distributed feedback as well as distributed input coupling;
- Cascade of resonators with distributed feedback;
- Cascade of integrators with distributed feed-forward and input coupling;
- Cascade of resonators with distributed feed-forward and input coupling.

An example of cascade of resonators with distributed feed-forward and input coupling structure is presented in [34]. The 5th order 4 bit DT ΣΔM achieves a peak SNDR of 72 dB in a signal bandwidth of 12.5 MHz. The local feedback loops introduce two additional notches in the NTF(z). They improve noise shaping by suppressing the quantization noise in the middle and close to the edge of the signal band frequencies.

By using structures with distributed feedbacks and feed-forwards it is possible to improve modulators' SNR by NTF pole and zero optimization and, therefore, enhance overall system stability.

2.3.5. Multistage Noise Shaping (MASH) ΣΔM

The previously described categories of modulators were single-loop converters. An alternative is a cascade modulator architecture also called MASH ΣΔM. This type of ΣΔM is built by cascading lower order modulators as shown in Fig. 2.16.

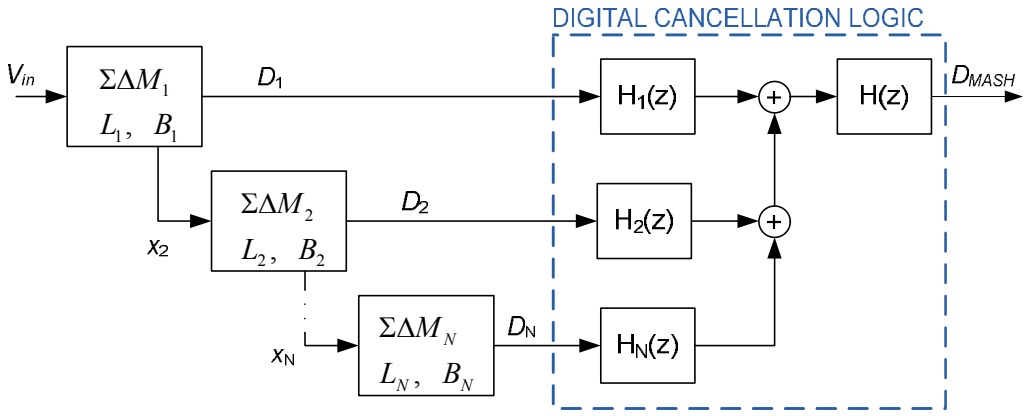

Fig. 2.16 General MASH ΣΔM structure

The input signal is quantized by the first modulator resulting in signal D_1, The second stage then quantizes the quantization error of the first modulator producing D_2. This scheme can be repeated several times. The digital output signals are then combined in the digital cancellation logic block to cancel the quantization noise from all the modulators except the last one. Large

SNR can be achieved using this scheme. The remaining quantization noise (of the last stage) is shaped by the NTF, whose order equals the sum of the orders of all the low-order modulators. So, in case of a MASH ΣΔM consisting of two 2nd-order modulators, the NTF of the final output signal will be 4th order (Fig. 2.17). In this case, the quantization error of the 2nd stage is filtered twice. Firstly by the 2nd ΣΔM and secondly by the digital cancellation logic. One can notice that, in the output signal there is no quantization error from the first stage ΣΔM, which, theoretically, is completely cancelled. The MASH ΣΔM output contains only 2nd stage quantization error. Moreover the input signal of the 2nd ΣΔM is like white noise This means that, the 2nd stage quantization error is very similar to true white noise and the 2nd stage does not generate harmonics [4, p. 129].

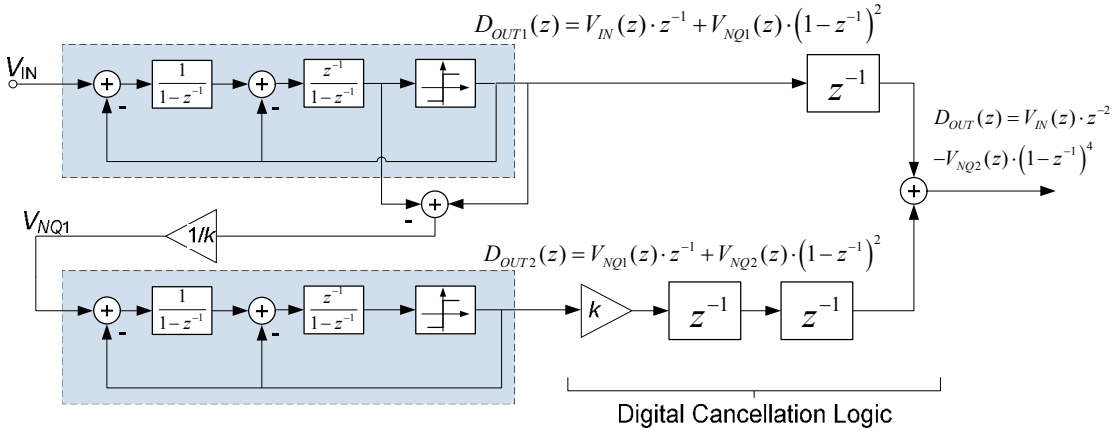

Fig. 2.17 Example of 4th order MASH ΣΔM.

In a MASH architecture there is the possibility of using a multi-bit quantizer in the 2nd stage modulator without using DAC nonlinearity correction since the 2nd stage output signal containing the nonlinearity error is multiplied in digital cancellation logic block by NTF of the 1st stage, which suppresses this error in the baseband.

MASH structures allow achieving high order noise filtering even using low order modulators. Since the constituting lower order ΣΔMs are stable, the whole MASH ΣΔM is stable because there are only forward paths between stages without common feedbacks. This is a clear advantage over high order single-loop ΣΔMs, whose stability is only conditional.

In single-loop ΣΔM architectures, the components' mismatch errors can change the coefficients of the STF and of the NTF, but this corresponds only to a small decreases in the SNR of the overall modulator. The reason is because the loop filter gain remains sufficiently large in the signal bandwidth, which results in significant quantization error suppression in this frequency region [4, p. 132]. Therefore, these A/D architectures can be relatively insensitive to mismatch of analog components. MASH architectures, on the other hand, require matching between the analog (defined by the modulator circuits) and the digital (defined by the digital cancellation logic) transfer functions. In this case, integrator leakage and mismatch effects degrades the

accuracy of the cancellation, which results in the appearance of poorly shaped noise from previous (especially from the first) stages in the output spectrum. Moreover, the idle tones performance for MASH ΣΔMs depend on amount of uncancelled noise. It is an important problem especially for continuous-time ΣΔMs, which are more sensitive to components imperfect matching. Therefore, the circuit nonlinearities limit the maximum number of stages of a given MASH modulator. When this limit is reached, no gain in performance can be achieved by adding more stages.

2.3.6. Switched-Capacitor, Active-RC and Gm-C Integrators

The basic building block of a ΣΔM is the integrator. Fig. 2.18a illustrates a discrete-time forward Euler switched-capacitor integrator. During phase Φ_1, the input voltage charges capacitor C_1 and the amplifier (op-amp) output voltage is sampled on capacitor C_3 (Fig. 2.18b). This voltage dramatically changes during Φ_2 when the slewing and settling processes take place. The presented integrator implements transfer function $H(z) = z^{-1} / (1 - z^{-1})$.

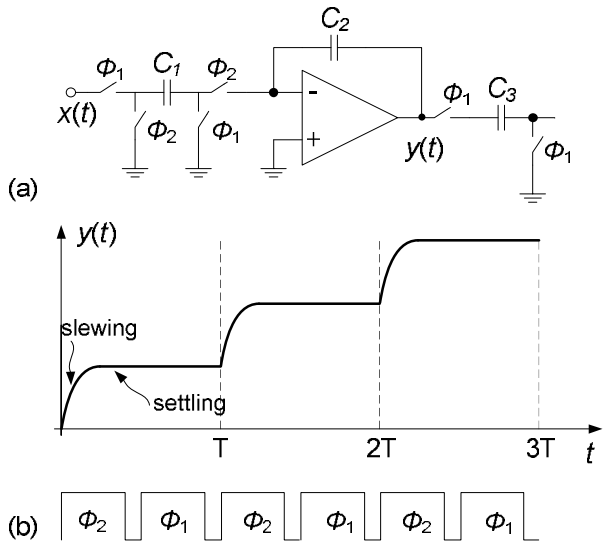

Fig. 2.18 A discrete-time switched-capacitor integrator

Fig. 2.19 shows two frequently used continuous-time integrators, active-RC and Gm-C. Both have ideal transfer function $H(s) = 1/(s\tau)$, where τ, the time constant is shown for both cases in Fig. 2.19. Because of non-idealities, usually active-RC integrators have better linearity and the Gm-C type can operate at higher frequencies [35].

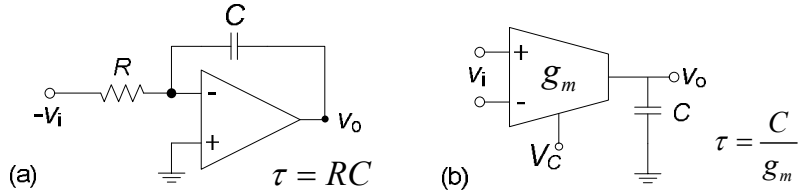

Fig. 2.19 Continuous-time integrators: (a) Active-RC and (b) Gm-C

In some cases, in order to take advantage of both types of integrators, ΣΔMs use front-end active-RC integrator and Gm-C structures for the remaining integrators, where required linearity is more relaxed [29].

2.3.7. Band-pass Modulators

Up to now, it has been assumed that the signal band is located at low frequencies. However, a signal with a given bandwidth can be placed around an intermediate frequency f_C, called center or notch frequency. In this case a band-pass loop filter has to be used instead of a low-pass, and the modulator is called a band-pass ΣΔM. The design and analysis of both types of systems are similar (besides the difference in loop filter structure). The main performance metrics have the same expressions in both cases i.e. SNR, SNDR, DR. Band-pass modulators operate in a similar manner as low-pass ΣΔMs, and they have the same advantages over Nyquist-rate converters. The NTF of band-pass ΣΔM is band-stop instead of high-pass. This means that, the quantization noise is suppressed around f_C instead of around DC as depicted in Fig. 2.20.

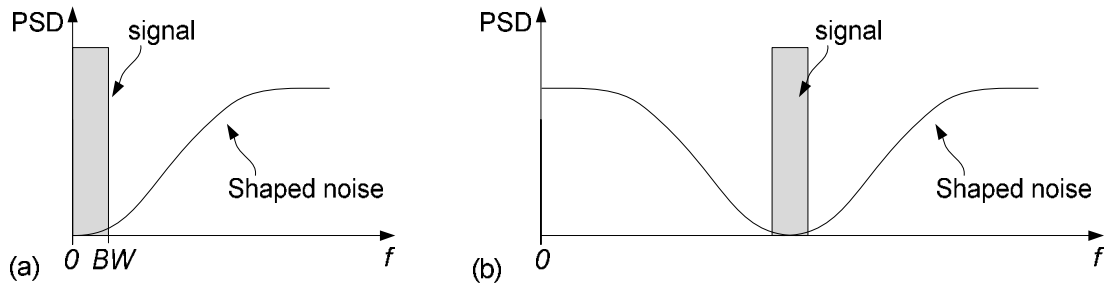

Fig. 2.20 Conceptual output power spectral density of (a) low-pass and (b) band-pass modulators.

Fig. 2.21 illustrates an example of the NTF zero-pole locations of the low-pass and band-pass ΣΔMs. For the low-pass case, zeros are located at DC ($z = 1$) and in case of band-pass at the notch frequency e.g. choosing $fc = F_S/4$ results in $z = \pm j$. This means that, a band-pass ΣΔM uses resonators rather than integrators.

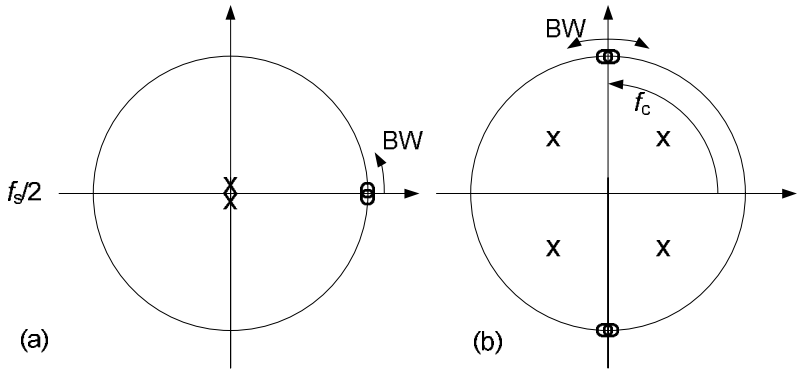

Fig. 2.21 Example of pole-zero location of (a) low-pass and (b) band-pass NTFs.

2.4. Methods of Reducing Effect of DAC Nonlinearities in Multi-bit ΣΔM

As stated before, DAC errors influence directly the input of the modulator. Its nonlinearities introduce distortion appearing at the modulator output signal spectra. Therefore, ideally, the DAC linearity should be equal or better than the overall system linearity. This task is somehow problematic for high resolution modulators (e.g. 16-19 bit ΣΔM) and, therefore, some DAC linearization techniques are used, e.g.: dual quantization, dynamic element matching, mismatch shaping algorithms, analog calibration and digital correction.

Dual quantization concept is based on the idea of combining single- and multi-bit quantizers in one modulator. The circuit takes advantage of the inherent linearity of the single-bit quantizer and significantly reduced quantization noise of the multi-bit architecture. Dual quantization is more often used in MASH structures. Usually, the last stage of the MASH modulator has a multi-bit quantizer and the other stages contain single-bit quantizers. In this case, the nonlinearity of last stage does not introduce signal distortion since it has a noise-like input signal. The improved stability of the last stage makes possible using a more aggressive NTF. Proper matching within the circuit allows cancelling the larger error introduced by the stages with single-bit quantizers.

It is also possible to use dual quantization technique in single-loop architectures [4, ch. 6.2]. The example is shown in Fig. 2.22. In this case a multi-bit quantizer and a DAC can be used for the last integrator of the ΣΔM, while remaining integrators use feedback from single-bit quantizer. The nonlinear distortion introduced by the *B*-bit DAC is divided by the transfer functions of the 1st and the 2nd integrators and, hence, is not significant for high OSRs. The single- and multi-bit outputs can be combined in the digital cancellation logic (DCL) in order to cancel quantization error introduced by single-bit quantizer, leaving only in the ΣΔM output the one introduced by multi-bit ADC.

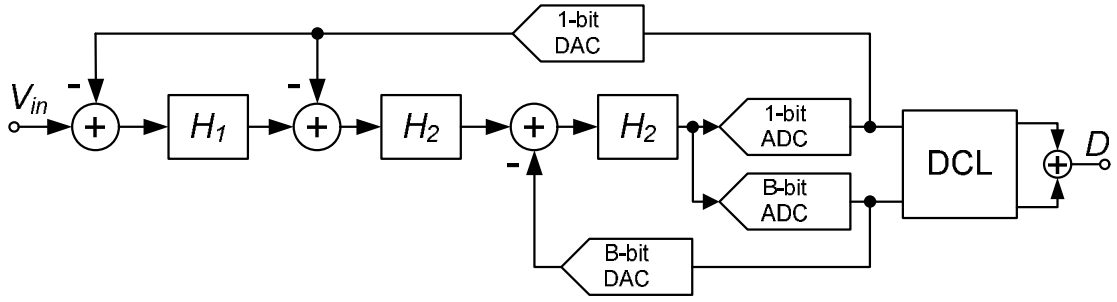

Fig. 2.22 Dual quantization in single-loop ΣΔM.

When either the dual quantization cannot be used or additional DAC linearization is needed, other techniques can be used.

A multi-bit DAC circuit with thermometer coded digital input, containing 2^B output levels, usually uses 2^B-1 unit elements (containing e.g. C's, R's or I sources), whose summed output

signals (e.g. charges, currents) result in an analog signal (Fig. 2.23). However, mismatches among the different unit elements result in harmonic distortion and increased noise floor (due to the folding of the high frequency quantization noise into the signal band) present in output signal spectrum. Assuming that for a given *K* value of DAC input code, a given *K* unit elements are enabled in a non-linear DAC, the mentioned nonlinearities occur. However, by randomly choosing the *K* unit elements used each time it is possible to randomize the static nonlinearity of the DAC and convert energy of harmonic spurs into pseudo random noise [4, ch. 6.3]. Nevertheless this randomization process increases in-band noise floor in the output signal spectra.

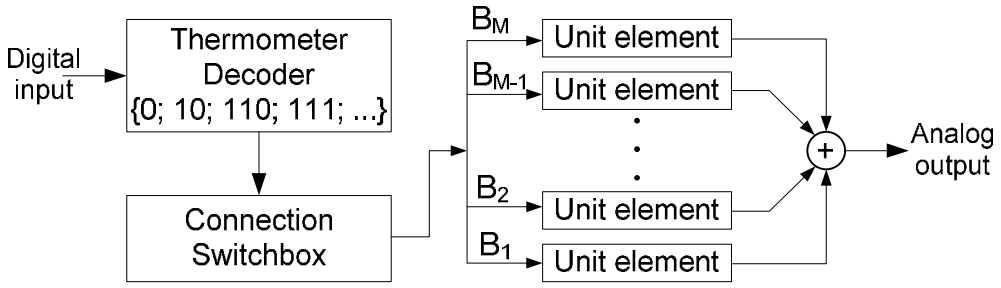

Fig. 2.23 Parallel unit element DAC with thermometer coded digital input

To deal with this problem, it is possible to utilize other techniques of unit elements' selection in order to achieve mismatch error shaping (move part of the DAC error from low to high frequency range). These dynamic element matching techniques try to drive the average error in each DAC level to zero over time [4, ch. 6.4]. Dynamic element matching of the DAC elements greatly reduces their matching requirements. For example, if the static mismatch within the DAC is the main error source than a mismatch shaping algorithm like data weighted averaging may improve DAC's linearity. An overview of first order shaping data weighted averaging variants is presented in detail in [36].

The dynamic element matching techniques rely on oversampling and noise shaping. In case of a ΣΔM using low OSR (from 4 to 10) they become less efficient. The different strategy is to acquire the DAC error in a digital form and then perform its correction in the digital domain. The acquisition can be done either at the power-up or in background during the normal modulator operation [4, ch. 6.5]. In [37] the 3rd-order, single-loop, continuous-time ΣΔM with an internal 4-bit quantizer circuit is proposed. The modulator with an OSR of 10 achieves a peak SNDR of 63.5 dB and a peak SFDR of 81 dB over a 25 MHz signal bandwidth while consuming 8 mW. DAC nonlinearities are corrected in the subsequent digital circuit implemented in a field programmable gate array (FPGA) board. The unit element mismatches are digitally estimated, which allows obtaining the required correction factors. Moreover, in order to achieve a low-power operation, all amplifiers are compensated for finite gain-bandwidth product related non-idealities (by modeling them and then tuning circuit coefficients).

The need of dynamic element matching depends on required accuracy of the unit elements, which improves with area. In [38] 3rd-order ΣΔM that used a resistive-based DAC with optimized unity value of resistance is presented. The 32 differential 5 bit reference voltages are generated using a single resistive divider. By increasing the area of the unity resistance, an increase of the matching accuracy within DAC is obtained without additional power penalty. Proper resistor sizes and layout of the resistive DAC limit the high-order distortion terms. In this ΣΔM the op-amp sharing between 1st and 2nd integrators is used to save power. This ΣΔM obtains a peak SFDR of 96dB in a 100 kHz bandwidth without the need of neither digital calibration nor dynamic element matching.

2.5. Stability of ΣΔMs

A ΣΔM, as any feedback system, is potentially unstable. Nevertheless the 1st-order ΣΔM can be considered as almost unconditionally stable. Theoretically, it can recover from any initial conditions and operates properly as long as its input signal amplitude does not exceed the reference voltage fed back into the modulator input [4, ch. 2.7]. The 2nd-order modulator is less stable and its allowable input signal range is smaller than in case of a 1st-order ΣΔM [4, ch. 3.3.2]. However, it is fairly easy to design it to work in a proper stable state. Therefore, the aforementioned MASH structures often utilize these low order modulators. This is because the stability considerations concern only separated stages, ignoring interconnections between them. It is, therefore, possible to build high order cascade modulator, whose stability is mainly assured by the low order stages.

The single-loop high order modulators are considered conditionally stable. The widely used approximate criterion predicting instability of ΣΔM is the (modified) Lee's criterion [39]. According to this criterion a ΣΔM is likely to be stable if

$$\max\left|\mathrm{NTF}(z)\right| < 1.5 \tag{2.17}$$

The max|NTF(z)| usually corresponds to NTF(-1). It should be mentioned that Lee's criterion is neither necessary nor sufficient. This is because more deep analysis of modulator stability has to be performed. If the integrators outputs start to saturate this can lead them to low frequency oscillations and in consequence driving the integrators outputs between the high and low saturation levels. This situation can happen when the quantizer is overloaded, which can be triggered by a large input signal amplitude. In case of multi-bit architectures, its linearized model allows more precise prediction of the allowable range of input signal amplitudes. However, the single-bit ΣΔM contains variable gain block (quantizer), inserted into the loop and the whole system is stable for a limited range of quantizer gains. The quantizer gain is signal dependent and it affects the placement of the ΣΔM close loop poles, causing instability if they leave the unit circle. Fig. 2.24 illustrates a plot of the root locus of an example of a high order active ΣΔM, while the quantizer gain varies [4, ch. 4]. For $g > g_{crit}$ all roots are within unit circle and system is stable. However, for $g < g_{crit,}$ one pair of roots moves outside of unit circle. The

stability of the system is reduced by decreasing the values of g, which corresponds to increasing quantizer input signal. The root locus can give a rough idea about the ΣΔM stability, but more complicated methods can be used to model a single-bit ΣΔM, like e.g. extension of the quasi-linear model proposed in [40]. Nevertheless, in order to investigate the stability of a given converter, extensive simulations are required for high order ΣΔMs even for the ones using multi-bit quantizers.

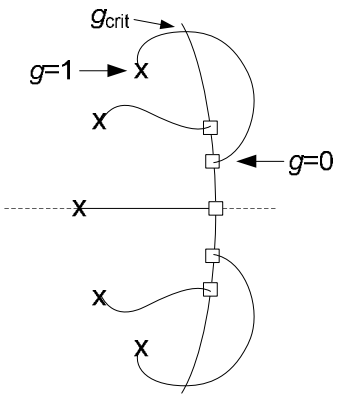

Fig. 2.24 Root locus of the example 5th -order ΣΔM affected by varying quantizer gain, *g*.

Another condition causing oscillations of ΣΔM is related with the modulator state variables (usually defined as the integrator output signals). One can define stable and unstable regions of the state variables space. If the initial conditions of the integrators, on power-up, correspond to unstable region, the ΣΔM will start to oscillate when the system is switched on. Then the oscillation can be kept (instability) or can be attenuated by the system dynamics leading to stabilization (it is hard to predict which situation will take place). Therefore, in order to bring stability to the modulator the output of integrators can be limited by using limiting elements in parallel with the integrating capacitors. Another possibility is to detect long strings of ones or zeros at the output bit-stream, which are caused by modulator instability and then:

- temporarily reset all or only few last integrators outputs to zero;
- temporarily lower the order of the modulator by changing interconnections in circuit and reset other integrators;
- temporarily eliminate the comparator from the signal path and directly feedback its input signal, turning modulator into stable filter [30, p. 560].

As mentioned before, in order to predict the behavior of ΣΔM, Lees's criterion can be used as well as liner modulator models. Nevertheless, extensive simulations are always necessary even in case of multi-bit modulators.

2.6. Strategies to Improve Figure of Merit

The value of FoM depends mainly on three parameters: SNDR, signal bandwidth and P_C. Fig. 2.25 illustrates the theoretical influence ΣΔM's order L and OSR on in-band power noise, which is strongly related to SNDR.

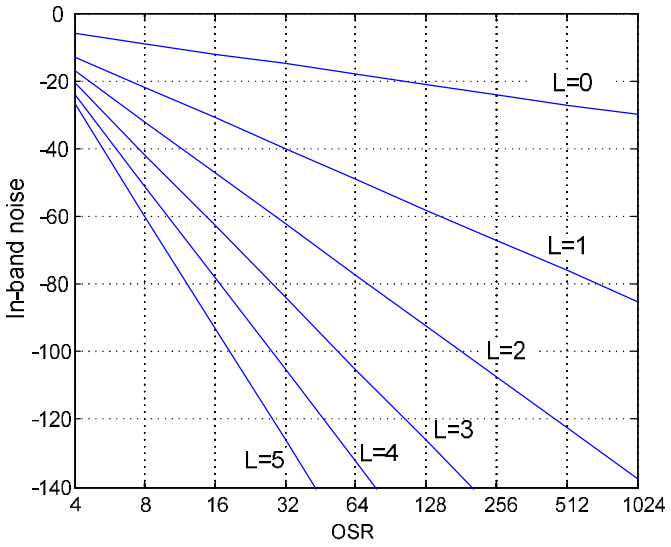

Fig. 2.25 Theoretical in-band noise power vs. OSR [4 ch. 1].

Strategies to improve modulator performance and energy efficiency can be classified as [29]:

- Increasing order of modulator, *L*. Fig. 2.25 depicts that theoretically there can be dramatic improvements in the decreasing in-band power noise by using higher order modulators. However, it should be mentioned that the higher the order of a single-loop modulator the more significant stability problems can occur. The alternative can be employing a cascaded ΣΔM topology that allows for higher noise shaping and relaxes the stability issue. Nevertheless, additional integrators lead to higher power consumption of the overall modulator.

- Increasing the OSR. As mentioned before, for each doubling OSR the quantization noise will decrease by $6L+3$ dB, which means that the effective resolution, improves by $L+0.5$ bits. Moreover by using higher OSR it is easier to achieve a higher bandwidth. However, increasing the OSR translates into higher power consumption.

- Increasing the number of bits in the quantizer, *B*. For each additional bit added to the quantizer the SNR can be improved by 6 dB (1 bit). Nevertheless, in many cases the multi-bit feedback DAC will require the use of techniques for compensating its nonlinearity.

- Decreasing the power consumption, P_C. All designers tend to decrease the current consumption of their circuits. It is important to identify blocks in which the trade-off between performance and P_C allows to decrease it (e.g. decreasing gains of amplifiers). Then proper optimization techniques can be used to achieve this aim.

As one can notice there are close relationships between ΣΔM's performances, power consumption and stability, making modulator's design a trade-off between different factors. The next chapter is focused on state-of-the-art ΣΔM and it gives an insight into currently used methods improving the figure of merit (FoM_W and FoM_S).

3. LITERATURE REVIEW

This chapter gives a brief overview of the architectures and techniques used in designing recent single-loop and cascaded ΣΔMs. Some methods used to implement more power efficient integrators and quantizers are also presented. Moreover, this chapter describes jitter reduction techniques and it presents design parameters and key performance parameters of selected ΣΔMs that are classified by their adopted architectures. The ΣΔMs mainly are classified according to their architecture as: continuous-time, discrete-time, single-loop, cascaded, single-bit and multi-bit ΣΔMs.
Moreover, a coarse categorization based on the area of application is also used. This course categorization, shown in Table 3.1, is defined by low, medium and high bandwidth and low, moderate and high resolution. Examples of specifications of a few standards operating with signal bandwidth from 0.2 MHz up to 20 MHz are presented in Table 3.2.

Table 3.1 Course ΣΔM categorization based on the achieved SNDR and BW.

BW	**Low**	**Medium**	**High**
	< 5 MHz	5 MHz ≤ 20 MHz	> 20 MHz
SNDR	**Low**	**Moderate**	**High**
	< 62 dB (< 10 bit)	62 dB ≤ 74 dB (10 bits ≤ 12 bits)	> 74 dB (> 12 bits)

Table 3.2 Specification of standards [41].

Standard	GSM	BT	UMTS	DVB-H	WiMAX	WLANa	WLANn
BW [MHz]	0.2	0.5	1.96	3.8	10	10	20
SNDR [dB]	80	75	65	55	60	65	50

The constant size reduction of CMOS technologies has resulted in an increase of the transition frequency of CMOS transistors but, on the other hand, it has also resulted in the reduction and variability of the intrinsic gain of these devices [2]. As a consequence, it has become more difficult to design high gain high bandwidth amplifiers with reduced power dissipation. Consequently, the design of ADCs that require such amplifiers, including ΣΔMs, becomes more difficult and challenging.

As stated before, there are several possible choices for implementing a ΣΔM architecture [3]. Firstly, continuous-time modulators are becoming more popular than discrete-time modulators

since they can operate at higher clock rates (roughly 2-4 times faster). A popular architecture is the feed-forward topology, which has the advantage of reduced signal amplitude at the output of the integrators allowing reducing the amplifiers gain requirements [6, 42]. For a given distortion requirement i.e. dynamic linearity, the integrators' loop gain can be considerably lower in a feed-forward than in a feedback architecture. The work presented in [6] obtains a peak SNDR of 73.6 dB in an 18 MHz signal bandwidth while consuming 3.9 mW. The circuit from [42] obtains peak a SNDR of 60.6 dB in a 60 MHz signal bandwidth and consumes about 20 mW. These ΣΔMs [6, 42], using feed-forward paths, achieve moderate resolution over a medium and a high signal bandwidth, respectively. However, the feed-forward topology reveals problems with out-of-band components in the input signal, since it tends to have a magnitude of STF greater than 0 dB in the out-of-band region (SFT peaking), which amplifies out-of-band signals causing possible saturation of the modulator. The solution can be, as described in the next section, using a 0-L MASH topology that offers the advantage of having a flat STF even with a feed-forward loop filter topology.

One can observe that recent ΣΔM designs trends include higher order loop filters (integrators) [5], digitally assisted DAC correction [6, 7], and reduced number of op-amps [5, 8]. These trends contribute to an improvement of the figures of merit (FoMs) and to the decrease of the ADC active area. The work from [5] presents a 4^{th} order ΣΔM that achieves a peak SNDR of 70 dB in a 10 MHz signal bandwidth, while consuming 2.57 mW and also a 3^{rd}-order ΣΔM that achieves a peak SNDR of 68.8 dB in a 3 MHz signal bandwidth while consuming 1.36 mW. Both structures use higher order loop filters (integrators) relaying on a single op-amp. In [8], a 3^{rd}-order ΣΔM with a single gain stage (CMOS inverter) op-amp is presented. The op-amp is implemented with digitally assisted biasing and a common-mode control. This modulator uses a third-order loop filter (integrator) based on the mentioned single gain stage, which allows reducing the power dissipation. The proposed circuit achieves a peak SNDR of 68.6 dB in a 10 MHz signal bandwidth while consuming 1.82 mW and occupying an active area of only 0.039 mm^2. As previously mentioned, a DAC digital correction is another popular technique. In the circuit described in [7] all DAC unit element mismatches are digitally estimated at start-up and an analog auxiliary DAC linearization is implemented within a modulator loop filter. This work achieves a peak SNDR of 67.5 dB over a 25 MHz signal bandwidth while consuming 8.5 mW.

The described techniques are suitable for building ΣΔMs operating with moderate resolutions at low to medium-high signal bandwidths. Moreover, techniques for reducing the number of amplifiers in the modulator also reach lower power consumptions, as described in [5, 8].

3.1. MASH Architectures and Unity-STF

In case of high order ΣΔ modulators, MASH and sturdy MASH (SMASH) [43] structures reveal better stability and allow for more aggressive noise-shaping than their single-loop counterparts.

Therefore, implementations of various MASH-like architectures can be found in recent publications [9-12].

A SMASH architecture reduces the modulator's sensitivity to noise leakage that is usually a drawback of a conventional MASH topology [43]. Fig. 3.1 depicts a general SMASH architecture, where the output signal is obtained from direct subtraction of the outputs of the two stages, without the need of using digital cancellation logic. Consequently the problematic issue of matching analog and digital filtering functions is, somehow, relaxed. The DAC used in the first stage has to handle the summation of the digital outputs of both stages and, hence, its full scale has to be greater than the quantizers. Moreover, this DAC requires a resolution larger than one bit, meaning that dynamic element matching techniques should be used to avoid linearity issues associated to the inherent mismatch errors. Comparing to MASH, the SMASH structure is less sensitive to circuit non-idealities like finite op-amp gain and variations of the modulators' coefficients.

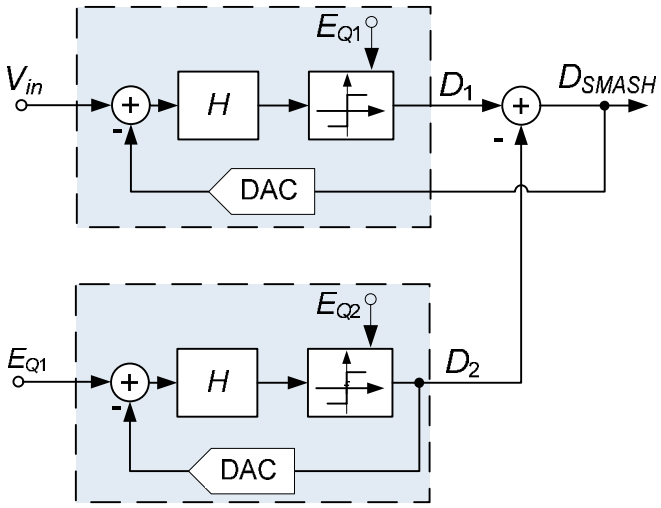

Fig. 3.1 General SMASH structure.

The enhanced version of SMASH named mixed-order SMASH is presented in [43]. In this circuit, instead of using one DAC driven by D_{SMASH} at the input of the first ΣΔM, two DACs are used (one for each output signal, D_1 and D_2). Hence, the linearity requirements of both DACs and the complexity of the dynamic element matching are relaxed. The mixed-order SMASH structure has, therefore, advantages over the SMASH architecture. Moreover, the first and the second stage quantization noise experience different (thus mixed) orders of noise shaping and, consequently, the accuracy of this modulator is comparable to that of the MASH structure even with the use of low-gain amplifiers. The SMASH modulator, from the same authors, has been presented in [44] and it achieves a peak SNDR of 74 dB in a 0.625 MHz signal bandwidth while consuming 3.3 mW. The circuit, described in [12], utilizes the continuous-time 3-1 SMASH architecture that allows operating in high bandwidth with moderate-high resolution. In the second stage it uses delay-less unity-gain in-band STF_2. This cascaded 4^{th} order ΣΔM offers

lower out-of-band STF peaking than in case of 4th order single-loop ΣΔM when the feed-forward loop is used. It achieves a peak SNDR of 74.6 dB in a 50 MHz signal bandwidth while consuming 78 mW.

An interesting concept that can be used in both single-loop and MASH-like modulators is a unity-SFT structure presented in [45]. The concept of unity-STF is depicted in Fig. 3.2. By adding feed-forward paths, the modulator obtains a flat STF = 1, without affecting the NTF. This modification causes that, ideally, the input signal component is cancelled by the feedback path. As a consequence the output swings of the integrators are reduced and the nonlinearities of the integrators do not introduce in-band harmonic distortion to output signal spectrum, because they only process quantization noise. An upgrade of this concept has been proposed in [46]. It eliminates the adder in front of the quantizer, avoids its 'kick-back' effect to the input stage and it relaxes timing of the dynamic element matching used in the multi-bit DAC.

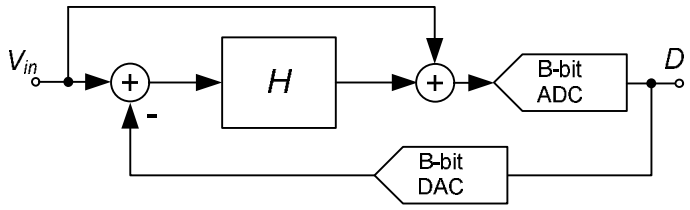

Fig. 3.2 Block diagram of ΣΔM with unity-STF.

In [41] a SMASH ΣΔM architecture using unity-STF in both stages has been employed. These two techniques are used to achieve a larger SNDR than in the case of an original SMASH architecture while relaxing amplifiers' required gains and the modulator's sensitivity to device mismatch. It targets at medium bandwidth and moderate resolution applications.

In order to achieve good dynamic performance in single-loop and MASH architectures, high gain amplifiers in the integrators are often required. In the case of large signal bandwidths, together with moderate-high resolutions, these amplifiers become difficult to design and this translates into an increase of the power dissipation of the ΣΔMs. Therefore, one can use multi-stage, multi-path feed-forward amplifiers that are able to achieve high gain at high frequencies with lower power consumption when compared to conventional Miller-compensated multi-stage amplifiers. The feed-forward amplifier can be designed to have high gain in signal bandwidth and low gain for the remaining bandwidth. The continuous-time 0-3 MASH modulator from [9] uses multi-path feed-forward amplifiers together with feed-forward loop filter topology to reduce their gain specifications. It achieves a peak SNDR of 71.4 dB in a 50 MHz signal bandwidth while consuming 235 mW. The 0-L MASH topology with a feed-forward loop style is a special case of a SMASH architecture that provides a flat STF. The examples, presented in this section, show that MASH-like ΣΔMs are suitable for medium-high bandwidth, moderate-high resolution applications.

3.2. Integrator Circuits

By using digital circuits in critical building blocks of a ΣΔM one can take advantage from the technology downscaling and progressive reduction of supply voltage. Consequently it is possible to further decrease the power consumption of the circuits.

In [47, 48], a 3rd order discrete-time ΣΔM using class-C inverters is presented. The class-C inverters replace the operational transconductance amplifier (OTA), a block that can consume significant amount of the overall power of the A/D conversion system. The switched-capacitor integrator relying on class-C inverters is depicted in Fig. 3.3. When the supply voltage is chosen to be lower or equal to the sum of the threshold voltage of PMOS and NMOS transistors ($V_{DD} \leq |V_{TN}|+|V_{TP}|$), the inverter behaves as a class-C amplifier. It has lower power consumption and higher slew rate comparing to a traditional single-stage OTA. Capacitors C_S sample the input voltage which is, in the opposite phase, transferred to C_1. The auto-zeroing (when the inverter works in a unity gain configuration) allows cancellation of the unknown inverter offset voltage (sampled by C_C in Φ_1,) and forming a virtual ground node V_G. The common-mode feedback capacitors C_M are discharged to the signal ground level during Φ_1 and form a common-mode voltage detector at Φ_2. A pseudo-differential integrator reduces nonlinearities and improves noise immunity. The ΣΔM described in [47, 48] has been designed to work in the audio bandwidth (20 kHz). It achieves 81 dB peak SNDR and consumes 36 μW operating with supply voltage of 0.7 V.

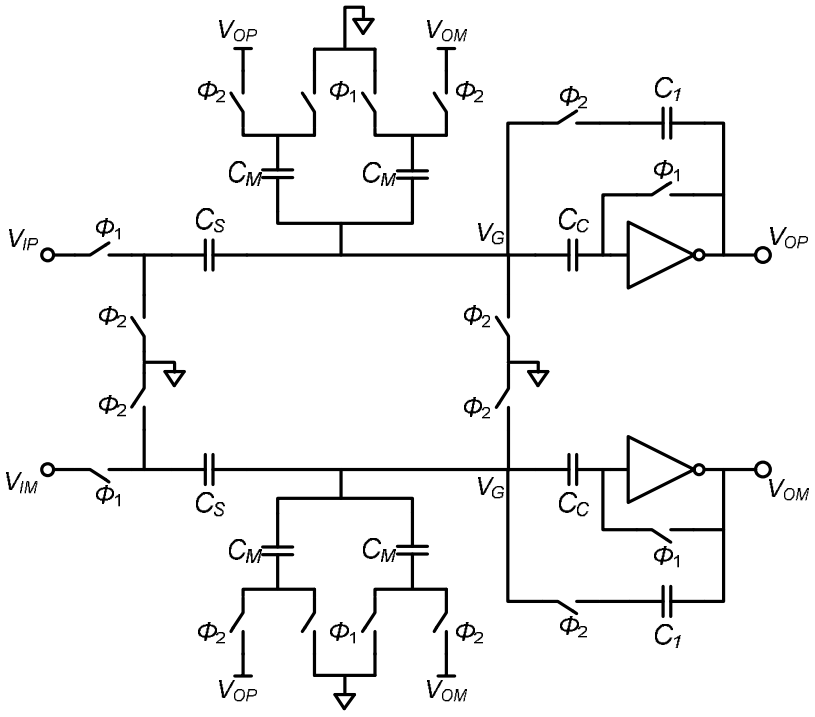

Fig. 3.3 Pseudo-differential SC integrator using class-C inverters [47, 48].

Another ΣΔM using inverter based integrator has been presented in [49] where the OTA is

constructed with inverter unit cells. An example of a fully differential switched-capacitor ΣΔM where the OTAs have been replaced by comparators is proposed in [50]. These ADCs [49, 50] work with very low signal bandwidth and achieve moderate resolution. In [8], a 3rd-order ΣΔM is described and it uses only a single gain stage CMOS inverter op-amp to save power. It processes medium signal bandwidth achieving moderate resolution. It reaches a peak SNDR of 68.6 dB in a 10 MHz signal bandwidth while consuming 1.82 mW and occupying a small active area of 0.039 mm^2.

Inverter-based integrators allow reducing ΣΔM's power consumption. The presented examples have demonstrated that they are able of achieving high resolutions in low signal bandwidths or moderate resolutions in medium signal bandwidths.

Generally, most of the loop filters in continuous-time or discrete-time realizations of ΣΔMs are built using the architectures previously discussed in Chapter 2.3.6. The amplifiers of active integrators provide higher close-loop gain, reducing input-referred noise. On the other hand, even with the use of the techniques described previously, their power consumption is still a significant part of the total circuit power consumption and with the reducing supply voltage their design becomes more complicated. One possibility to deal with the problem of designing high gain amplifiers is to select passive or quasi-passive ΣΔM architectures, where the processing gain of the comparator is used in the feedback loop of the modulator's filter, thus it becomes possible to eliminate the OTAs from the circuit [13]. Passive integrators provide signal attenuation and, therefore, are more sensitive to noise coupling than active integrators that use amplifiers. On the other hand, passive ΣΔMs are simpler (have less hardware complexity) compared to their active counterparts, do not suffer from the nonlinearities of active elements and allow the possibility of significant power reduction.

It is possible to use a passive switched-capacitor circuits to implement the loop filter of the ΣΔM such as the modulators described in [13], [17] and [15]. These circuits use first order *RC* circuits where the resistor is replaced by a switched-capacitor branch. The basic switched-capacitor low-pass filter is shown in Fig. 3.4. The transfer function of this circuit is given by [15]:

$$H(z) = \frac{\dfrac{C_R}{C_R + C_1}}{z - \dfrac{C_1}{C_R + C_1}} = \frac{\alpha}{z - \beta} \;; \quad \beta = 1 - \alpha \tag{3.1}$$

where C_R is the capacitor implementing the resistor in the *RC* circuit and C_1 is the capacitor of the *RC* circuit. Equation (3.1) represents discrete-time low-pass filter with unity DC gain and attenuation at higher frequencies that is defined by factor α. This equation shows that the switched-capacitor circuit from Fig. 3.4 behaves as a discrete-time integrator with losses.

$$H_{\max} = \left|H(z=1)\right| = \left|\frac{\alpha}{1-\beta}\right| = 1; \quad H_{\min} = \left|H(z=-1)\right| = \left|\frac{\alpha}{1+\beta}\right| \approx \frac{\alpha}{2-\alpha} \tag{3.2}$$

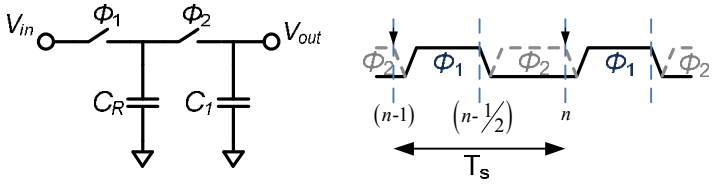

Fig. 3.4 Basic switched-capacitor low-pass filter.

In order to increase the ratio between the H_{max} and H_{min} the gain of the circuit (α) should be reduced. By using a small α value (by making C_1 larger than C_R), the pole of the circuit is moved closer to the unity circle (by making β closer to 1). The ΣΔM from [13] operates in signal bandwidth of 20 kHz and achieves 77 dB SNDR while consuming 230 μW. The circuit in [15] achieves a peak SNDR of 56 dB in bandwidth of 10 MHz and it consumes 5.5 mW.

A 2nd-order continuous-time modulator is described in [18]. It utilizes an RLC filter as a replacement of an active integrator, so the sampling frequency is not limited by the op-amp of the integrator. The consequences of using only passive loop filter are the very small signal amplitudes at the outputs of the integrators, resulting in a small amplitude available at the input of comparator, which can require one or more pre-amplification blocks.

Although passive integrators do not provide any gain it is possible to use a voltage set-up switched-capacitor circuit to introduce some extra gain into the passive integrator [13, 14]. In the 2nd-order passive ΣΔM, described in [14], the second integrator embeds a 5-stage (N = 5) switched-capacitor gain boosting in order to alleviate the strong attenuation of the passive integrator. The 5-stage gain-boost integrator ideally provides gain with magnitude of 5. However, due to parasitic capacitances of the switches the real gain has a magnitude of only 3.25. The integrators of this ΣΔM are depicted in Fig. 3.5. It shows the simple low-pass filter integrator and the N-stage (N = 2, for simplicity) gain-boost passive integrator. Their ideal transfer functions and the -3 dB bandwidths are respectively given by [14]:

$$H(z) = \frac{z^{-1}}{1 + \frac{C}{C_S} - \frac{C}{C_S} \cdot z^{-1}} \; ; \quad f_{-3dB} = \frac{f_S}{2 \cdot \pi \cdot \left(1 + \frac{C}{C_S}\right)} \tag{3.3}$$

$$H_{N\ stages}(z) = \frac{z^{-1}}{\frac{1}{N} + \frac{C}{C_S} - \frac{C}{C_S} \cdot z^{-1}} \; ; \quad f_{-3dB\ N\ stages} = \frac{f_S}{2 \cdot \pi \cdot \left(1 + N \cdot \frac{C}{C_S}\right)}. \tag{3.4}$$

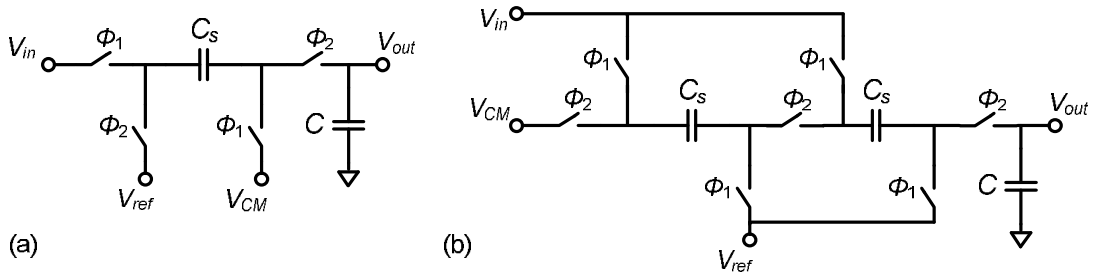

Fig. 3.5 Simple low-pass filter (a) and gain-boost filter, N=2 for simplicity (b).

A possible alternative is to use a mixed active-passive topology. The study and comparison of following structures of ΣΔMs: active-active ($\Sigma\Delta M_{AA}$), active-passive ($\Sigma\Delta M_{AP}$) and passive-passive ($\Sigma\Delta M_{PP}$) is presented in [14]. Using active integrators improves the modulator's SNDR but it also increases the total power consumption. Designed for a 500 Hz signal bandwidth, the $\Sigma\Delta M_{AA}$, $\Sigma\Delta M_{AP}$, and $\Sigma\Delta M_{PP}$ achieve 76 dB, 70 dB and 67 dB peak SNDRs, while consuming 2.1 μW, 1.27 μW, and 0.92 μW, respectively, from a 0.9 V supply.

The passive-active topology has been also used in the ΣΔM proposed in [15], where one active Gm-C integrator separates two passive integrators avoiding a loading effect between passive filters and, simultaneously, providing additional gain suppressing thermal noise. In [19] a passive *RC* stage is followed by an active Gm-C stage to achieve 2nd-order noise filtering. Jitter sensitivity is addressed by utilizing finite impulse response filters in the feedback. In [20] a 5th order single-bit continuous-time ΣΔM with an active-passive loop filter is described. The first two stages of the loop filter are active-RC integrators. Passive filters are placed in the third and fifth stages of the loop filter to mitigate their noise contribution. In this way, the power consumption is reduced and the loading effect of the passive integrators is mitigated. The passive filter from [20], illustrated in Fig. 3.6, is a lossy integrator with a single pole and zero. Due to the fact that DC gain is one, the output noise of the passive filter is directly referred to the input. The transfer function of this integrator is shown in (3.5). This ΣΔM achieves a peak SNDR of 60.26 dB for a 2 MHz bandwidth, while consuming 9 mW.

$$H(s) = \frac{1 + s \cdot (R_2 \cdot C_1)}{1 + s \cdot (R_1 + R_2) \cdot C_1}. \tag{3.5}$$

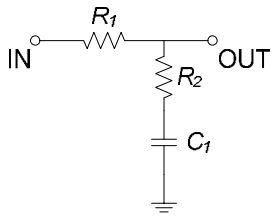

Fig. 3.6 Passive filter circuit

In [16], a 3rd-order 1-bit continuous-time ΣΔM employing passive *RC* integrators is described. This structure uses a single feedback path and the stability in the loop is obtained because its 2nd and 3rd integrators (that are similar to Fig. 3.6) implement zeros (through the series resistor R_2).

These two resistors, also allow the 2nd and 3rd integrators to implement feed-forward paths since, at high frequencies, they work as a "resistor divider". Additionally, two differential pair gain blocks are incorporated in the loop filter between adjacent integrators to avoid loading effect of the following stage and to provide extra gain for the loop filter (~15 dB). This ΣΔM achieves FoM of 27.5 fJ/conv.-step and a peak SNDR of 69.1 dB for a 2 MHz bandwidth, while working with 0.7 V supply and consuming 256 uW. This work proves that structures with passive integrators are able to achieve a very high energy efficiency.

The passive ΣΔMs presented in this section achieve moderate-high resolution when operating at low signal bandwidths, and low resolution in case of operating at medium bandwidths. The gain achieved with gain-boost integrator, ideally can help to alleviate the issue of strong attenuation of the passive integrator. However, in practice, this gain is lowered by the parasitic capacitances. Moreover, the need of using additional switches in the signal path may add additional in-band harmonic distortion to output signal spectrum. One advantage of the passive structures is that they allow decreasing the power dissipation of the ΣΔMs and also allow the possibility of reducing supply voltage beyond the nominal values.

3.3. Multi-bit Quantizers

Flash ADC quantizers are used very often [9, 37, 51] in multi-bit ΣΔMs. They can be made of resistive ladder, bank of comparators and some logic circuitry. The number of comparators in a flash ADC increases exponentially with the number of bits, which contributes to high power consumption and large increase of circuit area. In order to decrease the number of comparators, in [52] a tracking quantizer composed of three comparators with interpolation is used instead of a 4-bit flash ADC. In this quantizer the set of three comparators is followed by logic and by an up/down counter. The counter changes its value depending on the outputs of the comparators and it adjusts the comparators' reference voltages (provided by the R-string ladder). The quantizer output signal is obtained by combining the counter output and the comparators output signals. The main advantage of this tracking ADC is its lower power consumption (~20 % of the total power of a 4-bit flash ADC) and the reduced number of comparators. This ΣΔM achieves a peak SNDR of 70 dB in a 2 MHz signal bandwidth while consuming 3 mW.

The work reported in [6] presents a ΣΔM using highly digital quantizer based on a fully dynamic flash architecture with the number of comparators reduced by half. This work uses comparators with fixed references and additionally, an input tracking mechanism is used to select only those comparators that are in the input tracking range, meaning that the others will stay in reset mode and, therefore, will not consume power. This design has 9 comparators, and only 4 of them are activated in each cycle to track the high-frequency input signal. This ΣΔM uses a feed-forward loop filter, a digitally assisted DAC correction and the referred quantizer. As presented in the beginning of this chapter, this ΣΔM achieves a peak SNDR of 73.6 dB in an 18 MHz signal bandwidth while consuming 3.9 mW.

The dynamic range of the above mentioned quantizers becomes limited with low supply voltage due to the comparators' offset and hysteresis. This issue can be alleviated by using voltage-controlled oscillator (VCO) or pulse-width modulation (PWM) based quantizers.

A VCO-based quantizer translates amplitude-based information into a time-based by use of voltage-to-frequency conversion and, additionally, it provides inherent 1st-order noise shaping. Nevertheless, a VCO has a nonlinear voltage to frequency conversion function, which limits the modulator's SNDR. In [53] the VCO-based quantizer provides 1st-order noise-shaping and its direct connection to the internal DACs of the ΣΔM provides implicit dynamic element matching of the DAC elements. The order of the loop filter is selected by the desired suppression of VCO nonlinearity (due to large signal swing at the VCO's input) rather than the quantization error. This ΣΔM achieves a peak SNDR of 72 dB in a signal bandwidth of 10 MHz, while consuming 40 mW.

The modulator from [54] uses the VCO's output phase rather than the output frequency. It helps alleviating the VCO's nonlinearity and allows reducing the signal distortion that limits the performance of VCO-based ΣΔMs. In this case, the VCO's input swing spans only over a small range of the nonlinear tuning curve. It relaxes the requirement of the loop filter's order. However, the ΣΔM with the VCO using output phase loses the dynamic element matching property, meaning that it has to be explicitly added to the circuit. The dynamic element matching can consume a significant amount of power especially at very high sampling rates. The ΣΔM from [54] achieves a peak SNDR of 78 dB in a signal bandwidth of 20 MHz, while consuming 87 mW.

The ΣΔM described in [55] combines the advantages of both frequency and phase quantization. It processes the VCO output in separated phase and frequency paths that are summed and applied to the feedback DAC. This architecture is not susceptible to VCO non-linearity, thus it relaxes the loop filter requirement and contains implicit dynamic element matching. This ΣΔM achieves a peak SNDR of 71.5 dB in a signal bandwidth of 50 MHz, while consuming 54 mW.

Another approach is proposed in [56]. A continuous-time ΣΔM with residue-cancelling VCO-based quantizer. Its block diagram is shown in Fig. 3.7. It uses two quantizers: 4 bit flash ADC_F and 30-level noise shaping VCO quantizer (VCO_Q). The former one coarsely quantizes the loop filter output, while the latter processes the residue signal, which is the quantization error of the ADC_F, E_{Q1}. Consequently the nonlinearity of the VCO_Q does not introduce harmonic tones. In order to cancel out E_{Q1} and leave only shaped the quantization error of VCO_Q, E_{Q2}, in the ΣΔM output, the digital filter, $H_M(z)$, filtering ADC_F output is used. Since the first quantizer is the flash the ADC_F, the DAC that requires dynamic element matching that is placed after the ADC_F output. This ΣΔM achieves a peak SNDR of 78 dB with a sampling frequency of 600 MHz and a 10 MHz bandwidth, while consuming 16 mW.

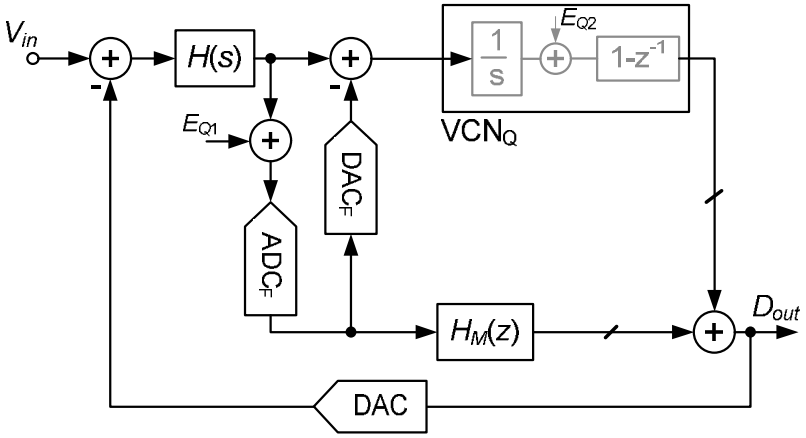

Fig. 3.7 Block diagram of the VCO-based ΣΔM from [56].

An example of a VCO-based reconfigurable continuous-time ΣΔM is described in [57]. It is mainly digital-based and it does not contain analog integrators, feedback DACs, comparators, or reference voltages. A 1st-order ΣΔM is based on a voltage-controlled ring oscillator proceeded by a phase decoder and digital differentiator with transfer function of $(1-z^{-1})$. The system utilizes digital background calibration and self-cancelling dither techniques and achieves a peak SNDR of 67–78 dB for a signal bandwidth of 3.9–18 MHz and a sampling frequency of 0.5–1.15 GHz while consuming from 8–17 mW. This ΣΔM, implemented in a 65 nm CMOS technology, is mainly digital-based and, therefore, it should scale well for deeper CMOS technology nodes. The second generation of this circuit, implemented in the same technology, is presented in [58] where the SNDR spans over 70-75 dB, the bandwidth spans 5–37.5 MHz while consuming from 11.5–39 mW.

Another circuit allowing exchanging amplitude resolution for time resolution is the pulse-width modulation (PWM)-based quantizer presented in Fig. 3.8a [59]. In this case, the output of the loop filter is converted to pulse $p(t)$ with a given width. During each clock period (divided into few time steps, T_Q), a pulse with discrete levels of width is used to represent the sample (Fig. 3.8b) instead of the usual discrete levels of amplitude (divided into voltage steps, V_Q) (Fig. 3.8c). The time-to-digital converter generates digital codes that are discrete representations of the edges of the $p(t)$ signal, and it also generates a 'time-quantized' feedback pulse signal $p_q(t)$ that corresponds to the output code, which is then fed back to the loop filter. The quantization error of the time-to-digital converter and the nonlinearity error of the PWM are shaped by the loop filter. The ΣΔM from [59] achieves a peak SNDR of 60 dB in a 20 MHz signal bandwidth while consuming 10.5 mW.

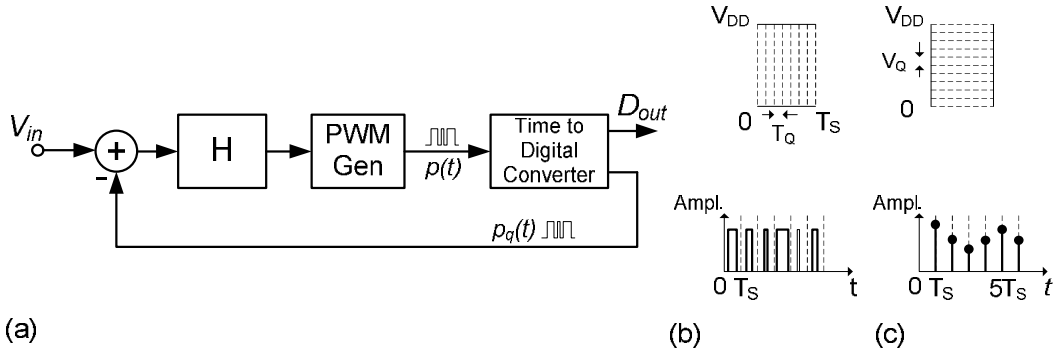

Fig. 3.8 (a) PWM-based quantizer [59] (b) discrete levels of pulse width (c) discrete levels of amplitude.

As stated before, ΣΔMs widely use multi-bit quantizers because they allow improving the modulator's performance (theoretically the SNR increases 6 dB per each bit added to the quantizer). This section presented examples of multi-bit ΣΔMs achieving moderate resolutions in low-to-high signal bandwidths and in the case of using VCO-based quantizers, high resolutions in medium signal bandwidths.

3.4. Jitter Reduction Techniques

In a continuous-time modulator architecture jitter is a critical issue to be taken into account. In this section three common jitter reduction methods are briefly described.

A straightforward method relies on using multi-bit structure. The jitter contribution is proportional to the DAC step height. The more bits are used the shorter step height and better resolution of the ADC. Hence, the jitter requirements become more relaxed. The drawback of this solution is the quantizer power consumption that increases for every additional bit together with the need of using dynamic element matching techniques to reduce the distortion from the multi-bit DAC.

The second method is based on replacing the current-mode DAC (current-steering) by a switched-capacitor based DAC. A current-mode DAC output is a constant current pulse, with a width determined by the clock signal. In the case of jitter error, any variations in the duration of the current pulse translate into an error in the amount of charge transferred to the integrator, resulting in added noise to the ΣΔM. A switched-capacitor based DAC generates a current spike appearing at the beginning of the clock phase, when the most of the charge is transferred into the integrator. Hence, the ΣΔM becomes much less sensitive to clock jitter. The concept of switched-capacitor feedback DAC is used for example in [60] and [61].

Another method of jitter reduction relays on applying a bit-stream of a single-bit quantizer into a finite impulse response (FIR) filter proceeding a DAC. In this case the DAC contain N cells and its response pulse is widened over N periods, averaging the jitter contribution. A modulator using this method is still a single-bit architecture and, hence, no linearization techniques are required. The drawback of this solution is the increased loop-delay, which has to be taken into

consideration in order not to lower the system stability. The concept of a FIR filter proceeding a multi-bit DAC is used and can be found for example in [62-64].

3.5. Summary

Table 3.3 and Table 3.4 summarize the performance parameters of the recent single-loop discrete-time and continuous-time ΣΔMs, respectively. These modulators are also categorized by their quantizer type. Table 3.5 presents the recent cascade ΣΔMs distinguishing between discrete-time and continuous-time architectures. The main criterion for choosing these ΣΔMs is their low FoM_W among similar recently published modulators. In all cases the parameters and performance of each modulator are summarized by:

- Minimum channel length of the transistors in the technology process;
- Area occupied by the circuit on the chip;
- Signal-to-noise-plus-distortion ratio (SNDR) achieved by the ΣΔM;
- Dynamic range (DR) achieved by the ΣΔM;
- Power consumption, P_C of the circuit;
- Sampling frequency, F_S of the modulator;
- Modulator's bandwidth;
- Figure of merit FoM_W, defined in Chapter 2.2;
- Figure of merit FoM_S, defined in Chapter 2.2.

Fig. 3.9 and Fig. 3.10 depict the graphs: FoM_W versus 2·bandwidth (2·BW) and SNDR versus 2·bandwidth (2·BW), respectively, of the data listed in tables ΣΔMs. From the literature review analyzed and presented in this chapter, the following observations can be made [3, 29]:

- Continuous-time architectures became more popular than the discrete-time. The majority of recent ΣΔMs are built with use of continuous-time architectures. One can notice that, the trend in designing ΣΔMs is to extend the covered range of specifications, by increasing the bandwidth. Continuous-time ΣΔMs can work with roughly 2-to-4 times higher clock rates than discrete-time ΣΔMs. Therefore, they are able to operate at higher signal bandwidths [65, 66] achieving in most cases moderate resolutions.

- The recent designs use the following techniques: feed-forward loop filter topology, higher order loop filters (integrators), reduced number of op-amps, digitally assisted DAC correction, multi-stage, multi-path feed-forward amplifiers.

  Single-loop architectures are used more often than cascaded ones. Nevertheless, recent works presented ΣΔMs achieving moderate resolutions in high signal bandwidths [9, 12].

  Most of the ΣΔMs targeting wide-band applications use multi-bit quantizers with

dynamic element matching or digital correction techniques in order to reduce the effect of DACs' nonlinearity. Nevertheless, recent works show ΣΔMs using single-bit FIR filters proceeding multi-bit DACs operating at high sample rates [67].

The referred techniques and their combinations are used in order to increase resolution and power efficiency of modulators.

- The passive or passive-active loop filter architectures can be used in order to design ΣΔMs with higher power efficiency and moderate resolutions.

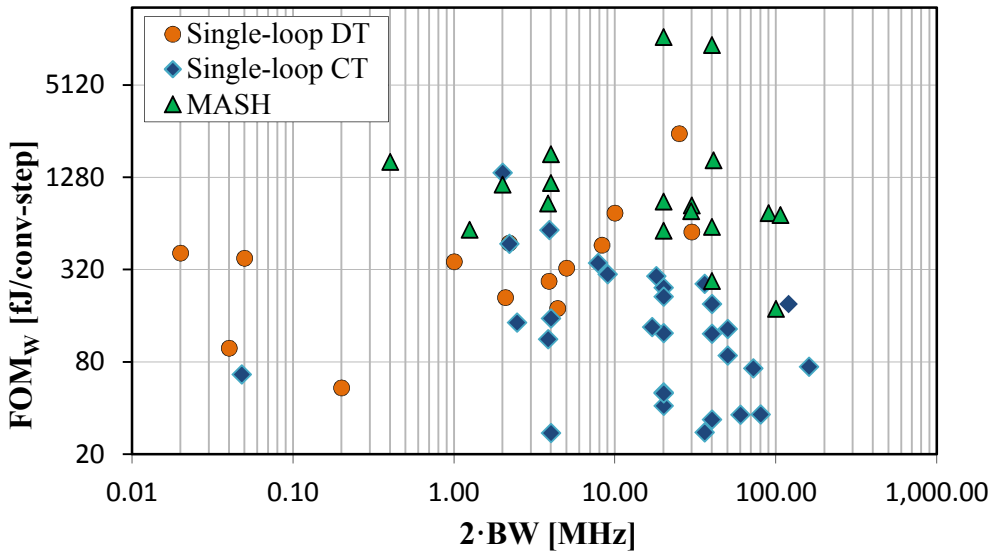

Fig. 3.9 The graph FoM$_W$ vs. 2·BW of the state-of-the-art ΣΔMs.

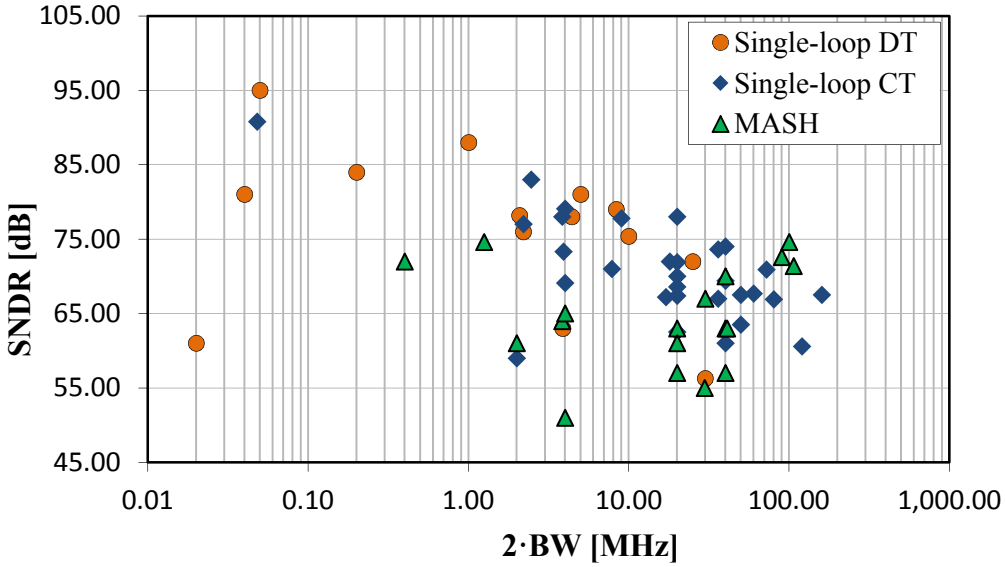

Fig. 3.10 The graph SNDR vs. 2·BW of the state-of-the-art ΣΔMs.

Table 3.3 State-of-the-art single-loop low-pass discrete-time ΣΔMs.

Single-bit quantizer									
Ref	**Tech. [µm]**	**Area [mm2]**	**SNDR [dB]**	**DR [dB]**	**P_C [mW]**	**F_S [MHz]**	**BW [MHz]**	**FoM_W [fJ/conv-step]**	**FoM_S [dB]**
[47]	0.18	0.715	81.0	85.0	0.036	4	0.02	98.1	172.4
[68]	0.18	0.44	78.2	79.3	2.9	50	1.04	209.5	164.8
[69]	0.13	0.602	75.0	88.0	7.4	64	0.5	1610	166.3
[70]	0.13	0.338	61.0	64.0	0.0075	1.4	0.01	409.0	155.2
[71]	0.045	0.04	56.3	59.6	9	1500	15	562.1	151.8
Multi-bit quantizer									
Ref	**Tech. [µm]**	**Area [mm^2]**	**SNDR [dB]**	**DR [dB]**	**P_C [mW]**	**F_S [MHz]**	**BW [MHz]**	**FoM_W [fJ/conv-step]**	**FoM_S [dB]**
[38]	0.18	0.492	84.0	88.0	0.14	3.2	0.1	54.0	176.5
[72]	0.18	2.32	78.0	86.0	5.1	144	2.2	178.5	172.3
[73]	0.09	0.26	63.0	66.0	1.2	38.4	1.94	267.9	158.1
[74]	0.18	3.67	81.0	83.0	15	60	2.5	327.1	165.2
	0.18	3.67	79.0	81.0	28	100	4.17	461.3	162.7
[75]	0.18	2.16	95.0	100.0	0.87	5	0.025	378.5	174.6
[76]	0.18	1.1	76.0	85.0	5.4	132	1.1	476.0	168.1
[77]	0.18	3.75	75.4	76.0	36	80	5	748.1	157.4
[34]	0.18	0.95	72.0	84.0	200	200	12.5	2458.9	162.0

Table 3.4 State-of-the-art single-loop low-pass continuous-time ΣΔMs.

Single-bit quantizer									
Ref	**Tech. [µm]**	**Area [mm^2]**	**SNDR [dB]**	**DR [dB]**	**P_C [mW]**	**F_S [MHz]**	**BW [MHz]**	**FoM_W [fJ/conv-step]**	**FoM_S [dB]**
[62]	0.09	0.12	70.9	83.0	15	3600	36	72.8	176.8
[78]	0.18	0.55	83.0	83.0	4.1	76.8	1.23	144.4	167.8
[42]	0.045	0.49	60.6	61.5	20	6000	60	190.4	156.3
[64]	0.18	0.2	77.0	77.3	6	281.6	1.1	470.8	159.9
[60]	0.065	0.71	73.3	79.0	8.55	124.8	1.95	580.2	162.6
[79]	0.18	0.14	59.0	89.0	2	64	1	1373.1	176.0
[16]	0.065	0.013	69.1	76.2	0.256	320	2	27.5	175.1
[67]	0.016	0.0194	66.9	67.8	5.25	2400	40	36.3	166.6
	0.016	0.0194	67.7	68.2	4.3	1800	30	36.1	166.6
	0.016	0.0194	69.4	70	3.24	1200	20	33.6	167.9
	0.016	0.0194	67.4	68.7	1.94	600	10	50.6	165.8
[8]	0.065	0.039	68.6	71.2	1820	650	10	41.4	138.6

Multi-bit quantizer									
Ref.	**Tech. [µm]**	**AREA [mm²]**	**SNDR [dB]**	**DR [dB]**	**P_C [mW]**	**F_S [MHz]**	**BW [MHz]**	**FoM_W [fJ/conv-step]**	**FoM_S [dB]**
[5]	0.04	0.051	70.0	70.6	2.57	300	10	50	165.9
[80]	0.18	0.72	90.8	93.5	0.09	3.072	0.024	66.2	177.8
[51]	0.09	0.23	67.5	72.0	8.5	500	25	87.7	166.7
[63]	0.04	0.085	78.0	83.0	2.8	245.76	1.92	112.3	171.4
[81]	0.13	1.2	74.0	76.0	20	640	20	122.1	166.0
[56]	0.09	0.36	78.0	79.1	16	600	10	123.2	167.1
[37]	0.09	0.15	63.5	70.0	8	500	25	130.9	164.9
[82]	0.065	0.084	79.1	80.0	4.52	128	2	153.9	166.5
[83]	0.065	0.08	61.0	63.0	7	2560	20	190.9	157.6
[84]	0.11	0.32	62.5	70.2	5.32	300	10	244.1	162.9
[57]	0.065	0.07	67.0	70.0	17	1152	18	258.1	160.2
	0.065	0.07	72.0	76.0	17	1152	9	290.3	163.2
	0.065	0.07	77.8	80.0	17	1152	4.5	297.7	164.2
	0.065	0.07	71.0	71.5	8	500	3.91	353.1	158.4
[6]	0.028	0.08	73.6	78.1	3.9	640	18	27.7	174.7
[85]	0.09	0.12	67.2	69.3	4.3	300	8.5	135.1	162.3
[86]	0.02	0.1	67.5	73	23	2814	80	74.2	168.4
[87]	0.13	1.3	71.9	80	13.7	185	10	213.0	168.6

Table 3.5 State-of-the-art cascade low-pass ΣΔMs.

Discrete-time implementation									
Ref.	**Tech. [µm]**	**AREA [mm²]**	**SNDR [dB]**	**DR [dB]**	**P_C [mW]**	**F_S [MHz]**	**BW [MHz]**	**FoM_W [fJ/conv-step]**	**FoM_S [dB]**
[88]	0.09	1	70.0	72.0	27.9	420	20	269.9	160.6
[44]	0.18	1.92	74.6	76.9	3.2	20	0.625	583.3	159.8
[89]	0.032	0.13	63.0	66.0	28	400	20	606.4	154.5
[90]	0.13	0.2	64.0	70.0	4.3	38.4	1.92	864.6	156.5
[91]	0.13	0.4	63.0	67.0	20.5	240	10	888.0	153.9
[92]	0.09	0.4	61.0	66.0	2.1	40	1	1145.2	152.8
	0.09	0.4	72.0	78.0	2.1	40	0.2	1613.6	157.8
	0.09	0.4	51.0	58.0	2.1	40	2	1811.0	147.8
[93]	0.09	0.076	65.0	66.0	6.83	320	2	1175.0	150.7
[94]	0.09	1.3	63.0	67.0	78	327.68	20.5	1649.8	151.2
[10]	0.065	0.28	67.0	67.0	46	240	15	838.1	152.1

Continuous-time implementation									
Ref.	**Tech. [µm]**	**AREA [mm²]**	**SNDR [dB]**	**DR [dB]**	**P_C [mW]**	***F_S* [MHz]**	**BW [MHz]**	**FoM_W [fJ/conv-step]**	**FoM_S [dB]**
[11]	0.065	0.17	61.0	70.0	10.5	208	10	572.6	159.8
	0.065	0.17	55.0	61.0	10.5	208	14.9	769.1	152.5
[95]	0.18	2.1	57.0	67.0	216	160	20	9335.1	146.7
	0.18	1.7	57.0	67.0	122	160	10	10545.2	146.1
[12]	0.028	0.34	74.6	85.0	78	1800	50	177.7	173.1
[9]	0.028	0.9	72.6	90	235	3200	45	749.0	172.8
	0.028	0.9	71.4	88	235	3200	53.3	726.0	171.6

4. PASSIVE SIGMA-DELTA MODULATORS

The power dissipation of ΣΔMs can be reduced by selecting passive or mixed active-passive architectures, in which the processing gain of comparator is used in the feedback loop of the ΣΔM's filter [14]. This allows reducing the number of amplifiers and their corresponding gain. This solution is very appealing for deep nanometer CMOS technologies, because a comparator can achieve large gain through positive feedback, which improves with faster transistors and does not require a complicated compensation scheme.

This chapter compares active and passive ΣΔMs and it describes a method of estimating the gain of a single-bit quantizer. Then, discrete-time and continuous-time implementations of passive integrators are presented and their thermal and jitter noise analyzes are presented. In the last section, a general design methodology for ΣΔMs based on genetic algorithm is presented.

4.1. Active vs. Passive ΣΔM

The main difference between passive and active ΣΔMs is distribution of the loop gain. While in active ΣΔM it is distributed among all the integrators, in passive ΣΔM it is mainly concentrated in the quantizer. Because passive integrators can only attenuate, the signal amplitude at the input of the quantizer is significantly reduced. Therefore, a single-bit quantizer (comparator) is commonly used in passive modulators instead of multi-bit quantizer. This means, the processing gain of the comparator gain is larger than one because its output amplitude is close to V_{DD}. In an active structure the comparator has a processing gain close to one.

A basic building block in a ΣΔM is an integrator, H, which can be mathematically represented in ideal form as $z^{-1}/(1-z^{-1})$ or k/s, respectively in discrete-time and continuous-time domains. These transfer functions at DC become ∞, providing complete cancellation of the quantization noise for a DC signal. For simplicity, in further analysis, discrete-time integrators are considered. The ideal integrator is not feasible and, in reality, the transfer function of an active integrator is typically given by:

$$H_A = \frac{z^{-1}}{1-\beta_A \cdot z^{-1}}; \quad \beta_A = 1-\alpha_A; \quad \alpha_A \sim \frac{1}{A} \tag{4.1}$$

where A denotes the finite gain of an amplifier used to implement an active integrator. On the other hand, a passive integrator can be described by:

$$H_P = \frac{\alpha_P \cdot z^{-1}}{1-\beta_P \cdot z^{-1}}; \quad \beta_P = 1-\alpha_P \tag{4.2}$$

This integrator does not have an amplifier and its maximum gain at low frequencies is equal to one.

4.1.1. Analysis of a 1st-Order ΣΔM

In order to better understand the differences between active and passive modulators it is useful to analyze the behavior of a 1st-order ΣΔM. Fig. 4.1 depicts its generic linear model, where H_1 is the integrator's transfer function, E_{TN1} is its thermal noise, b_1 is the feedback factor, G_C is the comparator's processing gain and E_C, E_Q denote comparator and quantization noises, respectively. Fig. 4.1 presents also some differences between active and passive structures. The ΣΔM's output signal D_{OUT} in baseband is given by:

$$D_{out} = \frac{H_1 \cdot G_C \cdot V_{IN} + E_{TN1} \cdot H_1 \cdot G_c + E_C \cdot G_C + E_Q}{1 + H_1 \cdot G_C \cdot b_1} \tag{4.3}$$

$$\text{Denominator}\{D_{out}\} = 1 + H_1 \cdot G_C \cdot b_1 \approx H_1 \cdot G_C \cdot b_1 \tag{4.4}$$

$$D_{out} \approx \frac{V_{IN}}{b_1} + \frac{E_{TN1}}{b_1} + \frac{E_C}{H_1 \cdot b_1} + \frac{E_Q}{G_C \cdot H_1 \cdot b_1} \tag{4.5}$$

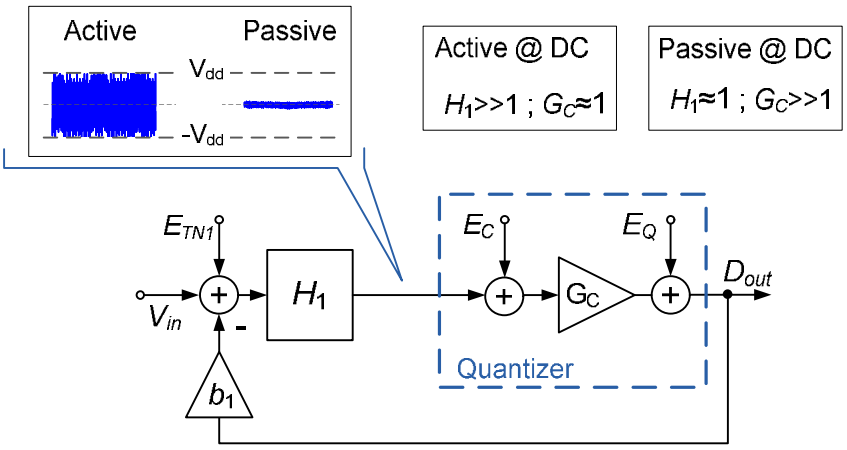

Fig. 4.1 Linear model of single-loop 1st-order ΣΔM.

In an active modulator, the integrator comprises an amplifier and, therefore, its low frequency transfer function $H_1 >> 1$. This means that, the amplitudes of the input and output signals of the comparator are similar causing that its processing gain $G_C \approx 1$. The first feedback factor b_1 defines the maximum amplitude of the modulator because it is added (subtracted) to the input signal. For simplicity, it is considered that $b_1 = 1$. The equation of D_{OUT} when an active integrator is used is given by (4.6). One can notice that, if $H_1 >> 1$, E_C and E_Q are strongly attenuated by H_1 and E_{TN1} is added directly to V_{in}.

$$\text{if active: } D_{out} \approx V_{IN} + E_{TN1} + \frac{E_C}{H_1} + \frac{E_Q}{H_1} \tag{4.6}$$

In a passive ΣΔM, the output signal D_{OUT} in the baseband is described by (4.7), where the passive integrator's transfer function is $H_1 \approx 1$. The design of the comparator becomes more important in the passive approach than in the active one sine it has to produce signal with digital level from a strongly attenuated input signal (Fig. 4.1). It can be seen that, if $G_C >> 1$, the quantization noise is considerably suppressed and E_C and E_{TN1} are added directly to V_{in}. The passive ΣΔM's SQNR is defined by G_C and the SNR is limited by thermal noise.

$$\text{if passive: } D_{out} \approx V_{IN} + E_{TN1} + E_C + \frac{E_Q}{G_C} \tag{4.7}$$

4.1.2. Dead Zones

When the input, V_{IN}, of a ΣΔM is zero, its output signal alternates between +1 and -1. For a small input DC signal, δ, the output also alternates between +1 and -1 but, after a certain number of clock cycles, two or more +1 in a row will occur. The average value of the output bit-stream is equal to the value of the input signal δ. A ΣΔM with an ideal integrator has an infinite precision for DC signals. In the case of an active integrator with finite op-amp gain, for a certain range of V_{in} around 0 the output signal will not change. This range is called dead zone or dead band and it occurs if the input signal is $\delta < \frac{\beta_A - 1}{\beta_A + 1}$ [4 ch. 2.8]. By making β_A close to 1 the dead zone is reduced (this translates into increasing the gain of the amplifier in the integrator). If the integrator is ideal (β=1) the dead zone does not exist.

In case of a ΣΔM with a passive integrator the same behavior can be observed. The dead zone depends on β_P and it is possible to have $\beta_P = \beta_A$, by adjusting the value of α_P. This means that, active and passive structures have the same behavior. In the case of passive ΣΔMs it is considered that the comparator is always capable of producing a valid output logic level. Even if the output of the passive integrator has smaller amplitude (α_P times smaller) than the active one, the digital output is the same in both structures. Therefore, the only difference between the two types of modulators is that the output amplitude of the passive integrator is smaller than the output amplitude of the active integrator. This means that, the passive integrator is more sensitive to thermal noise due to the smaller amplitude levels. Besides this difference, the two modulators behave exactly the same, having the same input (analog) to output (digital) transfer function. Moreover, as long as $\beta_P = \beta_A$, the dead zone of a passive ΣΔM is the same as an active ΣΔM.

4.1.3. Analysis of a 2nd-Order ΣΔM

Fig. 4.2 depicts a linear model of a 2nd-order passive-active ΣΔM, where H_1, H_2 are the passive

integrators' transfer functions, E_{TN1}, E_{TN2} are their thermal noises, G is an inter-stage low gain block, b_1, b_2 are feedback factors, G_C is the comparator's processing gain and E_C, E_Q denote comparator and quantization noises, respectively.

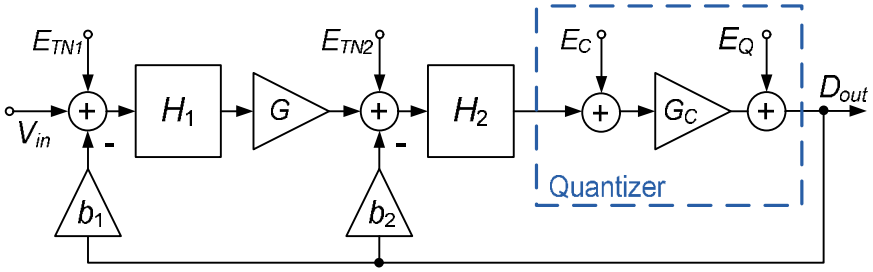

Fig. 4.2 Linear model of single-loop 2nd-order ΣΔM.

Before describing the behavior of a passive-active ΣΔM it is important to analyze an active-active structure. In an active-active ΣΔM, integrators H_1 and H_2 have internal amplifiers (in that case G can be neglected) meaning that at low frequencies $H_{1,2}>>1$. Therefore, the noise sources E_{TN2}, E_C and E_Q are suppressed by the integrators' gain. $G_C\approx1$ and the contribution of E_C and E_Q can be neglected as well since they are considerably attenuated. This means that, for the overall noise reduction, the noise of the first integrator H_1 is critical, causing its OTA to consume a significant part of the ΣΔM power. Usually the performance of the OTA used in H_2 is less important and its biasing current can be scaled down to reduce the analog power.

In the case of the passive-active ΣΔM from Fig. 4.2 the following equations describe the output signal D_{OUT} in the baseband, where the passive integrators' transfer functions are $H_{1,2}\approx1$.

$$D_{out}=\frac{G\cdot G_C\cdot V_{IN}+E_{TN1}\cdot G\cdot G_c+E_{TN2}\cdot G_C+E_C\cdot G_C+E_Q}{1+G_C\cdot(b_2+b_1\cdot G)} \tag{4.8}$$

$$\text{Denominator}\{D_{out}\}\approx G_C\cdot G\cdot\left(b_1+\frac{b_2}{G}\right)\approx G_C\cdot G\cdot b_1 \tag{4.9}$$

$$D_{out}\approx\frac{V_{IN}}{b_1}+\frac{E_{TN1}}{b_1}+\frac{E_{TN2}}{b_1\cdot G}+\frac{E_C}{b_1\cdot G}+\frac{E_Q}{G_C\cdot G\cdot b_1} \tag{4.10}$$

To interpret (4.10), one has to remember that V_{in} cannot exceed b_1 in order not to saturate the modulator. Also notice that the digital output of the ΣΔM is a number that represents the ratio between V_{in} and b_1 and, therefore, the maximum theoretical (V_{in}/b_1) is 1. Since b_1 defines the maximum amplitude of V_{in}, it should be kept close to the maximum voltage allowed in the circuit. Moreover, one can conclude that if $G_C>>1$, the quantization noise is considerably suppressed, that E_C and E_{TN2} are attenuated by G and that E_{TN1} is added directly to V_{in}. This means that, the ΣΔM's SQNR is mainly defined by G_C (because $G_C>G$) and the SNR is mainly limited by the thermal noise of the first integrator, E_{TN1}.

4.2. Approximation of the Gain of the Comparator

In the previous sections one could notice the importance of the processing gain of the comparator, which attenuates the quantization noise in passive ΣΔM. Here this comparator's gain is investigated by analyzing a first order passive ΣΔM (Fig. 4.3). In this modulator the loop filter is a passive integrator that, as shown in previous sections, does not provide any gain and attenuates the signal at higher frequencies causing a very small amplitude in the output signal (comparator's input). This means that, using a multi-bit quantizer is impractical in passive ΣΔMs (due to the requirement of using comparators with very small offset voltages) and, normally, a single-bit quantizer (comparator) has to be used.

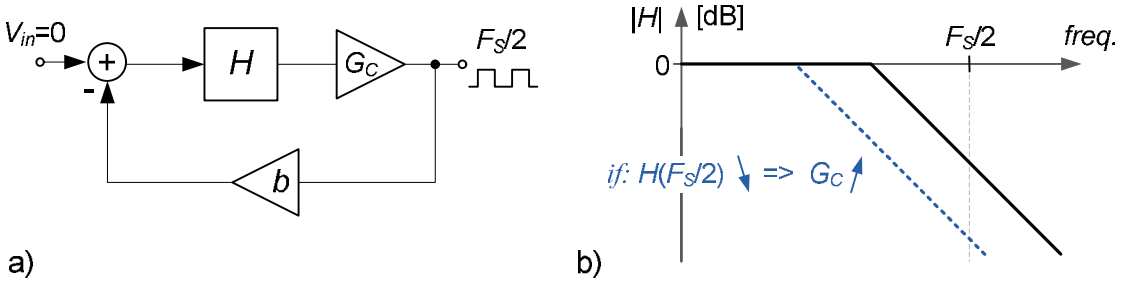

Fig. 4.3 First order ΣΔM with V_{in} = 0 (a) and frequency response of a first order passive loop filter (b).

The equivalent gain of the comparator (G_C) is not constant due to its changing input signal amplitude and constant output value. Nevertheless, one can estimate it as a ratio of the comparator's output *rms* value to its input *rms* value and determine these values from simulation. It can also be estimated using the approach described in [13]. When the input of the modulator is 0, the output bit-stream will be a square wave with a frequency equal to $F_s/2$, where F_s denotes sampling frequency. Therefore, the feedback signal will be a square wave with amplitude equal to b and frequency $F_s/2$. The integrator's output will mainly consists of an attenuated sine wave at $F_s/2$. This attenuation depends on the transfer function H at $F_s/2$ and the feedback factor b. Therefore, G_C can be estimated by calculating the transfer function from the output to the input of the comparator and evaluating this function at $F_s/2$. Hence:

$$G_C = \frac{1}{\left|b \cdot H(F_S/2)\right|} = \frac{1}{\left|b \cdot H(z=-1)\right|} \tag{4.11}$$

One can notice that, since H is a low-pass filter, by decreasing the frequency of the pole a higher G_C value can be achieved as it is shown in Fig. 4.3. Substituting H in (4.11) by transfer function from (4.2) results in an equation for G_C that is presented in (4.12). In practice, since the feedback factor b defines maximum amplitude of the modulator's input signal, it cannot be adjusted (lowered) in order to increase value of G_C because this would result in a reduced input voltage range for the ΣΔM.

$$G_C = \frac{2-\alpha}{b \cdot \alpha} \approx \frac{2}{b \cdot \alpha} \tag{4.12}$$

A 2nd-order ΣΔM can be built by adding a second integrator in cascade with the 1st-order modulator with a negative feedback at the input, as shown in Fig. 4.4. The maximum input signal of the modulator is given by b_1. The second feedback factor b_2 can be adjusted (lowered) leading to higher value of G_C than in case of 1st-order ΣΔM and stronger quantization noise attenuation.

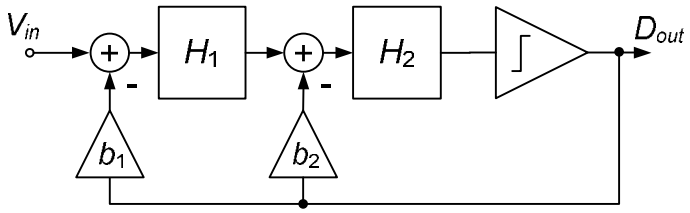

Fig. 4.4 Second-order ΣΔM.

Estimation of G_C in the 2nd-order ΣΔM can be done as described before. However, when the input of the modulator is 0, the output bit-stream will be a square wave with a frequency equal to $F_s/4$. The second integrator, together with its feedback, has a dominating influence in the value of G_C, because of the additional gain in the loop obtained by making $b_2<1$. Considering the transfer function from (4.2) G_C can be approximated as:

$$G_C \approx \frac{1}{2} \cdot \frac{2-\alpha}{b_2 \cdot \alpha} \approx \frac{1}{b_2 \cdot \alpha} \tag{4.13}$$

4.3. Concept of Ultra-Incomplete Settling (UIS) in a Switched-Capacitor Integrator

As shown before, ΣΔMs using passive integrators allow avoiding the design of high gain amplifiers because they use comparators to provide part of this gain. In the following sections discrete-time and continuous-time implementations of passive integrators are presented.

The capacitor voltage in an *RC* circuit after a step input with amplitude V_{in}, is given by:

$$v_c(t) = V_{in} \cdot \left(1 - e^{-t/R_{on} \cdot C}\right) + V_{C0} \cdot e^{-t/R_{on} \cdot C} \tag{4.14}$$

where V_{C0} is the initial voltage in the capacitor, just before the input step. Fig. 4.5 shows a plot of (4.14) as a function of time, for generic values of C and R_{on}. In the normal operation of a switched-capacitor circuit it is expected that the capacitor is either (almost) completely charged or discharged at the end of the clock phase, corresponding to the complete settling area in the graph of Fig. 4.5. If the duration of the clock phase is much smaller than the time constant of the circuit, the *RC* circuit operates under the ultra-incomplete settling (UIS) condition $T_s \ll R \cdot C$. This can be achieved by adding an explicit resistance R, with the appropriate value, in series

with the switch. In case of UIS, the voltage in the capacitor at the end of the phase becomes a function of the input voltage (V_{in}) and of the capacitor voltage value in the previous clock cycle (V_{C0}).

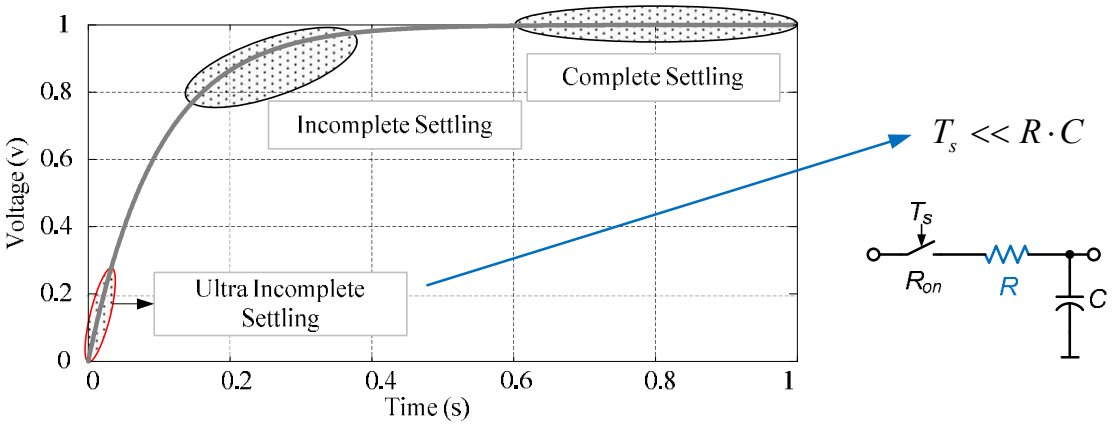

Fig. 4.5 Capacitor voltage for a step input (normalized time).

4.4. Discrete-Time Passive Integrator

The proposed switched-capacitor integrator circuit (single-ended version) is shown in Fig. 4.6. The input signal is applied to the resistor in phase Φ_1 and the output signal is the capacitor voltage. The output signal established at the end of Φ_1 is hold during Φ_2. A feedback path is defined by switches controlled by Φ_1 and D, connecting the bottom plate of C to either $V_{ref}+$ or $V_{ref}-$. Signal D denotes the output bit-stream of the ΣΔM voltage that is equal to either +1 or -1.

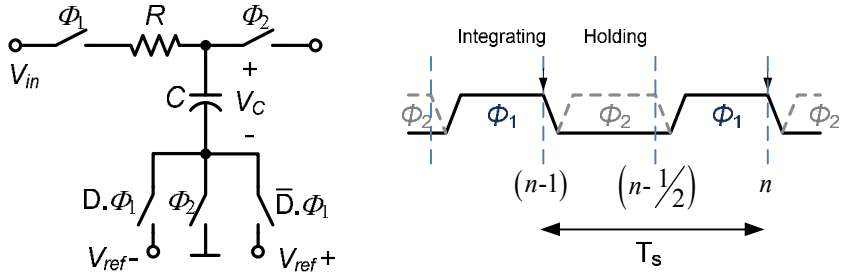

Fig. 4.6 Schematic of a single-ended switched-capacitor integrator and corresponding timing diagram.

The passive switched-capacitor integrator circuit works under UIS (first voltage region in Fig. 4.5) during phase Φ_1. In order to analyze its behavior we first analyze a ΣΔM that can be built using this passive switched-capacitor circuit. Fig. 4.7 depicts a schematic of the first-order ΣΔM with the differential passive integrator. The input signal is firstly sampled in C_{SH}, at the end of phase Φ_2, and then it is transferred into the integrator. During phase Φ_1, C_{SH} is connected to C_1 through series resistor R. The switched-capacitor integrator is followed by comparator with zero threshold voltage and by a D-type flip-flop (DFF) producing the output bit stream D.

In order to derive the integrator's transfer function, the circuit from Fig. 4.7 is analyzed in phase

Φ_1 when integration takes place. Fig. 4.8a depicts the S/H and the integrator circuit in phase Φ_1. Fig. 4.8b and Fig. 4.8c show its transformation that is analyzed underneath in order to obtain discrete-time transfer function and Z transfer function of the switched-capacitor integrator. Equation for the voltages in the loop depicted in Fig. 4.8c is:

$$2 \cdot v_1(t) + 2 \cdot R \cdot i_C(t) - 2 \cdot v_{SH}(t) + V_{ref} = 0 \tag{4.15}$$

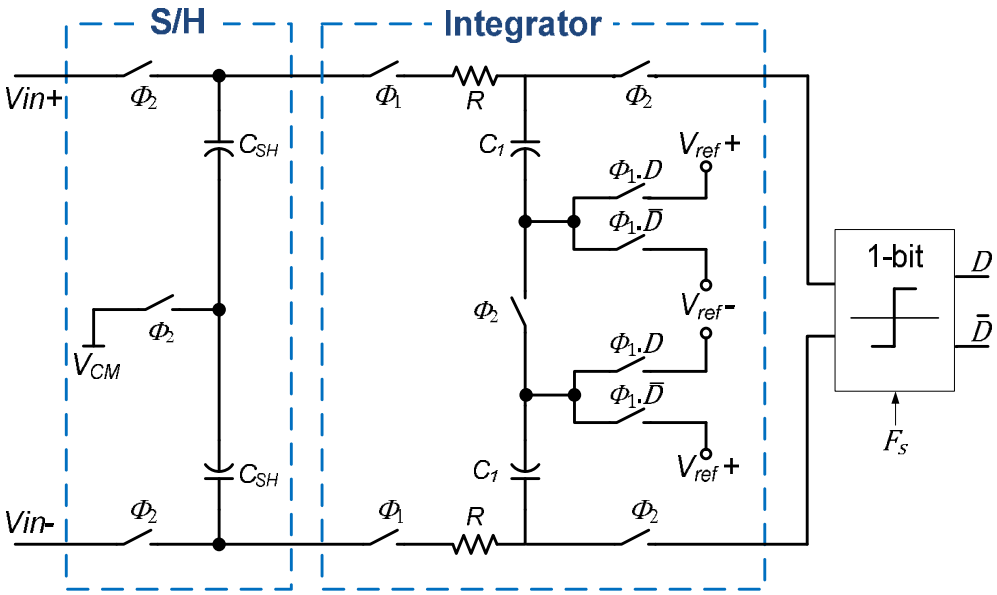

Fig. 4.7 1st-order ΣΔM built using differential passive UIS switched-capacitor integrator.

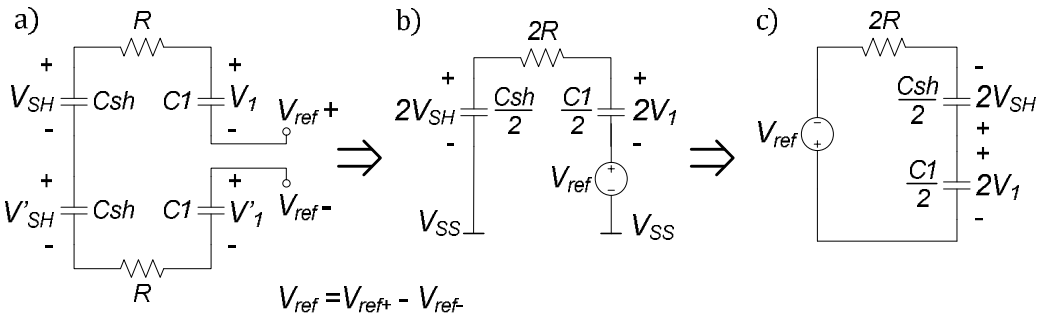

Fig. 4.8 S/H and integrator circuits in phase Φ1 (a) and they transformation (b, c).

From the equation for current flowing through capacitors:

$$C_1 \cdot \frac{dv_1(t)}{dt} = -C_{SH} \cdot \frac{dv_{SH}(t)}{dt} \tag{4.16}$$

we can write:

$$v_{SH}(t) = -\frac{C_1}{C_{SH}} \cdot v_1(t) + \frac{C_1}{C_{SH}} \cdot v_1(0) + v_{IN} \tag{4.17}$$

where $V_{IN} = v_{SH}(0)$, represents the sampled value of the input voltage in phase Φ_2. From (4.15) and (4.17) it is obtained:

$$v_1(t)\cdot\left[\frac{C_{SH}+C_1}{C_{SH}}\right]+R\cdot C_1\cdot\frac{dv_1(t)}{dt}=\frac{C_1}{C_{SH}}\cdot v_1(0)+V_{IN}-\frac{V_{ref}}{2} \tag{4.18}$$

The permanent and transient solutions of (4.18) are considered, yielding:

$$v_1(t)=v_{1p}(t)+v_{1t}(t) \tag{4.19}$$

For the permanent solution $\mathrm{dv_1(t)/dt}=0$, and it can be written:

$$v_{1p}(t)=\frac{C_1}{C_{SH}+C_1}\cdot v_1(0)+\frac{C_{SH}}{C_{SH}+C_1}\cdot\left(V_{IN}-\frac{V_{ref}}{2}\right) \tag{4.20}$$

In transient solution, we assume zero initial conditions and zero values of all the inputs.

$$v_{1t}(t)=-\tau\cdot\frac{dv_1(t)}{dt} \tag{4.21}$$

$$v_{1t}(t)=V_0\cdot e^{-\frac{t}{\tau}} \tag{4.22}$$

In above equations $\tau=R\cdot C_{EQ}$ and $C_{EQ}=C_1\cdot C_{SH}/(C_1+C_{SH})$. By substituting (4.20) and (4.22) into (4.19) we achieve:

$$v_1(t)=V_0\cdot e^{-\frac{t}{\tau}}+\frac{C_1}{C_{SH}+C_1}\cdot v_1(0)+\frac{C_{SH}}{C_{SH}+C_1}\cdot\left(V_{IN}-\frac{V_{ref}}{2}\right) \tag{4.23}$$

Obtaining V_0 by solving (4.23) for $t = 0$:

$$v_1(0)=V_0\cdot e^0+\frac{C_1}{C_{SH}+C_1}\cdot v_1(0)+\frac{C_{SH}}{C_{SH}+C_1}\cdot\left(V_{IN}-\frac{V_{ref}}{2}\right) \tag{4.24}$$

$$V_0=\frac{C_{SH}}{C_{SH}+C_1}\cdot\left(v_1(0)-V_{IN}+\frac{V_{ref}}{2}\right) \tag{4.25}$$

yields to:

$$v_1(t)=\frac{C_{SH}}{C_{SH}+C_1}\cdot\left(v_1(0)-V_{IN}+\frac{V_{ref}}{2}\right)\cdot e^{-\frac{t}{\tau}}+\frac{C_1}{C_{SH}+C_1}\cdot v_1(0)+\frac{C_{SH}}{C_{SH}+C_1}\cdot\left(V_{IN}-\frac{V_{ref}}{2}\right) \tag{4.26}$$

The (switched) *RC* circuit operates under the ultra incomplete settling condition $T_s \ll \tau$. Therefore, the exponential term can be approximated with:

$$if:\quad T_s \ll \tau \quad\Rightarrow\quad e^{-T_S/2\cdot\tau}\approx 1-\frac{T_s}{2\cdot\tau} \tag{4.27}$$

This approximation can be verified by plotting both functions (Fig. 4.9). One can notice, it is

valid for $0.5 \cdot T_S / (R \cdot C_1) < 0.1$.

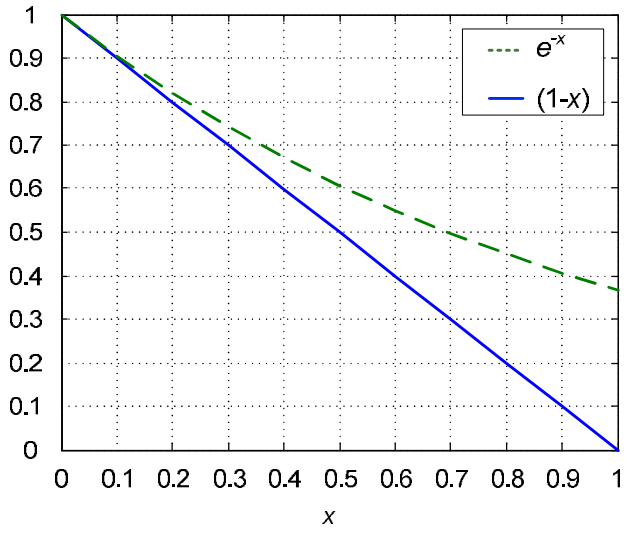

Fig. 4.9 e^{-x} versus (1 -x) approximation

By substituting (4.27) in (4.26), one can obtain:

$$v_1\left(\frac{T_S}{2}\right) \approx V_{IN} \cdot \frac{T_S}{2 \cdot R \cdot C_1} + v_1(0) \cdot \left(1 - \frac{T_S}{2 \cdot R \cdot C_1}\right) - \frac{V_{ref}}{2} \cdot \frac{T_S}{2 \cdot R \cdot C_1} \tag{4.28}$$

$$v_1\left(\frac{T_S}{2}\right) \approx \alpha \cdot V_{IN} + v_1(0) \cdot \beta - \alpha \cdot \frac{V_{ref}}{2} \tag{4.29}$$

where

$$\alpha = \frac{T_S}{2 \cdot R \cdot C_1} \qquad \beta = 1 - \alpha \tag{4.30}$$

Equation (4.29) provides the voltage on capacitor C_1 at the end of the phase Φ_1, which is the output voltage of the integrator. Fig. 4.10 depicts the voltage changes in capacitors C_1 and C_{SH} (which samples and holds V_{IN}).

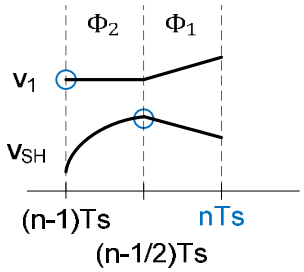

Fig. 4.10 Typical voltage waveforms in capacitors C1 and CSH.

Note that during phase Φ_2 capacitor C_{SH} operates under the complete settling condition. Taking into consideration that $v_1(0) = v_1[n-1]$ and $v_{IN} = V_{SH}(0) = V_{IN}[n-0.5]$ (Fig. 4.10) and (4.29), one can write:

$$v_1[n] = v_1\left[n-1\right]\cdot\beta + V_{IN}\left[n-\frac{1}{2}\right]\cdot\alpha - \frac{V_{ref}}{2}\cdot\alpha \tag{4.31}$$

At this point, it is important to note from (4.31) that, as long as the UIS condition is valid, the voltage v_1 is independent of the value of the input sampling capacitance C_{SH}. From (4.31), assuming reference input equal to zero, the Z transfer function of the integrator can be obtained.

$$H(z) = \frac{v_1(z)}{V_{IN}(z)} = \frac{\alpha\cdot z^{-\frac{1}{2}}}{1-\beta\cdot z^{-1}} \tag{4.32}$$

This expression shows that a switched-capacitor branch, under the right condition, can behave as a passive discrete-time first-order filter. The maximum and minimum gain values of (4.32) (note that β=1-α) are given, respectively, by:

$$H_{\max} = \left|H(z=1)\right| = \left|\frac{\alpha}{1-\beta}\right| = 1; \quad H_{\min} = \left|H(z=-1)\right| = \left|\frac{\alpha}{1+\beta}\right| \approx \frac{\alpha}{2-\alpha} \tag{4.33}$$

These expressions show that in order to increase the ratio between the maximum and minimum gain it is necessary to reduce the gain of the circuit (α), which means that the signal amplitude will be very small. Using a small α value moves the pole of the circuit closer to the unity circle (by making β closer to 1). A small value of α implies that the proposed RC integrator attenuates its input signal producing a small amplitude output signal.

4.4.1. Non-Ideal Effects in the Passive UIS Switched-Capacitor Integrator

The existence of parasitic capacitances and finite on-resistance in the switches influences the performance of the ΣΔM. These effects become more important for higher clock frequencies. Therefore, it is important to take into consideration these effects while designing high F_{clk} passive ΣΔMs.

Fig. 4.11 a) depicts single-ended branch of the discrete-time integrator including the relevant parasitic capacitances. In phase Φ_1 the integrator's input switch is closed and the signal from S/H passes, through resistor R, into capacitor C_1 (integration), simultaneously charging C_P (parasitic capacitance due to the switch and resistor). In phase Φ_2 the voltage on C_1 should be held to let the comparator to produce correct value. However, the previously charged C_P discharges through R, causing an unwanted integration during this phase. Due to the UIS, even a small value C_p is enough to provide the same amount of charge to C1 as the one received during the integration phase. This second integration increases the gain of the integrator, which can cause early saturation of the modulator for higher magnitude values.

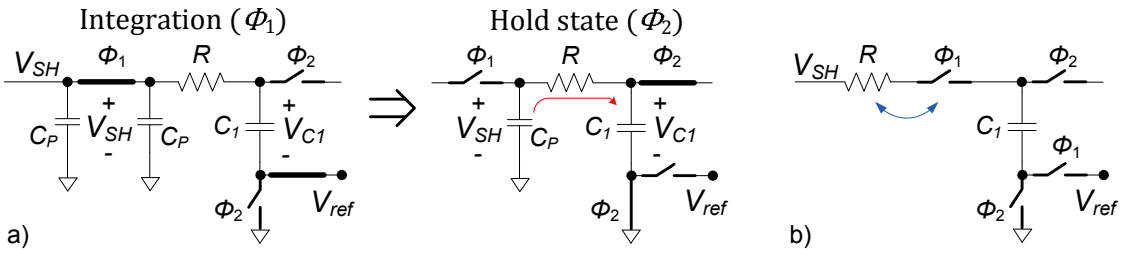

Fig. 4.11 Single-ended branch of the discrete-time integrator with parasitic capacitances (a) and integrator with moved input switch (b).

There is a simple solution that can reduce significantly the influence of this parasitic capacitance, as it is shown in Fig. 4.11 b). Moving the integrator's input switch after *R*. This causes the resistor *R* to be disconnected from the integrating capacitor, therefore, eliminating the unwanted integration during the second phase. Since C_P is now connected in parallel with C_I it does not cause integration in phase Φ_2. One can notice that, moving the input switch does not change any of the equations derived in the previous sections. The parasitic capacitance of the feedback switch also is connected in parallel with the main capacitor *C* (that is much bigger) and can be neglected. The R_{ON} of this switch limits the transfer speed and, therefore, R_{ON} should be kept small.

4.5. Continuous-Time Passive Integrator with Switched-Capacitor Feedback

Although the UIS switched-capacitor passive integrator has the desired behavior, due to using switches in the input and output signal paths, it becomes more challenging to design at higher clock frequencies. Turning on and off these switches at high clock frequencies increases power dissipation. Moreover, keeping the non-ideal effects (due to parasitic capacitances) under control becomes more difficult. In order to solve some of these issues a new passive continuous-time *RC* integrator is proposed. The circuit (single-ended version) with its timing scheme is shown in Fig. 4.12.

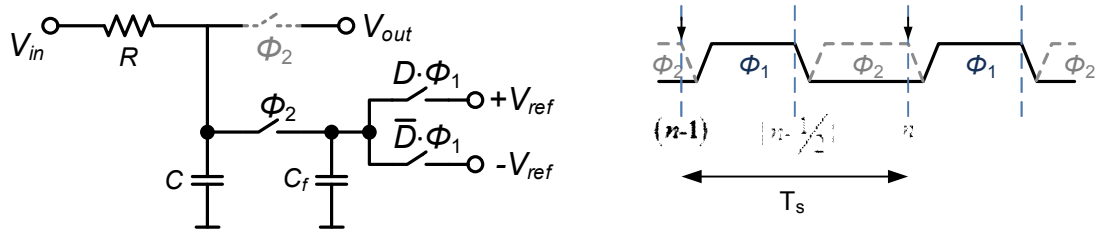

Fig. 4.12 Schematic of a single-ended RC integrator and corresponding timing diagram.

The input signal is applied to the resistor *R* and the output signal will be available at the top-plate of the capacitor *C*. In order to add a feedback path, a second capacitor should be connected in parallel with the input capacitor, *C*, during one clock phase. This feedback capacitor, C_f, is

pre-charged in the previous clock phase either to V_{ref} or -V_{ref}. Signal D denotes the ΣΔM output bit-stream voltage that is equal either to +1 or -1. The output switch in Fig. 4.12 (marked in grey dashed line) represents the sampling operation of the quantizer. The output voltage of the circuit is basically a linear combination of V_{in} and of D. The output of the integrator can be calculated at the discrete-time instants defined by the sampling clock signal shown in Fig. 4.12, resulting in the discrete-time transfer function of the circuit. First, the capacitor voltage due to the feedback is calculated. The feedback capacitor C_f is during phase Φ_1 pre-charged to $\pm V_{ref}$ (depending on value of D) and then, during Φ_2, part of this charge is transferred into C. The charge conservation principle results in (neglecting the R_{ON} of the switches):

$$Q_C^{\Phi_2} + Q_{C_f}^{\Phi_2} = Q_C^{\Phi_1} + Q_{C_f}^{\Phi_1} \tag{4.34}$$

$$V'_C\left(n \cdot T_S\right) \cdot (C + C_f) = V_C\left[\left(n - \tfrac{1}{2}\right) \cdot T_S\right] \cdot C + D\left[\left(n-1\right) \cdot T_S\right] \cdot V_{ref} \cdot C_f \tag{4.35}$$

$$V'_C\left(n \cdot T_S\right) = V_C\left[\left(n - \tfrac{1}{2}\right) \cdot T_S\right] \cdot \frac{C}{C + C_f} + D\left[\left(n-1\right) \cdot T_S\right] \cdot V_{ref} \cdot \frac{C_f}{C + C_f} \tag{4.36}$$

where $Q_{C,Cf}$ represents charge in C and C_f at phases Φ_1 and Φ_2, V_C and V'_C are the sampled voltages at C before and after applying feedback, respectively. Equation (4.36) shows that the feedback is proportional to V_{ref} and C_f. The use of a switched-capacitor structure causes that the feedback current exists only during phase Φ_2 implying a rapid change of V_C. The R_{ON} of these switches limits this transfer speed and, therefore, R_{ON} should be kept small. Moreover, the parasitic capacitance of the switches adds to C_f, affecting the feedback coefficient, which is important especially when the feedback capacitor C_f has a small value. These issues should be taken into account during circuit and layout design and by correct sizing of the feedback switches (by simulating their influence on the value of the feedback factor). In other words, the settling of the voltage on the feedback capacitor C_f should be ensured and, in case of the parasitic capacitance associated with the switches being a significant part of C_f, value of C_f can be decreased to get closer to the required value of the feedback coefficient.

In the following analysis it is considered that V_{in} changes very slowly (i.e. large OSR condition), hence it can be assumed constant during a clock period. First we analyze circuit from Fig. 4.12 in Φ_1. The output voltage of the integrator during phase Φ_1, is given by:

$$v_c(t) = V_{in} \cdot \left(1 - e^{-t/\tau}\right) + V_{C0} \cdot e^{-t/\tau} \tag{4.37}$$

where t in this cases is $T_s/2$ because we consider one phase duration, $\tau = R \cdot C$ and V_{C0} is the voltage across C at the beginning of phase Φ_1. The output voltage at the end of Φ_1 is (the end of phase Φ_1 is $(n\text{-}1/2) \cdot T_s$):

$$V_C\left[\left(n-½\right)\cdot T_S\right]=V_{in}\cdot\left(1-e^{\frac{-T_S}{2\cdot R\cdot C}}\right)+V_C\left[\left(n-1\right)\cdot T_S\right]\cdot e^{\frac{-T_S}{2\cdot R\cdot C}}. \tag{4.38}$$

Using the same approach the output voltage of the integrator at the end of Φ_2, is given by (where equivalent $C_{eq} = C + C_f$):

$$V_C\left[n\cdot T_S\right]=V_{in}\cdot\left(1-e^{\frac{-T_S}{2\cdot R\cdot C_{eq}}}\right)+V'_C\left[n\cdot T_S\right]\cdot e^{\frac{-T_S}{2\cdot R\cdot C_{eq}}}. \tag{4.39}$$

The $V'_C(n\cdot T_S)$ (voltage in C after applying feedback) can be obtained from (4.36), resulting in:

$$V_C\left[n\cdot T_S\right]=V_{in}\cdot\left(1-e^{\frac{-T_S}{2\cdot R\cdot C_{eq}}}\right)+\left[V_C\left[\left(n-½\right)\cdot T_S\right]\cdot\frac{C}{C_{eq}}+D\left[\left(n-1\right)\cdot T_S\right]\cdot V_{ref}\cdot\frac{C_f}{C_{eq}}\right]\cdot e^{\frac{-T_S}{2\cdot R\cdot C_{eq}}}. \tag{4.40}$$

The final value of output voltage at the end of Φ_2 is obtained from (4.40) using $V_C[(n\text{-}1/2)\cdot T_S]$ from (4.38):

$$\begin{aligned}V_C\left(n\cdot T_S\right)=V_{in}\cdot&\left[1-e^{\frac{-T_S}{2\cdot R\cdot C_{eq}}}+\frac{C}{C_{eq}}\cdot\left(1-e^{\frac{-T_S}{2\cdot R\cdot C}}\right)\cdot e^{\frac{-T_S}{2\cdot R\cdot C_{eq}}}\right]+\\&+V_C\left[\left(n-1\right)\cdot T_S\right]\cdot\frac{C}{C_{eq}}\cdot e^{\frac{-T_S}{2\cdot R\cdot C}}\cdot e^{\frac{-T_S}{2\cdot R\cdot C_{eq}}}+\\&+D\left[\left(n-1\right)\cdot T_S\right]\cdot V_{ref}\cdot\frac{C_f}{C_{eq}}\cdot e^{\frac{-T_S}{2\cdot R\cdot C_{eq}}}\end{aligned} \tag{4.41}$$

$$\begin{aligned}V_C\left(n\cdot T_S\right)=V_{in}\cdot&\left[1-e^{\frac{-T_S}{2\cdot R\cdot C_{eq}}}+\frac{C}{C_{eq}}\cdot\left(e^{\frac{-T_S}{2\cdot R\cdot C_{eq}}}-e^{\frac{-T_S}{2\cdot R\cdot C}-\frac{T_S}{2\cdot R\cdot C_{eq}}}\right)\right]+\\&+V_C\left[\left(n-1\right)\cdot T_S\right]\cdot\frac{C}{C_{eq}}\cdot e^{\frac{-T_S}{2\cdot R\cdot C}-\frac{T_S}{2\cdot R\cdot C_{eq}}}+\\&+D\left[\left(n-1\right)\cdot T_S\right]\cdot V_{ref}\cdot\frac{C_f}{C_{eq}}\cdot e^{\frac{-T_S}{2\cdot R\cdot C_{eq}}}.\end{aligned} \tag{4.42}$$

The exponential terms from (4.42) can be approximated according to:

$$\text{if: } x\ll 1 \quad\Rightarrow\quad e^x\approx 1+x. \tag{4.43}$$

This approximation, as shown in Fig. 4.9, is valid for x<0.1, that, taking into consideration all the exponential terms, is valid for this work. The final value of output voltage of the integrator from Fig. 4.12 at the end Φ_2 is:

$$V_C\left(n\cdot T_S\right)\approx V_{in}\cdot\frac{T_S}{R\cdot C_{eq}}+V_C\left[\left(n-1\right)\cdot T_S\right]\cdot\frac{C}{C_{eq}}\cdot\left(1-\frac{T_S}{2\cdot R\cdot C_{eq}}-\frac{T_S}{2\cdot R\cdot C}\right)+$$
$$+D\left[\left(n-1\right)\cdot T_S\right]\cdot V_{ref}\cdot\frac{C_f}{C_{eq}}\cdot\left(1-\frac{T_S}{2\cdot R\cdot C_{eq}}\right). \tag{4.44}$$

This equation can be written as:

$$V_C\left(n\cdot T_S\right)\approx V_{in}\cdot\alpha+V_C\left[\left(n-1\right)\cdot T_S\right]\cdot\beta+D\left[\left(n-1\right)\cdot T_S\right]\cdot\gamma \tag{4.45}$$

where α, β and γ represent adequate factors from (4.44). For analysis purpose, β can be simplified by considering that $C \approx C_{eq} = C + C_f$ (because in practice $C_f << C$):

$$\alpha=\frac{T_s}{R\cdot\left(C+C_f\right)}; \tag{4.46}$$

$$\beta=\frac{C}{C_{eq}}\cdot\left(1-\frac{T_S}{2\cdot R\cdot C_{eq}}-\frac{T_S}{2\cdot R\cdot C}\right)\approx\frac{C}{C_{eq}}\cdot\left(1-\alpha\right)\approx\left(1-\alpha\right) \tag{4.47}$$

In order to improve its performance the continuous-time integrator is implemented as a differential circuit shown in Fig. 4.13. This integrator comprises two resistors, hence the value of α has a $2\cdot R$ term, while β can be described in the same way as above:

$$\alpha=\frac{T_s}{2\cdot R\cdot(C+C_f)}\qquad\beta\approx\frac{C}{C_{eq}}\cdot\left(1-\alpha\right)\approx\left(1-\alpha\right) \tag{4.48}$$

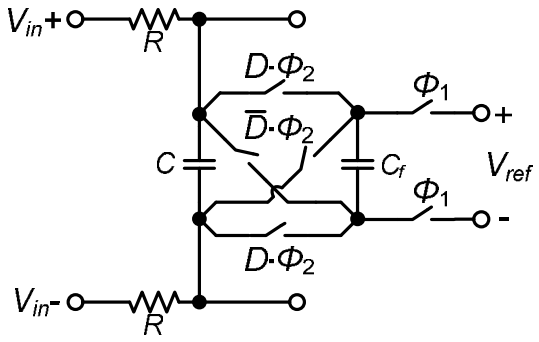

Fig. 4.13 Schematic of a differential RC integrator

Applying the Z transform to (4.45), and assuming reference input equal to zero, results in the discrete-time lossy-integrator transfer function:

$$H(z)=\frac{V_C(z)}{V_{in}(z)}=\frac{\alpha}{1-\beta\cdot z^{-1}}. \tag{4.49}$$

This shows that behavior of the circuit, under the right conditions, can be interpreted as non-delaying passive discrete-time first-order integrator. The maximum and minimum gain values of $H(z)$ are given, respectively, by:

$$H_{\max} = \left|H(z=1)\right| = \left|\frac{\alpha}{1-\beta}\right| = 1; \quad H_{\min} = \left|H(z=-1)\right| = \left|\frac{\alpha}{1+\beta}\right| \approx \frac{\alpha}{2-\alpha} \tag{4.50}$$

In order to have the frequency response closer to an ideal integrator it is necessary to have β as close to 1 as possible. This implies using α as small as possible. A very small integrator gain α will result in a very small amplitude for the integrator output signal.

4.6. Thermal Noise Analysis

4.6.1. Passive Discrete-Time Integrator

The single-ended passive discrete-time integrator, based on UIS, and its timing diagram are shown in Fig. 4.6. In equilibrium, the sampled thermal noise power at the terminals of a capacitor inside an *RC* circuit is given by $k \cdot T/C$. In the case of UIS, the voltage in the capacitor does not have time to reach the equilibrium condition and therefore, it is necessary to recalculate the thermal noise power in the capacitor. We analyze circuit when the integration takes place in phase Φ_1, which duration is $T_s/2$. The step response of this circuit is composed of two parts, the first occurs before the switch opens ($t<T_s/2$) and is given by:

$$v_1(t) = C_{SH} \cdot \left(\frac{1}{C_1 + C_{SH}} - \frac{e^{\frac{-t}{C_{EQ} \cdot R}}}{C_1 + C_{SH}} \right) \cdot V_{ref} \tag{4.51}$$

where $C_{EQ} = C_1 \cdot C_{SH} / (C_1 + C_{SH})$. The second occurs after the switch opens ($t>T_s/2$) and is given by a constant (the sampled voltage value). The impulse response of the circuit is given by the derivative of the step response $\left(h(t) = \frac{dv_1(t)/dx}{V_{ref}} \right)$, resulting in:

$$h(t) = \begin{cases} \frac{1}{R \cdot C_1} \cdot e^{\frac{-t}{C_{EQ} \cdot R}} & 0 \le t \le \frac{T_S}{2} \\ 0 & t > \frac{T_S}{2} \end{cases} \approx \begin{cases} \frac{1}{R \cdot C_1} & 0 \le t \le \frac{T_S}{2} \\ 0 & t > \frac{T_S}{2} \end{cases} \tag{4.52}$$

In this calculation, the approximation $\exp(t/(C_{EQ} \cdot R)) = 1$ is used, that gives ~99 % accuracy in the frequency response comparing to exact value of $h(t)$ (for the components values used in discrete-time ΣΔM design examples that are presented in the next sections). The transfer function, in the frequency domain, can be obtained by applying the Fourier transform to the previous expression:

$$H(f) = \int_{-\infty}^{\infty} h(t) \cdot e^{-2 \cdot \pi \cdot f \cdot t} dt = \frac{1}{R \cdot C_1} \cdot \frac{\sin(\pi \cdot f \cdot T_S)}{\pi \cdot f} \tag{4.53}$$

The thermal noise power sampled into the capacitor, at the end of integration phase Φ_1, is given by:

$$P_{NT} = \int_0^\infty 4 \cdot k \cdot T \cdot R \cdot \left|H(f)\right|^2 df = 4 \cdot k \cdot T \cdot R \cdot \frac{1}{R^2 \cdot C_1^2} \cdot \frac{T_S}{2} = \frac{2 \cdot k \cdot T \cdot T_S}{R \cdot C_1^2} \tag{4.54}$$

where k is a Boltzmann constant and T is temperature. This noise power is calculated integrating the power spectral density of the noise in R multiplied by the squared modulus of the frequency response from 0 Hz to infinity. Therefore, the result includes the noise contribution of all frequencies aliased back to $Fs/2$. The input referred noise can be calculated by:

$$P_{NTinput} = \frac{P_{NT}}{\alpha^2} = \frac{2 \cdot k \cdot T \cdot T_S}{R \cdot C_1^2 \cdot \alpha^2} = \frac{2 \cdot k \cdot T \cdot \alpha}{C_1 \cdot \alpha^2} = \frac{2 \cdot k \cdot T}{C_1 \cdot \alpha} \tag{4.55}$$

This expression shows that, since α is small, the input referred noise power is necessarily higher than in an active switched-capacitor circuit (a similar result was also reached for the passive switched-capacitor circuit in [15]). This means that, passive switched-capacitor circuits should use larger capacitance values than their active counterparts, in order to reach similar thermal noise performances. However, it is important to notice that this is only a minor drawback in terms of area, since the (static) power dissipation does not increase. Moreover, the amount of charge that the reference voltage buffers need to supply to the circuit is very small due to the incomplete settling behavior of the circuit. Hence, there is also no significant overhead in terms of dynamic power dissipated in charging and discharging the capacitors.

4.6.2. Passive Continuous-Time Integrator

The single-ended passive continuous-time integrator and its timing diagram are shown in Fig. 4.12. The noise analysis of the integrator circuit can be separated into two parts. First, considering the noise due to the feedback DAC (when the charge stored in C_f passes through the switch to C) and, second, considering the RC branch. The first analysis results in a noise power given by:

$$P_{NT1} = \left(\frac{k \cdot T}{C_f} + \frac{k \cdot T}{C_{eq1}}\right) \cdot \left(\frac{C_f}{C + C_f}\right)^2 \approx \frac{2 \cdot k \cdot T \cdot C_f}{C^2}. \tag{4.56}$$

where $C_{eq1} = (C \cdot C_f) / (C + C_f)$ is the equivalent capacitance of C and C_f during phase Φ_2 when both capacitors are connected in series (as seen by the noise source in the switch). Considering that $C_f << C$ then $C_{eq1} \approx C_f$ (with ~99 % accuracy for the components values used in continuous-time ΣΔM design example that are presented in the next sections). Equation (4.56) takes into account the noise created in both clock phases (pre-charging C_f and charge redistribution between C_f and C. The feedback input referred noise power is given by:

$$P_{NT1\_input} = \frac{P_{NT1}}{\alpha^2} \approx \frac{2 \cdot k \cdot T \cdot C_f}{C^2 \cdot \alpha^2}. \tag{4.57}$$

The second part of the analysis considers the noise contribution due to continuous-time operation of the integrator. The time varying nature of the circuit is due to the total value of capacitor changing from phase Φ_1 (C) to phase Φ_2 ($C+C_f$). An exact calculation would require splitting the calculation into two steps, each step using a different capacitance value, resulting in two different expressions. However since $C_f \approx C/100$, the difference between the two analyzes would be very small. Therefore, the noise contribution due to the continuous-time operation of the integrator is analyzed during one clock period with duration T_s, considering a total capacitance value of ($C+C_f$) and assuming no feedback signal. The step response of the integrator is given by (4.37). The impulse response of the circuit is given by the derivative of the step response, resulting in:

$$h(t) = \begin{cases} \dfrac{1}{R \cdot (C + C_f)} e^{\frac{-t}{R \cdot (C + C_f)}} \approx \dfrac{1}{R \cdot (C + C_f)} & 0 \le t \le T_S \\ 0 & t > T_S \end{cases} \tag{4.58}$$

In this calculation the approximation $e^{\frac{-t}{R \cdot (C + C_f)}} \approx 1$ is used, that gives more than 98 % accuracy in the frequency response comparing to exact value of $h(t)$ (for the components values used in design examples that are presented in the next sections). The transfer function, in the frequency domain, can be obtained by applying the Fourier transform to the previous equation:

$$H(f) = \int_{-\infty}^{\infty} h(t) \cdot e^{-2 \cdot \pi \cdot f \cdot t} dt = \frac{1}{R \cdot (C + C_f)} \cdot \frac{\sin\left(2 \cdot \pi \cdot f \cdot T_S\right)}{\pi \cdot f}. \tag{4.59}$$

The thermal noise power sampled into the capacitor, at the end of a clock period T_s is given by:

$$P_{NT2} = \int_0^{\infty} 4 \cdot k \cdot T \cdot R \cdot \left|H(f)\right|^2 df = 4 \cdot k \cdot T \cdot R \cdot \frac{T_S}{\left[R \cdot (C + C_f)\right]^2} = \frac{4 \cdot k \cdot T \cdot T_S}{R \cdot (C + C_f)^2}. \tag{4.60}$$

The input referred noise of the RC branch is given by:

$$P_{NT2\_input} = \frac{P_{NT2}}{\alpha^2} = \frac{4 \cdot k \cdot T \cdot T_S}{R \cdot (C + C_f)^2 \cdot \alpha^2} = \frac{4 \cdot k \cdot T \cdot \alpha}{(C + C_f) \cdot \alpha^2} = \frac{4 \cdot k \cdot T}{(C + C_f) \cdot \alpha}. \tag{4.61}$$

The total input referred thermal noise power of the integrator is the sum of (4.57) and (4.61). In order to obtain a good performance from the ΣΔM the value of α is typically very small because this allows obtaining good frequency discrimination from the integrator. This means that, in order to reduce the input referred noise it is necessary for capacitor C to have a large capacitance value (similarly to discrete-time integrator). It is important to notice that this is only a minor drawback in terms of area, and that the power dissipation does not increase because, as it is shown in next sections describing ΣΔM design examples, there are no amplifiers in the circuit.

4.7. Jitter Analysis

4.7.1. Passive Continuous-Time Integrator

In a continuous-time ΣΔM (with the loop filters either based on Gm-C or active-*RC* building blocks) the jitter clock causes two types of errors. The first error is due to the sampling of the signal at the input of the quantizer, which can be neglected because it is attenuated by the noise shaping effect of modulator. The second error is caused by the feedback DACs and, since it occurs at the input node, without attenuation, it can significantly limit the modulator's accuracy [61]. Most continuous-time ΣΔMs use rectangular feedback waveforms (Fig. 4.14 a), like non-return-to-zero (NRZ) or return-to-zero (RZ). Fig. 4.14 b) shows a comparison between the continuous-time current-mode DAC waveform and the switched-capacitor DAC waveform. In the case of the switched-capacitor feedback, most of the charge is transferred at the beginning of clock phase so the jitter affecting feedback causes a relatively small charge error and it does not influence significantly the ΣΔM [96]. In the case of a continuous-time DAC waveform, the jitter causes a larger amount of charge error because charge is transferred at a constant rate over the entire clock phase.

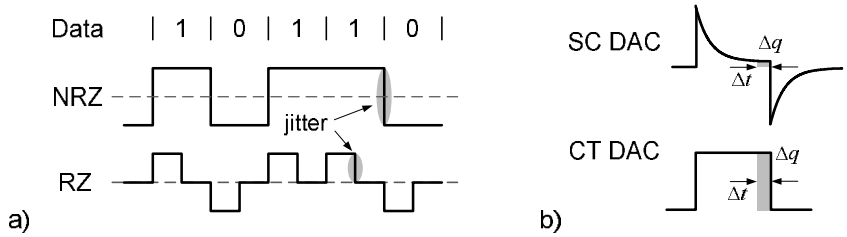

Fig. 4.14 Clock jitter in the feedback of a CT ΣΔM. (a) Simplified waveforms in NRZ and RZ DAC, (b) SC vs. CT DAC waveforms.

In this circuit the effect of the jitter (considering the integrator from Fig. 4.12) can be analyzed using (4.44). This equation shows that the integrator's output is defined by three terms: V_{in}, $V_C[(n\text{-}1)\cdot T_S]$ and D. One can analyze the jitter influence on each of these terms separately. In the third term, the switched-capacitor feedback current (controlled by D) has a characteristic as the one shown in Fig. 4.14 b). Therefore, it is considered to be not affected by jitter noise. The effect of jitter does not depend neither on input signal frequency nor on the input signal amplitude. The reason is that the integrator's output signal is mainly constituted by high frequency noise and it contains multiple frequencies components where an input signal component is only a fraction of it.

The remaining term in (4.44), $V_C[(n\text{-}1)\cdot T_S]$, is affected by jitter noise. During phase Φ_2 when capacitors C and C_f are connected, part of charge (proportional to the capacitor voltage V_C) is removed from C (this operation is independent on feedback charge controlled by D). Any variation in the duration of Φ_2 (due to the jitter timing error Δt) will result in a slight variation in the sampled value of the integrator's output. This means that, jitter noise is transformed into a

voltage error that can be described by adding a timing error Δt to T_S in the second term of (4.44), after zeroing V_{in} and D (where $C_{eq} = C + C_f$):

$$V_C\left(n \cdot T_S\right) = V_C\left[\left(n-1\right) \cdot T_S\right] \cdot \frac{C}{C_{eq}} \cdot \left(1 - \frac{T_S \pm \Delta t}{2 \cdot R \cdot C_{eq}} - \frac{T_S \pm \Delta t}{2 \cdot R \cdot C}\right) \qquad (4.62)$$

$$V_C\left(n \cdot T_S\right) = V_C\left[\left(n-1\right) \cdot T_S\right] \cdot \frac{C}{C_{eq}} \cdot \left(1 - \frac{T_S}{2 \cdot R \cdot C_{eq}} - \frac{T_S}{2 \cdot R \cdot C} \pm \frac{\Delta t}{2 \cdot R \cdot C_{eq}} \pm \frac{\Delta t}{2 \cdot R \cdot C}\right). \qquad (4.63)$$

From this expression it is possible to obtain the voltage error caused by the jitter noise:

$$V_{C\_jitter} \approx V_C\left[\left(n-1\right) \cdot T_S\right] \cdot \frac{C}{C + C_f} \cdot \left(\frac{\pm \Delta t}{2 \cdot R \cdot \left(C + C_f\right)} \pm \frac{\Delta t}{2 \cdot R \cdot C}\right) \qquad (4.64)$$

It is possible to conclude from (4.64) that the jitter influence can be reduced by increasing the RC time constant.

4.7.2. Passive Discrete-Time Integrator

Fig. 4.15 illustrates the RC_1 branch of the integrator and a graph of current flowing through C_1. Usually, typical discrete-time ΣΔMs have low sensitivity to clock jitter because the voltage on the capacitor is settled and moderate changes of clock phase's duration do not result in a significant voltage error (Fig. 4.15b). However keeping in mind that the proposed discrete-time integrator is a switched-capacitor filter using UIS, jitter becomes a significant issue. In this case, similarly to continuous-time ΣΔMs, shorter or longer phase duration causes that the voltage on C_1 can be encumbered with a voltage error (Fig. 4.15a) that depends on the time instant when the switch opens. Hence, the higher F_{clk} is used, the more significant this error can be.

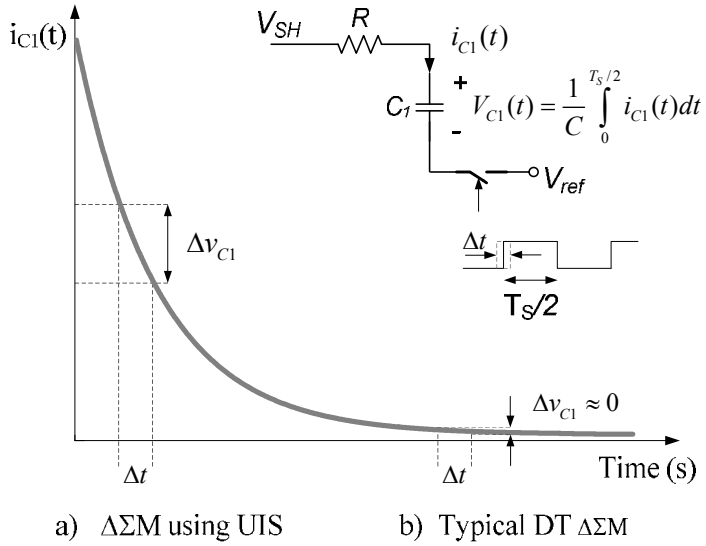

Fig. 4.15 Integrator's capacitor current change vs. jitter.

4.8. Systematic Design Methodology Using Optimization Based on Genetic Algorithm

Due to use of passive integrators and the low gain blocks, the thermal noise contribution of all the building blocks used in a passive ΣΔM have significant weight in overall SNR of the modulator. This means that, the design of passive ΣΔM becomes rather difficult. Therefore, an optimization design methodology taking into account these issues as well as mismatch errors between the circuit's components would be of great use. In this section a general design methodology for ΣΔMs is presented. It is based on a genetic algorithm (GA) and using hybrid cost functions.

The performance of a given ΣΔM can be estimated by using equations derived from its transfer functions based on a linear model of the quantizer. However, these equations are not very accurate in predicting problems such as distortion in the ΣΔM. An alternative is to run a simulation of the ΣΔM including the quantizer, in order to determine more accurately its behavior. This approach is very computation intensive and it requires a long time. Therefore, the adopted solution is a hybrid one. Firstly, the stability and performance of a given ΣΔM is evaluated using equations and only if the performance is acceptable, then an accurate simulation is executed. Moreover, a given ΣΔM is tested by randomly changing its component values using the expected tolerance of the selected technology. This allows verifying if a given design solution is either sensitive or not to component variations.

The presented systematic design methodology is based on a genetic algorithm optimization approach and its design flow is shown in Fig. 4.16. A conceptually similar idea applied to simple analog circuits (e.g., amplifiers and filters) has been presented in [97].

The design flow assumes that a given ΣΔM architecture and its desired specifications are initially provided. The ΣΔM is defined by a chromosome (which is a set of design parameters called genes) containing, among others, values of the R's, C's and V_{ref}'s used in the modulator. These values define the design space, which is limited by maximum and minimum values of each design parameter. Initially, a population consisting of N randomly generated chromosomes is created. Each chromosome (defining a ΣΔM) is evaluated and its fitness is calculated based on the desired specifications. The fitness value is used to sort the chromosomes of the population. The two chromosomes with the highest fitness values pass into new population. The remaining chromosomes of the new population are then created by selecting parents from the old one. Chromosomes with better fitness have higher probability of being chosen as parents. Each "gene" of a new chromosome is defined by randomly selected corresponding "gene" from either parent 1 or 2 (with 50% of probability). Then, the value of this new "gene" is either multiplied or not (with 50% of probability) by a random factor (mutation). This procedure is repeated during a given number of generations. It is important to mention that the value of the mutation factor decreases as the number of generation increases, allowing the algorithm to

converge into a solution.

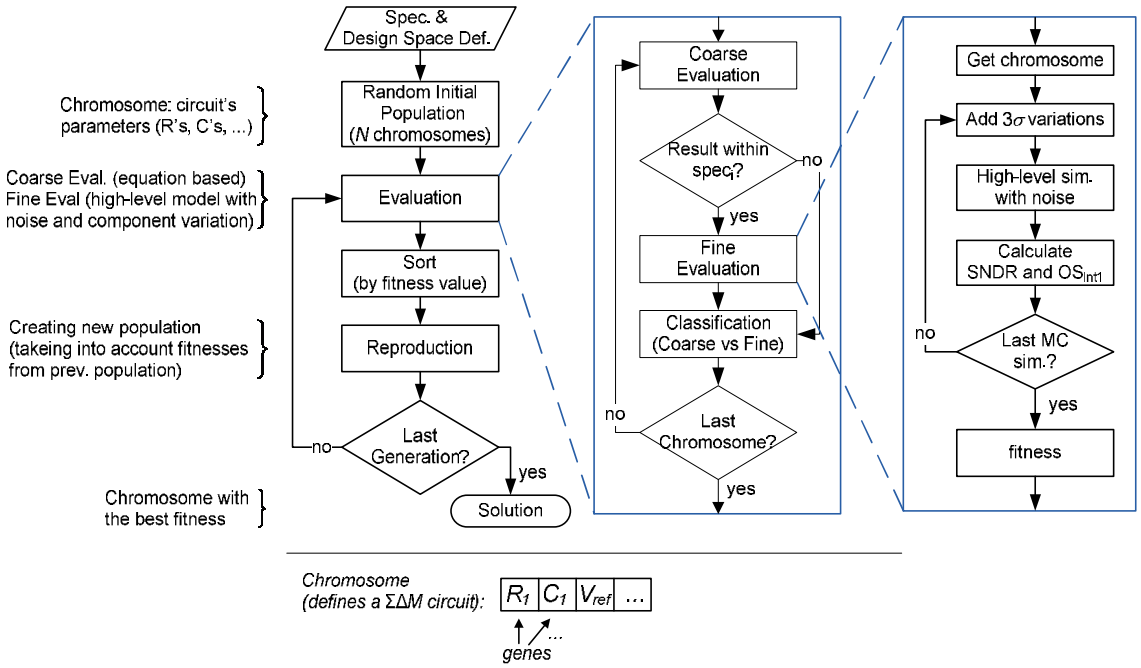

Fig. 4.16 Genetic algorithm optimization flow.

In order to evaluate the fitness of each chromosome (defining a ΣΔM), it is necessary to determine its SNDR and others parameters (e.g. output swing, area, etc.). The existence of the quantizer in the modulator complicates this task. Using a linearized model of ΣΔM it is possible to obtain relatively simple equations that allow predicting its SNDR, however, these equations can introduce significant errors, especially in the case of large input signals. In case of modulators with orders larger than two, it is also difficult to predict modulator's stability. By simulating a behavior model of the modulator that includes the non-linear quantizer it becomes possible to obtain a much more reliable prediction of the SNDR value, however the simulation time is much longer and would result in an unacceptable long optimization time. The adopted solution first performs a coarse evaluation, where equations are used to predict the SNDR value and the potential instability of the ΣΔM. This produces a coarse fitness value and, if this value is larger than a certain threshold value, the ΣΔM undergoes a fine evaluation that allows obtaining better SNDR and stability estimations. Fine evaluation uses a Monte-Carlo (MC) analysis, which runs several simulation of a high level model including ΣΔM's noise sources, where process and mismatch variations are added to chromosome under test. The fitness values of the chromosomes that undergo the fine evaluation are by design always larger than the fitness values of the chromosomes that only undergo coarse evaluation. Total fitness f_T is obtained as the product of M partial fitnesses, f_i, each one depending on i-th specification, s_i, as follows:

$$f_T = \prod_{i=1}^{M} f_i(s_i) \tag{4.65}$$

where the functions $f_i(s_i)$ may assume two forms, depending on the desired target: either maximize or minimize (e.g. maximize the SNDR and minimize the area):

$$f_{i\_\max}(s_i) = 1 - e^{-w_i \cdot (s_i / s_{i\_Des})} \tag{4.66}$$

$$f_{i\_\min}(s_i) = e^{-w_i \cdot (s_i / s_{i\_Des})} \tag{4.67}$$

The s_i and s_{i_Des} represent the achieved and desired specification, respectively. The variable w_i is a weight factor used to prioritize a given partial fitness.

The presented, hybrid, approach performs a more time consuming fine evaluation only on part of the chromosomes which shortens the optimization time. At the end of optimization process, a chromosome with the biggest fitness is the solution of the optimization problem. This allows selecting the design solution that is closest to the desired specification and that is the most insensitive to components variations.

4.9. Summary

In this chapter the active and passive ΣΔM structures have been compared. Equations of approximated processing gain of comparator have been derived as well. It has been demonstrated that both structures have the same behavior (produce the same output for given input signal) and the dead zones of passive ΣΔM are the same as in the case of active ΣΔM (as long as $\beta_P = \beta_A$). The passive ΣΔM's SQNR is mainly defined by the processing gain of the comparator, G_C, and the SNR is limited by thermal noise. Moreover, using an inter-stage gain helps attenuating thermal noises of second integrator and comparator as well as it additionally decreases the quantization noise. Finally, it was shown that an *RC* circuit using UIS can be used to implement a passive integrator.

Moreover, in this chapter there were presented the thermal and jitter noise analyzes of the proposed discrete-time and continuous-time integrators. In both structures, by increasing capacitor value the thermal noise contribution can be reduced. Passive ΣΔMs with the described discrete-time integrator using UIS are sensitive to the jitter because of their RZ DAC (similarly to continuous-time modulators). Susceptibility to jitter noise of the continuous-time integrator can be overcame by increasing the associated *RC* time constants.

In the last section of this chapter it has been described a systematic design methodology for optimization of ΣΔMs based on a genetic algorithm and using hybrid cost functions.

5. EXAMPLES OF PASSIVE AND PASSIVE-ACTIVE ΣΔMS

This chapter presents case studies and design examples of ΣΔM architectures using the previously discussed passive integrators. The case studies here described include 1st-order, 3rd-order single-loop ΣΔMs and cascaded MASH ΣΔMs. The design examples refer to the 2nd-order single-loop ΣΔM and the 2-1 MASH modulator that have been fabricated. The study provided in this chapter includes analyzes of the high level models as well as analyzes of the transistor level implementations of the proposed modulators.

5.1. Case Study: 1st-Order Discrete-Time ΣΔM

5.1.1. Block Diagram and Transfer Functions

The block diagram of the 1st-order ΣΔM is shown in Fig. 5.1. The input signal V_{in} is sampled in the S/H circuit and then it passes to the passive integrator (based on the UIS concept) that is represented by its Z transfer function (derived in Chapter 4.4). The output signal of the integrator enters the comparator that is followed by a D-type flip-flop that produces the output bit-stream D. These two blocks together have a delay of $z^{-1/2}$. The block diagram includes noise sources of the circuit; namely: thermal noise, comparator noise and quantization noise.

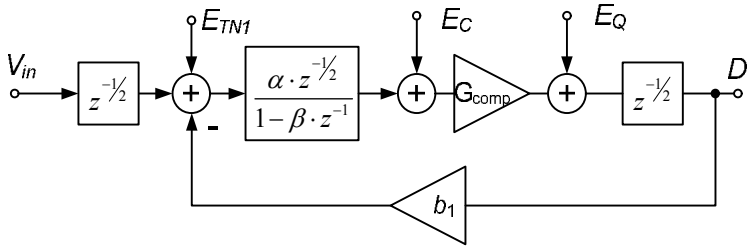

Fig. 5.1 Block diagram of the passive 1st-order ΣΔM.

Fig. 5.2 depicts plots of the STF and the NTFs of the modulator, when the passive ΣΔM is clocked with clock frequency of 100 MHz and with the components values given in Table 5.1. One can notice that, these plots, as well as the equations describing the transfer functions, are consistent with conclusions drawn in Chapter 4.1. The plots of the STF and the NTF_{TN1} show a plateau at the 0 dB level, meaning that E_{TN1} is added directly to V_{in}. The input referred noise voltage of the comparator (E_C) can be critical in a passive ΣΔM because the input voltage of the

comparator has small amplitude. E_C is not attenuated at low frequencies and at high frequencies it is amplified and shaped by the modulator's loop. As expected, the NTF_Q is a high-pass transfer function that, at low frequencies, is significantly attenuated by the comparator gain G_C. The approximated equation for G_C can be obtained from (4.12) showing that its value is inversely proportional to the integrator's α factor, that is given in (4.30). This means that, a small α value results in strong attenuation of the quantization noise E_Q. The equations of the transfer functions together with their values at DC are given below (considering $b_1 = 1$).

$$\mathrm{STF} = \frac{D}{V_{in}} = \frac{G_C \cdot \alpha \cdot z^{-\frac{3}{2}}}{1 + (b_1 \cdot G_C \cdot \alpha - \beta) \cdot z^{-1}}; \qquad \left|\mathrm{STF}(z=1)\right| = \frac{G_C}{G_C + 1} \approx 1 \tag{5.1}$$

$$\mathrm{NTF_C} = \frac{D}{E_C} = \frac{G_C \cdot (1 - \beta \cdot z^{-1}) \cdot z^{-\frac{1}{2}}}{1 + (b_1 \cdot \alpha \cdot G_C - \beta) \cdot z^{-1}}; \qquad \left|\mathrm{NTF_C}(z=1)\right| = \frac{G_C}{G_C + 1} \approx 1 \tag{5.2}$$

$$\mathrm{NTF_Q} = \frac{D}{E_Q} = \frac{(1 - \beta \cdot z^{-1}) \cdot z^{-\frac{1}{2}}}{1 + (b_1 \cdot \alpha \cdot G_C - \beta) \cdot z^{-1}}; \qquad \left|\mathrm{NTF_Q}(z=1)\right| \frac{1}{G_C + 1} \approx \frac{1}{G_C} \tag{5.3}$$

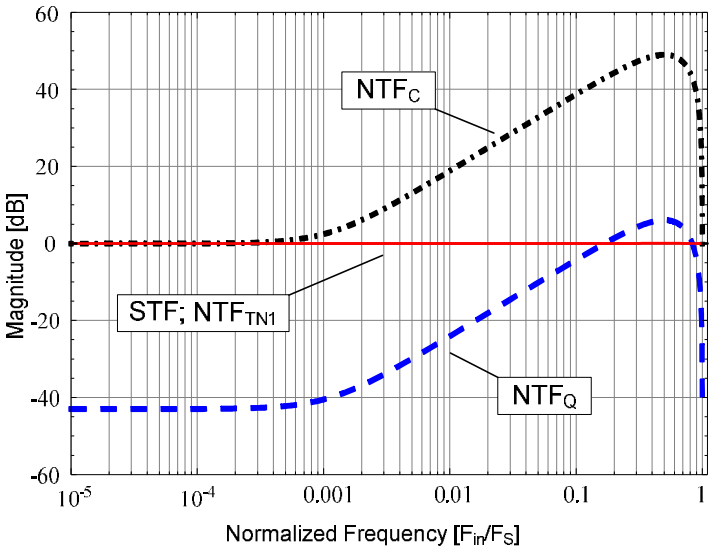

Fig. 5.2 Ideal graphs of STF and NTFs of the 1st-order passive ΣΔM.

5.1.2. Circuit Implementation

In order to verify the UIS concept, two passive ΣΔMs (with F_S = 100 and 300 MHz) were fully designed and simulated at transistor level. The schematic of the differential modulator architecture is shown in Fig. 5.3. The modulator design parameters are summarized in Table 5.1. These parameters result in α equal to 0.0036 (for F_S = 100 MHz) and 0.0028 (for F_S = 300 MHz).

The circuit is clocked with two non-overlapping phases, generated from a NAND based clock generator depicted in Fig. 5.4. The transmission gate equalizes the delay introduced by the input inverter. The internal inverters (marked with stars) are used to define the non-overlapping time between two phases.

Table 5.1 The 1st-order passive ΣΔM design parameters.

Parameter	F_S	C_{SH}	R	C_1	$V_{ref}+$; $V_{ref}-$	α
Value	100 MHz	10 pF	140 kΩ	10 pF	1.1; 0 [V]	0.0036
	300 MHz	10 pF	60 kΩ	10 pF	0.85; 0.25 [V]	0.0028

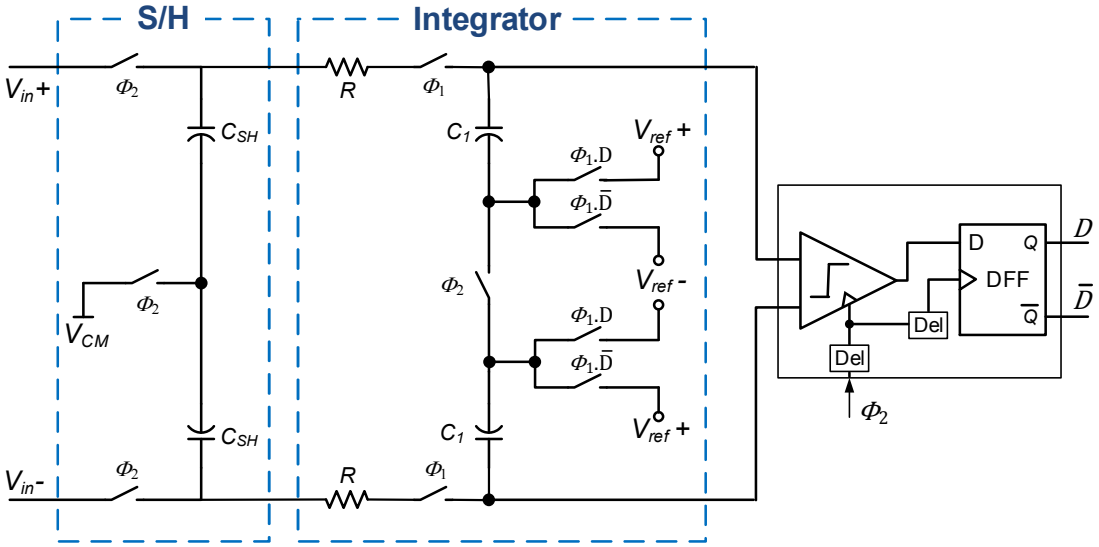

Fig. 5.3 Complete schematic of the passive 1st-order ΣΔM modulator circuit.

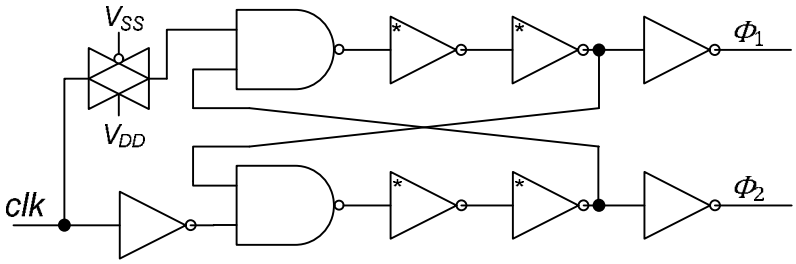

Fig. 5.4 Generator of two non-overlapping phases.

The switches in the signal path require a larger input swing range than the one that could be provided by a transmission gate. Therefore, in this approach, they are designed as clock bootstrapped NMOS switches (Fig. 5.5). When the switch is ON, the transistor gate voltage is set to the level of $V_{DD}+V_{SW\_IN}$, where V_{SW_IN} is the voltage at the input of the switch. In other words, during the ON state the V_{GS} voltage of the NMOS switch is close to V_{DD} regardless of V_{SW_IN}. Therefore, the switch maintains good resistance linearity. This is done by charging a MOS capacitor (that is inside the bootstrapping circuit) during the off period. The drawback of this method is the added complexity to the circuit, reduced NMOS switch life-time due to

higher V_{GS} voltage and higher power consumption. The advantage is an improved, when comparing to transmission gate, input swing range and switch linearity. The feedback switches are realized by simple PMOS and NMOS transistors because $V_{ref}+$ and $V_{ref}-$ values are close to V_{DD} and V_{SS}, respectively. The signals controlling feedback switches are obtained using AND gates. The middle switch of the integrator and the switch connected to V_{CM} (common-mode voltage equal to $V_{DD}/2$) are transmission gates formed by pairs of transistors (NMOS and PMOS), where the PMOS are sized four times wider than the NMOS. This allows obtaining similar ON-resistance of both transistors.

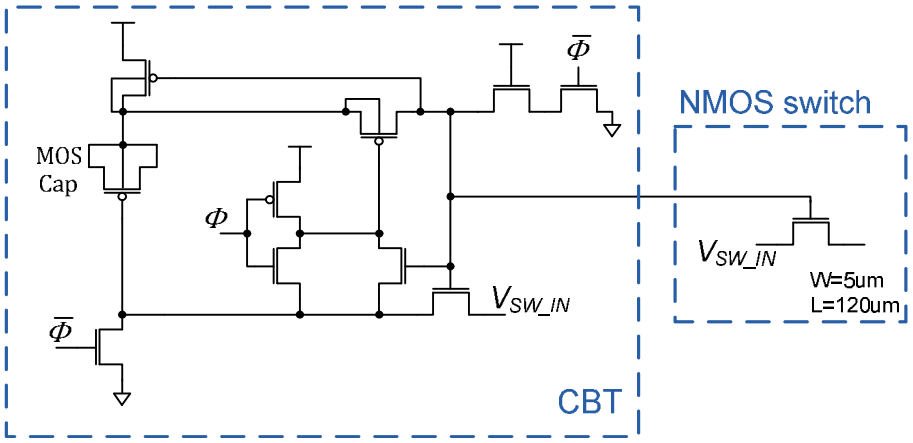

Fig. 5.5 Clock bootstrapped NMOS switches.

As described in the previous sections, the output signal of the passive integrator is considerably attenuated. It is connected to the comparator (depicted in Fig. 5.6), that must amplify a small amplitude signal into a digital level (V_{DD} or 0 V) and, therefore, it should have a large gain. This is achieved by employing positive-feedback (a back-to-back inverter connection) in the comparator. This structure is based on the sense amplifier of [98]. The comparator and the D-type flip-flop were designed to minimize the risk of meta-stability. These two circuits guaranty that after half clock cycle (one phase duration) the output is always a clear logic level.

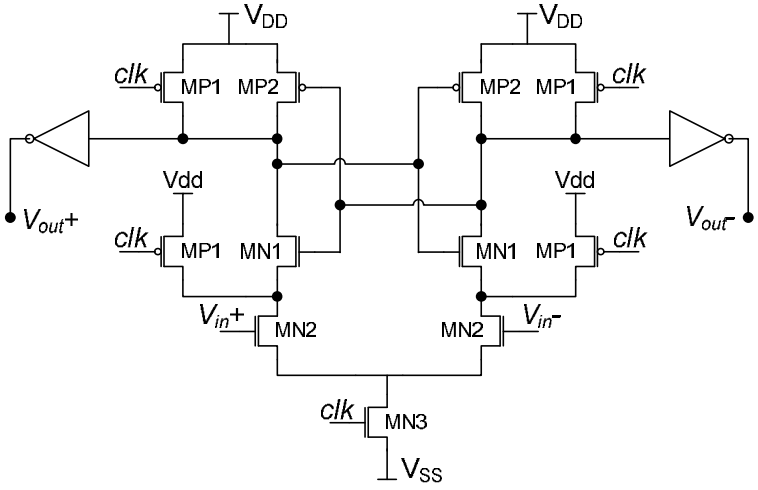

Fig. 5.6 Electrical schematic of the comparator [98].

5.1.3. Electrical Simulations

Both passive ΣΔMs, with F_S = 100 MHz and F_S = 300 MHz, were simulated by applying input sine wave signals with frequencies of 40 kHz and 46 kHz, respectively, and performing exhaustive electrical transient-noise simulations. The power spectral density of the output signals for an input signal with amplitude of 600 $mV_{pp,diff}$, are shown in Fig. 5.7. One can notice that, the circuits achieve 20 dB/decade noise shaping. Table 5.2 summarizes the circuits' performance parameters, for an input signal with 600 $mV_{pp,diff}$ amplitude.

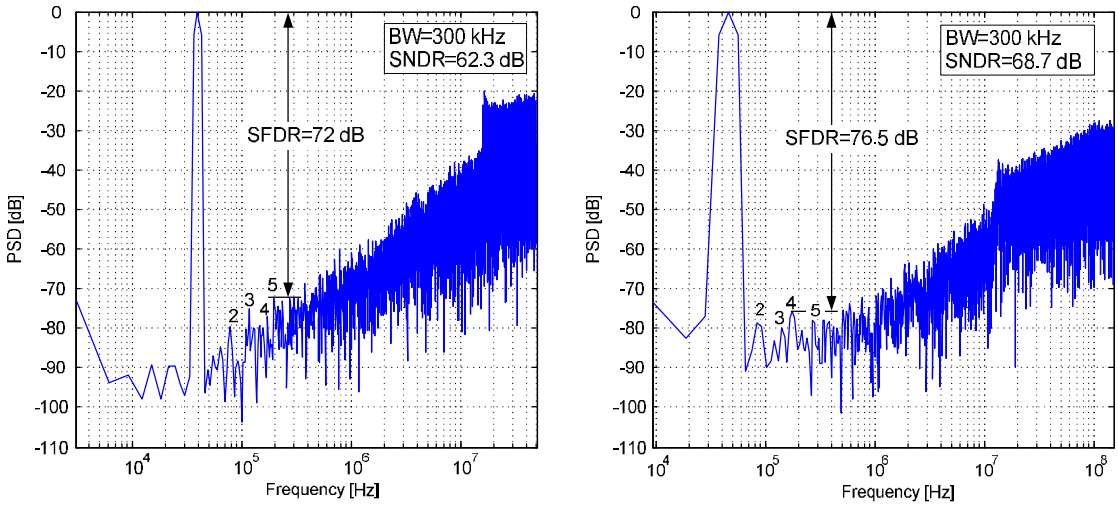

Fig. 5.7 2^{15} point PSD of the 1st-order ΣΔM for F_S = 100 MHz, F_S = 300 MHz.

Table 5.2 Simulated key performance parameters of the 1st-order ΣΔMs.

Tech. [µm]	V_{suply} [V]	F_S [MHz]	BW [kHz]	SNR [dB]	SNDR [dB]	THD [dB]	P_C [µW]	FoM_W [fJ/ conv.-step]
0.13-CMOS	1.1	100	300	63	62.3	-69	114	196.7
		300	300	71.6	68.7	-71.9	232	191

5.1.4. Case Study Summary

This section presented the case study of the 1st-order ΣΔM circuit with the discrete-time passive integrator using UIS. This approach, based on analysis provided in previous chapters, allowed building a ΣΔM with dynamic elements thus reducing the power dissipation. The electrical simulations confirmed validity of using the UIS concept in ΣΔMs.

5.2. Design Example #1: 2nd-Order Discrete-Time ΣΔM

In this section, the design example of the 2nd-order ΣΔM is described and analyzed. This circuit has been physically fabricated and its measured results are presented in Chapter 6.

5.2.1. Block Diagram and Transfer Functions

The linear model of the 2nd-order ΣΔM is shown in Fig. 5.8, where the two passive integrators are represented by their *Z* transfer functions that have been derived in Chapter 4.4. The input signal V_{in} is sampled by the S/H circuit and then it passes through the 1st integrator, the inter-stage gain *G* and, finally, it drives the 2nd integrator. The passive integrators are based on the UIS concept. Next, the signal is applied to the comparator that is followed by a D-type flip-flop (DFF) producing an output bit-stream *D*. The block diagram in Fig. 5.8 includes the main noise sources of the circuit; namely: thermal noises, comparator noise and quantization noise. Fig. 5.9 shows the plots of the STF and of the NTFs of the modulator, whose components values are given in Table 5.3. The plots of transfer functions are consistent with the conclusions drawn in Chapter 4.1, as well as with the conclusions derived from the analysis of the 1st-order ΣΔM presented in the previous section. In 2nd-order ΣΔM, the second feedback factor can be adjusted (lowered) resulting in higher comparator processing gain G_C than in case of 1st-order ΣΔM. This allows for stronger quantization noise attenuation. One can notice that, the inter-stage gain, *G*, additionally decreases (besides *Gc*) the quantization noise and it helps attenuating the thermal noise of both, the second integrator and of the comparator.

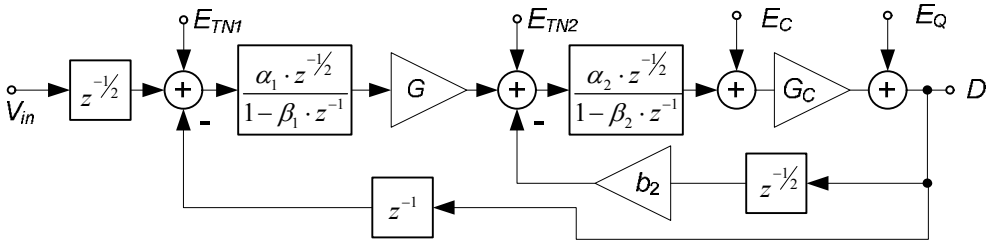

Fig. 5.8 Linear model of the proposed ΣΔM based on UIS

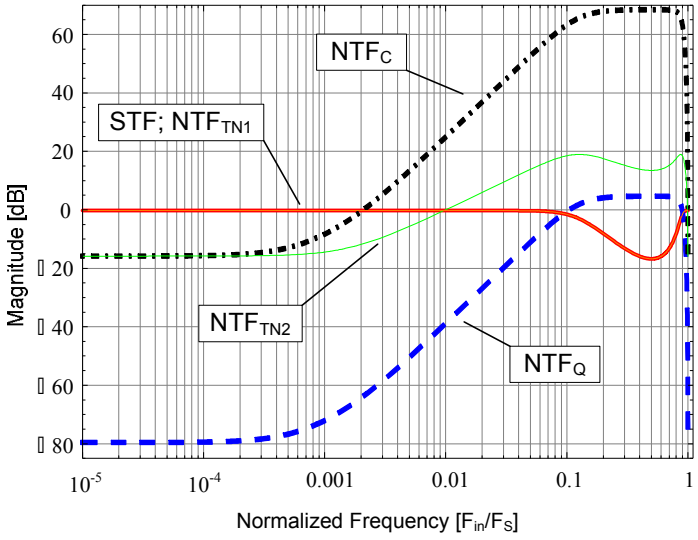

Fig. 5.9 Ideal graphs of STF and NTFs of the 2nd-order passive ΣΔM.

In order to understand the sensitivity of the modulator to the variation of its coefficients with process and temperature, a 500-case Monte-Carlo (MC) analysis was performed (Fig. 5.10). The simulation used a high level model of the modulator, based on the block diagram of Fig. 5.8. It resulted in a mean SNDR value of 76 dB with a standard deviation of 2.2 dB. In each run, the values of the resistances, capacitances and transconductance were randomly changed using a Gaussian variable with a 3σ value of 20 %. High level simulations were also used to determine the influence of the jitter noise of the clock in the performance of the modulator. These simulations showed that there is no degradation of the SNDR for jitter noise values smaller than 10 ps *rms*.

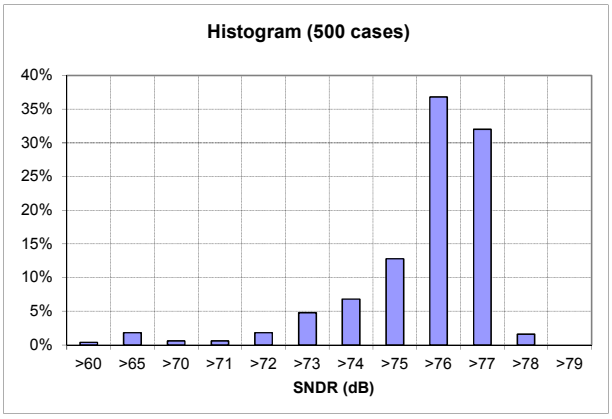

Fig. 5.10 Histogram of the SNDR obtained through 500-case MC analysis of 2nd-order ΣΔM.

5.2.2. Circuit Implementation

The complete schematic of the differential 2nd-order ΣΔM is shown in Fig. 5.11. The component values and gain coefficients are shown in Table 5.3.

The clock phases are generated by the circuit presented in Fig. 5.4 and the employed comparator is depicted in Fig. 5.6. The switches in the signal path are the clock bootstrapped NMOS switches shown in Fig. 5.5. These blocks are described in section 5.1.2. The feedback switches of the first integrator are simply realized by PMOS and NMOS transistors because V_{ref1}+ and V_{ref1}- values are close to V_{DD} and V_{SS}, respectively. The feedback switches of the second integrator, the middle switches of both integrator and the switch connected to V_{CM} (common-mode voltage equal to $V_{DD}/2$) are transmission gates formed by pairs of transistors (NMOS and PMOS), where the PMOS is sized four times wider than the NMOS. This allows obtaining similar ON-resistance of both types of transistors. Signals controlling feedback switches are obtained with use of AND gates.

A ΣΔM can be built using the passive *RC* integrator as shown in the previously described case study. This is straightforward in the case of a 1st-order ΣΔM; however in case of a higher order modulator, it is necessary to cascade, at least, two passive integrators. When the capacitor in the

2nd integrator samples the voltage of the capacitor in the 1st integrator, partial charge redistribution between the two capacitors occurs, changing the voltage in the first capacitor. This problem is solved by using a simple gain stage in order to isolate the two integrators. Moreover, as previously explained, an inter-stage gain helps attenuating the thermal noise of the second integrator and of the comparator as well as additionally decreases (with Gc) the quantization noise. This block is implemented as a differential pair loaded by resistors R_2 and its gain is determined by $G=gm\cdot R_2$ where gm is the transconductance of the differential pair. The resistance R_2 is also a part of the RC time constant of the 2nd integrator that determines the value of α_2. The bias current of this gain circuit, I_{buff}, has a small value (8 µA), because its resistors are large in order to achieve the UIS condition.

As described in section 4.2 the equivalent comparator's gain is approximated as $G_C=1/(\alpha_2\cdot b_2)$. This requires $\alpha_2<<1$ and $b_2<1$ to increase this gain and, consequently, the quantization noise is suppressed. The output voltage of the 1st integrator is mainly composed by the high frequency E_Q signal and the V_{in} component is only a fraction of this voltage because the first feedback cancels a significant part of V_{in}. The 1st integrator has to provide attenuation ($\sim G/b_2$) to guaranty that output amplitude of block G is smaller than the feedback voltage of the 2nd integrator (to avoid saturation). Moreover, the distortion added to V_{in} by G (a differential pair) is reduced due to the small value of V_{in} in the output signal of the 1st integrator.

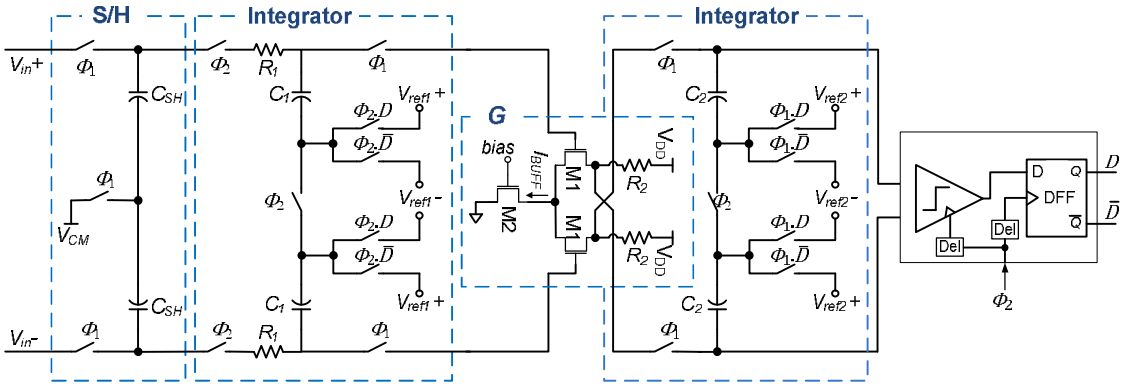

Fig. 5.11 Complete schematic of the ΣΔM including clocking circuitry

Table 5.3 Passive component values and gain coefficients.

Parameter	C_{SH}	R_1	R_2	C_1	C_2	G	$V_{ref1}+$; $V_{ref1}-$	$V_{ref2}+$; $V_{ref2}-$
Value	7 pF	140 kΩ	140 kΩ	3.5 pF	10 pF	6	1.2; 0 [V]	0.66; 0.44 [V]
Parameter	α_1	α_2	b_2					
Value	0.01	0.0036	0.22					

5.2.3. Electrical Simulations

The 2nd-order ΣΔM, with F_S = 100 MHz, has been simulated by applying input sine wave signals with frequency of 61 kHz and performing exhaustive electrical transient-noise simulations. The power spectral density of the output signal for an input signal with amplitude of 600 $mV_{pp,diff}$ is

shown in Fig. 5.12. One can notice that, the circuit achieves 40 dB/decade noise shaping. Table 5.4 summarizes the 2nd-order ΣΔM's performance parameters, for an input signal with 600 $mV_{pp,diff}$ amplitude.

Table 5.4 Simulated key performance parameters of the 2nd-order ΣΔM.

Tech. [µm]	V_{suply} [V]	F_S [MHz]	BW [kHz]	SNR [dB]	SNDR [dB]	P_C [µW]	FoM_W [fJ/ conv.-step]
0.13-CMOS	1.2	100	300	78.6	74	220	90

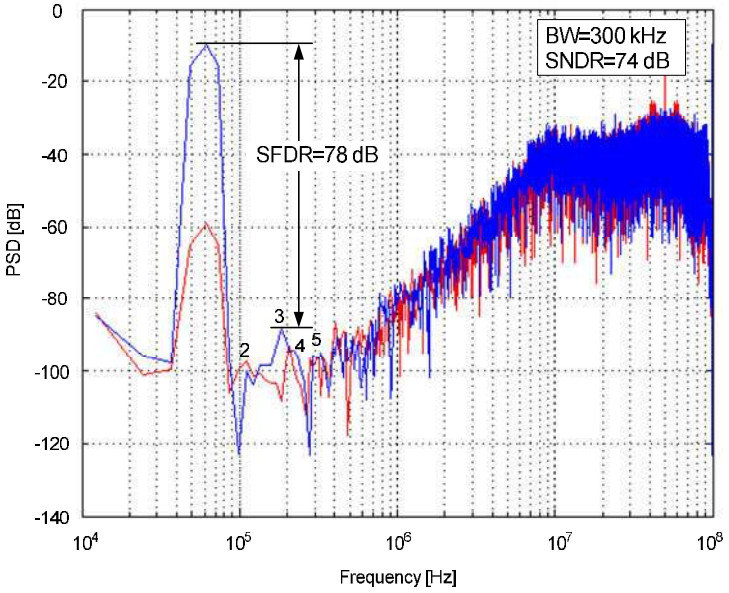

Fig. 5.12 PSD with 2^{13} point of the output bit-stream of the ΣΔM, obtained by electrical transient noise simulation of the complete circuit, for 2 $mV_{pp,diff}$ and 600 $mV_{pp,diff}$ amplitudes of the input signal.

5.2.4. Design Example Summary

This section presented the design example of 2nd-order ΣΔM with the discrete-time passive integrators using UIS. This circuit was designed in a 130 nm CMOS technology and is has been decided to send it to fabrication in order to prove of the UIS concept (its measured results are presented in Chapter 6). In the next section there are presented case studies of higher order ΣΔMs.

5.3. Case Studies of Higher Order Architectures of ΣΔMs

This section discusses several higher order ΣΔM architectures that were studied and subjected to the genetic algorithm based optimization process in order to explore their potential for achieving high performance. The presented architectures are: single-loop 3rd-order ΣΔM, SMASH and MASH modulators.

The optimization methodology used in testing the ΣΔMs is described in Chapter 4.8. It is an

iterative procedure based on the genetic algorithm (GA) using hybrid cost functions. Referring to Fig. 4.16 the list of specifications comprises the sampling frequency, F_S, the modulator bandwidth (BW) and desired value of the SNDR that defines the fitness f_T. The first stage of the optimization is a coarse evaluation, in which, stability condition is checked. The coarse SNDR is calculated with use of the following noise powers: P_Q - quantization, P_{TN} – thermal and P_C – comparator (in case of cascaded structures the first stage SNDR is calculated):

$$P_Q = \frac{2 \cdot \Delta^2}{12 \cdot F_S} \int_0^{BW} \left| NTF_Q(F) \right|^2 dF \tag{5.4}$$

$$P_{TNi} = \frac{2 \cdot k \cdot T}{C_i \cdot \alpha_i \cdot F_S} \int_0^{BW} \left| NTF_{TNi}(F) \right|^2 dF \tag{5.5}$$

$$P_C = \frac{2 \cdot \sigma_C^{\,2}}{F_S} \int_0^{BW} \left| NTF_C(F) \right|^2 dF \tag{5.6}$$

where σ_c=140·10^{-6} μV is the input referred noise of the comparator was obtained from an electrical transient noise simulation of this circuit (Fig. 5.6).

Next, the obtained value of the SNDR is used to calculate f_T from (4.66). When the modulator is stable and the resulting f_T is sufficient (given value, in this case corresponding to SNDR = 60 dB) the fine evaluation is performed using the high level model of the ΣΔM to calculate the SNDR of the circuit, for a given set of design variables (*R*'s, *C*'s, *G*'s …). This model includes the behavior of the comparator and, therefore, the impact of this component in the circuit's linearity is included in the optimization procedure. The high level model also includes the thermal noise sources of the circuit, and consequently, it explores the trade-offs between noise and linearity. Only the non-linear behavior of the differential pair is not included. This limitation is addressed, by imposing a limit for the output voltage swing of the first integrator (this will be further explained during the analysis of the 3rd-order ΣΔM), forcing the algorithm to select only the design solutions that have the output swing of input of the first gain block smaller than a given value (e.g. 80 $mV_{pp,diff}$ if the *G* of the gain block is ~20 dB). The final design solution is the one achieving the best SNDR. This procedure was applied to different ΣΔM architectures under study in order to determine the one with the best potential for implementing a high performance ΣΔM based on UIS.

5.3.1. Third-Order ΣΔM

The first architecture to be explored is a 3rd-order multi feedback and feed-forward ΣΔM. Its conceptual block diagram is illustrated in Fig. 5.13, where each feedback and feed-forward includes a separate coefficient. The feed-forward paths are difficult to implement due to the large signal amplitude difference between the different nodes of the circuit (e.g. V_{in} = 600 $mV_{pp,diff}$ while $V_{Int2\_out} \approx$ 40 $mV_{pp,diff}$). For the same reason, the feedback paths marked in red

would require additional gain blocks. Due to this, architectures with these additional feedback and fee-forward paths are automatically rejected by the optimizer.

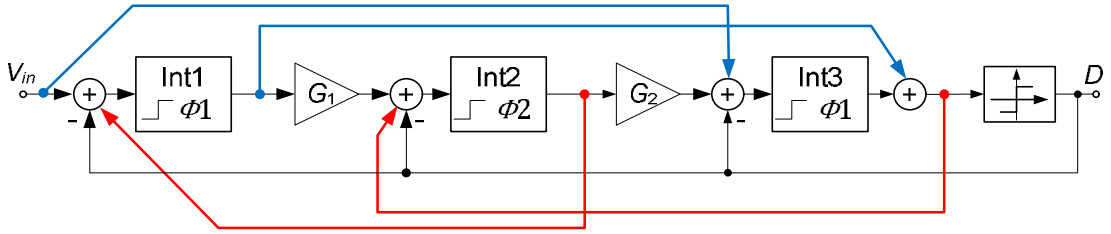

Fig. 5.13 A 3rd-order multi feedback and feed-forward ΣΔM

The block diagram of the selected architecture of the 3rd-order ΣΔM is depicted in Fig. 5.14. Its simplified single-ended schematic is presented in Fig. 5.15. The adjacent integrators are separated by two gain stages G_1 and G_2 (implemented as a differential pair circuit loaded by resistors R_2 and R_3, respectively). The comparator, with zero threshold voltage, amplifies the small amplitude signal at the output of the third integrator into a digital level (1.1 V or 0 V). The comparator is followed by a D-type flip-flop (DFF), producing the output bit stream D.

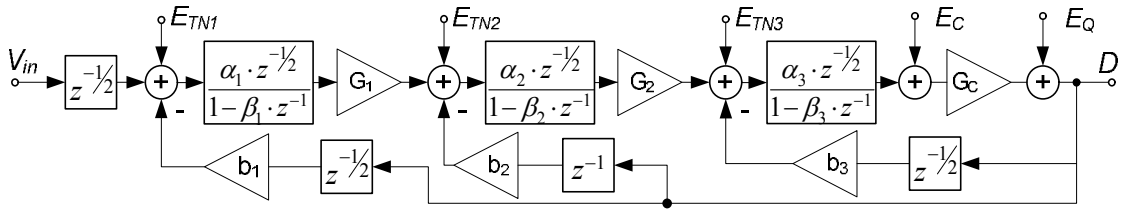

Fig. 5.14 A block diagram of the 3rd-order ΣΔM.

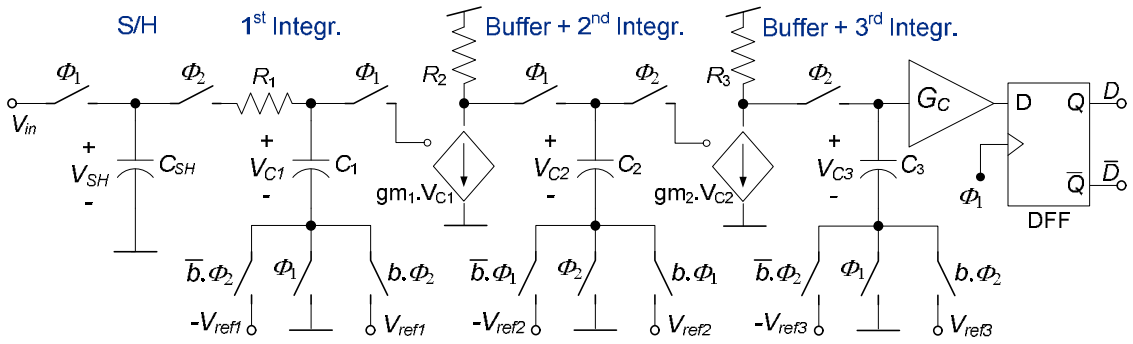

Fig. 5.15 A simplified single-ended version of the 3rd-order ΣΔM circuit.

The modulator was first optimized to work with F_S = 100 MHz. Then the circuit sized with the parameters obtained from optimization parameters was subjected to electrical simulations. Results from the optimizer and from the electrical transient simulations are shown in Table 5.5. One can notice that, in the case of the electrical transient simulation with the transistor level gain blocks, the SNDR is strongly reduced by the distortion introduced by this gain circuits, causing appearance of high harmonics. It was observed that the first gain block G_1 (a simple differential pair) introduces significant distortion because of its nonlinear gain characteristic.

Although, the 1st integrator's output signal is mainly composed by the high frequency E_Q signal because the first feedback b_1 cancels a significant part of V_{in} at its input (thus reducing distortion added to by G_1), the amplitude of the input signal of G_1 should be limited or otherwise, the distortion can become the dominant factor limiting circuit's SNDR. As mentioned before, to overcome this issue, the output swing of the first integrator's signal has to be limited. This condition implies that the other gain blocks G_2 and G_3 will not introduce distortion once their input signals are additionally attenuated by the other passive integrators.

Table 5.5 Simulated key performance parameters of the 3rd-order ΣΔM (F_S = 100 MHz).

Simulation	F_S [MHz]	BW [MHz]	SNDR [dB]	SNR [dB]	THD [dB]
GA optimization – high level	100	0.7	**75.5**	76.3	-83
Electrical sim. - ideal components			**75**	76.5	-85
Electrical sim. - real gain blocks			**55.6**	76.3	-55.6

The previous study and analysis have shown that 1st, 2nd and 3rd-order ΣΔM architectures using passive and passive-active structures are capable to achieve moderate resolution (62 dB < SNDR ≤ 74 dB). If the nonlinearity of the gain stages is properly addressed, the circuit's SNDR is mainly limited by the thermal noise. This noise contribution can be lowered by increasing size of the capacitances in the integrators or by increasing OSR. However, very big capacitances would lead to a large active area of the fabricated circuit, while an increase of the OSR could be realized by decreasing bandwidth or increasing F_S (that would increase the power consumption). These constraints define the most suitable resolution and bandwidth application for the passive-active ΣΔM structure. Therefore, it was decided to design a moderate resolution (62 dB < SNDR ≤ 74 dB) ΣΔM for a medium signal bandwidth (5 MHz < BW ≤ 20 MHz), which occupies small active area. Due to the available technology (CMOS 65 nm) and in order to minimize the risk of comparator metastability, it was decided that the maximum acceptable value of the clock frequency would be 1 GHz.

Considering the new requirements, the next optimizations have been carried out on the architectures of 2nd and 3rd-order ΣΔMs working with F_S = 1 GHz. During the preliminary analysis a signal bandwidth of 10 MHz and a SNDR larger than 70 dB have been targeted. As mentioned before, an additional limitation of the 1st gain block input amplitude was included into the procedure of the fine evaluation. The resulting performance is presented in Table 5.6. One can notice that, the improvement of the SNDR in the 3rd-order ΣΔM structure over the 2nd-order one is not significant. This is because, the output swing amplitudes of the 2nd and 3rd integrators are small in order to keep the loop stable. That makes their thermal noise contribution more significant. Moreover, taking into consideration the possible instability issues of the 3rd-order structure, it was decided to adopt this architecture. Furthermore, the 2nd-order structure was also not selected because of its insufficient SNDR value.

Table 5.6 GA optimization results of the 3rd-order ΣΔM (F_S = 1 GHz).

Type of ΣΔM	F_S [GHz]	BW [MHz]	SNDR [dB]	SNR [dB]	THD [dB]
2nd-order	1	10	**64**	64	-83.6
3rd-order			**67**	68	-80

5.3.2. SMASH ΣΔM

The next architecture of ΣΔM to be studied is the SMASH. It has the advantage of cascading two stages ΣΔMs without requiring digital cancellation logic. Therefore, contrary to MASH structure, it does not have the problem of mismatch between analog (the ΣΔM stages) and digital (the digital cancellation logic) transfer functions that can degrade the modulator's performance. The SMASH circuit is less sensitive to non-idealities like finite op-amp and variations of modulator's coefficients. The 4th order SMASH ΣΔM is shown Fig. 5.16. The output signal D_{SMASH} is obtained from direct subtraction of outputs D_1 and D_2. In order for the SMASH architecture to work properly, the input signal of the 2nd stage has to be the quantization noise of the 1st stage, E_{Q1}. It can be relatively easy extracted by a subtracting block when a comparator's gain is close to unity. In case of the passive ΣΔM, the comparator gain is much larger than unity, meaning that the comparator's input signal amplitude (~30 $mV_{pp,diff}$) is much smaller in comparison to its output (~V_{DD}). Therefore, it is difficult to extract the E_{Q1} and consequently obtain a proper quantization noise, E_{Q1}, cancellation, due to large G_{C1}. During various attempts the genetic algorithm optimization procedure could not converge to obtain a valid design solution able to correctly cancel E_{Q1}. Therefore, it was concluded that the SMASH architecture could not be implemented using passive ΣΔMs.

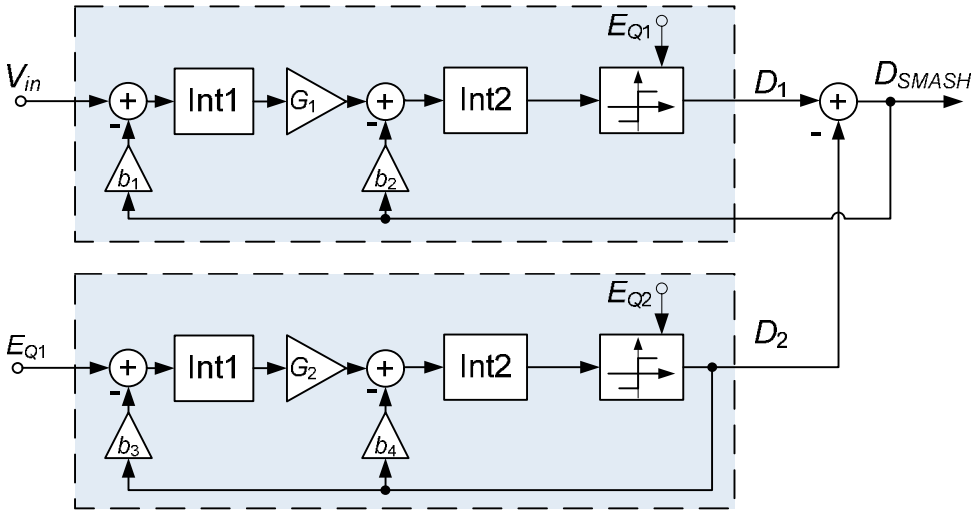

Fig. 5.16 A 4th order SMASH ΣΔM.

5.3.3. MASH ΣΔM

Fig. 5.17 presents the 4th order MASH modulator built using two 2nd-order ΣΔMs. The advantage of the MASH architecture is that it allows obtaining stable modulator operation with higher order noise shaping and it allows cancelling the 1st stage quantization noise, E_{Q1}. Moreover, E_{Q1} does not need to be an input signal of the 2nd MASH stage. It is possible to apply the input of the 1st stage comparator to the input of the 2nd stage ΣΔM. In this architecture it is necessary to use digital cancellation logic. The 2+2 MASH modulator, depicted in Fig. 5.17, clocked at F_S = 1 GHz was subjected to the genetic algorithm optimization process.

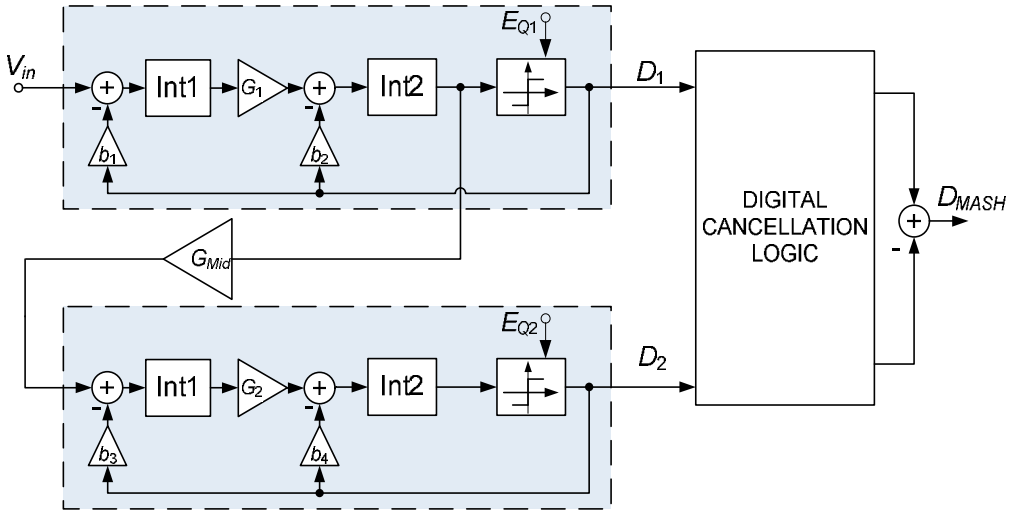

Fig. 5.17 A 4th order MASH ΣΔM.

The results of this optimization, together with the results of the previously presented architectures, are depicted in Table 5.7. This table also shows results of the 2–1 MASH structure, that achieves the same performance as 2+2 MASH modulator. This is because, in case of 2+2 MASH structure, the thermal noise contribution of the 2nd stage becomes more significant (due to low amplitudes of its integrators' output signals) and it cancels the advantage of adding an additional order. This could be circumvent by using very high G_{Mid} (e.g. ~100) that would increase the 2nd stage input amplitude but the feasible value of G_{Mid} is from ~10 to ~15 (for a gain block consisting a differential pair loaded by resistors). Moreover, the 2–1 MASH architecture requires simpler digital cancellation logic than the 2+2 MASH.

Table 5.7 GA optimization results of four ΣΔM architectures clocked at F_S = 1 GHz.

Type of ΣΔM	F_S [GHz]	BW [MHz]	SNDR [dB]	SNR [dB]	THD [dB]
2nd-order	1	10	64	64	-83.6
3rd-order			67	68	-80
MASH 2+2			77	77.6	-86.4
MASH 2–1			77	77.8	-86

5.3.4. Case Studies Summary

The analysis of different higher order ΣΔM topologies, supported by the design methodology based on optimization, revealed that the passive-active modulator structure is suitable for moderate resolutions (62 dB < SNDR ≤ 74 dB) and medium signal bandwidths (5 MHz < BW ≤ 20 MHz) applications. Therefore, it was decided to design a ΣΔM achieving SNDR larger than 70 dB for a signal bandwidth of 10 MHz that occupies small active area. The genetic algorithm optimization results presented in Table 5.7, shows that the 2–1 MASH modulator achieves the best performance over 10 MHz signal bandwidth. Therefore, the next section will describe, as a design example, the implementation and the practical realization of this architecture.

5.4. Design Example #2: Continuous-Time 2-1 MASH ΣΔM

The goal of the ΣΔM design presented in this section is to achieve SNDR > 70 dB in a signal bandwidth of 10 MHz. The MASH architecture was chosen as the most promising for this purpose, as pointed out in the previous section. The technique used in case of passive ΣΔMs requires higher clock frequencies than other techniques used to design ΣΔMs. This means that, if the signal bandwidth is increased, the clock frequency has to increase in order to maintain the circuit's peak SNDR.

Section 4.5 presented the implementation of the continuous-time passive integrator using UIS. The advantage of the continuous-time structure over the discrete-time is a lack of switches in the signal path. These switches can introduce distortion (due to the variation of ON resistance) and require power hungry bootstrapping circuitry to partially reduce their nonlinearity. When the clock frequency increases, these switches have to increase in size, and their associated parasitic capacitance become larger, resulting in the appearance of second-order effects in the passive integrator circuit. The large switches also result in increased clock feed-through and charge injection that can degrade the common-mode voltage of the circuit and provide additional distortion. Therefore, the continuous-time integrator structure has been adopted to build a cascaded 2-1 MASH ΣΔM.

5.4.1. Block Diagram and Transfer Functions

The block diagram of the continuous-time 3rd-order 2-1 MASH ΣΔM is presented in Fig. 5.18. It consists of two stages: a 2nd-order and a 1st-order ΣΔMs and of the digital cancellation logic (DCL) that combines the outputs of both stages (D_1 and D_2) to cancel E_{Q1} and shape E_{Q2} by NTF_{Q1}. Signal V_{int2} is the input signal of the comparator in the first stage ΣΔM (2nd-order) that is amplified by G_{Mid} and applied to input of the second stage ΣΔM. The block diagrams of the 1st and the 2nd MASH stages are depicted in Fig. 5.19 and Fig. 5.20, respectively. In these diagrams each integrator is represented by its equivalent Z transfer function $H_i(z)=\alpha_i/(1-\beta_i \cdot z^{-1})$ that was derived previously in Chapter 4.5. Coefficients b_1, b_2 and b_3 denote feedback coefficients. They are obtained using the factor γ from (4.45) and (4.41) and dividing it by α. They can be approximated as:

$$b_1 \approx \frac{V_{ref1,2}}{\alpha_1} \cdot \frac{C_{f1}}{C_1 + C_{f1}}; \qquad b_2 \approx \frac{V_{ref1,2}}{\alpha_2} \cdot \frac{C_{f2}}{C_2 + C_{f2}}; \qquad b_3 \approx \frac{V_{ref3}}{\alpha_3} \cdot \frac{C_{f3}}{C_3 + C_{f3}} \tag{5.7}$$

where $V_{ref1,2}$ is the reference voltage applied to the 1st and 2nd integrators and V_{ref3} is the reference voltage applied to the 3rd integrator. The gains of the comparators G_{C1} and G_{C2} can be approximated as $G_{C1}=1/(\alpha_2 \cdot b_2)$ and $G_{C2}=1/(\alpha_3 \cdot b_3)$.

Blocks G and G_{Mid} separate adjacent integrators in order to prevent loading effect and provide gain (~20 dB). Next, in each MASH stage a single-bit quantizer (comparator) is used, followed by a D-type flip-flop. These two blocks together have a delay of z^{-1}. The component values, α_i factors, comparators' gains and feedback factors are shown in Table 5.8. The block diagram from Fig. 5.19 and Fig. 5.20 include the noise sources of the circuits, namely: thermal noise, comparator noise and quantization noise.

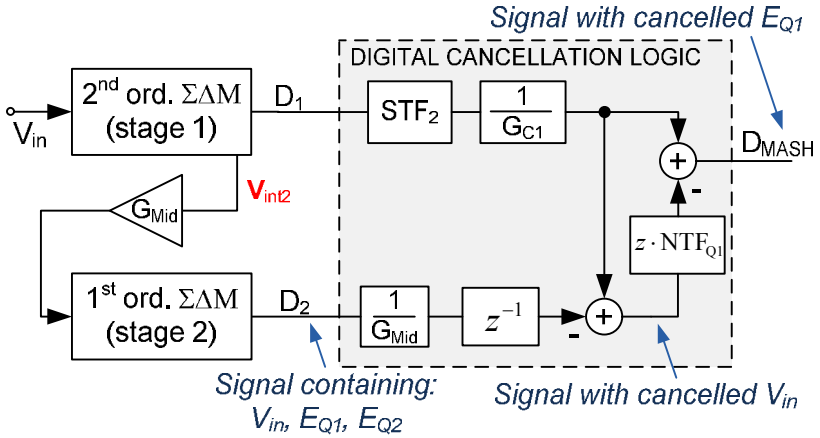

Fig. 5.18 Block diagram of the proposed 2-1 MASH ΣΔM.

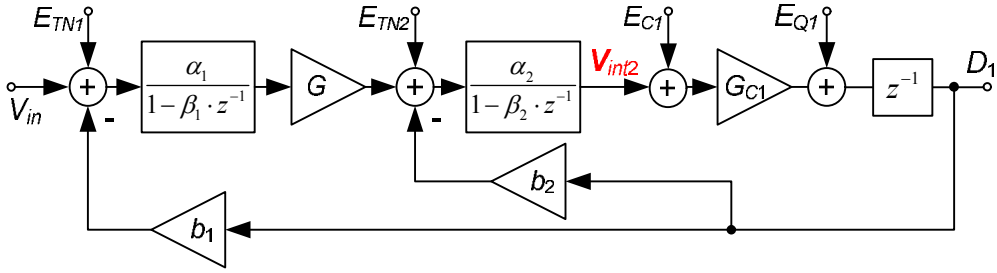

Fig. 5.19 Block diagram of the proposed first stage ΣΔM.

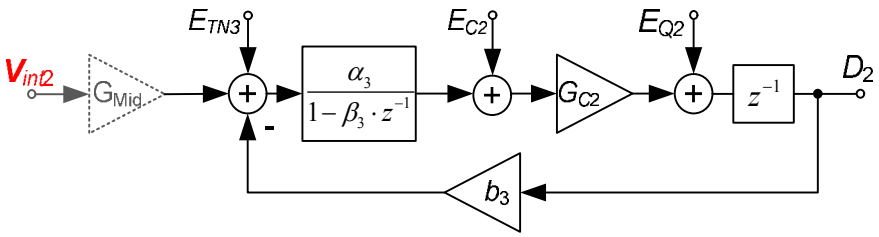

Fig. 5.20 Middle gain block G_{Mid} and the proposed second stage ΣΔM.

Since the proposed ΣΔM (build using the passive integrators derived in section 4.5) can be equivalently described in the *Z* domain, an analysis of the block diagrams from Fig. 5.19 and Fig. 5.20 and analysis of their transfer functions leads to the same conclusions as in case of discrete-time 1st and 2nd-order ΣΔMs described in sections 5.1 and 5.2. Fig. 5.21 depicts the plots of the STF and of the NTFs of the first stage of MASH modulator. These plots are consistent with conclusions drawn in section 4.1 and the equations describing the circuit transfer functions. Briefly summarizing: E_{TN1} is added directly to V_{in}; the level of E_C can be critical in a passive ΣΔM; $\mathrm{NTF_{Qi}}$ is a high-pass transfer function that, in low frequencies, is significantly attenuated by the comparator gain G_{Ci}. Moreover, the inter-stage gain G helps attenuating E_{TN2} and E_{C1} as well as additionally decreases (besides G_{C1}) the quantization noise E_{Q1}. The equations of the transfer functions of the first MASH stage together with their values at DC are given below.

In order to analyze $\mathrm{STF_1}$ from (5.9) one should take into consideration that it is relative to b_1, meaning that V_{in} cannot exceed b_1 and maximum theoretical (V_{in}/b_1) is 1. This means that, at DC $\mathrm{STF}(z = 1) \approx 1$.

$$\mathrm{STF_1} = \frac{D_1}{V_{in}} = \frac{G \cdot G_{C1} \cdot z \cdot \alpha_1 \cdot \alpha_2}{z^2 + z \cdot (G_{C1} \cdot (b_2 + G \cdot b_1 \cdot \alpha_1) \cdot \alpha_2 - \beta_1 - \beta_2) + \beta 1 \cdot (-G_{C1} \cdot b_2 \cdot \alpha_2 + \beta_2)} \tag{5.8}$$

$$\mathrm{STF_1}(z = 1) = \frac{G_{C1} \cdot G}{1 + G_{C1} \cdot G \cdot \left(b_1 + \frac{b_2}{G} \right)} \approx \frac{G_{C1} \cdot G}{G_{C1} \cdot G \cdot b_1} \approx \frac{1}{b_1} \tag{5.9}$$

$$\mathrm{NTF_{Q1}}(z) = \frac{D_1}{E_{Q1}} = \frac{(z - \beta_1) \cdot (z - \beta_2)}{z^2 + z \cdot \left[G_{C1} \cdot \alpha_2 \cdot (b_2 + G \cdot b_1 \cdot \alpha_1) - \beta_1 - \beta_2 \right] + \beta_1 \cdot (\beta_2 - G_{C1} \cdot b_2 \cdot \alpha_2)} \tag{5.10}$$

$$\mathrm{NTF_{Q1}}(z = 1) = \frac{1}{1 + G_{C1} \cdot G \cdot \left(b_1 + \frac{b_2}{G} \right)} \approx \frac{1}{G_{C1} \cdot G \cdot b_1} \tag{5.11}$$

$$\mathrm{NTF_{C1}}(z = 1) = \frac{G_{C1}}{1 + G_{C1} \cdot G \cdot \left(b_1 + \frac{b_2}{G} \right)} \approx \frac{G_{C1}}{G_{C1} \cdot G \cdot b_1} \approx \frac{1}{G_1 \cdot b_1} \tag{5.12}$$

The equations of $\mathrm{STF_2}$ and $\mathrm{NTF_{Q2}}$ of the second MASH stage are given below.

$$\mathrm{STF_2} = \frac{G_{C2} \cdot \alpha_3}{z + G_{C2} \cdot b_3 \cdot \alpha_3 - \beta_3} \tag{5.13}$$

$$\mathrm{NTF_{Q2}} = \frac{1 - \beta_3 \cdot z^{-1}}{z + G_{C2} \cdot b_3 \cdot \alpha_3 - \beta_3} \tag{5.14}$$

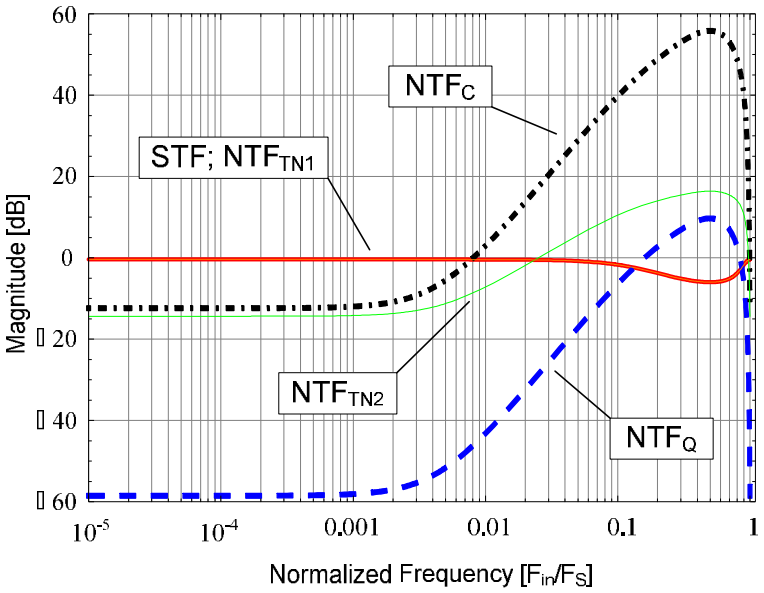

Fig. 5.21 Ideal graphs of STF and NTFs of the first stage of the MASH modulator, the 2nd-order ΣΔM.

As mentioned before, the equivalent comparators' gain is approximated as $G_{C1}=1/(\alpha_2 \cdot b_2)$ and $G_{C2}=1/(\alpha_3 \cdot b_3)$. This requires $\alpha_{2,3}<<1$ and $b_{2,3}<1$ in order to increase these gains and, consequently, provide more quantization noise attenuation.

The output voltage of the 1st integrator is mainly composed by the high frequency E_{Q1} signal and the V_{in} component is only a fraction of this voltage because the first feedback cancels a significant part of V_{in}. This implies two things. Firstly, a significant part of the power of the 1st integrator output signal is located in higher frequencies. The 1st integrator has to provide attenuation ($\sim G/b_2$) to guaranty that output amplitude of G is smaller than the feedback voltage of the second integrator (to avoid saturation). This requires $\alpha_1 \approx 1/(G/b_2)<<1$. Secondly, due to the small value of V_{in} in the output signal of the 1st integrator, distortion added to V_{in} by G (a single differential pair) is reduced and the maximum voltage swing of this gain block input signal does not have to be limited very strongly. In case of the proposed circuit, this is addressed by reducing the 1st integrator output swing to 80 $mV_{pp,diff}$. This is achieved during the optimization process (described earlier). The *gm* of the differential pair of the second gain block G_{Mid} does not introduce significant distortion because its input signal amplitude is very small. The output swing (OS) of each integrator is presented in Fig. 5.22, which depicts schematic of the MASH ΣΔM.

The feedback factors $b_{2,3}$ should be kept small to increase the loop gains of both stages (by increasing $G_{C1,C2}$). However, making $b_{2,3}$ too small requires higher attenuation of the 1st integrator, making its thermal noise contribution more significant. As mentioned before, the SNR of the passive ΣΔM is limited by the integrators' thermal noises, which are defined by values of *C*'s and by the comparator thermal noise that can be controlled by its proper sizing (described in the next section). The circuit has to be designed taking into account all the

mentioned constraints. In this work, the design solution was obtained through the optimization process.

Table 5.8 The 2-1 MASH passive ΣΔM design parameters.

C_1 [pF]	C_2 [pF]	C_3 [pF]	R_1 [kΩ]	R_2 [kΩ]	R_3 [kΩ]	C_{f1} [fF]	C_{f2} [fF]	C_{f3} [fF]	G [dB]	G_{Mid} [dB]	$V_{ref1,\,2}$ [V]	V_{ref3} [V]
13.7	2.1	2.3	2.1	10	20	220	13	7	19.6	19.6	0.9	0.44
C_{CM1} [pF]	C_{CM2} [pF]	C_{CM3} [pF]		a_1	a_2	a_3	G_{c1} [dB]	G_{c2} [dB]	b_1	b_2	b_3	
2.5	0.47	0.5		0.015	0.021	0.0097	46	59	0.84	0.23	0.12	

5.4.2. Circuit Implementation

A complete schematic of the differential MASH modulator is presented in Fig. 5.22. The two stages are the 2nd and the 1st-order ΣΔMs, respectively. The component values, α_i factors, comparators' gains and feedback factors can be found in Table 5.8. The modulator is based on the passive integrators previously described in Chapter 4.5. In each integrator, during one phase, the feedback signal is applied to the main capacitor C_i by transferring charge from the feedback capacitor C_{fi} that in the proceeding phase was connected to the adequate $\pm\Delta V_{ref\text{-}i}$ voltage. The integrators are described with following α and β values that are taken from (4.48):

$$\alpha_i = \frac{T_s}{2 \cdot R_i \cdot (C_i + C_{fi})} \qquad \beta_i \approx \frac{C_i}{C_i + C_{fi}} \cdot (1 - \alpha_i) \tag{5.15}$$

where the C_i is in fact an equivalent capacitance of the differential capacitor C and two common-mode capacitors C_{CM}. The additional capacitors C_{CM} are used to help reducing the common-mode voltage swing at the integrator's output. This common-mode voltage swing can be caused by the common-mode charge injection of the switches connected to the integrators nodes.

The circuit is clocked with two non-overlapping phases generated from NAND based clock generator depicted in Fig. 5.23. The internal inverters (marked with stars) are used to define the non-overlapping time between two phases. The feedback switches are implemented as transmission gates formed by pairs of transistors (NMOS and PMOS) and signals controlling feedback switches are obtained using AND gates.

The parasitic capacitances C_p of the switches connecting capacitors C_i and C_{fi}, depend on the node voltage and therefore, vary with the input signal, meaning that C_p has different value for the maximum and minimum amplitude of V_{in}. Nevertheless, these parasitic capacitances are very small in comparison to C_i and C_{fi} and their variation does not introduce significant distortion. In the case of the 1st integrator, simulation results show that C_{p_min}=6.9 fF, C_{p_max}=12 fF and the variation from the average value of C_p is ΔC_p=0.017% of C_1+C_{f1}. The values of C_p and ΔC_p in other integrators are even smaller and their impact is less significant.

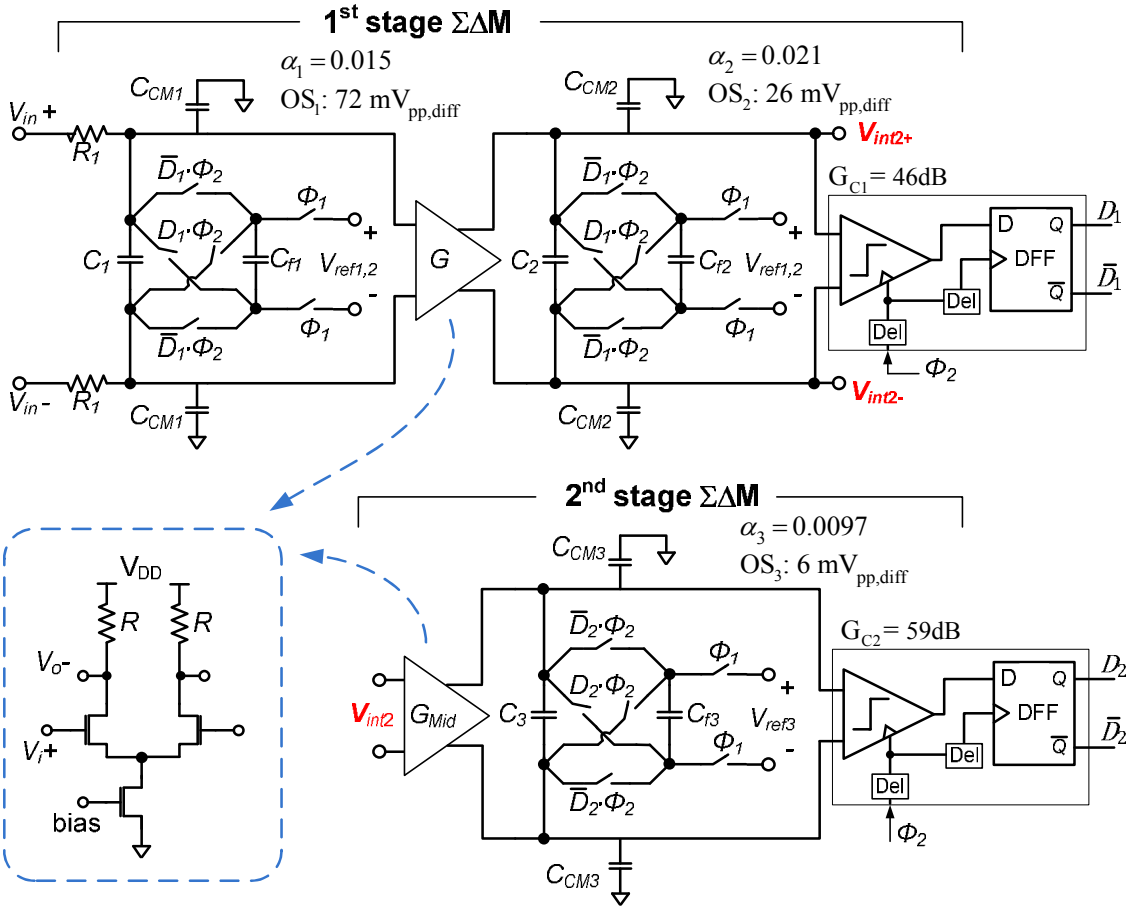

Fig. 5.22 Schematic of the proposed MASH modulator.

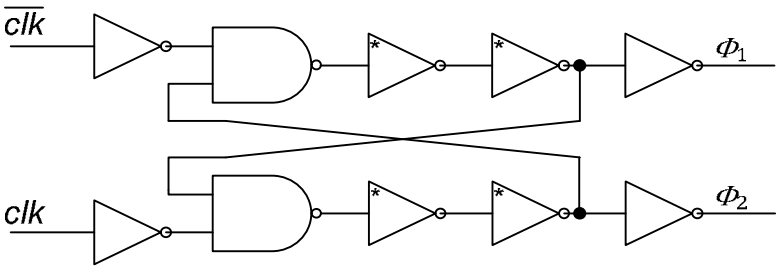

Fig. 5.23 NAND based two-phase clock generator.

Blocks *G* and G_{Mid} separate adjacent integrators preventing loading and provide gains (~20 dB). They are implemented as differential pairs loaded by resistors (Fig. 5.24). These resistors, besides being the load of the gain stages, are also part of the *RC* time constants of the 2nd and 3rd integrators. The low gain amplifiers use the resistances because this provides a gain that is well determined ($G = gm \cdot R$). If an active load was used instead, the gain would depend on the r_{ds} value of the load transistors. The variation of r_{ds} would also increase the variation of the *RC* constant of the integrator and since r_{ds} varies with V_{ds} it could also introduce extra distortion into

the circuit. Since the output common-mode voltage, V_{O_CM}, of the gain blocks can change according to process, temperature and supply voltage (PVT) variations, a replica bias circuit is used to adjust the buffers' output common-mode voltages to the desired value (half of V_{DD}) by regulating their bias currents [99, 100], as shown in Fig. 5.24.

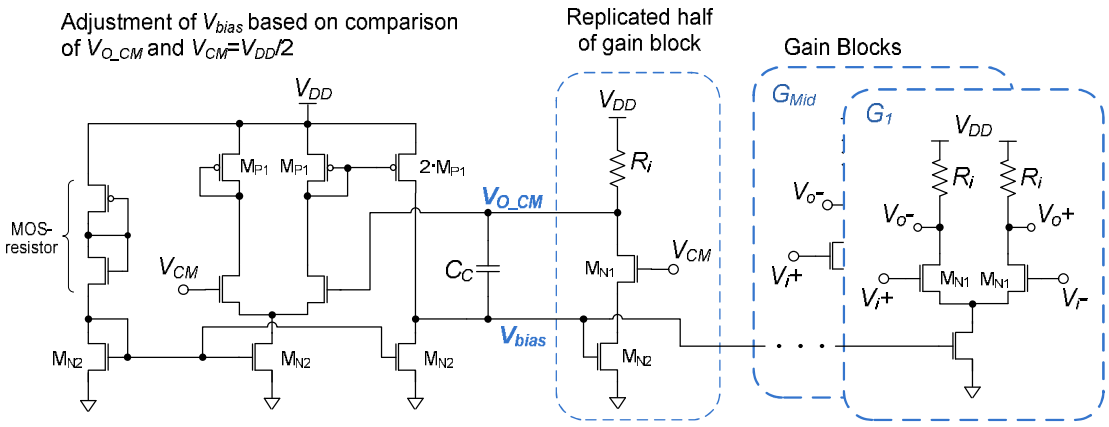

Fig. 5.24 The Gain Blocks with the replica bias circuit.

The outputs of the second and third integrators are connected to the comparators. Each comparator, depicted in Fig. 5.6, must amplify a small amplitude signal into a digital level (V_{DD} or 0 V) and, therefore, they should have a large gain. This can be achieved by employing positive-feedback (a back-to-back inverter connection) in the comparators. This structure is based on the sense amplifier described in [98]. In order to minimize its noise contribution its sizing is based on the noise analysis presented in [101]. There are two main factors that influence the input referred noise of the comparator. By increasing these factors, that are shown in (5.16), the input referred noise decreases.

$$\frac{\beta_{MN2}}{\beta_{MN3}} = \frac{W_{MN2} / L_{MN2}}{W_{MN3} / L_{MN3}}; \qquad \frac{\beta_{MN1}}{\beta_{MN3}} = \frac{W_{MN1} / L_{MN1}}{W_{MN3} / L_{MN3}} \tag{5.16}$$

It was decided not to relax the design of the first comparator (that experiences a larger input signal amplitude than the second one) in order to maximize performance of the first stage ΣΔM. The sigma value of the input referred noise of the comparator, operating at 1 GHz, is: σ_c = 140 μV. This value was used in the optimization process. Moreover, the comparator and the D-type flip-flop were designed to minimize the risk of metastablity. These two circuits guaranty that after 500 ps (half clock cycle) the output is a clear logic level.

5.4.3. Digital Cancellation Logic (DCL) Implementation

The output signals from both stages, D_1 and D_2, enter the DCL block that is presented in Fig. 5.18. Excess-loop-delays of both stages are equal to *Ts* and in *Z* domain are interpreted as a z^{-1} delays. Constant value of excess-loop-delay facilitates proper operation of the digital cancellation logic. Since the signal D_2, besides the quantization noise of the 1st and 2nd stages (E_{Q1} and E_{Q2}) also contains the input signal V_{in} the DCL performs operation of cancellation of

V_{in} (from D_2) and E_{Q1} (from D_1 and D_2). The quantization noise E_{Q2} is shaped by the noise transfer functions of both stages, achieving 60 dB/decade noise shaping. The $1/G_{C1}$ gain block inside the DCL compensates the first stage comparator gain. The z^{-1} and z blocks compensate the delay of the first stage D-type flip-flop. The DCL can be simplified considering that the objective is to cancel the quantization noise of the first modulator only inside the signal band (up to 10 MHz). Since the denominators of NTF_{Q1} and STF_2 have poles located at higher frequencies than the signal band, it is only necessary to use the DC gain factor of the denominator part. This is done by evaluating the denominators of NTF_{Q1} and STF_2 at $z = 1$ and using these values to scale the output signals of the two modulators. The modified DCL is presented in Fig. 5.25. Its coefficients can be derived from NTF_{Q1} and STF_2 and are presented in (5.17) and (5.18). In order to avoid explicit multiplications it is possible to use multiplexers controlled by the two bit-streams of the two modulators to select between a positive and a negative value for the coefficient. This approach requires only D-type flip-flops, multiplexers and adders, therefore, is more power and hardware efficient than the typical DCL from Fig. 5.18.

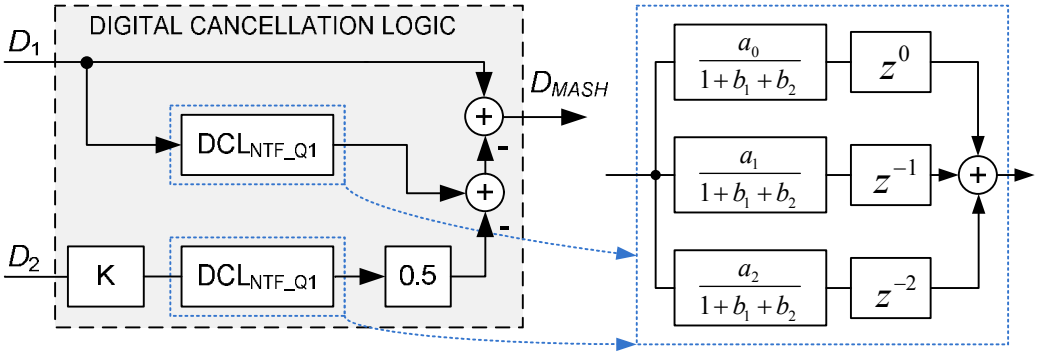

Fig. 5.25 First modification of digital cancellation logic (DCL) block.

$$\mathrm{DCL}_{\mathrm{NTF\_Q1}} = \frac{Numerator\left\{\mathrm{z}\cdot\mathrm{NTF}_{\mathrm{Q1}}(z)\right\}}{Denominator\left\{\mathrm{NTF}_{\mathrm{Q1}}(z=1)\right\}} = \frac{a_0 + a_1\cdot z^{-1} + a_2\cdot z^{-2}}{1+b_1+b_2} \tag{5.17}$$

$$K = \frac{Denominator\left\{\mathrm{STF}_2(z=1)\right\}}{G_{C2}\cdot\dfrac{\alpha_3}{G_{C1}}\cdot G_{Mid}}. \tag{5.18}$$

It is possible to further simplify the DCL. One can notice that, the modified DCL is in fact a finite impulse response filter with inputs: $D_1[n]$, $D_1[n\text{-}1]$, $D_1[n\text{-}2]$, $D_2[n]$, $D_2[n\text{-}1]$, $D_2[n\text{-}2]$ that can be implemented as 6-bit look-up table. In other words the set of equations describing DCL gives a unique value (with 15 bits resolution) for each combination of the DCL inputs (64 combinations). These values are shown in Table 5.9. The final DCL can be built as a decoder using 270 logic gates and 4 D-type flip-flops. This simplification leads to further reduction in power and in number of components (avoiding multipliers, adders and multiplexers). The DCL

coefficients are calculated during designing phase and do not require adjustment or calibration during the circuit operation.

Table 5.9 Modified digital cancellation logic (DCL) described as a look-up table.

No	$D_1[n]$, $D_1[n\text{-}1]$, $D_1[n\text{-}2]$, $D_2[n]$, $D_2[n\text{-}1]$, $D_2[n\text{-}2]$	DCL out
0	'000000'	-513
1	'000001'	3835
2	'000010'	-9462
3	'000011'	-5114
4	'000100'	4092
5	'000101'	8440
6	'000110'	-4857
7	'000111'	-509
8	'001000'	-2219
9	'001001'	2129
10	'001010'	-11168
11	'001011'	-6820
12	'001100'	2386
13	'001101'	6734
14	'001110'	-6563
15	'001111'	-2215
16	'010000'	2999
17	'010001'	7347
18	'010010'	-5950
19	'010011'	-1602
20	'010100'	7604
21	'010101'	11952
22	'010110'	-1345
23	'010111'	3003
24	'011000'	1293
25	'011001'	5641
26	'011010'	-7656
27	'011011'	-3308
28	'011100'	5898
29	'011101'	10246
30	'011110'	-3051
31	'011111'	1297

No	$D_1[n]$, $D_1[n\text{-}1]$, $D_1[n\text{-}2]$, $D_2[n]$, $D_2[n\text{-}1]$, $D_2[n\text{-}2]$	DCL out
32	'100000'	-1297
33	'100001'	3051
34	'100010'	-10246
35	'100011'	-5898
36	'100100'	3308
37	'100101'	7656
38	'100110'	-5641
39	'100111'	-1293
40	'101000'	-3003
41	'101001'	1345
42	'101010'	-11952
43	'101011'	-7604
44	'101100'	1602
45	'101101'	5950
46	'101110'	-7347
47	'101111'	-2999
48	'110000'	2215
49	'110001'	6563
50	'110010'	-6734
51	'110011'	-2386
52	'110100'	6820
53	'110101'	11168
54	'110110'	-2129
55	'110111'	2219
56	'111000'	509
57	'111001'	4857
58	'111010'	-8440
59	'111011'	-4092
60	'111100'	5114
61	'111101'	9462
62	'111110'	-3835
63	'111111'	513

5.4.4. Optimization procedure

In a MASH architecture the mismatch between the analog (the ΣΔM stages) and the digital (digital cancellation logic) transfer functions can degrade the modulator's performance. This issue has been addressed by the design methodology (described in Chapter 4.8) of the proposed MASH ΣΔM that uses an optimization algorithm to maximize the SNDR. During the execution of the optimization algorithm (Fig. 4.16), each chromosome, which represents set of a design parameters (R_i's, C_i's, C_{fi}'s, G's, V_{ref}'s), is evaluated by the high level model of MASH ΣΔM that takes into consideration thermal, comparators' and quantization noises. This model, describes the modulator as a combined continuous-time/discrete-time system, where the behavior of the integrators during clock phases is calculated using differential equations, allowing to obtain the output voltage at the end of each clock phase ($v_{ci}[(n\text{-}1)\cdot T_s]$, $v_{ci}[n\cdot T_s]$, etc). At each iteration of the optimization algorithm, it is run a Monte-Carlo (MC) analysis, with included process and mismatch variations of R_i's, C_i's, C_{fi}'s, G and G_{Mid} in order to determine the average SNDR. The values of variations are given in Table 5.10. These variations are only added to the analog part, while the digital cancellation logic uses the nominal values in order to obtain a final design solution that has a low sensitivity, avoiding the need for calibration. Moreover, in order to reduce the distortion of the first differential pair, its input signal amplitude is also optimized to be smaller than 80 $mV_{pp,diff}$.

After the optimization, a 1000-case MC analysis (using a high-level model of the MASH modulator) with process and mismatch variations of R_i's, C_i's, C_{fi}'s, G and G_{Mid} (given in Table 5.10) resulted in a mean peak SNDR value of 72.9 dB with a standard deviation of 1.3 %. During this analysis the digital cancellation logic used the nominal values and it was not subjected to the variation in order to confirm a small sensitivity of the design solution to mismatch between analog (the ΣΔM stages) and digital (the digital cancellation logic) parts. The histogram of the SNDR distribution of MC analysis is shown in Fig. 5.26.

In order to illustrate the design point selected by the optimization process, the high level model of the modulator was additionally simulated varying each design parameter around the optimal design point. The result of this simulation for the MASH modulator is depicted in Fig. 5.27 and, for the 2nd-order ΣΔM (first stage of MASH modulator), in Fig. 5.28. These graphs demonstrate that the result of the optimization procedure achieves the maximum peak SNDR (for BW=10 MHz) and that the selected solution has also a low sensitivity to components' variations. Note that the graphs in Fig. 5.27 show that it is possible to obtain a larger SNDR from MASH modulator by decreasing R_1 value. However this would make the circuit more sensitive to the variation of this component and could lead to modulator's overload (faster SNDR drop for variation of R_1 larger than -30 %).

It is possible to conclude that in this system, variation of the modulator components does not significantly affect the circuit performance. The reason for that is the design method that takes

into consideration process and mismatch components variations.

Table 5.10 3σ values of the circuit components' variations.

Variation	R_i	C_i	C_{fi}	G, G_{Mid}
Global 3 σ - process	16%	18%	25%	6%
Local 3 σ - mismatch	0.2%	0.2%	0.2%	0.2%

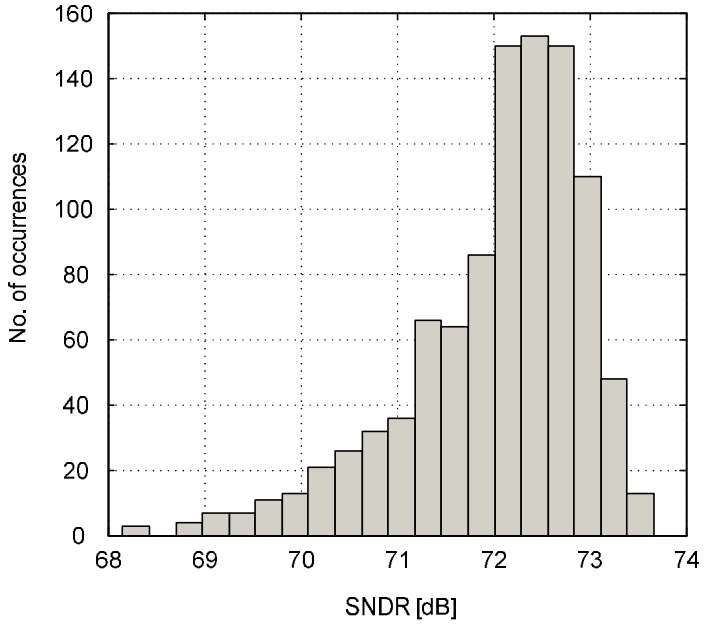

Fig. 5.26 SNDR histogram of the MASH ΣΔM of 1000-case MC analysis with process and mismatch variations added to the values of the modulator's components.

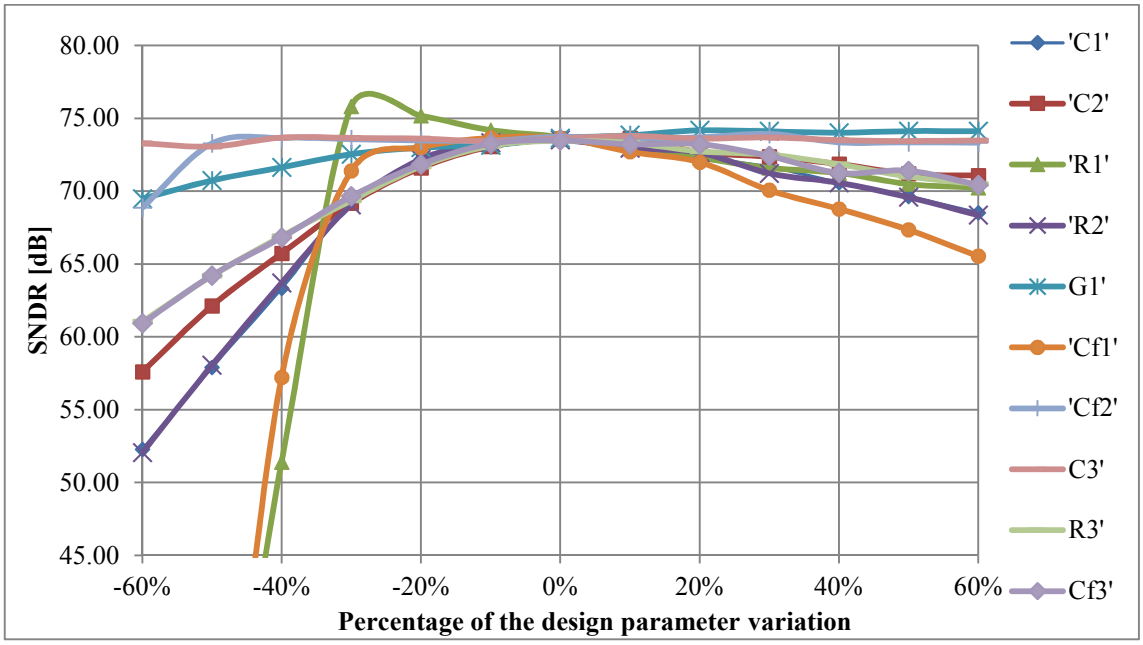

Fig. 5.27 SNDR of the MASH modulator versus variation of the components around the optimal design point selected by the genetic algorithm based optimizer.

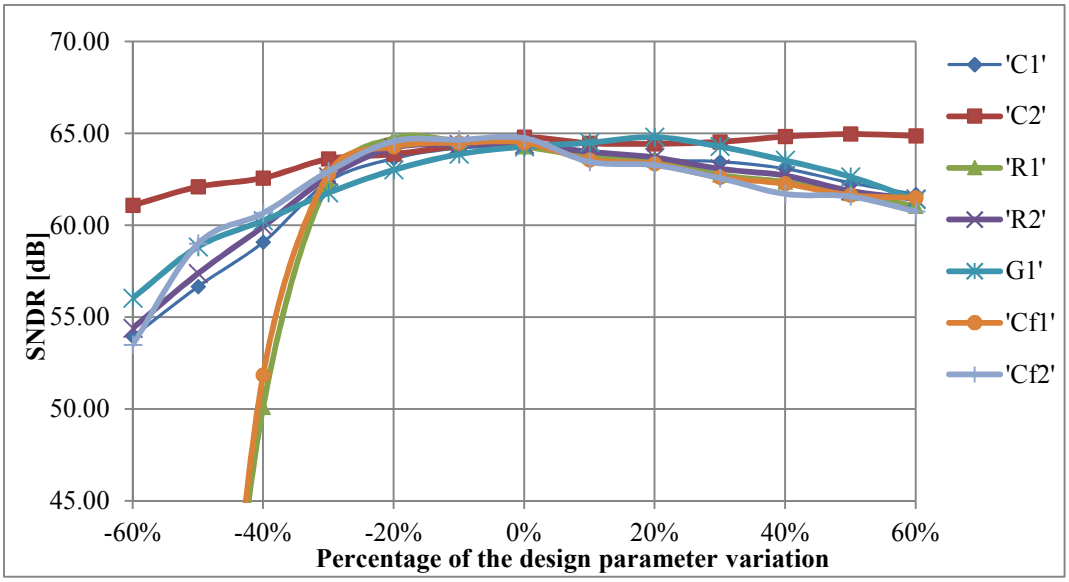

Fig. 5.28 SNDR of the 2nd-order ΣΔM (first stage of the MASH modulator) vs variation of the components around the optimal design point selected by the genetic algorithm based optimizer.

5.4.5. Electrical Simulations

In this section the simulation results of the 2–1 MASH ΣΔM and, additionally, the 2nd-order (first stage) modulator are presented. This allows for a comparison between the single-loop and cascaded modulators, built using passive integrators and low gain stages. The circuit, clocked with frequency, F_S = 1 GHz, was simulated by applying input sine wave signal with frequency of 1.34 MHz and performing exhaustive electrical transient-noise simulations. The power spectral densities of the output signals for an input signal with amplitude of 600 $mV_{pp,diff}$, are shown in Fig. 5.29. One can notice that, the circuits achieve 60 dB/decade and 40 dB/decade noise shaping, respectively. Table 5.11 summarizes the circuits' performance parameters.

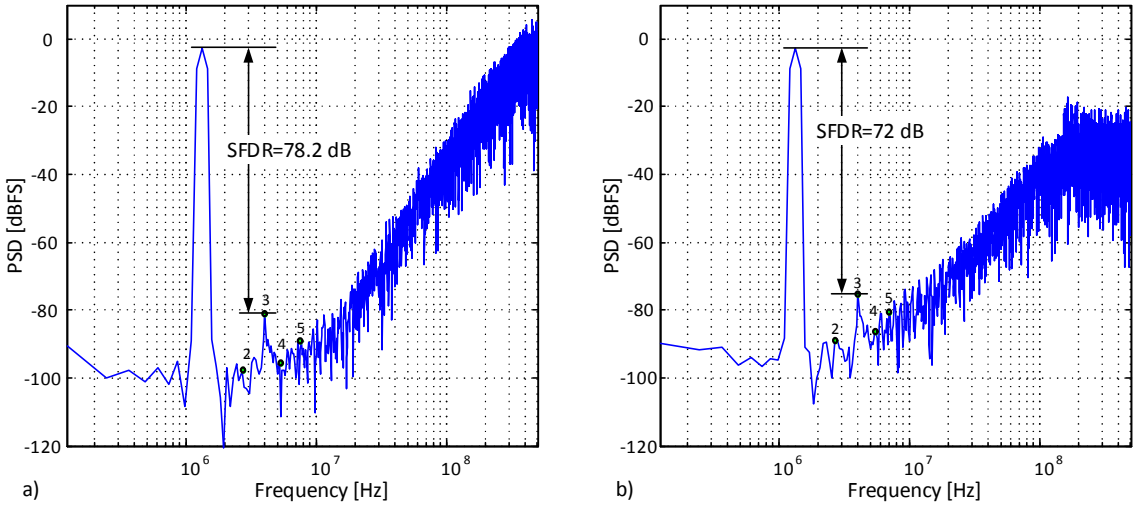

Fig. 5.29 The 2^{13} point PSD of a) the 2-1 MASH ΣΔM b) the 2st-order ΣΔM (first stage).

Table 5.11 Simulation results of the 2–1 MASH ΣΔM and the 2nd-order ΣΔM.

	Tech. [nm]	F_s [GHz]	BW [MHz]	SNDR [dB]	SNR [dB]	THD [dB]	P_C^* [mW]	FoM_W [fJ/conv-step]
2-1 MASH	65	1	10	73	77.1	-75.2	1.33*	18.2
2nd ord.				63.4	65.3	-67.9	0.83	34.3

* This includes additional power consumption of the synthesized DCL: 0.27 mW

5.4.6. Design Example Summary

In this section, a 2–1 MASH ΣΔM using passive *RC* integrators and low gain stages (~20 dB) instead of high gain amplifiers was presented and analyzed. This circuit has been chosen as the design of the ΣΔM capable to obtain SNDR > 70 dB in signal bandwidth of 10 MHz, based on the comparison of several architectures. The circuit's sensitivity to components variation was reduced by using a genetic algorithm based design methodology that takes into consideration process and mismatch components variations. The measured results of the fabricated 2–1 MASH modulator are depicted in the next chapter.

5.5. Summary

In this chapter various ΣΔM architectures using passive integrators were discussed. The two design examples that have been presented were laid out and fabricated. The goal of implementing and fabricating the 2nd-order single-loop ΣΔM, working with clock frequency of 100 MHz, was mainly to prove the UIS concept. The second design example is expected to work with a medium signal bandwidth and to obtain a moderate dynamic resolution (SNDR). This is because its clock frequency is higher in order to maintain the intended modulator's performance. Therefore, the goal is to build ΣΔM with bandwidth of 10 MHz and a SNDR larger than 70 dB, working with clock frequency of 1 GHz.

Moreover, as it was shown in this chapter, the higher order single-loop structure does not ensure sufficient SNDR. Therefore, a cascaded modulator architecture has been selected for designing the second prototype. The next chapter presents the two integrated prototypes and the corresponding measured results of the 2nd-order single-loop ΣΔM and of the 2–1 MASH modulator.

6. INTEGRATED PROTOTYPES AND MEASURED RESULTS

This chapter describes the layout design, evaluation procedure and measured results of the two integrated prototype circuits designed in order to demonstrate the techniques proposed in the this thesis, namely:

- A discrete-time 2nd-order ΣΔM designed in a 130 nm CMOS technology
- A continuous-time 2-1 MASH ΣΔM designed in a 65 nm CMOS technology

The architecture and circuit implementation of these two ΣΔMs has been discussed in sections 5.2 and 5.4. After the schematic design, several electrical simulations have been run to confirm the correct operation of the circuit. The circuit have been laid out. This task includes layout floor planning and layout drawing that has to comply with the design rules defined by a technology design kit. These are verified using the design rule check (DRC) deck. The next procedure is the layout *versus* schematic (LVS), verifying the compliance of schematic and layout. Then, in order to obtain the parasitics associated to the layout (parasitic *R*'s and *C*'s) the extraction tool has been used. The extracted *C*'s represent capacitances between various nodes (coupled) and from nodes to substrate. After obtaining a new netlist containing parasitics the post-layout simulations can be performed. They allow comparing the obtained results with the ones form schematic electrical simulations.

In sections 6.1 and 6.2 the corresponding integrated chips are analyzed from the layout perspective, which is complemented with the description of the floor-planning. Afterwards, a description is given about the design of the printed-circuit-board (PCB) as well as the testing setup. Finally, the different measurement results obtained from the integrated circuit prototypes are presented and carefully analyzed.

6.1. Discrete-Time 2nd-Order ΣΔM

This section presents the layout design and evaluation process of the discrete-time 2nd-order ΣΔM using passive UIS integrators. The prototype implementation details of the circuit are discussed in the section 5.2. The main purpose of this prototype is to confirm experimentally the validity of the UIS concept. The measurement results are presented at the end of this section.

6.1.1. Layout

This ΣΔM circuit was designed in a 130 nm single-poly eight-metal (1P8M) CMOS technology with metal-insulator-metal (MiM) capacitors. This circuit uses only standard V_T NMOS and PMOS devices, MiM capacitors and resistors implemented using high-resistive-poly. Fig. 6.1 depicts the layout of the 2nd-order ΣΔM, highlighting its main blocks and components.

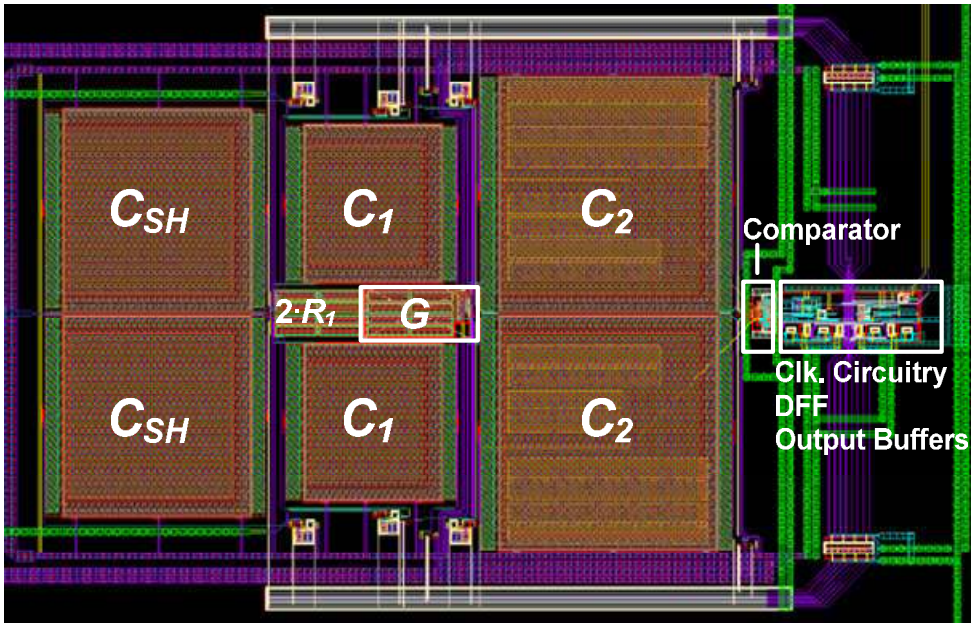

Fig. 6.1 Layout of the 2nd-order ΣΔM

In order to avoid problems with non-ideal effects, good layout practices, such as described in [102] were followed. The ΣΔM circuit is differential, hence, in the layout the positive and the negative modulator's halves and their signal paths are made symmetrical. Paths with the analog signal pass along the layout axis of symmetry from the left to the right side of the circuit. The analog blocks are more sensitive to noise than the digital ones and they should be protected from any potential noise sources. It is important to minimize the coupling effect from digital circuitry and clock lines to analog blocks and signal lines. Therefore, the clock circuitry (phase generator, delay blocks, AND gates, buffers) and the rest of the digital circuitry used after the comparator (D-type flip-flop, buffers) are placed relatively far from the analog blocks, at the right center region. Moreover, the distribution of the clock phases and clock signals controlling the feedback switches is located at the outer boundary of the modulator. Further, three separated power supplies coming from separated pads are used: analog (VDD_A and VSS_A), mixed-mode (VDD_M and VSS_M) and digital (VDD_D and VSS_D). This minimizes the probability of injecting noise from the digital to the analog circuitry through the power supply and ground connections, improving the noise immunity of the ΣΔM. The power connections are distributed around the overall circuit and are made wide in order to reduce their resistance and, consequently, the voltage spikes that can occur across them. All the important blocks (e.g. comparator, gain block,

digital circuitry) are surrounded by guard rings in order to improve the circuit isolation from substrate noise. The shortest possible length is used for the important signal paths in order to minimize their connection resistances and hence the voltage drops across these metal lines. Also, in order to minimize resistance in the path and improve fabrication reliability, the vias and contacts are used liberally whenever the signal has to pass to another layer.

In order to expedite the assembly of the prototyped chip, a pad ring with the electrostatic discharge protection (ESD) scheme, that was previously used in an unrelated ΣΔM prototype circuit [103], was reused. Since this pad ring has more pads that the ones required by this ΣΔM, some of the pads in the pad ring were left unconnected. The pad ring is shown in Fig. 6.2 and it allows interfacing the prototype input and output signals. The names and the functionality of the used pads are described in Fig. 6.2 and Table 6.1, respectively. The digital pads, that connect the input and the output signals to/from the digital circuitry, are separated (by using cutting cells) from the analog and mixed-mode pads that drive the input signal, power supplies and reference signals. This separation minimizes the noise injected from digital to analog blocks through the power supply and ground busses. The die microphotograph of the ΣΔM is depicted in Fig. 6.3 and the modulator occupies an area of 300x536 μm^2 ($\approx$ 0.16 mm^2).

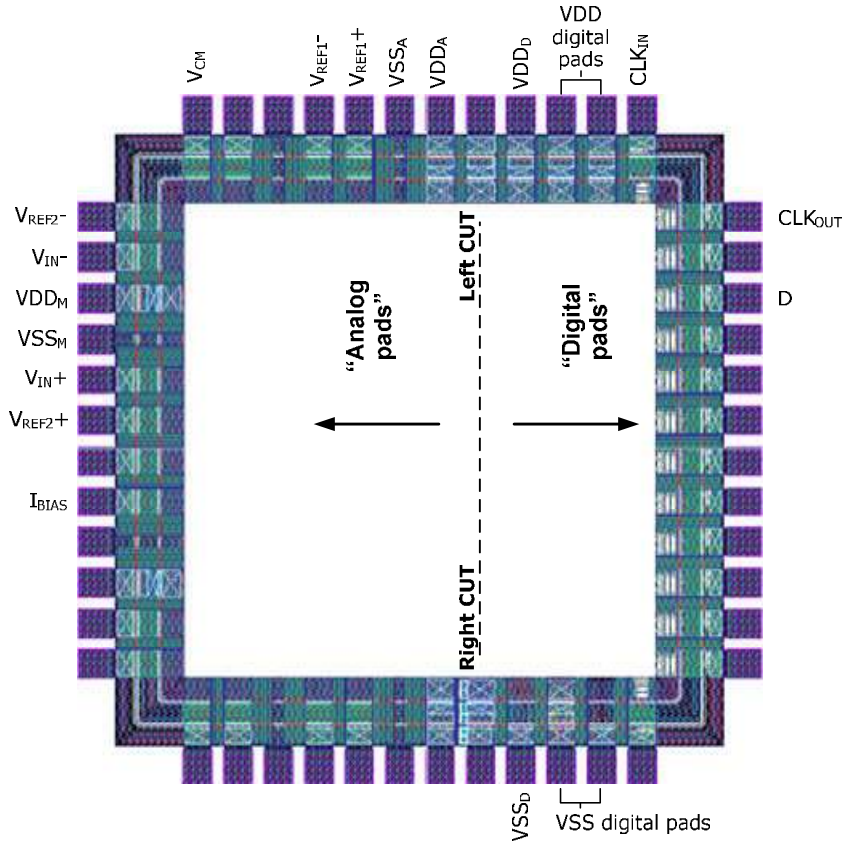

Fig. 6.2 Layout of the pad ring with the names of the used pads (for interfacing the 2nd-order ΣΔM).

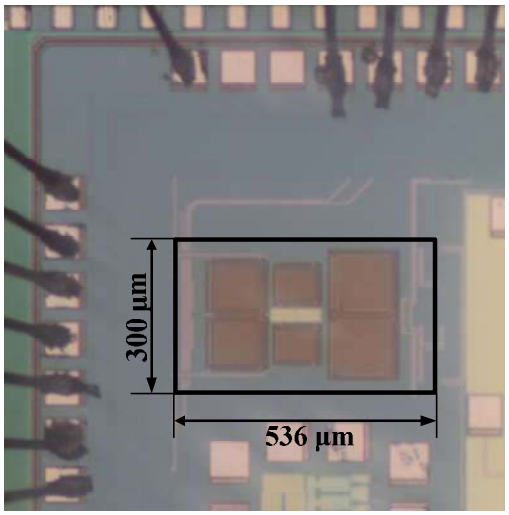

Fig. 6.3 Chip die photograph of the 2nd-order ΣΔM circuit.

Table 6.1 List of pads used to interface the 2nd-order ΣΔMs prototype.

Pad	Value	Functionality
V_{CM}	0.55 V	Common-mode voltage of the S/H block
$V_{REF1}+$	1.1 V	Positive reference voltage of the 1st integrator
$V_{REF1}-$	0 V	Negative reference voltage of the 1st integrator
$V_{REF2}+$	0.66 V	Positive reference voltage of the 2nd integrator
$V_{REF2}-$	0.44 V	Negative reference voltage of the 2nd integrator
I_{BIAS}	8 µA	Gain block biasing current
$V_{IN}+$	analog	Positive input signal
$V_{IN}-$	analog	Negative input signal
CLK_{IN}	digital	Clock input signal
CLK_{OUT}	digital	Clock output signal of the ΣΔM data
D	digital	ΣΔM output bit-stream
VDD_A	1.2 V	Analog power supply
VDD_D	1.1 V	Digital power supply
VDD_M	1.2 V	Mixed-mode power supply
VSS_A	0 V	Analog ground
VSS_D	0 V	Digital ground
VSS_M	0 V	Mixed-mode ground
VDD_{AUX}	3.3 V	Auxiliary power supply for digital pads
VSS_{AUX}	0 V	Auxiliary ground for digital pads

6.1.2. Experimental Set-Up

In order to experimentally evaluate the ΣΔM circuit, the same printed circuit board (PCB) design, used to test the ΣΔM from [103], was also reused. This board is pin compatible with the used pad ring, which simplified the experimental set-up. The PCB and its main areas are shown in Fig. 6.4. These main areas include: power supplies, input and output signal paths, clock input,

references and common-mode voltages, gain block biasing current and the place where the device under test (DUT) is mounted. The PCB has four layers, of which the top and bottom layers are assigned for routing and the two inner ones are designated for ground and power planes. The power supply plane is divided into three distinct areas: an analog VDD_A supply equal to 1.2 V for the chip, a digital VDD_D supply equal to 1.1 V for the chip and an auxiliary VDD_{AUX} supply equal to 3.3 V for the chip I/O digital pads and for the PCB. A common ground plane on layer 2 is used, which simplifies the PCB design. Taking into consideration that the noisy signals (e.g. clock input, digital outputs) are kept apart from the most noise-sensitive signals (e.g. analog inputs), the ground plane effectiveness in maintained.

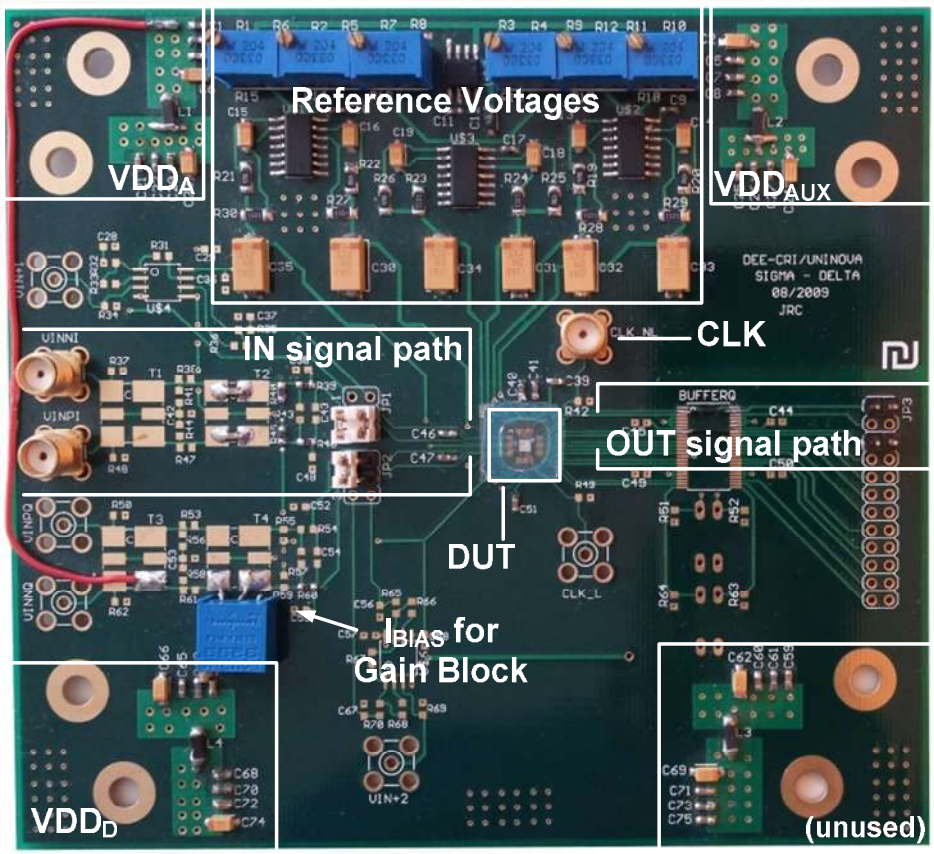

Fig. 6.4 Photograph of the PCB evaluation board for the 2nd-order ΣΔM.

Each supply voltage passes through a ferrite bead and a set of bypass capacitors (some of them placed very close to the DUT). This approach allows removing (shorting to ground) unwanted AC signal components appearing in the DC power supplies. The values of the bypass capacitors are: 0.01 µF, 0.1 µF, 1 µF and 10 µF. The ferrite bead enhances the effectiveness of the bypass capacitors. At high frequencies the ferrite bead has a very high impedance while the bypass capacitors have much lower impedance. This causes that the most of transient current flows though these capacitors to the ground. At low frequencies the ferrite bead has a very small impedance, due to a very small equivalent series resistance (~mΩ), ensuring a proper power supply for the chip with negligible voltage drop across the ferrite bead. In order to help stabilize

the supply voltages, bypass capacitors are also placed next to the DUT. In fact, in order to avoid most of the parasitic inductance of the PCB traces they are located as close as possible to the DUT which improves effectiveness of the bypassing. The references and common-mode voltages are built around a precision, low-dropout 1.2 V voltage reference circuit (MAX6120, supplied from VDD_{AUX}) and are independently adjusted to the desired values with a set of trimmer resistors. After preparing the test PCB and soldering the components, the chip sample was containing the prototype circuit direct-bonded to the board (chip-on-board technique). This approach allows obtaining a low inductance in the bonding wires and less parasitic influence between the evaluation board and the chip interconnections, because package-related parasitics are avoided.

Fig. 6.5 shows the simplified schematic of the measurement setup. The differential balanced input signal for the ΣΔM is generated by an ATS-2 Audio Precision Analyzer. The clock source (Tektronix AWG510) generates a 100 MHz clock signal that is directly connected to the chip. The power supply voltages for the chip and PCB are provided by Tektronix PS 2521G, a programmable power supply with current limiting. The internally buffered reference voltages of the circuit are regulated by set of trimmer resistors. The differential reference voltage for the first integrator is 1.1 V ($V_{REF1}+$ = 1.1 V and $V_{REF1}–$ = 0 V), the differential reference voltage for the second integrator is 0.22 V ($V_{REF2}+$ = 0.66 V and $V_{REF2}–$ = 0.44 V) and the common-mode voltage, V_{CM}, is 0.55 V. The ΣΔM output signal, D, is captured on the logic analyzer, Agilent 16702B, and transferred to a PC for processing. This processing includes calculation of power spectral density of the modulator's output signal.

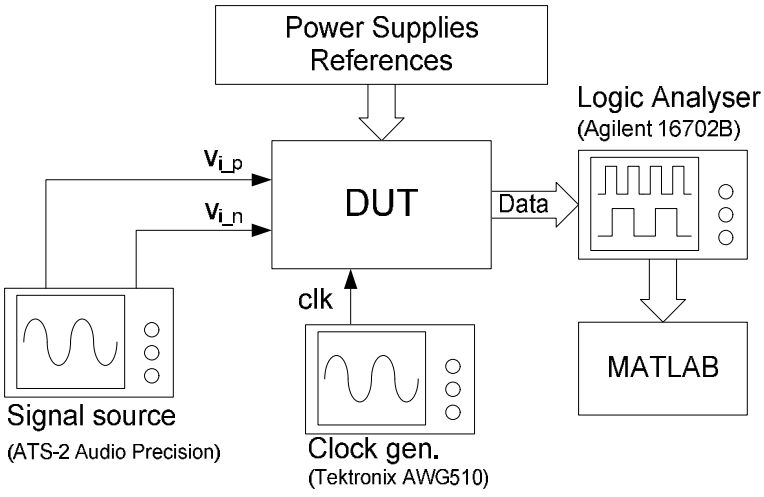

Fig. 6.5 Simplified schematic of the test setup of the DT 2nd-order ΣΔM.

6.1.3. Measured Results

Three evaluation boards, with three direct-bonded chip-on-board samples, were assembled and tested. These circuits were tested by applying a balanced 22 kHz input sine wave signal with varying amplitude, obtaining the output bit-stream and then computing the FFT. The circuits

worked properly and their measured key performance parameters are depicted in Table 6.2. These results show that the performance is consistent across the three integrated circuit samples.

Table 6.2 Measured key performance parameters of the DT 2nd-order ΣΔM (F_{in}=22 kHz).

Sample	Tech. [nm]	*Fs* [MHz]	BW [kHz]	Area [mm²]	SNR [dB]	SNDR [dB]	DR [dB]	THD [dB]	P_C* [µW]	FoMw [fJ/conv-step]	FoMs [dB]
I	130	100	300	0.16	73.6	72.14	77.9	-79	285*	145	168
II					73.5	72.3	77.9	-80.4	288*	142.8	168
III					73.9	72.8	78.2	-80.7	298*	139.3	168

*P_C is calculated excluding references and two digital output buffers driving the output pads.

Fig. 6.6 depicts an FFT of the ΣΔM output signal for a 0.912 $V_{pp,diff}$ (-1.6 dB_{FS}) input signal amplitude, for sample III. The SNR/SNDR *vs*. input amplitude graphs, for sample III, are shown in Fig. 6.7. In order to minimize the spectral leakage a 128 K Blackman-Harris window is used to plot power spectral density. Moreover, the results are obtained through averaging seven FFTs.

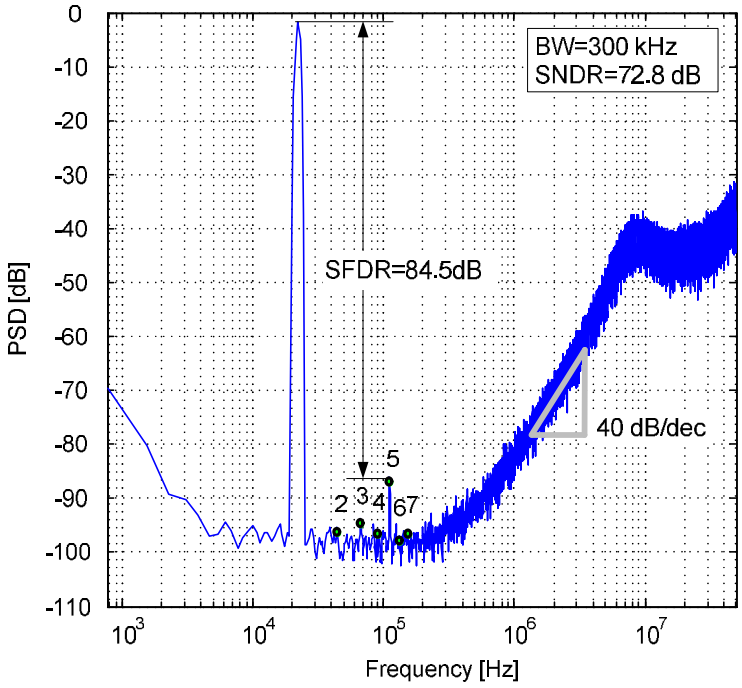

Fig. 6.6 Measured spectra of the 2nd-order ΣΔM for F_{in}=22 kHz, THD=-80.7 dB (sample III)

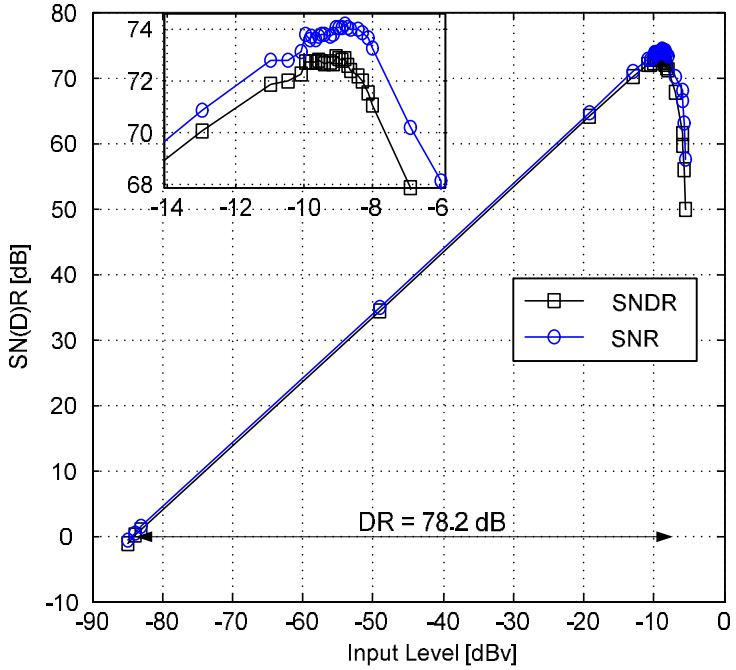

Fig. 6.7 SNR/SNDR vs. amplitude graphs for a 22 kHz input signal (sample III)

This section presented layout design and evaluation process of the passive-active discrete-time 2nd-order ΣΔM based on the implementation of switched-capacitor integrators using ultra incomplete settling. This approach allowed building a ΣΔM with mostly passive elements thus reducing the power dissipation. The circuit was designed using a 130 nm CMOS technology and three prototype samples have been tested. The measured key performance parameters were consistent across the samples. The circuit from sample III dissipates 298 μW from a 1.2 V analog and digital power supply voltages. The measured peak $SNDR_{max}$, peak SNR_{max} and DR are 72.8 dB, 73.9 dB and 78.2 dB, respectively, for a signal bandwidth of 300 kHz. This results in a FoM_W of 139.3 fJ/conv.-step and FoM_S of 168 dB.

6.2. Continuous-Time 2-1 MASH ΣΔM

This section presents the layout design and evaluation process of the continuous-time 2-1 MASH ΣΔM using *RC* integrators and low gain stages. The design methodology and the implementation details of the circuit were discussed in the section 5.4. The measurement results summarizing the ΣΔM's key performance parameters are presented at the end of this section.

6.2.1. Layout

The continuous-time 2-1 MASH ΣΔM was designed in a 65 nm single-poly seven-metal, low power with access to general purpose devices CMOS process with a power supply voltage value of 1 V. Metal-insulator-metal (MiM) capacitors and standard V_T transistors were used. Fig. 6.8 depicts layout of the 2-1 MASH ΣΔM with highlighted main blocks and components.

Similarly to the previously described design example, the layout of this ΣΔM follows the same techniques for improving the circuit's noise immunity. It was also intended to reduce the coupling and cross talk between digital and analog blocks and critical signal paths. In the case of this circuit it is even more important because it is clocked with a 10x higher clock frequency than the previously described ΣΔM. The layout of the differential modulator is made to be as symmetrical as possible. The paths with the analog signal pass along the layout axis of symmetry from the left to the right side of the circuit. The analog blocks of both stages are laid out together and the digital blocks are placed at the peripheral region of the modulator (right center region). This means that, the clock circuitry (phase generator, buffers) and the rest of digital blocks used after the comparators (D-type flip-flops, delay blocks, logic gates, buffers) are separated from the analog blocks. The distribution of the clock phases and clock signals controlling feedback switches is located at the outer boundary of the modulator. All the important blocks (e.g. comparators, gain blocks with replica bias circuit, digital circuitry) are surrounded by guard rings. The lengths of the important signal paths are minimized in order to reduce their connection resistances and hence the voltage drops across these metal lines. In order to minimize resistance in the path and improve fabrication reliability, the vias and contacts are used liberally whenever the signal has to pass between layers.

In order to minimize noise injection from the digital to the analog circuitry through the power supply and ground connections, separated analog and digital power domains (coming from dedicated pads) are used. The first one is the analog power domain (VDD_A and VSS_A) for integrators, gain blocks with replica bias circuit, and comparators. The second one is the digital domain (VDD_D and VSS_D) for phase generator, D-type flip-flops, delay blocks, logic gates and buffers. The last one is the auxiliary digital domain (VDD_{AUX} and VSS_{AUX}) for auxiliary circuits, e.g. current mode logic buffers. Blocks in these domains are surrounded by guard rings connected to deep N-well layer isolating the substrate. This isolation eliminates the direct connection between the channel of NMOS transistor and the substrate. Although, noise currents can still capacitively couple into the substrate, they are much smaller than in case of the direct connection, when deep N-well layer is not used. The deep N-well also reduces the capacitance between the channel of PMOS transistor and the substrate, thus decreasing the noise coupling. Both these effects contribute strongly to the reduction of the substrate noise currents. Moreover, all the power connections are distributed around the overall circuit and are made wide in order to reduce their resistance and consequently the voltage spikes that can occur across them.

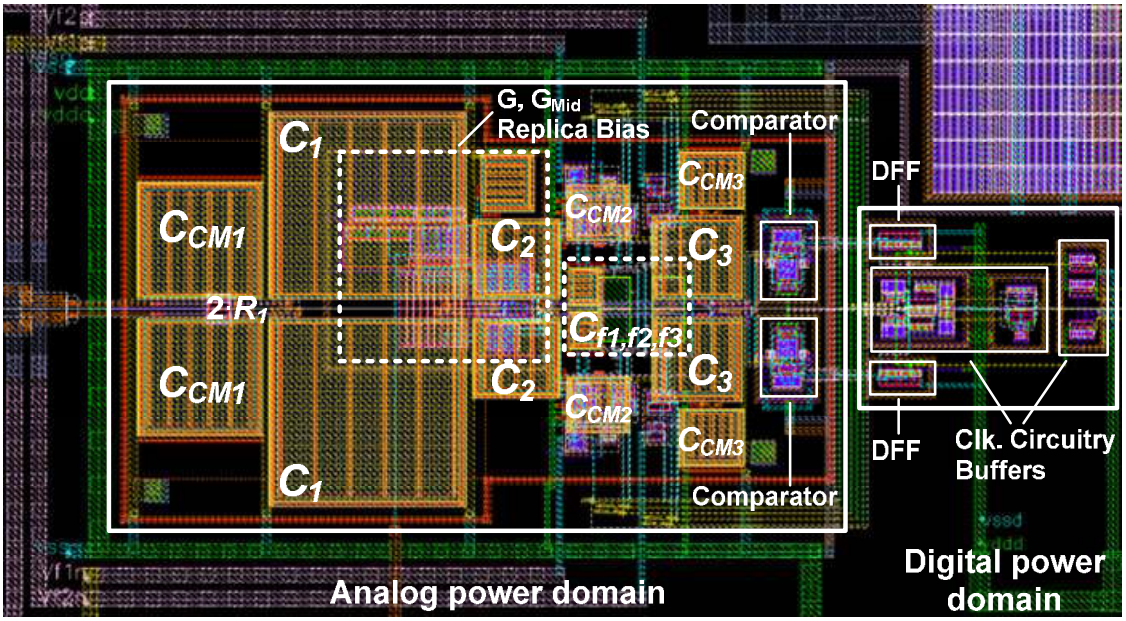

Fig. 6.8 Layout of the 2-1 MASH ΣΔM.

As mentioned before, the circuit is clocked with 1 GHz. Therefore, high frequency digital, full scale signals should not be inputted or outputted to/from the chip in order to avoid large substrate noise caused by the switching. Moreover, at this frequency the 50% duty cycle of the digital signal, passing through a pad and entering circuit, cannot be guaranteed (due to the difference between rise and fall times of the buffers used in the digital pad). Therefore, an external 2 GHz, low amplitude (0.4 $V_{pp,diff}$), sinusoidal clock signal is used, entering the chip through analog pads. Then, on chip, it is amplified (to the digital level: V_{DD} or 0 V) and divided by two to generate the desired 50% duty cycle 1 GHz clock signal. Moreover, the ΣΔM output signals, D_1 and D_2, of both stages of the MASH modulator, are outputted from the chip using current-mode logic (CML) buffers, located close to the output analog pads.

Fig. 6.9 depicts the I/O pad ring, used for interfacing the prototype input and output signals. It contains 22 analog pads. The digital pads are not used for the before mentioned reason. The pad ring is continuous and includes the electrostatic discharge protection. This continuity is obtained with filler and corner cells placed between pad cells. The names and functionality of the used pads are described in Fig. 6.9 and Table 6.3. The three power domains are separated with cutting cells. This minimizes the noise injected from digital to analog blocks through the power supply and ground busses. Fig. 6.10 depicts the micrograph of the test chip die. The ΣΔM occupies an area of about 0.027 mm^2.

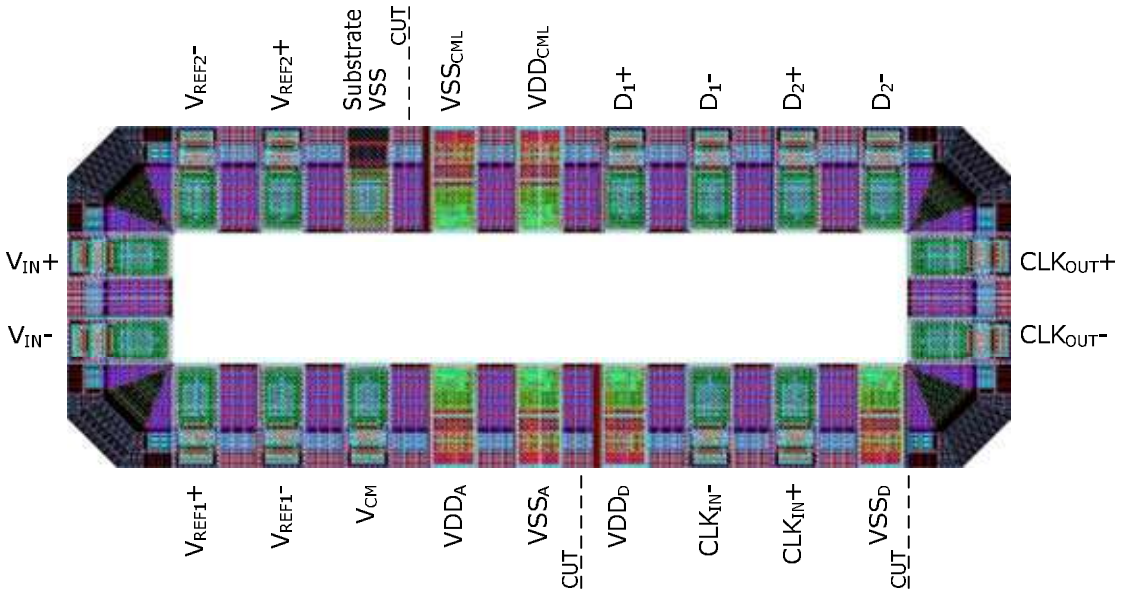

Fig. 6.9 Layout of the pad ring used to interface the 2-1 MASH ΣΔM.

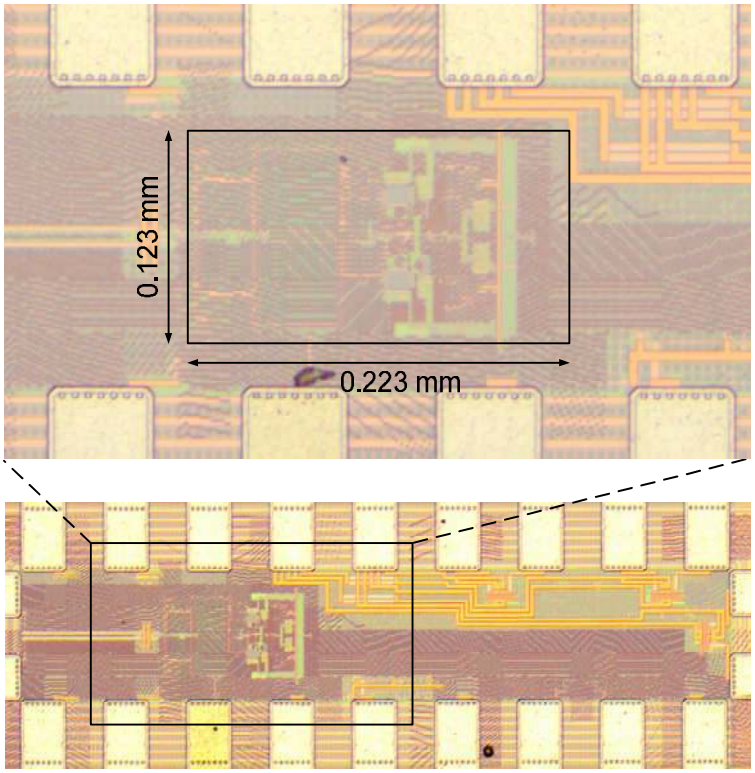

Fig. 6.10 Micrograph of the test chip die in 65 nm CMOS.

Table 6.3 List of pads used to interface the MASH ΣΔMs prototype.

Pad	Value / Amplitude	Functionality
V_{CM}	0.50 V	Common-mode voltage of the gain blocks' replica bias circuit
$V_{REF1,2}+$	0.95 V	Negative reference voltage of the 1st and 2nd integrators
$V_{REF1,2}-$	0.05 V	Positive reference voltage of the 1st and 2nd integrators
$V_{REF3}+$	0.72 V	Positive reference voltage of the 3rd integrator
$V_{REF3}-$	0.28 V	Negative reference voltage of the 3rd integrator
$V_{IN}+$	–	Positive input signal
$V_{IN}-$	–	Negative input signal
$CLK_{IN}+$	0.2 V	Positive clock input signal
$CLK_{IN}-$	–0.2 V	Negative clock input signal
$CLK_{OUT}+$	0.24 V	Positive clock output signal of the ΣΔM data
$CLK_{OUT}-$	–0.24 V	Negative clock output signal of the ΣΔM data
D_1+	0.24 V	The 1st stage ΣΔM output bit-stream (positive)
D_1-	–0.24 V	The 1st stage ΣΔM output bit-stream (negative)
D_2+	0.24 V	The 2nd stage ΣΔM output bit-stream (positive)
D_2-	–0.24 V	The 2nd stage ΣΔM output bit-stream (negative)
VDD_A	1 V	Analog power supply
VDD_D	1 V	Digital power supply
VDD_{AUX}	1 V	Auxiliary digital power supply
VSS_A	0 V	Analog ground
VSS_D	0 V	Digital ground
VSS_{AUX}	0 V	Auxiliary digital ground

6.2.2. Experimental Set-Up

In order to test the MASH ΣΔM, an evaluation printed circuit board (PCB) was designed using the CadSoft tool, EAGLE. The PCB with highlighted main zones is shown in Fig. 6.11. These main areas include: power supplies, input and output signal paths, clock signal path, reference voltages and the place where the DUT is mounted. Similarly to the previous test board design, the PCB has four layers, of which the top and bottom layers are assigned for routing and the two inner ones for power planes and common ground. The board has five power domains (generated from 4 input power connections). For the chip: 1 V analog VDD_A, 1 V digital VDD_D, 1 V auxiliary digital VDD_{AUX} and for the board: 1.2 V analog supply used for the generation of the reference and common-mode voltages, 3.3 V digital voltage for the output buffers.

The DUT power supplies, VDD_A, VDD_D, VDD_{AUX}, are built around CMOS low-dropout linear regulators (Analog Devices ADP1708), which provide high power supply rejection and achieve excellent line and load transient response. The linear regulators for VDD_A and VDD_D are powered up by external 4 V powers supplies, and the linear regulator for VDD_{AUX} is supplied by a 3.3V external voltage (also used for the output buffers). The value of each supply is adjusted with a trimmer resistor. The references and common-mode voltages are built around a precision, low-dropout 1.2 V voltage reference circuit (MAX6120, supplied from a dedicated external 4V

supply voltage) and are independently adjusted to the desired values with a set of trimmer resistors.

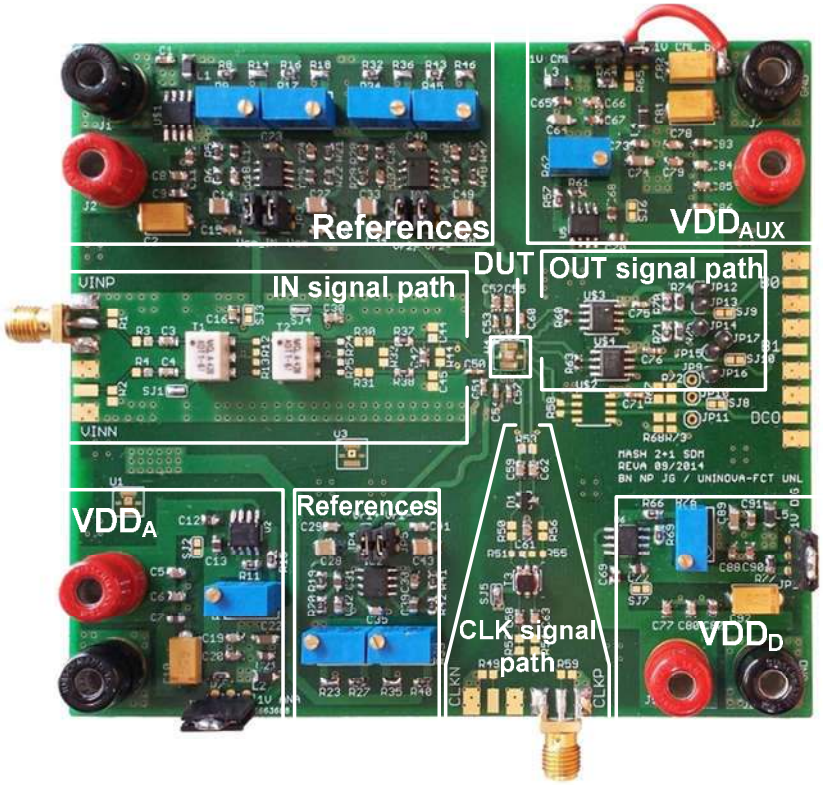

Fig. 6.11. Photograph of the test board for the MASH ΣΔM.

Similarly to the previous test board design, each supply voltage for the reference circuitry and the DUT passes through a ferrite bead and a set of bypass capacitors (some of them are placed very close to the DUT). This approach allows removing (shorting to ground) unwanted AC signal components appearing in the DC power supplies. The values of the bypass capacitors are: 1 nF, 10 nF, 100 nF, 1 µF and 10 µF. More details about the bypassing were presented in section 6.1.2.

The analog input and clock paths are laid out perpendicularly to each other in order to minimize the inductive coupling between them. Since the pairs of analog input and clock signal paths are differential, they are laid out as symmetrically as possible in order to reduce the possibility of signal distortion. This is especially important for the input signal. Moreover, the clock traces and the digital output signals are sized to have a 50 Ω characteristic impedance in order to avoid signal reflections. The output digital traces are delay-equalized (using meanders – zigzag traces). After preparing the test PCB and soldering the components, the chip sample was direct-bonded to the board (chip-on-board technique). This approach allows obtaining a low inductance in the bonding wires and less parasitic influence between the evaluation board and the chip interconnections, because package-related parasitics are avoided. Fig. 6.12 depicts photo of the DUT that is direct bonded to the test board.

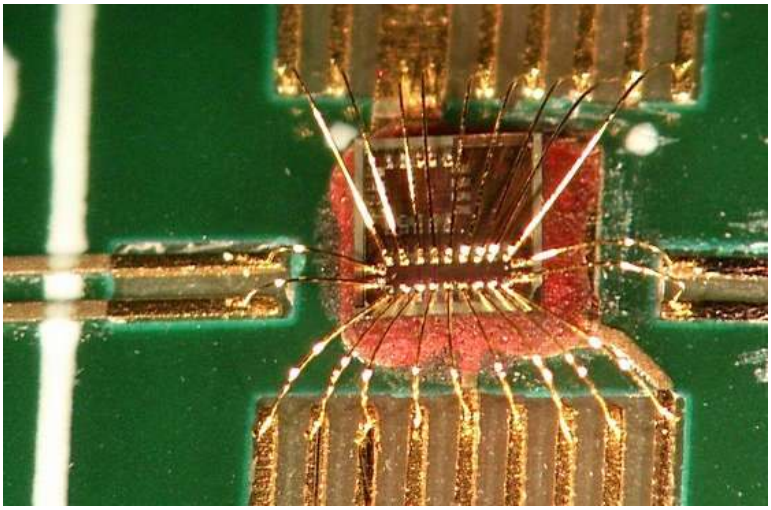

Fig. 6.12 DUT direct bonded to the test board.

Fig. 6.13 shows a simplified schematic of the measurement setup. During evaluation, it is critical to provide a low-distortion and low-noise signal (differential sinusoidal) at the inputs of the DUT, $V_{IN}+$ and $V_{IN}-$. Therefore, the input signal path consists of a low noise signal generator (SMB100A, Rohde&Schwarz), a band-pass filter (Allen Avionics) to attenuate the harmonic distortion and a balun (transformer ADT1-6T, Mini Circuits) performing the single-ended to fully differential conversion. This conversion can add even-order harmonics (mainly the second harmonic) to the signal, due to the transformer nonlinearities caused by its phase and amplitude imbalance. Although the phase and amplitude imbalance of the transformer are small (according to the data sheet), a second transformer (same model) is used after the first one, in order to additionally suppress any distortion that could appear within the effective bandwidth.

The power supply voltages for the chip and PCB are provided by the Tektronix PS 2521G, a programmable power supply with current limiting. An internally buffered, common-mode voltage (DC component) of the input differential signal, for the DUT, is set by a trimmer resistor, connected to the secondary central tap of the second transformer. This voltage is equal to 0.5 V. As mentioned previously, the reference voltages and the common-mode voltage, applied to the DUT, are also regulated by set of trimmers. A first differential reference voltage for the 1st and 2nd integrators is 0.9 V ($V_{REF1,2}+$ = 0.95 V and $V_{REF1,2}-$ = 0.05 V), a second differential reference voltage for the 3rd integrator (second MASH stage) is 0.44 V ($V_{REF3}+$ = 0.72 V and $V_{REF3}-$ = 0.28 V) and a common-mode voltage, V_{CM}, is nominally equal to 0.5 V.

The clock source (CG635, SRS) generates a 2 GHz sinusoidal clock signal with amplitude of 0.4 $V_{pp,diff}$ and a balun (transformer TC4-25X+, Mini Circuits) converts this single-ended signal to differential one. Then, as mentioned previously, on chip, it is amplified (to digital level: V_{DD} or 0 V) and divided by two to generate the 1 GHz clock signal (used by two-phase clock generator).

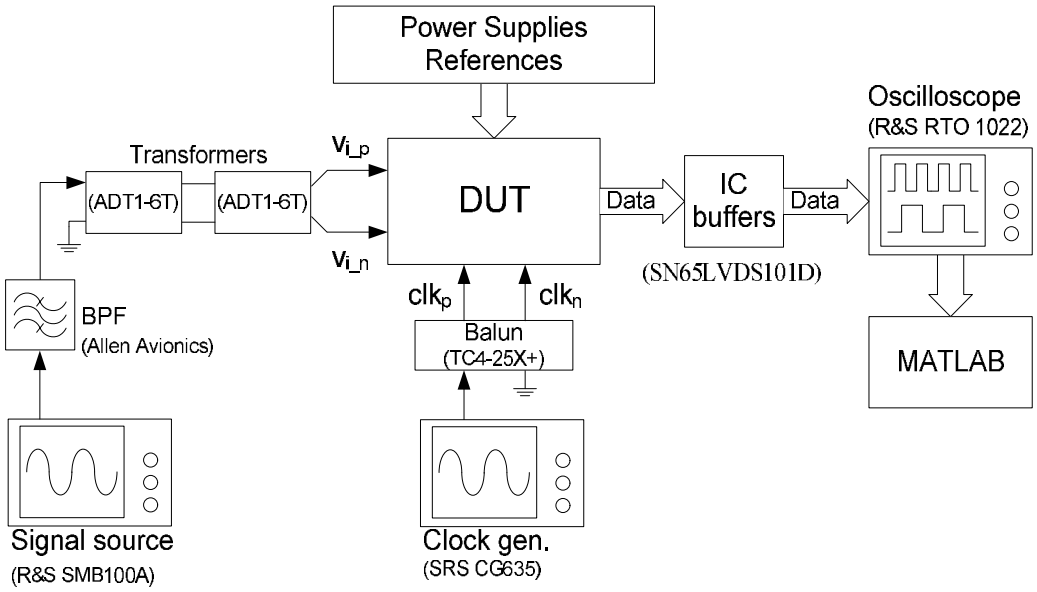

Fig. 6.13. Simplified schematic of the test setup.

The ΣΔM output signals, D_1 and D_2, of both stages of the MASH modulator, are outputted from the chip using current-mode logic buffers. Then, these signals are converted, on the PCB, to positive-emitter-coupled logic (PECL) format by output buffers, high-speed differential receivers and drivers connected as repeaters (SN65LVDS101D, Texas Instruments). These receivers are supplied from the external 3.3 V supply (used also for the linear regulator generating VDD_{AUX}). The final output waveforms are captured on digital oscilloscope (RTO 1022, Rohde&Schwarz) and transferred to a PC for processing. This processing includes the digital cancellation logic (DCL) operation and calculation of power spectral density of the 2-1 MASH ΣΔM output signals (from D_1 and D_2) and additionally power spectral density of the single-loop 2nd-order ΣΔM output signal (only from D_1). The digital cancellation logic coefficients are based on the nominal ΣΔM parameters i.e. α factors, β factors, gain values and feedback factors that were defined during the design phase. In order to minimize the spectral leakage a 64 K Blackman-Harris window is used to plot power spectral density. Moreover, the results are obtained through averaging of eight FFTs.

6.2.3. Measured Results

In this section the measured performance results of the 2–1 MASH ΣΔM and, additionally, the 2nd-order (first stage) modulator are presented. This allows for a comparison between the single-loop and cascaded modulators built using passive integrators and low gain stages. Four evaluation boards with four direct-bonded chip-on-board samples have been assembled and tested. These circuits were evaluated by applying a sine wave input signals with frequencies of 1 MHz and 10 MHz, and with varying amplitude, obtaining the output bit-streams and computing its power spectral density. The presented plots and graphs are from sample II. The tables with measured key performance parameters of all the samples, for the whole MASH modulator and

for the 1st-stage ΣΔM, are presented at the end of this section.

Fig. 6.14 and Fig. 6.15 present the output signal power spectral density of the MASH modulator. The input signal amplitude is 1.16 $V_{pp,diff}$ (-3.2 dB_{FS}) and input signal frequencies, F_{in}, are 1 MHz and 10 MHz. Similar power spectral density plots, shown in Fig. 6.16 and Fig. 6.17, are also obtained for the first stage ΣΔM (single-loop, 2nd-order) output signal. In that case, the input signal amplitude is 1.36 $V_{pp,diff}$ (-1.8 dB_{FS}).

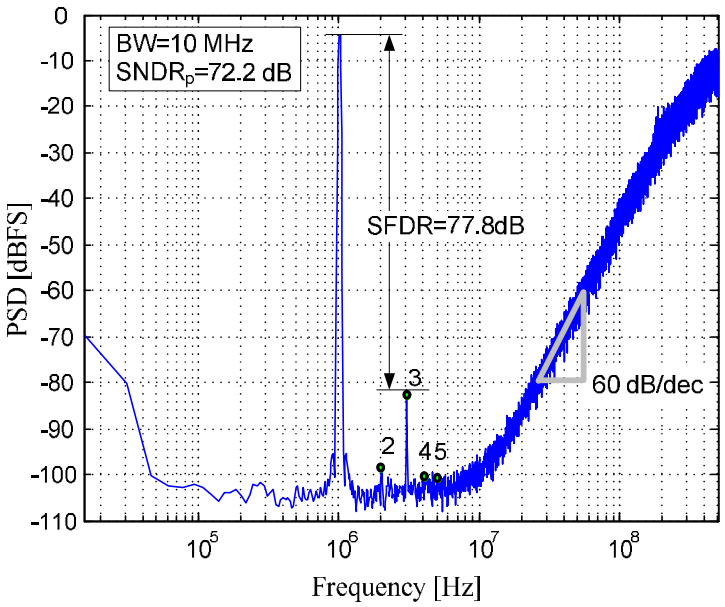

Fig. 6.14. Measured spectra of the 2-1 MASH ΣΔM (sample II) for F_{in}=1 MHz.

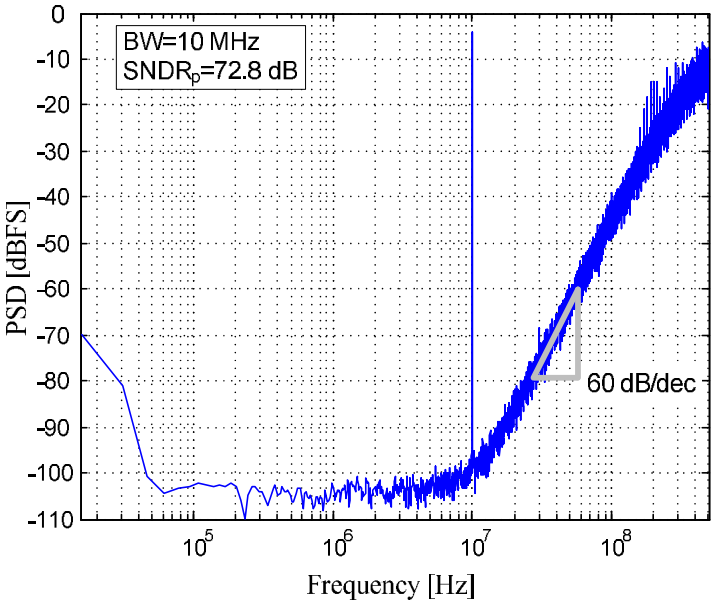

Fig. 6.15 Measured spectra of the 2-1 MASH ΣΔM (sample II) for F_{in}=10 MHz.

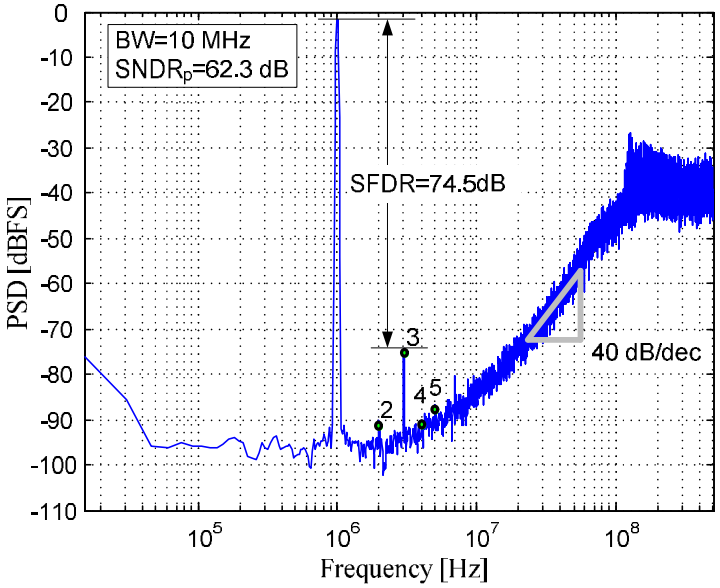

Fig. 6.16. Measured spectra of the 2nd-order ΣΔM (sample II) for F_{in}=1 MHz.

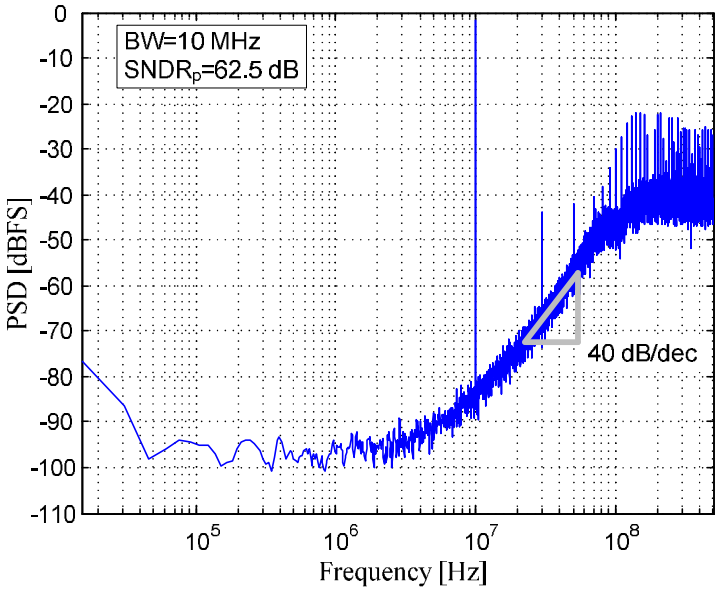

Fig. 6.17 Measured spectra of the 2nd-order ΣΔM (sample II) for F_{in}=10 MHz.

Fig. 6.18 shows a plot obtained for the two-tone test of IMD2/IMD3, performed for the MASH modulator. Input signals are placed near the band-edge (F_{in1}=10 MHz, F_{in2}=9.5 MHz) at -9.2 dB_{FS} amplitudes. Since two input signals are applied, their amplitudes are 6 dB lower than in case presented in Fig. 6.14 and Fig. 6.15 where only one input signal is used. The two-tone test results in IMD2/IMD3 of -78.5/-76.1dB, respectively. Fig. 6.19 shows results of the same test for the first stage ΣΔM (single-loop, 2nd-order), at -7.8 dB_{FS} input amplitudes. In that case IMD2/IMD3 are -77.5/-65.1dB, respectively.

In order to minimize the spectral leakage, a 64 K Blackman-Harris window was used to calculate all the presented power spectral density plots. The results were obtained through

averaging eight FFTs.

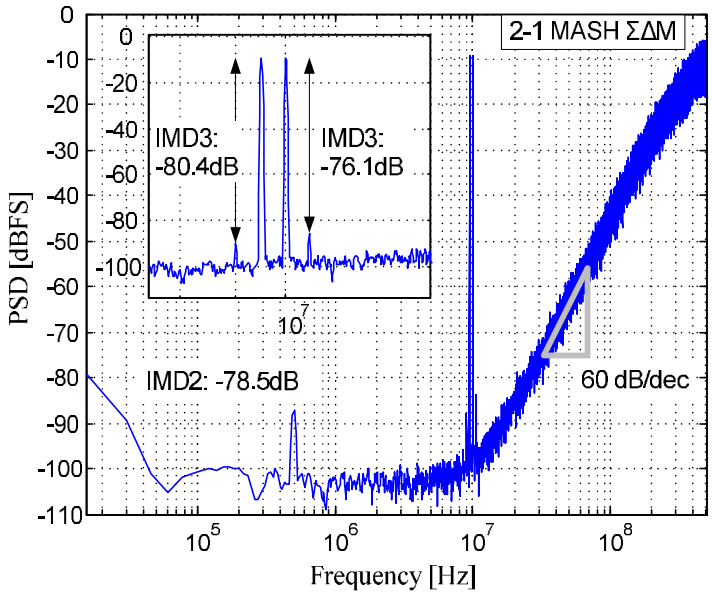

Fig. 6.18 Measured spectra with two input tones near 10 MHz of the 2-1 MASH ΣΔM (sample II).

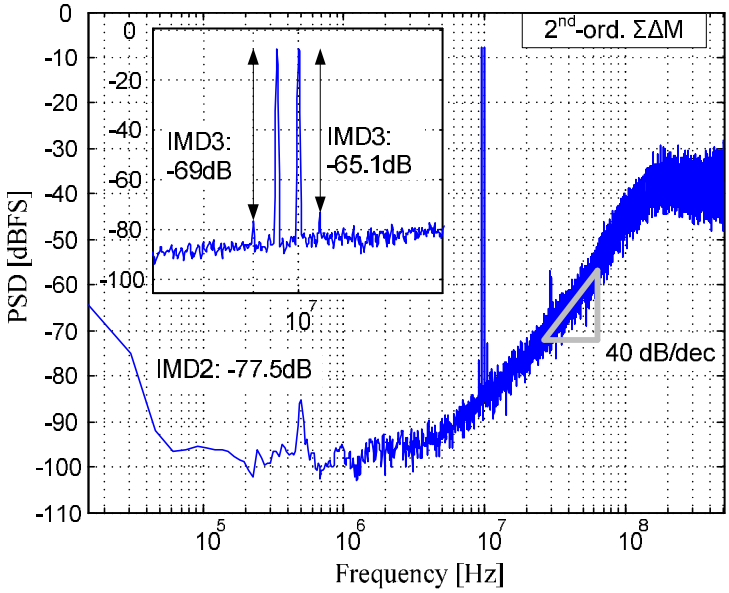

Fig. 6.19 Measured spectra with two input tones near 10 MHz the 2nd-order single-loop ΣΔM (sample II).

Fig. 6.20 and Fig. 6.21 show the SNR/SNDR *vs*. input amplitude graphs (for input signal frequency, F_{in}, of 1 MHz) for 2-1 MASH modulator and single-loop 2nd-order ΣΔM, respectively. Moreover, for the MASH modulator, additional measurements for ±5 % V_{DD} and ±5 % $V_{ref\,i}$ variations were performed. The former one resulted in the worst case peak SNDR of 70.5 dB, while the latter did not affect the modulator's peak SNDR value.

Fig. 6.22 depicts the relation between SNDR and *rms* period jitter of modulators, measured for input signal frequency, F_{in}, of 1 MHz. The jitter was obtained by adding white noise to clock signal.

Fig. 6.23 shows the percentage power break-down of the MASH ΣΔM. In the digital part the most power hungry is the clock tree circuitry, due to the high clock frequency. The analog power is divided between comparators, gain blocks and DAC switches. Most of the power dissipation (98 %) of the reference circuit (external $V_{ref\,i}$-s connected to $C_{f\,i}$) is due to the first integrator feedback circuit.

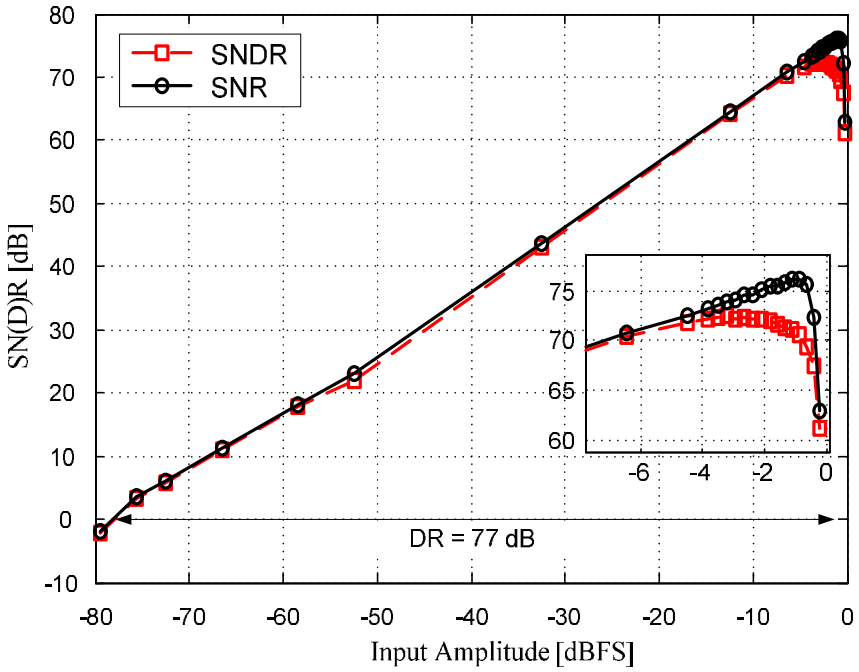

Fig. 6.20 Measured SN(D)R as a function of input signal amplitude for 2-1 MASH ΣΔM (sample II).

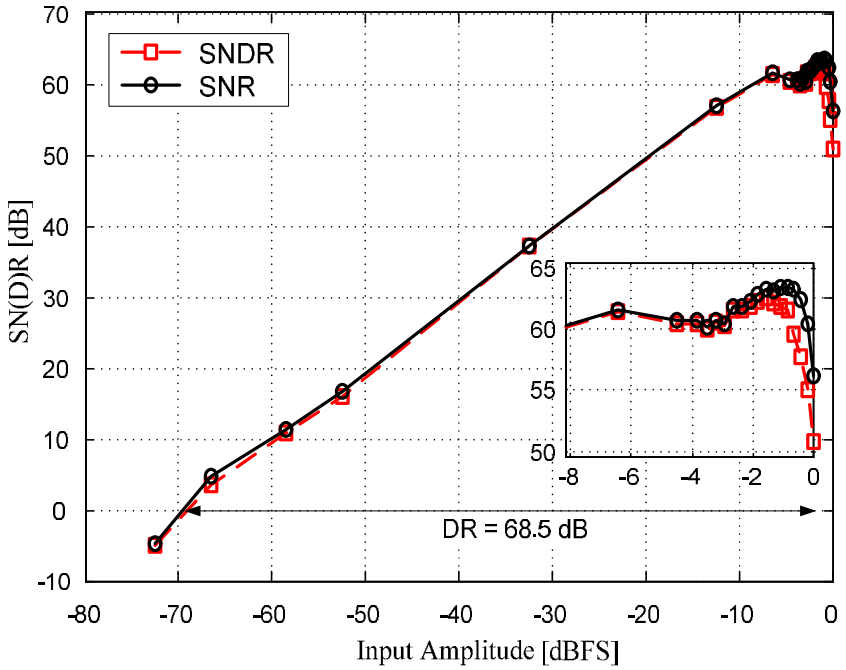

Fig. 6.21 Measured SN(D)R as a function of input signal amplitude 2nd-order single-loop ΣΔM (sample II).

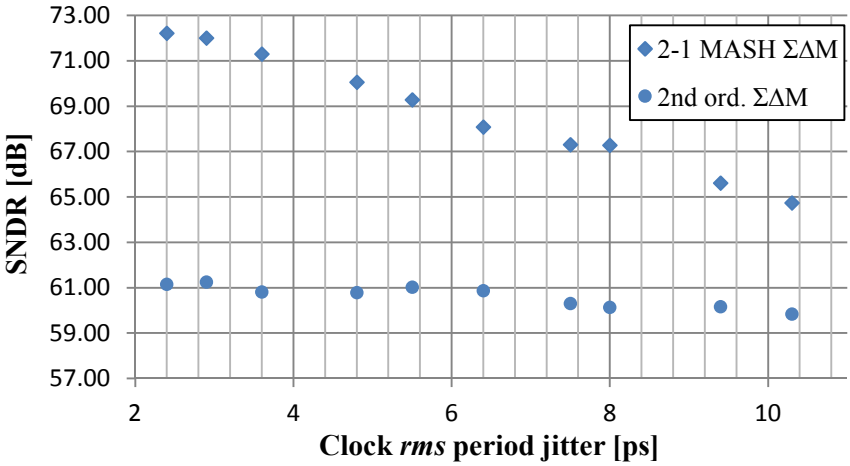

Fig. 6.22 Measured SNDR vs. clock *rms* period jitter, F_{in}=1 MHz, (sample II).

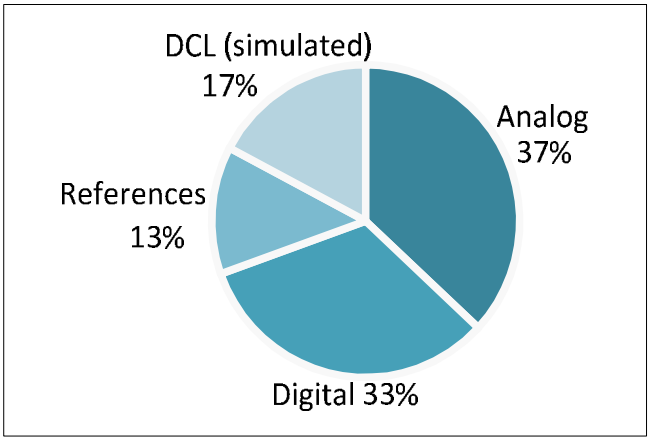

Fig. 6.23 Percentage power break-down of the 2-1 MASH ΣΔM (sample II).

The presented modulator uses the passive integrators that have been discussed in detail in chapter 4.5.The continuous-time passive integrator uses a switched-capacitor branch that implements the feedback DAC operation. As described in [104], the switched-capacitor DAC can reduced the alias rejection of the modulator. Therefore, in order to investigate this issue, an additional PCB was assembled with a new chip-on-board DUT sample. In this case the input transformer (TC4-25X+, Mini Circuits) has a higher bandwidth value, allowing applying to the chip an input signal with frequency, F_{in}, close to the clock frequency. The measurements for various F_{in} from 980 MHz to 1.02 GHz showed an alias suppression of ~51 dB for the MASH modulator as well as for the single-loop 2nd-order ΣΔM (first stage). This means the specification for the anti-aliasing filter can be greatly relaxed due to the alias suppression provided by the modulator and a higher value of the oversampling ratio. If, for example, more than 80 dB alias attenuation is required, a simple *RC* filter would suffice (because it would provide a 40 dB attenuation at 1 GHz).

The measured key performance parameters are depicted in Table 6.4 (for the whole MASH

modulator) and in Table 6.5 (for the 1st-stage ΣΔM). The values of power consumption, P_C, given in Table 6.4 include measured power of the implemented MASH modulator (excluding auxiliary input/output circuitry that are not an integral part of the modulator, such as current-mode logic output buffers) and the simulated power of the synthesized digital cancellation logic (DCL). E.g. in the case of sample II, the measured modulator's power consumption is 1.3 mW and, obtained from the electrical simulation, the power of the DCL is 270uW, giving in total 1.57 mW. This total P_C is shown in the Table 6.4.

The stand-alone 2nd order ΣΔM (first stage of the MASH modulator) together with clock circuitry consumes around 78 % of total MASH modulator power (not including power of DLC, which is not used in this case). This percentage value was estimated from an electrical simulation.

Table 6.4 Measured key performance parameters of the 2–1 MASH ΣΔM (F_{in}=1 MHz).

Sample	Tech. [nm]	F_s [GHz]	BW [MHz]	Area [mm^2]	SNDR$_P$ [dB]	SNR$_P$ [dB]	THD$_P$ [dB]	DR [dB]	P_C* [mW]	FoM$_W$ [fJ/conv-step]	FoM$_S$ [dB]
I	65	1	10	0.027	72.1	74.8	-79.4	75	1.56*	23.6	173
II					72.2	76.1	-81.2	77	1.57*	23.6	175
III					71.7	76.1	-79.5	73	1.53*	24.3	171
IV					71	75.6	-77.7	74	1.53*	26.4	172

* This includes additional power consumption of the synthesized DCL: 0.27 mW (simulated)

Table 6.5 Measured key performance parameters of the 2nd-order ΣΔM (F_{in}=1 MHz).

Sample	Tech. [nm]	F_S [GHz]	BW [MHz]	Area [mm^2]	SNDR$_P$ [dB]	SNR$_P$ [dB]	THD$_P$ [dB]	DR [dB]	P_C* [mW]	FoM$_W$ [fJ/conv-step]	FoM$_S$ [dB]
I	65	1	10	0.024	62.9	63.8	-75.8	69	1*	44	169
II					62.3	63.4	-75.6	68.5	1*	47.7	168
III					62.1	63.7	-75.5	68	0.98*	47	168
IV					61.8	63.3	-74.8	68	0.98*	48.9	168

* Estimated as 78% of the MASH ΣΔM P_C (not including power of DLC)

This section presented layout design and evaluation process of the passive-active 2-1 MASH ΣΔM. The circuit was designed using a 65 nm CMOS technology and four prototype samples were tested. The measured results of the 2–1 MASH ΣΔM and, additionally, the 2nd-order (first stage) modulator were presented. The MASH structure in comparison to the single-loop circuit achieves around 9.5 dB better SNDR, 12 dB better SNR and two times better FoM$_W$, while dissipating around 0.55 mW more power. The key performance parameters are consistent across all integrated circuit samples. The combination of cascaded topology and passive *RC* integrators with low gain blocks results in both the reduction of the power dissipation and of the chip size, as well as in a very low FOM$_W$.

7. CONCLUSIONS AND FUTURE WORK

7.1. Conclusions

This thesis described the analysis, the systematic design methodology and the experimental evaluation of ΣΔMs based on passive integrators and low gain stages. Two design examples have been implemented and manufactured. In the first prototype, a discrete-time 2nd-order ΣΔM, was designed in a 130 nm CMOS technology. The ΣΔM circuit was based on the implementation of discrete-time switched-capacitor integrators using the ultra incomplete settling (UIS) consept. This approach allowed building a ΣΔM with mostly dynamic elements thus reducing the power dissipation. The main purpose of this design was to prove the validity of the UIS concept, which was confirmed by the measured key performance parameters that were consistent across three prototype samples. The 2nd-order ΣΔM circuit (sample III), clocked at 100 MHz and consuming 298 μW, achieved a peak DR/SNR/SNDR of 78.2/73.9/72.8 dB, respectively, for a signal bandwidth of 300 kHz. This resulted in a FoM_W of 139.3 fJ/conv.-step and a FoM_S of 168 dB.

In the second prototype, a continuous-time 2-1 MASH modulator, has been designed in a 65 nm CMOS technology. Its design goal was achieving a moderate resolution (medium SNDR) for a medium signal bandwidth. The measured key performance parameters were consistent across four prototype samples. Table 7.1 compares performance of the DUT from sample II with the state-of-the-art ΣΔMs operating with a signal bandwidth from 5 to 50 MHz.

Table 7.1 Comparison of the 2-1 MASH ΣΔM prototype (sample II) with the prior ΣΔMs.

	2-1 MASH	**2nd-order**	ISSCC '15 [12]	JSSC '14 [31]	ISSCC '13 [6]	VLSI '15 [67]	VLSI '15 [105]
Process [nm]	**65**	65	28	65	28	40	28
Area [mm^2]	**0.027**	0.024	0.34	0.039	0.08	0.0194	0.066
Supply [V]	**1**	1	1.2/1.5	1.1	1.2 / 1.5	-	0.9/1.8
P [mW]	**1.57***	1**	78	1.82	3.9	1.94	3.16
F_S [GHz]	**1**	1	1.8	0.65	0.64	0.6	0.432
BW [MHz]	**10**	10	50	10	18	10	5
DR [dB]	**77**	68.5	85	71.2	78.1	68.7	83.9
SNDR [dB]	**72.2**	62.3	74.6	68.6	73.6	67.4	80.5
FoM_W [fJ/step]	**23.6**	47.7	177.7	41.4	27.7	50.5	36.4
FoM_S [dB]	**175**	168.4	173.1	168.6	174.7	165.8	175.9

* Measured 1.3mW (two MASH stages) + 0.27mW (DCL - simulated)

** Estimated as 78% of the MASH ΣΔM P_C (not including power of DLC, which is not used in this case)

Fig. 7.1 depicts the power efficiency (P_C/(2·BW)) of oversampling ADCs as a function of SNDR, with highlighted position of the prototype MASH modulator (sample II). The cascaded topology of the ΣΔM using passive *RC* integrators and low gain blocks results in high power efficiency and reduction of the chip size. To the best of the author's knowledge the circuit achieves the lowest Walden FOM_W for ΣΔMs with signal bandwidths in the range 5 MHz to 50 MHz, reported to date.

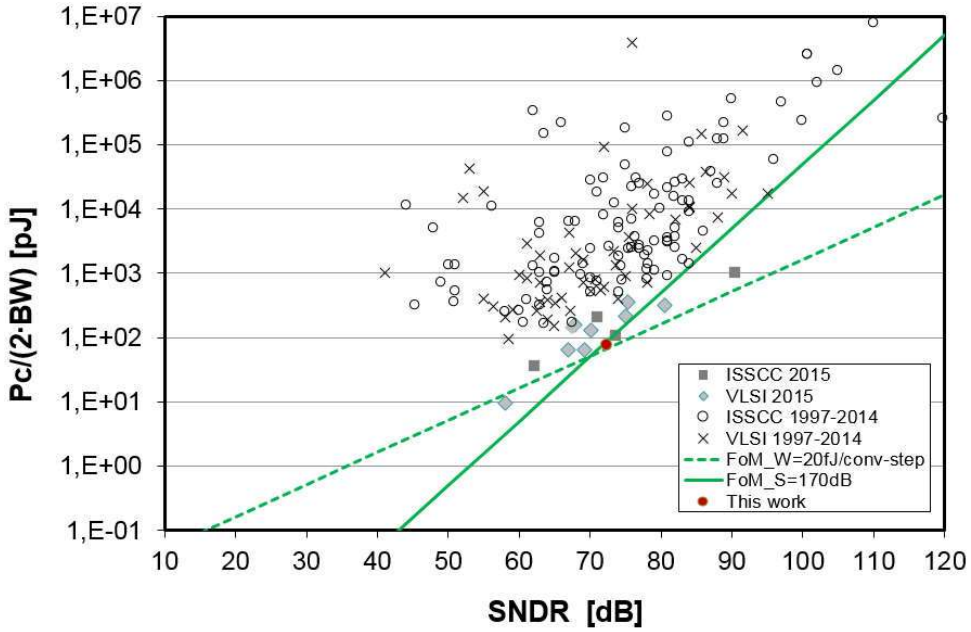

Fig. 7.1 Power efficiency (P_C/(2·BW)) of oversampling ADCs as a function of SNDR [106] (where $FoM_W=P/(2\cdot BW\cdot 2^{(SNDR-1.76)/6.02)}$, $FoMS=SNDR+10\cdot log_{10}(BW/P)$).

Besides the core issue that concerned the implementation of physical prototypes, this research thesis also focused on giving a general overview about the passive and mixed passive-active ΣΔMs.

The proposed discrete-time and continuous-time implementations of passive integrators have been presented in Chapter 4 and their thermal and jitter noise analyzes have been provided as well. In both integrator structures, the thermal noise contribution can be bounded by the nominal capacitance values. Although the discrete-time passive integrator achieves the desired behavior, designing it at higher clock frequencies becomes more challenging due to the necessity of using switches in the input and output signal paths. Fast switching contributes to an increase in power dissipation and parasitic capacitances aggravate non-ideal effects. In order to solve these issues, a continuous-time passive *RC* integrator has been proposed.

Chapter 4 presented also the main operation differences between active and passive ΣΔMs. In an active ΣΔM loop gain is distributed among all its integrators, while in a passive ΣΔM it is mainly concentrated in the quantizer. An SQNR of the passive ΣΔM is defined by the comparator and inter-stage gains, and the peak SNR is limited by the integrators' and the

quantizer's thermal noise.

The use of passive integrators, introduces attenuation in the circuit, resulting in low voltage swings at the output of the integrators. This requires a lower level of thermal noise power in a passive integrator in order to achieve comparable SNR to an active integrator. This can be achieved by using larger capacitors. The thermal noise power in the signal band can also be reduced by increasing the oversampling ratio (OSR) of the ΣΔM. This means that, if the signal bandwidth is increased, the clock frequency would have to increase in order to maintain the same SNDR. The ΣΔM design methodology based on optimization using genetic algorithm (described in the last section of Chapter 4) takes all these factors into account in order to obtain an optimal design.

The passive and passive-active ΣΔMs have less hardware complexity compared to their active counterparts, do not require complex high gain amplifiers and allow for significant reduction of the modulator's power consumption. Chapter 5 presented various ΣΔM case studies and two design examples. The first design example was a 2^{nd}-order single-loop ΣΔM. Its high level model as well as transistor level implementation were analyzed. This ΣΔM, working with clock frequency of 100 MHz, confirmed validity of the ultra incomplete settling concept.
The case studies, analyzed in Chapter 5, included 1^{st}-order, 3^{rd}-order single-loop ΣΔMs and cascaded ΣΔMs. The analysis of different higher order ΣΔM topologies, supported by the optimization, allowed selecting the ΣΔM architecture for the second prototype. It was decided to obtain a moderate resolution (62 dB < SNDR ≤ 74 dB) in a medium signal bandwidth (5 MHz < BW ≤ 20 MHz). The higher order single-loop structure did not ensure sufficient SNDR. Hence, a cascaded modulator architecture has been selected as the most promising one for designing the second prototype. The studies of the high level model and the transistor level implementation of the chosen architecture (2-1 MASH, based on the continuous-time passive integrators and low gain stages) were presented in Chapter 5.4. The goal was to design ΣΔM with bandwidth of 10 MHz and a peak SNDR larger than 70 dB, working with clock frequency of 1 GHz.

The chip floor-planning, layout design, evaluation printed-circuit-board, testing setup and measured data obtained from the experimental evaluation of both ΣΔMs prototypes were presented in Chapter 6. Finally, the conclusions drawn from the measurement results were discussed at the beginning of this section.

7.2. Future Work

The circuit that has been designed and developed in this research thesis achieved the intended performance and power efficiency. Nevertheless, there are few issues that can be further investigated. In this section recommendations for the future work are presented:

- The digital cancellation logic has been synthesized and subjected to electrical simulation. The next step could be its on-chip implementation. Since it is a digital

circuit, its behavior should not change, nevertheless, laying it out together with the both MASH modulator stages would allow testing the complete system.

- During the optimization process of the MASH ΣΔM, in order to reduce the distortion of the first differential pair, its input signal amplitude has been optimized to be smaller than a certain value. Instead of using this absolute criterion, the nonlinear behavior of the gain block could be modeled and then included in the optimization process. This would further improve the correspondence between high-level model and transistor-level circuit.

- In the passive and active-passive ΣΔMs the signal amplitude at the input of the quantizer is significantly reduced. Therefore, a single-bit quantizer (comparator) is commonly used in these modulators instead of multi-bit quantizer. Theoretically, it could be possible to overcome this limitation by employing a time-resolution quantizer, e.g. VCO-based or PWM-based quantizer. This modification could improve modulator's performance. On the other hand, it would increase circuit's complexity, total power dissipation and it would introduce nonlinear effects of either quantizer or multi-bit DAC. Nevertheless, it would be useful to investigate this idea.

- Passive integrators have ability to operate at low supply voltages, thus, the passive loop filter architectures can be used to design ΣΔM with significant power consumption reduction. Since the presented architectures use differential pairs and positive feedback in the comparator to provide the required gain, these circuits could be designed to work at lower power supply voltages (than the nominal one defined by the foundry) and consequently achieve higher power efficiency. In this case it would be important to retain or even improve the modulator's performance with reduced supply voltage.

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