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Design of Ultra-Low Phase Noise and High Power Integrated Oscillator in 0.25μm GaN-on-SiC HEMT Technology

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***Abstract*—A novel ultra-low phase noise and high power integrated oscillator is presented in this letter. The proposed oscillator, based on GaN-on-SiC high electron mobility transistor (HEMT) with 0.25 μm gate length and 800 μm gate width, delivers 21 dBm output power when biased at V_{GS} = -3 V and V_{DD} = 28 V. Phase noise was measured to be -112 dBc/Hz at 100 kHz offset and -135 dBc/Hz at 1 MHz offset from 7.9 GHz carrier, respectively. To the best of our knowledge, it achieves the lowest phase noise compared to other GaN HEMT based integrated oscillators. It is also comparable in performance to the state-of-the-art ultra-low phase noise oscillators designed in InGaP technology, while delivering more than 10 times higher output power. In addition, this oscillator also exhibits a minimum second harmonic suppression of 28.65 dBc and more than 60 dBc third harmonic suppression. The chip size is 1.1 × 0.6 mm^2. The results show that the proposed oscillator has the potential to be used for both low phase noise and high power microwave source applications.**

***Index Terms*—GaN-on-SiC, high electron-mobility transistor (HEMT), integrated oscillator and ultra-low noise.**

I. Introduction

TRADITIONALLY, the majority of microwave oscillators are implemented on gallium arsenide (GaAs), indium phosphide (InP), or silicon germanium (SiGe) technology. As a result, they often have a relatively low output power level requiring the use of additional power amplifiers (PA). This leads to increased system complexity, cost and even causes reliability issues. Gallium nitride (GaN) high electron-mobility transistors (HEMTs) have been recognized as high power and high frequency device for next generation wireless, space, military and many other applications. The fundamental material properties of GaN allow much higher voltage handling and better heat sinking capability compared to InGaP and SiGe [1]. These material advantages enable oscillators to be realized with significant improvement in output power, potentially eliminating the need for additional PAs. Therefore, the research on high power integrated oscillator design in GaN HEMTs technology has attracted much attention in the literature [2-8].

Depending on the applications, the integrated oscillator can be classified as voltage-controlled oscillator (VCO) and fixed frequency oscillator (FFO). The VCO fabricated in GaN HEMTs technology was firstly presented in [2]. This VCO can operate at 6 GHz. It has 10% frequency tuning range, more than 28 dBm output power and phase noise (PN) of -92 dBc/Hz at 100 kHz offset frequency. Other GaN VCOs which also operate at C-band or X-band as presented in [3-5] have limited applications due to their relatively poor PN. A few FFO designs with improved PN had been presented in the literature [6-8], which traded frequency tuning range for PN. Even though high output power can be achieved, the PN of these GaN HEMT based oscillators are still inferior to that of the state-of-art InGaP counterparts [9, 10].

In this letter, an ultra-low PN integrated FFO fabricated in Cree's 0.25 μm GaN-on-SiC HEMT technology is reported. The die was attached on Printed Circuit Board (PCB) and heat sink for measurement purpose. Measurements showed that the proposed FFO operated at 7.9 GHz with 21 dBm output power and a DC-RF efficiency of 8.6%. Furthermore, the PN at 100 kHz and 1 MHz offset frequency was -113 dBc/Hz and -135 dBc/Hz, respectively.

II. Circuit Design and Simulation

The circuit schematic of the proposed oscillator is shown in Fig. 1. The Hartley topology with a fixed LC tank was chosen for the oscillator in order to achieve high output power and ultra-low PN while keeping good harmonic performance [6]. This topology also allows simple tuning of inductors through trimming. As shown in Fig. 1, the parasitic C_{GD} is extracted from the HEMT model, combined with other parasitic, forms the total capacitance C_t between Drain (D) and Gate (G). Inductor L_1 and L_2, with parasitic C_{DS} and C_{GS} absorbed respectively are expressed as L_1' and L_2', and must satisfy the oscillation condition at the frequency of interest. The closed loop gain A_{closed_loop} of the oscillator can be shown as

$$A_{closed\_loop} = \frac{-g_m s^3 L_1' L_2' C_t R_L}{s^3 L_1' L_2' C_t + s^2 (L_1' + L_2') C_t R_L + s L_1' + R_L} = 1, \quad (1)$$

where g_m is the transconductance of M_1 and R_L is the load of

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the oscillator. Shifting all the non-zero terms to one side and equating the imaginary and real part to zero separately gives the oscillation frequency f_{osc} and gain condition as shown below

$$f_{osc} = \frac{1}{2\pi\sqrt{(L_1' + L_2')C_t}}, \quad (2)$$

$$g_m R_L \geq \frac{L_1'}{L_2'}. \quad (3)$$

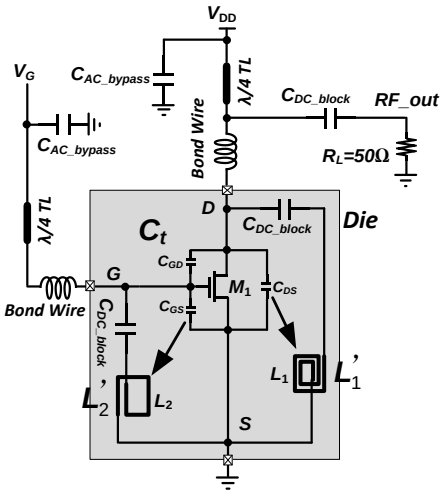

Fig. 1 The simplified circuit schematic of the proposed FFO

Generally, the oscillator should be biased inside or near the Class-C operation region in order to obtain excellent PN performance [11]. While Class-C operation is preferred for better PN, the oscillation condition cannot be satisfied. Measurement results showed that lower V_{GS} and closer to Class-C operation region gave lower PN, thus the lowest V_{GS} that still could maintain the oscillation was chosen. Larger HEMT device is preferred for its high gain when biased near the threshold voltage V_{TH}, which is around -3.1 V. The transistor was biased at V_{DD} = 28 V and V_{GS} = -3 V in this design in order to achieve good PN and high output power at the desired oscillation frequency.

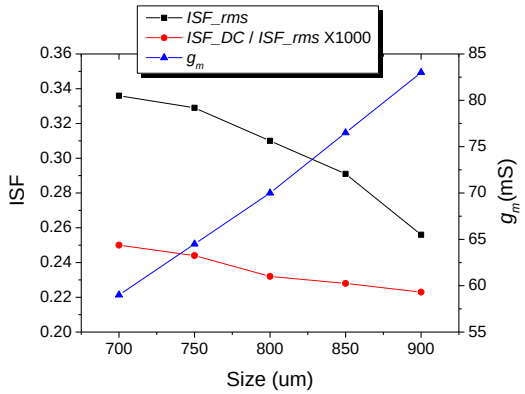

Fig. 2 ISF simulation results

Due to the absence of mature flicker noise model for the GaN HEMT, impulse sensitivity function (ISF) simulation is performed for this GaN FFO to get a good indication of the noise performance, regardless of the flicker noise model. This simulation also helps to determine the suitable device size. ISF_rms indicates the PN level while ISF_DC/ISF_rms indicates the $1/f^3$ corner of PN [12]. It can be seen from Fig. 2 that larger device can provide better PN and lower $1/f^3$ corner frequency simultaneously at the selected V_{GS}. Nevertheless this means larger die size and thus higher cost. In this design, a four-finger device with finger-width of 200 μm and length of 0.25 μm was selected to obtain a g_m = 70 mS to satisfy the start-up condition with reasonable margin.

The circuit was designed and simulated using Agilent Advanced Design System (ADS). The GaN HEMT model was from Cree's PDK. The square spiral inductors were optimized at 7.9 GHz based on electromagnetic (EM) simulations. The EM simulation showed that the unloaded Q values of inductors at 7.9 GHz were above 35, which contributed to a high Q LC tank and thus low PN [13]. Transient and harmonic simulations were also performed with bond wire and PCB effect taken into account. Monitoring these, along with the dynamic load-line at the drain port of the HEMT, the circuit was optimized for output power, PN and harmonic suppression.

III. Measurement Results

Measurements were performed on the test fixture using off-chip RF chokes, which were realized using transmission line (TL), and DC blocking capacitor for output as shown in Fig. 3. The die was attached to the PCB using epoxy, and then attached to the heat sink. The substrate of the PCB is Rogers 4350. Both the power spectrum and PN were measured using an Agilent E4407B spectrum analyzer. In Fig. 4, the output power of the FFO was plotted with the carrier frequency being at 7.9 GHz. The data was taken with the analyzer set to a 100 MHz span and a resolution bandwidth of 300 kHz. The output power was greater than 21 dBm (after taken into account of the 2.2 dB loss of the cable). The DC current was 52mA with a 28V supply, and DC-RF efficiency was calculated as 8.6%. The measurements also showed that second harmonic suppression was greater than 28 dBc and the third harmonic was more than 60 dBc.

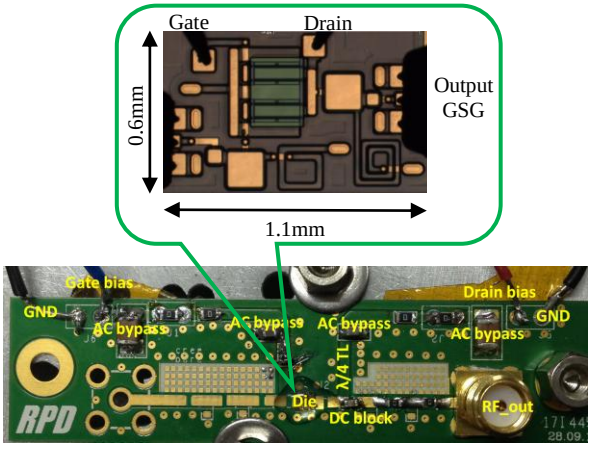

Fig. 3 The die and PCB photograph of the proposed FFO in test fixture

The PN was measured from a 10 kHz to a 100 MHz offset from the carrier as shown in Fig. 5. The measured PN was -112

dBc/Hz and -135 dBc/Hz at offsets of 100 kHz and 1 MHz, respectively.

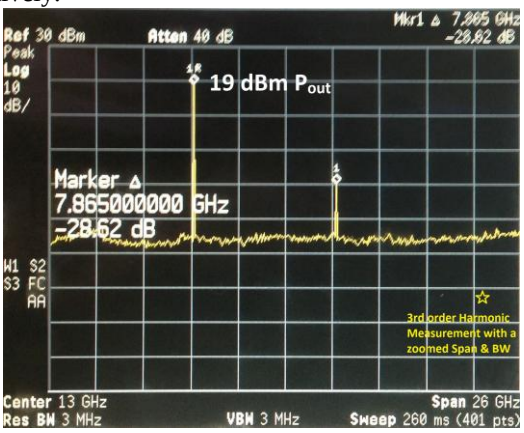

Fig. 4 Measured power spectrum of the proposed oscillator

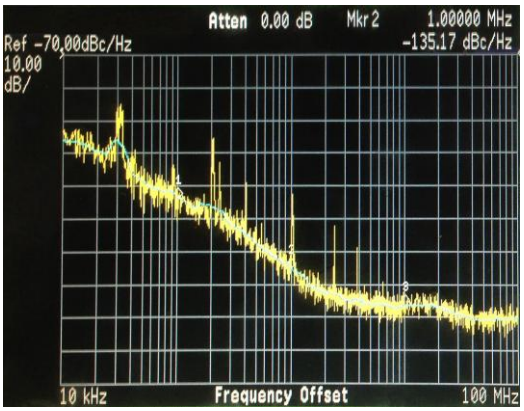

Fig. 5 Measured PN of the proposed oscillator at 7.9 GHz carrier frequency

A comparison of the state-of-the-art oscillators and the proposed oscillator is summarized in Table I. The Figure-of-Merit (FOM) used in this table is defined as

$$FOM = PN - 20\lg\left(\frac{f_{osc}}{\Delta f}\right), \quad (4)$$

where PN is the measured PN at 1 MHz offset frequency, f_{osc} is the oscillation frequency, and Δf is the offset frequency, which is 1 MHz in this case. Note that the FOM in Eqn. (4) does not include the DC power consumption, in contrast to the power-normalized FOM often used for VCOs in CMOS technology. GaN circuits target mainly to achieve high output power and ultra-low phase noise instead of aiming for low power consumption.

It is shown that our design has better FOM than the other designs in GaN HEMT technology. It is also shown that the proposed FFO can achieve much higher output power than the designs in InGaP technology with similar PN performance.

IV. Conclusion

An integrated FFO in GaN-on-SiC HEMT technology is presented in this letter. It is shown that ISF technique is a good way to overcome the lack of mature GaN HEMT flicker noise model in the FFO's design and simulation. It successfully demonstrated that the integrated FFO fabricated in GaN-on-SiC HEMT technology can achieve high power as previously reported, and feature ultra-low phase noise, which makes GaN-on-SiC HEMTs attractive to both high power and low noise microwave source applications.

TABLE I
COMPARISON OF PREVIOUSLY PUBLISHED OSCILLATOR AND THIS WORK

Reference*	Freq. (GHz)	P_{OUT} (dBm)	PN (dBc/Hz)		FOM
			100kHz	1MHz	@1MHz
GaN [2]	6	27	-92	-113	-188.6
GaN [3]	9	31.8	-77	-101	-180.1
GaN [4]	9.3	3.3	-82	-110	-189.4
GaN [5]	7	18	-81	-113	-189.9
GaN [6]	4.2	22.9	-86	-116	-188.5
GaN [7]	5.3	20.5	-105	-130	-204.5
GaN [8]	9.6	32.3	-87	-115	-194.6
This work	**7.9**	**21**	**-112**	**-135**	**-213.0**
InGaP [9]	6.4	5.5	-112	-138	-214.1
InGaP [10]	9.2	1	-111	-133	-212.3

* [2-4, 9-10] are VCOs and [5-8] are FFOs.

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