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Design of Ultra-Low-Power Analog-to-Digital Converters

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Abstract

Power consumption is one of the main design constraints in today's integrated circuits. For systems powered by small non-rechargeable batteries over their entire lifetime, such as medical implant devices, ultra-low power consumption is paramount. In these systems, analog-to-digital converters (ADCs) are key components as the interface between the analog world and the digital domain. This thesis addresses the design challenges, strategies, as well as circuit techniques of ultra-low-power ADCs for medical implant devices.

Medical implant devices, such as pacemakers and cardiac defibrillators, typically require low-speed, medium-resolution ADCs. The successive approximation register (SAR) ADC exhibits significantly high energy efficiency compared to other prevalent ADC architectures due to its good tradeoffs among power consumption, conversion accuracy, and design complexity. To design an energy-efficient SAR ADC, an understanding of its error sources as well as its power consumption bounds is essential. This thesis analyzes the power consumption bounds of SAR ADC: 1) at low resolution, the power consumption is bounded by digital switching power; 2) at medium-to-high resolution, the power consumption is bounded by thermal noise if digital assisted techniques are used to alleviate mismatch issues; otherwise it is bounded by capacitor mismatch.

Conversion of the low frequency bioelectric signals does not require high speed, but ultra-low-power operation. This combined with the required conversion accuracy makes the design of such ADCs a major challenge. It is not straightforward to effectively reduce the unnecessary speed for lower power consumption using inherently fast components in advanced CMOS technologies. Moreover, the leakage current degrades the sampling accuracy during the long conversion time, and the leakage power consumption contributes to a significant portion of the total power consumption. Two SAR ADCs have been implemented in this thesis. The first ADC, implemented in a 0.13-μm CMOS process, achieves 9.1 ENOB with 53-nW power consumption at 1 kS/s. The second ADC, implemented in a 65-nm CMOS process, achieves the same resolution at 1 kS/s with a substantial (94%) improvement in power consumption, resulting in 3-nW total power consumption. Our work demonstrates that the ultra-low-power operation necessitates maximum simplicity in the ADC architecture.

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List of Abbreviations

ADC	Analog-to-Digital Converter
AFE	Analog Front End
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DFF	D-type Flip Flop
DNL	Differential Nonlinearity
DSP	Digital Signal Processor
ENOB	Effective Number of Bit
ERBW	Effective Resolution Bandwidth
FFT	Fast Fourier Transform
FOM	Figure of Merit
INL	Integral Nonlinearity
ISSCC	International Solid-State Circuits Conference
JLCC	J-Leaded Chip Carrier
LPF	Low-Pass Filter
LSB	Least Significant Bit
MIM	Metal Insulator Metal
MSB	Most Significant Bit
SAR	Successive Approximation Register

SFDR	Spurious-Free Dynamic Range
SMR	Signal-to-Metastability-Error Ratio
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion

Chapter 1

Introduction

1.1 Motivation

An analog-to-digital converter (ADC) converts real-world continuous signals to discrete digital numbers. As the interface between the analog world and the digital domain, ADCs are ubiquitous in many applications. The applications that require ultra-low-power consumption in the ADC are frequently found in wireless sensor networks [1][2][3] and biomedical interfaces [4][5].These systems are typically powered by harvested energy or small batteries, thereby placing stringent requirements on the power consumption of the circuits.

Implantable medical electronics, such as pacemakers and cardiac defibrillators, are typical examples of devices where ultra-low-power consumption is paramount. The implanted units rely on a small nonrechargeable battery to sustain a lifespan of up to 10 years. Fig. 1.1 shows a simplified pacemaker system [6]. The ADC is a key component in such systems as the interface between the analog front end (AFE) and the digital signal processor (DSP). The bioelectric signals, shown in Fig. 1.2, have dynamic range between tens of micro-volt to hundreds of milli-volt, and they cover a frequency band where the highest frequency is less than 10 kHz [7]. Measuring these bioelectric signals requires medium-resolution, low-speed ADCs.

This thesis will focus on the design and implementation of ultra-low-power ADCs working at medium resolution (e.g., 10 bit) and low speed (e.g., 1 kS/s) for medical implant devices.

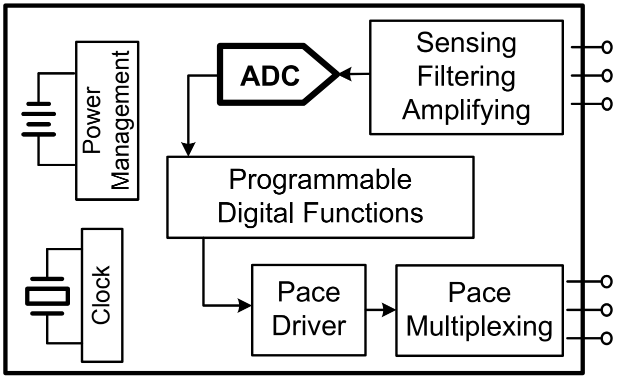

Power Management
Clock
ADC
Sensing Filtering Amplifying
Programmable Digital Functions
Pace Driver
Pace Multiplexing

Figure 1.1: A simplified pacemaker system.

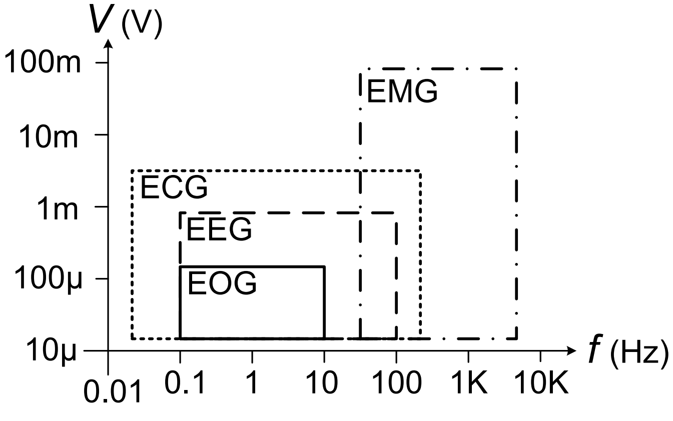
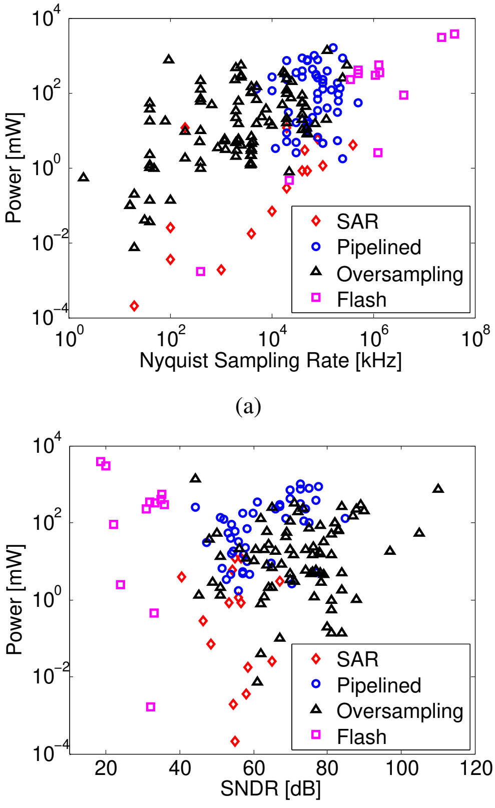


Figure 1.2: Voltage and frequency ranges of four classes of bioelectric signals, where EOG, EEG, ECG, and EMG refer to the electrooculogram, the electroencephalogram, the electrocardiogram, and the electromyogram, respectively.

1.2 Review of Power-Efficient ADC Architectures

Since ultra-low-power operation is critical in the design, architecture selection is driven by an examination of the power consumption of prevalent ADCs. Fig. 1.3 plots the power consumption of ADCs versus the sampling rate and the signal-to-noise-and-distortion ratio (SNDR), respectively. The ADCs were published in the international solid-state circuits conference(*ISSCC*) between 1997 and 2012 [8]. As shown, successive approximation register (SAR) ADCs and oversampling ADCs are typically used for low-speed, medium-to-high resolution applications. Pipelined ADCs dominate at medium-speed and medium-resolution applications, and flash ADCs at high-speed and low-resolution. With respect to the desired speed and resolution, SAR and oversampling ADCs are primary candidates due to their good power efficiency.



(a)

(b)

Figure 1.3: Published ADCs: (a) power vs. Nyquist sampling rate. (b) power vs SNDR.

Figure 1.4 shows the architecture of a basic SAR ADC. It consists of a sample-and-hold circuit, a digital-to-analog converter (DAC), a comparator, and a successive-approximation register. The SAR ADC works based on the binary-search algorithm. First, the input voltage is sampled. Then the conversion starts with an approximation of the most-significant-bit (MSB); the comparator compares the input voltage with half of the reference voltage; the SAR control logic stores the comparison result and simultaneously generates the next approximation; the DAC converts the digital information sent by the SAR to a voltage; based on the DAC output, the comparator does the comparison again. The conversion continues until the least-significant-bit (LSB) is decided. For an N-bit SAR ADC it usually takes at least N clock cycles to complete one conversion. Since there is only one comparator and no amplifiers in the converter, the SAR ADC is highly power-efficient [9]. Moreover, owing to its dynamic nature, the SAR ADC is also amenable to technology scaling [3].

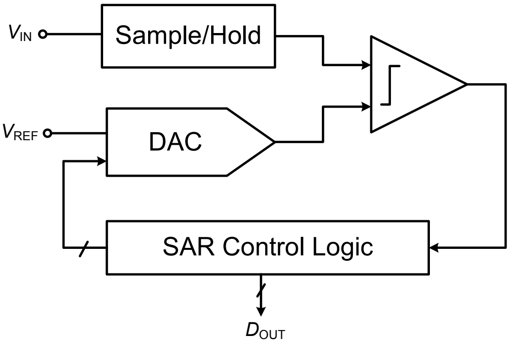


Figure 1.4: A basic SAR ADC.

The oversampling ADC is referred to $\Sigma\Delta$ ADC or $\Delta\Sigma$ ADC. Fig. 1.5 shows the topology of a basic first-order $\Sigma\Delta$ ADC. An integrator and a comparator are in the forward path. A 1-bit DAC in the feedback path provides $\pm V_{REF}$ to the adder input based on the comparator output. The output of the modulator, V_{OUT}, consists of a quantized value of the input signal delayed by one sample period, plus a differencing of the quantization error between the present and previous values [10]. Hence, the transfer function from V_{IN} to V_{OUT} follows that of a low-pass filter. While, the transfer function of the quantization noise follows that of a high-pass filter, thereby pushing the noise out of the signal bandwidth. The modulator is succeeded with a low-pass filter (LPF) which removes the out-of-band quantization noise and downsamples the signal. The oversampling feature of $\Sigma\Delta$ modulation eases the anti-aliasing requirements. In addition, the noise shaping characteristic makes $\Sigma\Delta$ ADC dominate in high-resolution regime [11][12].

Nonetheless, among the designs plotted in Fig. 1.3, SAR ADCs consume the lowest power in medium-resolution and low-speed regime. The ADC designs presented

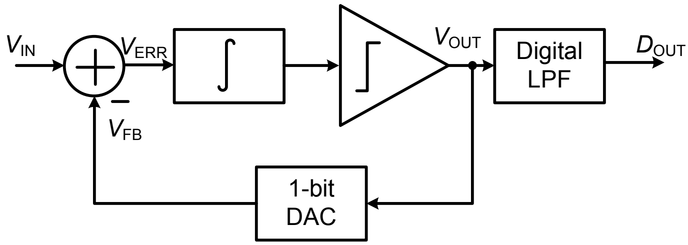


Figure 1.5: A basic first-order $\Sigma\Delta$ ADC.

in this thesis will utilize the SAR architecture. Ultra-low-power design challenges, strategies, as well as circuit techniques of SAR architecture will be addressed in the thesis.

1.3 Design Challenges and Strategies

As mentioned previously, conversion of the low frequency bioelectric signals does not require high speed, but ultra-low-power operation (e.g. in nW range). This combined with the required conversion accuracy makes the design of such ADCs a major challenge. So far, most of the research on ADCs has been focused on medium- and high-speed applications, while efficient design methodologies and circuit techniques for low-speed and ultra-low-power ADCs have not been explored in depth.

Trading speed for lower power consumption at such slow sampling rate is not a straightforward task. The major challenge is how to efficiently reduce the unnecessary speed and bandwidth for ultra-low-power operation using inherently fast devices in advanced CMOS technologies. Moreover, the leakage current degrades the sampling accuracy during the long conversion time, and the leakage power consumption contributes to a significant portion of the total power consumption. As an example, Fig. 1.6 shows the average power consumption of an inverter as a function of its switching frequency. The power consumption was simulated at two different supplies (1.0 V and 0.4 V) over two different sizes ($\mathrm{W_{min}/L_{min}}$ and $\mathrm{W_{min}/2L_{min}}$). It can be seen that the leakage power at 1-10 kHz can constitute more than 50% (50% at 10 kHz) of the total power.

Considering the above discussion and the fact that every nano-watt counts for such ADCs, the main key to achieve the ultra-low-power operation turns out to be the maximal simplicity in the ADC architecture and low transistor count. This essentially means that we avoid ADC techniques with additional complexity and circuit overhead, which are useful for higher sampling rates. Digital error correction [13][14][15] has been frequently used in high-speed ADCs, where capacitor redundancy is utilized to meet the linearity requirement without degrading the speed. However, the circuit overhead required for the digital post-processing leads to additional switching and

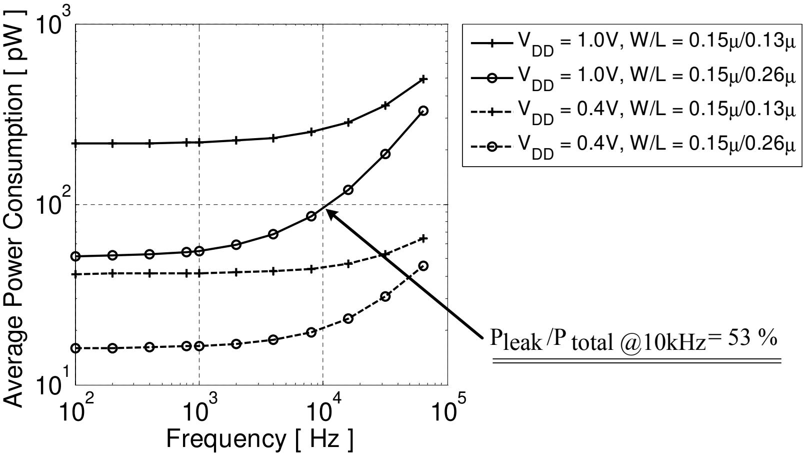


Figure 1.6: Simulated average power consumption versus switching frequency of an inverter with a fan-out of four in 0.13-μm CMOS process.

leakage power consumption. On-chip digital calibration [16][17] serves as an alternative solution without large amount of digital post-processing, but it requires additional calibrating capacitor arrays and registers. Besides, to ensure the calibration efficiency, the comparator offset should be removed prior to linearity calibration.

Taking advantage of the low speed, the proposed ADCs utilize matched capacitive DACs, being sized to achieve the targeted conversion accuracy without digital error correction or calibration, thus eliminating additional devices and significant leakage currents. Moreover, the matched capacitive DACs use switching schemes that allow full-range input sampling without additional voltage sources. The two designed SAR ADCs utilized a top-plate sampling scheme and a bottom-plate sampling scheme, which will be described in Chapter 4 and Chapter 5, respectively. Compared to the energy-efficient switching schemes [9][18][19], the employed approaches introduce less overhead in the SAR control logic [9][19] and avoid additional bias voltages in the comparator [18].

To further reduce the power consumption, lowering the supply voltage was employed in both ADCs. The first ADC in 0.13 μm process utilized a dual-supply voltage scheme which allows the SAR logic to operate at 0.4 V, reducing the overall power consumption of the ADC by 15% without any loss in performance. In dual-supply mode (1.0 V for analog and 0.4 V for digital), the ADC consumes 53 nW at a sampling rate of 1 kS/s and achieves the effective-number-of-bit (ENOB) of 9.1 bit. The second ADC took advantage of the availability of standard- and high-V_T devices in 65 nm process. The utilized multi-V_T design allowed the ADC to achieve 9.1-ENOB and consume 3-nW power consumption with a single supply voltage of 0.7 V, thereby reducing both the switching and leakage power consumption. Our measurement results (in Sec. 5.4) show that the ADC can operate down to a supply voltage of 0.6 V, achieving an optimal energy efficiency of 4.5 fJ/conversion-step with 8.8 ENOB at 1 kS/s.

1.4 Thesis Organization

This thesis outlines the study and designs of ultra-low-power SAR ADCs and is a result of the research performed at the Devision of Electronic Devices, Department of Electrical Engineering, Linköping University between April 2009 and June 2012. The research during this period has resulted in the following publications:

- **Dai Zhang** and Atila Alvandpour, ”A 3-nW 9.1-ENOB SAR ADC at 0.7 V and 1 kS/s”, accepted for publication in *proceedings of the European Solid-State Circuit Conference (ESSCIRC)*, Bordeaux, France, September 2012 [20].
- **Dai Zhang**, Ameya Bhide, and Atila Alvandpour, ”A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-μm CMOS for Medical Implant Devices”, in *IEEE Journal of Solid-State Circuits*, vol.47, no.7, pp.1585-1593, July, 2012 [21].
- **Dai Zhang**, Ameya Bhide, and Atila Alvandpour, ”A 53-nW 9.12-ENOB 1-kS/s SAR ADC in 0.13-μm CMOS for Medical Implant Devices”, in *proceedings of the European Solid-State Circuit Conference (ESSCIRC)*, pp.467-470, Helsinki, Finland, September 2011 [22].
- **Dai Zhang**, Christer Svensson, and Atila Alvandpour, ”Power consumption bounds for SAR ADCs”, in *proceedings of the European Conference on Circuit Theory and Design (ECCTD)*, pp.556-559, Linköping, Sweden, August 2011 [23].
- **Dai Zhang**, Ameya Bhide, and Atila Alvandpour, ”Design of CMOS sampling switch for ultra-low power ADCs in biomedical applications”, in *proceedings of the Norchip Conference*, pp.1-4, Tempera, Finland, November 2010 [24].

The rest of this thesis is organized as follows. Chapter 2 discusses the precision considerations of SAR ADC blocks. The analysis of power consumption bounds for SAR ADCs is described in Chapter 3. In Chapter 4 and Chapter 5, two SAR ADC designs are presented: a 53-nW 9.1-ENOB SAR ADC in 0.13 μm CMOS and a 3-nW 9.1-ENOB SAR ADC in 65 nm CMOS. Finally, the thesis is concluded in Chapter 6.

Chapter 2

SAR ADC Precision Considerations

During the conversion from an analog signal to a digital word, three major tasks are performed by the ADC: sampling, quantization, and comparison. For a SAR ADC, the three tasks are correspondingly executed in the sampling circuit, the capacitive DAC, and the comparator. In this chapter, we will analyze the design considerations of each block.

2.1 Sampling Circuit

A basic sampling circuit consists of a switch and a capacitor, shown in Fig. 2.1(a). When the switch is on, the input voltage is connected to the top-plate of the sampling capacitor. When the switch is off, the top-plate node of the capacitor is isolated, and the capacitor holds the sampled voltage value. Generally, the switch can be implemented by PMOS, NMOS, or CMOS devices. Fig. 2.1(b) shows the on-resistance versus the input voltage for the three types of switch. Compared with NMOS and PMOS, the CMOS switch has the lowest on-resistance and allows full-range input sampling.

The general design considerations of the sampling circuit are: thermal noise, aperture error, switch-induced error, track bandwidth, and voltage droop.

2.1.1 Thermal Noise

The thermal noise, introduced by the on-resistance of the switch, is given by kT/C_S, where k is the Boltzmann constant, T is the absolute temperature, and C_S is the sampling capacitor. Since the thermal noise appears as random errors which can't be calibrated, it will degrade the signal-to-noise ratio (SNR).

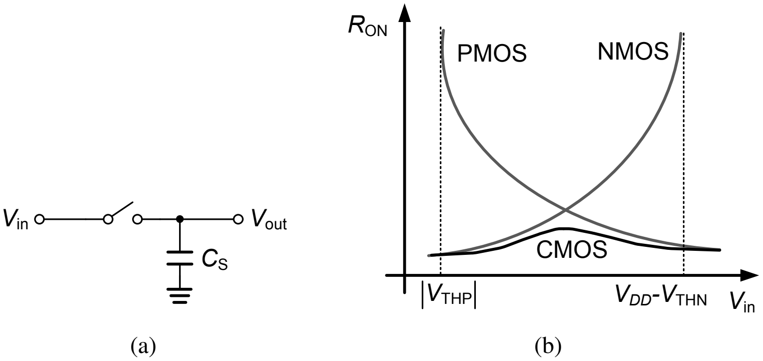


Figure 2.1: Sampling circuit:(a) basic circuit (b) switch on-resistance versus input voltage.

As we know, the quantization noise sets a fundamental limit on the SNR of the ADC. If we consider an N-bit ADC with a full-scale range voltage of V_{FS}, the quantization noise is given by

$$\overline{V_q^2} = \frac{V_{FS}^2}{12 \cdot 2^{2N}} \tag{2.1}$$

Assuming that the thermal noise is designed to be equal to the quantization noise, the total noise power will be increased by a factor of 2, thus decreasing the SNR by 3 dB. Then, the minimum value of sampling capacitor C_S can be calculated by

$$C_S = 12kT\frac{2^{2N}}{V_{FS}^2} \tag{2.2}$$

To get some feeling for the value of the sampling capacitor, Table 2.1 lists a set of capacitance versus ADC resolution for 1-V V_{FS}.

Table 2.1: Required Minimum Capacitance Versus Resolution based on Eq. (2.2)

N	C_S	unit
8	3	fF
9	13	fF
10	52	fF
11	208	fF
12	833	fF

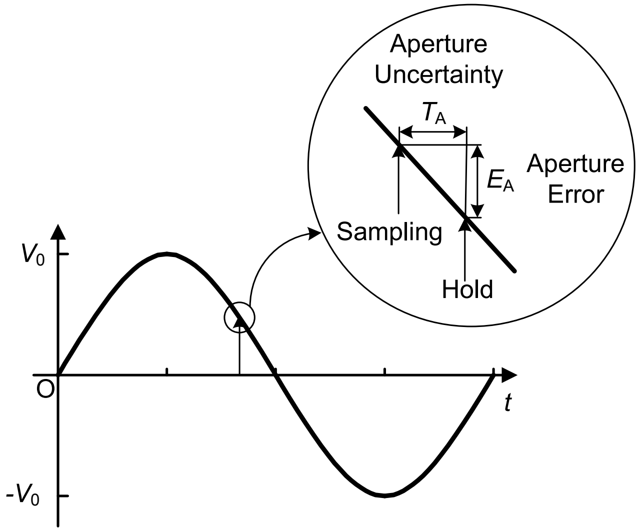


Figure 2.2: Aperture error.

2.1.2 Aperture Error

Aperture error is caused by the uncertainties in the time from sample mode to hold mode, as shown in Fig. 2.4. This variation is mainly due to the noise on the sampling clock. The aperture error voltage, denoted as E_A, depends on the slew rate of the input signal and the aperture uncertainty, denoted as T_A. For a sine wave input as shown, the maximum slew rate occurs at the zero crossing point and is given by

$$\frac{dV}{dt}|_{max} = 2\pi f_{IN} V_0 \tag{2.3}$$

where f_{IN} is the input frequency and V_0 is the input amplitude. To ensure the aperture error to be less than 1/2 LSB at the point of maximum slew rate, for N-bit converter we have

$$2\pi f_{IN} V_0 T_A < \frac{1}{2} LSB = \frac{2V_0}{2^{N+1}} \tag{2.4}$$

Hence the maximum input frequency is given by

$$f_{IN@MAX} = \frac{1}{\pi \times 2^{N+1} \times T_A} \tag{2.5}$$

Equation (2.5) can also be applied to the context of sampling time jitter. For instance, when a 10-bit converter suffers a jitter of 1 ps, the input frequency should be less than 150 MHz.

2.1.3 Switch-Induced Error

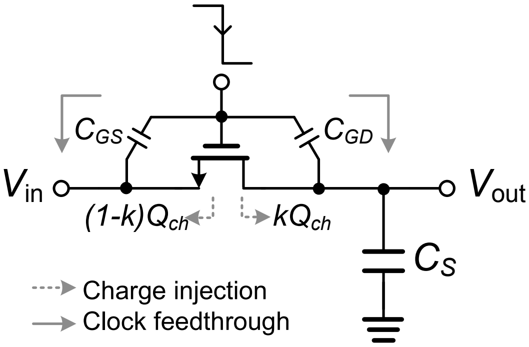


Figure 2.3: Sources of switch-induced error of sampling circuit.

Charge injection and clock feedthrough, shown in Fig. 2.3, collectively known as the switch-induced error, are the major error sources caused at the moment the switch turns off. Charge injection introduces error to the sampled voltage by depositing part of the charge from the conduction channel of the transistor onto the sampling capacitor. Clock feedthrough affects the sampled voltage by capacitance coupling during the transition of the sample signal. The switch-induced error voltage for both NMOS and PMOS can be approximated as [25]

$$\Delta V_{e,N} = -\frac{kW_N L_N C_{OX}(V_{DD} - V_{THN} - V_{IN})}{C_S} - \frac{C_{GD,N}}{C_S + C_{GD,N}} V_{DD} \quad (2.6)$$

$$\Delta V_{e,P} = \frac{kW_P L_P C_{OX}(V_{IN} - |V_{THP}|)}{C_S} + \frac{C_{GD,P}}{C_S + C_{GD,P}} V_{DD} \quad (2.7)$$

where k is the fraction of charge injected on the output node, C_{OX} is the gate-oxide capacitor, V_{THN} and V_{THP} are the threshold voltages, and $C_{GD,N}$ and $C_{GD,P}$ are the gate-drain overlap capacitance of NMOS and PMOS, respectively. In Eq. (2.6) for NMOS (respectively PMOS), the first part of the right-half side represents the charge injection error, which varies with the input signal in a linear fashion if body effect is neglected. The second part represents the clock feedthrough error, which is input-independent and can be taken as an offset error.

Since charge-injection error voltage is input-dependent, which will introduce conversion linearity error, it should be alleviated. A straightforward way is to increase the sampling capacitance with a sacrifice of speed. Alternative techniques, such as bottom-plate sampling, can also be used to reduce the error.

2.1.4 Track Bandwidth

The sampling circuit forms a low-pass RC network, which determines the track bandwidth

$$f_{3dB} = \frac{1}{2\pi R_{ON} C_S} \tag{2.8}$$

where R_{ON} is the on-resistance of the switch. Based on its exponential response, the time budget for the sampled voltage to settle with an error less than 1/2 LSB for N-bit resolution can be derived from

$$e^{-\frac{t}{R_{ON} C_S}} < \frac{1}{2^{N+1}} \tag{2.9}$$

Further assuming that a half-period sampling-clock is used as the time budget, it requires

$$f_{3dB} > \frac{ln2 \times (N+1)}{\pi} f_S \tag{2.10}$$

where f_S is the sampling frequency.

The switch resistance is strongly signal-dependent, thus leading to varying track bandwidth. For mid-rail input voltage, the switch resistance goes to the maximum value, which determines the minimum track bandwidth. Under this circumstance, Eq. (2.10) should be satisfied. Otherwise, the limited bandwidth will introduce nonlinear errors to the sampling.

2.1.5 Voltage Droop

Voltage droop introduced by the leakage current of the switch becomes a critical error source as the sampling rate goes low. The subthreshold leakage current of the transistor is the dominant leakage contributor to the switch, which is expressed as [26]

$$I_{DS} = \mu_0 C_{OX} \frac{W}{L} (m-1) V_T^2 \times e^{\frac{V_{GS} - V_{TH}}{m V_T}} \times (1 - e^{-\frac{V_{DS}}{V_T}}) \tag{2.11}$$

where m is the subthreshold swing coefficient, and V_T is the thermal voltage. Eq. (2.11) indicates that the leakage current shows nonlinear dependence on the input-output voltage difference across the switch, thereby introducing harmonic distortions.

2.2 Capacitive DAC

Once the input voltage is sampled, the ADC maps the input value to a corresponding digital form based on a set of reference voltages. This process is called quantization. In a SAR ADC, a capacitive DAC is commonly used to generate wighted reference voltages. Compared to a resistive DAC, the capacitor array is more easily fabricated with less mismatch errors, and it is also more power-efficient.

In this section, we will discuss the mismatch errors of capacitive DACs with a focus on two commonly-employed architectures: single binary-weighted array and split binary-weighted array.

2.2.1 Single Binary-Weighted Capacitive Array

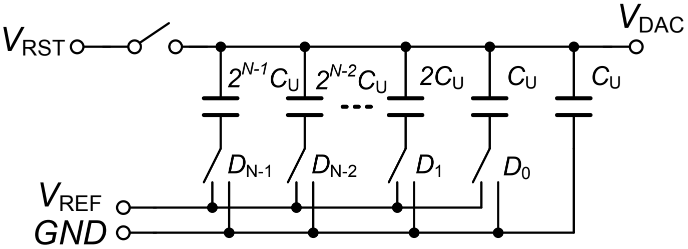


Figure 2.4: A single binary-weighted capacitive DAC.

Figure 2.4 shows a single binary-weighted capacitive DAC. It mainly works at two modes. During the reset mode, all the bottom-plate nodes are reset to ground and the top-plate node is connected to a reset voltage, allowing the capacitors to discharge. When comes to the conversion mode, the digital codes determine the switch status, generating a corresponding reference voltage.

The unit capacitor, denoted as C_U, should be kept as small as possible for power saving. In practice, it is usually determined by the thermal noise and capacitor mismatch. In Sec. 2.1.1, we have discussed the thermal noise. Here, we will focus on the mismatch.

Generally, the unit capacitor is modeled with a nominal value of C_u and a standard deviation of σ_u. For a binary-weighted capacitor array, the worst-case standard deviation of differential nonlinearity (DNL) and integral nonlinearity (INL) occur at the MSB code transition due to the accumulation of the capacitor mismatch. Following the analysis in [27], they can be expressed in terms of LSB as

$$\sigma_{DNL,MAX} = \sqrt{2^N - 1}\frac{\sigma_u}{C_u}LSB \tag{2.12}$$

$$\sigma_{INL,MAX} = \sqrt{2^{N-1}}\frac{\sigma_u}{C_u}LSB \tag{2.13}$$

Comparing Eq. (2.12) with Eq. (2.13), the derived worst-case standard deviation of DNL is larger than that of INL. Therefore, Eq. (2.12) is chosen to be a reference in the following analysis. For a typical metal-insulator-metal (MIM) capacitor, it has

$$\sigma(\frac{\Delta C}{C}) = \frac{K_\sigma}{\sqrt{A}} \tag{2.14}$$

$$C = K_C \cdot A \tag{2.15}$$

where $\sigma(\Delta C/C)$ is the standard deviation of capacitor mismatch, K_σ is the matching coefficient, A is the capacitor area, and K_C is the capacitor density parameter.

The standard deviation of a single capacitor to the nominal value is by factor $\sqrt{2}$ smaller than that of the difference between two capacitors. Thus, $\sigma(\Delta C/C)$ divided by $\sqrt{2}$ is equal to σ_u/C_U. For high yield, it is necessary to maintain $3\sigma_{DNL,MAX} < 1/2LSB$. Combining the earlier equations, we obtain a lower bounds for the mismatch-limited unit capacitor

$$C_U = 18 \cdot (2^N - 1) \cdot K_\sigma^2 \cdot K_C \tag{2.16}$$

Assuming a MIM capacitor in certain technology has a density of 2 fF/μm^2 and a matching of 1% μm. It leads to a minimum unit capacitance of 4 fF.

So far, the discussion is for the single-ended architecture. For the differential configuration, the unit capacitance can be reduced by half while still satisfying the mismatch requirement. This is because the differential mode doubles the signal range but only increases $\sqrt{2}$ times of the error voltage introduced by the mismatch.

2.2.2 Split Binary-Weighted Capacitive Array

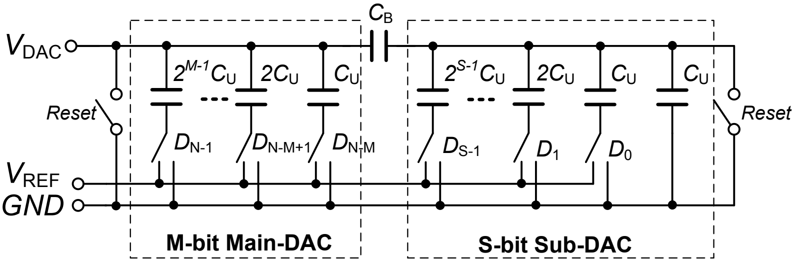


Figure 2.5: A split binary-weighted capacitive DAC.

A split binary-weighted capacitive DAC, shown in Fig. 2.5, is commonly used to reduce the total size of the capacitive array. It consists of an M-bit main-DAC and an S-bit sub-DAC, where $M + S = N$. Via a bridge capacitor, denoted as C_B in Fig. 2.5, the sub-DAC interpolates between transition voltages generated by the main-DAC. The bridge capacitance is commonly chosen to be the ratio of total sub-DAC capacitance and total main-DAC capacitance

$$C_B = \frac{2^S}{2^M - 1} \cdot C_U \tag{2.17}$$

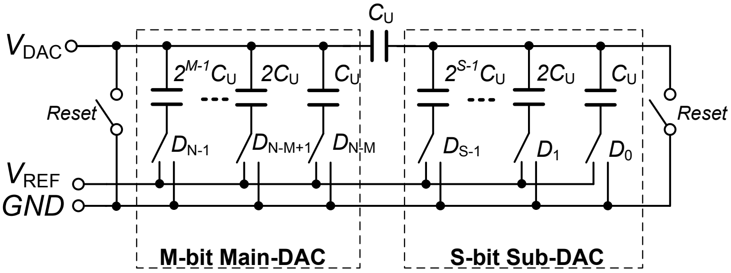


Figure 2.6: A modified split binary-weighted capacitive DAC to avoid fractional value of bridge capacitor.

Assuming M and S are both set to 5 to achieve 10-bit resolution, the bridge capacitor is calculated to be $32/31C_U$. The fractional value of C_B introduces layout difficulties and additional mismatch. Hence, to avoid the fractional value a modified split-DAC is employed, shown in Fig. 2.6, where the dummy capacitor at sub-DAC part is removed and the bridge capacitor is equal to the unit capacitor. This modification will introduce gain error to the conversion, which will be discussed in the following section.

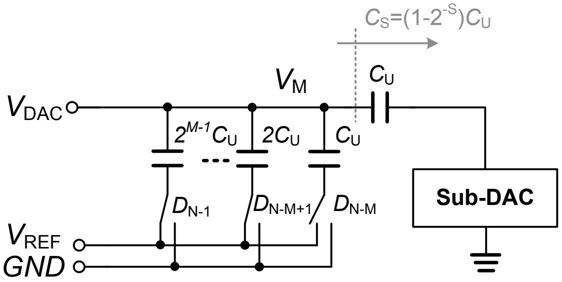
2.2.2.1 Gain Error

First, we consider the case, shown in Fig. 2.7, where the entire sub-DAC is connected to ground and several capacitors in the main-DAC is connected to V_{REF}. The voltage at V_M is

$$V_M = \frac{C^M_{VREF}}{(2^M - 1)C_U + (1 - 2^{-S})C_U} V_{REF} \tag{2.18}$$

$$= \frac{C^M_{VREF}}{2^M(1 - 2^{-N})C_U} V_{REF} \tag{2.19}$$

where C^M_{VREF} denotes the total capacitors connected to V_{REF} in the main-DAC.



CS=(1-2-S)CU
VM
CU
VDAC
2M-1CU
2CU
CU
DN-1
DN-M+1
DN-M
Sub-DAC
VREF
GND

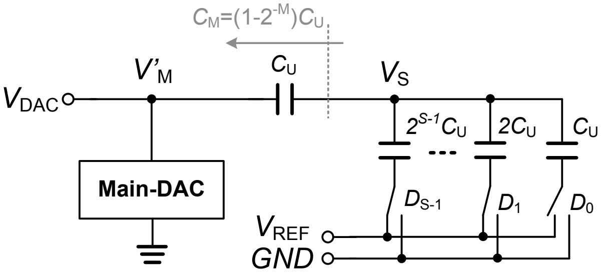
Figure 2.7: A simplified DAC circuit with the whole sub-DAC connected to ground.

Secondly, we consider the case, shown in Fig. 2.8, where the entire main-DAC is connected to ground and several capacitors in the sub-DAC is connected to V_{REF}. The voltage at V_S is

$$V_S = \frac{C^S_{VREF}}{(2^S - 1)C_U + (1 - 2^{-M})C_U} V_{REF} \tag{2.20}$$

$$= \frac{C^S_{VREF}}{2^S(1 - 2^{-N})C_U} V_{REF} \tag{2.21}$$

where C^S_{VREF} denotes the total capacitors connected to V_{REF} in the sub-DAC.



CM=(1-2-M)CU
V'M
CU
VS
VDAC
2S-1CU
2CU
CU
Main-DAC
DS-1
D1
D0
VREF
GND

Figure 2.8: A simplified DAC circuit with the whole main-DAC connected to ground.

Thirdly, we calculate the voltage at the top-plate of main-DAC, denoted as V'_M

$$V'_M = \frac{C_U}{(2^M - 1)C_U + C_U} V_S \tag{2.22}$$

$$= \frac{1}{2^M} V_S \tag{2.23}$$

Finally, we can derive the voltage at the DAC output, denoted as V_{DAC}, it is

$$\begin{aligned} V_{DAC} &= V_M + V'_M \qquad (2.24)\\ &= \frac{C^M_{VREF}}{2^M(1-2^{-N})C_U}V_{REF} + \frac{1}{2^M}\frac{C^S_{VREF}}{2^S(1-2^{-N})C_U}V_{REF} \qquad (2.25)\\ &= \frac{V_{REF}}{1-2^{-N}}(\frac{C^M_{VREF}}{2^M} + \frac{C^S_{VREF}}{2^N}) \qquad (2.26)\\ &= \frac{V_{REF}}{1-2^{-N}}\frac{2^S C^M_{VREF} + C^S_{VREF}}{2^N} \qquad (2.27) \end{aligned}$$

Equation (2.27) shows a gain factor of $1/(1-2^{-N})$. If necessary, the gain error introduced by the modified architecture can be calibrated in the digital domain.

2.2.2.2 Mismatch Error

Since the effect of the capacitor mismatch in the sub-DAC is reduced by $1/2^M$, as indicated in Eq. (2.23), the main-DAC dominates the total mismatch performance. Note that here we assume M is relatively large, which is commonly chosen to be equal to or larger than $N/2$ in practice.

Based on Eq. (2.12), the worst-case standard deviation of DNL for M-bit sub-DAC is

$$\sigma_{DNL,MAX} = \sqrt{2^M-1}\frac{\sigma_u}{C_u}LSB' \qquad (2.28)$$

where LSB' is equal to $V_{REF}/2^M$. Considering the mismatch error should be less than $1/2LSB$, where the LSB is equal to $V_{REF}/2^N$, we further write

$$\begin{aligned} \sqrt{2^M-1}\frac{\sigma_u}{C_u}\frac{V_{REF}}{2^M} &< \frac{1}{2}\frac{V_{REF}}{2^N} \qquad (2.29)\\ \frac{\sigma_u}{C_u} &< \frac{1}{2^{N-M+1}\sqrt{2^M-1}} \qquad (2.30) \end{aligned}$$

Following a similar method which derives the lower bounds of mismatch-limited unit capacitor for a single binary-weighted capacitive array in Sec. 2.2.1, we write the lower bounds of mismatch-limited unit capacitor for the modified split architecture

$$C_U = 18 \cdot (2^M-1) \cdot 2^{2(N-M)} \cdot K^2_\sigma \cdot K_C \qquad (2.31)$$

If we choose M to be equal to N, which means the split architecture returns to a single binary-weighted one, we will find Eq. (2.31) matches Eq. (2.16).

It will be informative to do a plot based on Eq. (2.31). Assuming 10-bit resolution, $K_\sigma = 1\%\mu m$ and $K_C = 1fF/\mu m^2$, the mismatch-limited minimum unit capacitance together with the corresponding total array capacitance versus main-DAC resolution are plotted in Fig. 2.9.

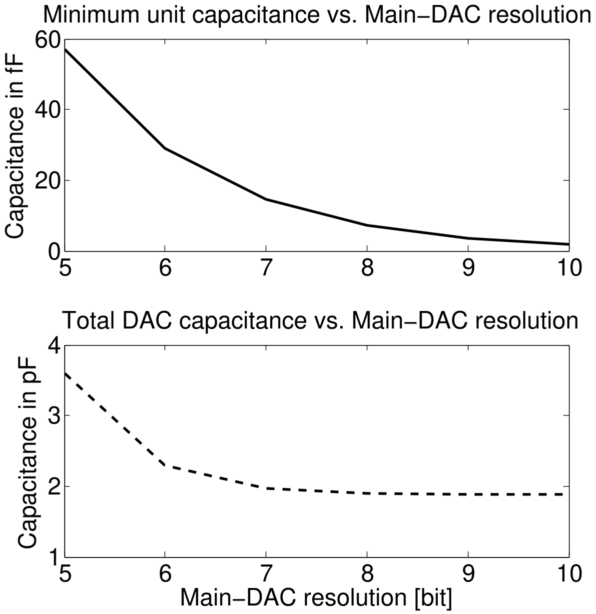


Figure 2.9: Unit capacitance and total array capacitance versus main-DAC resolution.

As shown, the linearity requirements impose much larger unit capacitance and total array capacitance to the split architecture compared to the single architecture. However, the actual implementation of the minimum capacitor could be limited by the technology design-kit, denoted as C_{PRE}. For a single architecture, a unit capacitance of C_{PRE} might be much larger than necessary to meet the linearity requirements, resulting in considerably large array capacitance. In this case, a split architecture is preferred, which requires larger unit capacitor but still arrives at smaller total array capacitance.

2.3 Comparator

The comparator is commonly composed of a pre-amplifier and a latch. However, recent state-of-arts in SAR ADC designs show a trend of directly using dynamic latch comparator to achieve moderate resolution with high power-efficiency.

In this section, we focus on one type of dynamic latch comparators, shown in Fig. 2.10. It works at two phases: reset and regeneration phases. The differential outputs are initially pre-charged (reset) to the supply voltage. During the regeneration phase, the outputs discharge toward ground at unequal speed depending on the input voltages. When these nodes are low enough, one of the cross-coupled inverters is activated and initiates the regeneration. Finally, one of the outputs is pulled towards ground, and another one is pulled up to the supply.

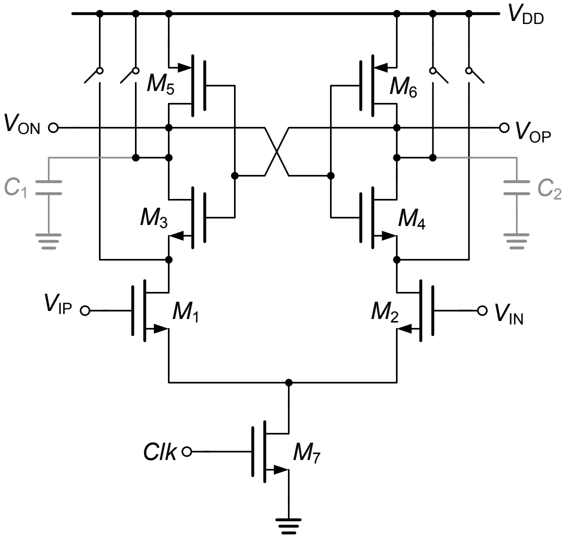


Figure 2.10: A dynamic latch comparator.

The general design considerations of the comparator, such as offset, noise, and metastability, will be discussed in the following sections.

2.3.1 Offset

There are mainly two types of offset voltages in the comparator: 1) offset voltage from the mismatch in transistor current factors and in threshold voltages due to process variation; 2) offset voltage from the mismatch in the parasitic capacitors.

It is well known that increasing the transistor size will reduce the first-type offset voltage. Here, we are more interested in the second-type offset voltage which is caused by the load capacitor mismatch. It has been demonstrated that a capacitive imbalance of 1 fF at the output of a simplified latch model (a cross-coupled inverter pair) can lead to offsets of several tens of millivolts [28]. In [28], it also shows that the offset voltage is more affected by the relative capacitance mismatch ($\Delta C_{12}/C_2$)

than the absolute capacitance mismatch (ΔC_{12}). A possible strategy to minimize the offset voltage is sizing up the cross-coupled inverter pair so that the relative mismatch is reduced. Moreover, if the requirement of comparator speed can be easily met, additional capacitors with good matching properties can be added to the output nodes to further reduce the relative mismatch.

2.3.2 Thermal Noise

Thermal noise is one of the critical limiting factors to the comparison accuracy. Unlike operational amplifiers whose operation regions of all the transistors are well-defined, the dynamic latch comparators possess time-varying nature, thus making the noise analysis more difficult. In [29], the authors performed noise analysis based on stochastic differential equations. In [30], the authors estimated the comparator decision error probability based on linear, periodically time-varying systems. They both show that the noise terms have the usual kT/C-form with the addition of some other factors. Here we refer to the result used in [31], where the input-referred thermal noise of the latch comparator is approximated to be

$$V_{nC}^2 = \kappa \frac{kT\gamma}{C_C} \tag{2.32}$$

where κ is an architecture-dependent parameter, γ is a thermal-noise factor, and C_C is the load capacitance at the bandwidth-limiting node of the comparator.

2.3.3 Flicker Noise

Apart from thermal noise, flicker noise is another important noise source. We start the estimation by referring a known result of flicker noise on the transistor gate [32], which is given by

$$V_{nF}^2 = \frac{K_f}{C_g} ln \frac{B_n}{f_L} \tag{2.33}$$

where K_f is the noise coefficient, C_g is the gate capacitance, B_n is the noise bandwidth, and f_L is a lower frequency limit. B_n and f_L can be further expressed with

$$B_n = \frac{g_m}{4C_C} \tag{2.34}$$

$$f_L = \frac{1}{t_{sys}} \tag{2.35}$$

where g_m is the transistor transconductance, C_C is the parasitic capacitance at the output, and t_{sys} is the system lifetime. g_m can be further expressed using the cut-off frequency f_T

$$g_m = 2\pi C_g f_T \tag{2.36}$$

Assume C_g is one-fourth of C_C, considering that C_C is at least contributed by two diffusion capacitors and two gate capacitors of the cross-coupled inverter. Combining all the above equations, we rewrite Eq. (2.33) as

$$V_{nF}^2 = \frac{4K_f}{C_C} \times ln(2\pi f_T t_{sys}) \tag{2.37}$$

We assume K_f is on the order of 10^{-25} V^2F [33], f_T is around 100 GHz, and t_{sys} is about 10 years. Hence, the flicker noise can be approximated to

$$V_{nF}^2 \approx 1.8e^{-23} \cdot \frac{1}{C_C} \tag{2.38}$$

Moving to the approximation of thermal noise, we evaluate Eq. (2.32) with assumption of $\kappa = 1$ and $\gamma = 1$ and obtain the value of thermal noise as

$$V_{nC}^2 \approx 4.1e^{-21} \cdot \frac{1}{C_C} \tag{2.39}$$

Comparing Eq. (2.38) to Eq. (2.39), the contribution of flicker noise is much less significant than that of thermal noise.

2.3.4 Metastability

Metastability is the phenomenon where a bistable element requires an indeterminate amount of time to generate a valid output [34]. The metastability in a latch comparator occurs when the differential input signal is so small that the latch does not have enough time to produce a well-defined logic levels, which might be interpreted differently by succeeding gates, leading to substantial conversion error. In this section, we calculate the probability of metastability taking place in the dynamic latch comparator.

During regeneration, the differential output voltage follows this equation

$$V_{O,diff} = A_k |V_{I,diff}| e^{t/\tau} \tag{2.40}$$

where $V_{O,diff}$ is the output voltage difference, A_k acts as a gain factor from the inputs to the initial imbalance of the inverter pair, $V_{I,diff}$ is the input voltage difference, and τ is the regeneration time constant of the comparator, given by $C_C/g_{m,INV}$. $g_{m,INV}$ is the total transconductance of the inverter.

Assume that the acceptable logic level (trip point) for $V_{O,diff}$ is $V_{DD}/2$, otherwise, metastable outputs will be caused. Based on the allowable comparator decision time, denoted as T_{max}, the minimum required input voltage difference can be expressed as

$$V_{I,diff@MIN} = \frac{1}{A_k}\frac{V_{DD}}{2}e^{-T_{max}/\tau} \tag{2.41}$$

Further assume that the input signal follows a uniform distribution across a voltage range V_M. The probability of metastable error p_M is equal to the probability when the input voltage difference is less than $V_{I,diff@MIN}$, we have

$$p_M = P(|V_{I,diff}| < V_{I,diff@MIN}) \tag{2.42}$$

$$= 2 \times \frac{V_{I,diff@MIN}}{V_M} \tag{2.43}$$

$$= \frac{1}{A_k}\frac{V_{DD}}{V_M}e^{-T_{max}/\tau} \tag{2.44}$$

In [35], the signal-to-metastability-error ratio (SMR) of SAR ADC was calculated to quantify the effect of the metastability. The metastability error power is defined by the product of the calculated probability and the power of output error voltage caused by metastable state. It shows that errors in the first bit contribute most to the output noise power [35].

Chapter 3

SAR ADC Power Consumption Bounds

As aforementioned, SAR ADCs are particularly successful in achieving low power consumption. In order to further reduce the power consumption of SAR ADCs, a deeper understanding of its lower bounds is essential. The power consumption bounds of SAR ADCs was discussed in [36]. However, we are less conservative than the authors in [36], thus arriving at comparatively lower bounds.

As we are looking for the lower power consumption bounds, we have limited our study to power-efficient SAR ADC architectures, such as a charge-redistribution SAR ADC [37]. As shown in Fig. 3.1, the ADC consists of a binary-weighted capacitive array, a dynamic latch comparator, and a SAR control logic. Since most of the SAR ADCs in the literature don't have a driver at the input, the sampling power, previously discussed in [31], will not be included in the following analysis.

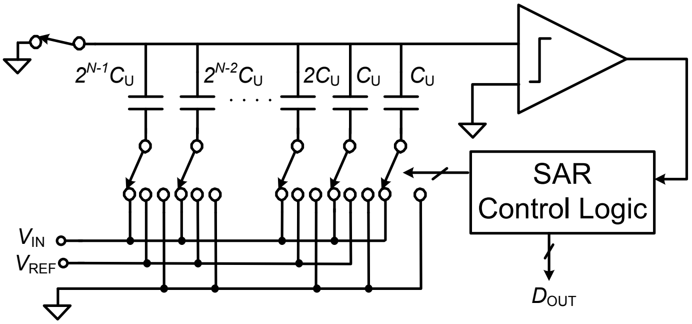


Figure 3.1: Charge-redistribution SAR ADC.

3.1 Power Consumption Estimation of DAC

Power consumption of the DAC depends on the unit capacitance, the input signal swing, and the employed switching approach. For a uniformly distributed input signal between ground and the reference voltage, the average switching power per conversion for N-bit can be derived as [18]

$$P_{DAC} = \zeta \sum_{i=1}^{N} 2^{N+1-2i}(2^i - 1) C_U V_{REF}^2 f_S \tag{3.1}$$

where V_{REF} is the reference voltage, f_S is the sampling frequency, and ζ is a normalized switching scheme-dependent parameter. For conventional switching approach [37], $\zeta = 1$.

The unit capacitor should be kept as small as possible for power saving. In practice, it is usually determined by thermal noise and capacitor mismatch. In Sec. 2.1.1, we derived the minimum sampling capacitance limited by thermal noise. Considering the DAC realizes the sample-and-hold function, Eq. (2.1) can be used to calculate the noise-limited minimum DAC array capacitance. Further deviding the calculated value by 2^N, we derive the noise-limited minimum C_U

$$C_{U,n} = 12kT \frac{2^N}{V_{FS}^2} \tag{3.2}$$

In Sec. 2.2.1, we derived the mismatch-limited minimum C_U. For ease of reference, we copy Eq. (2.16) here

$$C_{U,m} = 18 \cdot (2^N - 1) \cdot K_\sigma^2 \cdot K_C \tag{3.3}$$

Apart from the above two limiting factors, the process will also set a lower limit to the capacitance so that the total array capacitance at least need to be equal to the parasitic capacitance at the DAC output, which results in a 50% attenuation of the output voltage. The parasitic capacitance include both the gate capacitance of the comparator input and the parasitic capacitance of interconnection. We further assume it is comparable to the input capacitance of a minimum-sized inverter, which is denoted as C_{min}. Regarding the value of C_{min}, we follow the same assumption in [31], where C_{min} is equal to 1 fF for 65-90 nm CMOS processes.

Finally, C_U in Eq. (3.1) can be replaced with

$$C_C = \max(C_{U,n}, C_{U,m}, C_{min}) \tag{3.4}$$

3.2 Power Consumption Estimation of Comparator

We estimate the comparator power based on the dynamic latch comparator due to its high power efficiency. The schematic of the comparator is shown in Fig. 2.10. A typical signal transient behavior of the differential outputs and the supply current of the comparator is visualized in Fig. 3.2.

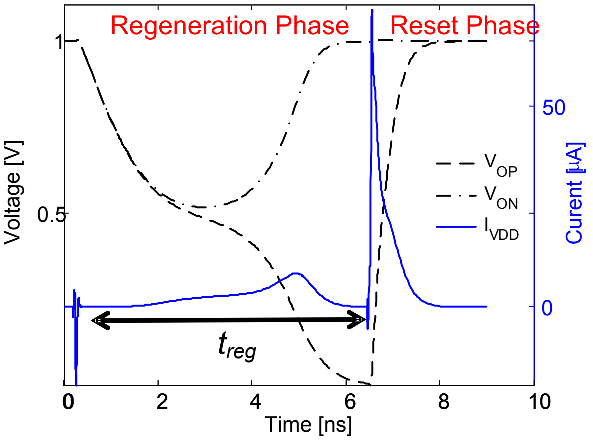


Figure 3.2: Typical signal transient behavior including the differential outputs and the supply current. Note that there is no static supply current.

To compute the charge during the regeneration mode, we denote that there is a current, I_D, flowing only during the regeneration time, t_{reg}. Hence, the total regenerative charge can be expressed as $2I_Dt_{reg}$. t_{reg} can be calculated from Eq. (2.40). For ease of reference, we copy Eq. (2.40) here

$$V_{O,diff} = A_kV_{I,diff}e^{t/\tau} \tag{3.5}$$

where $\tau = C_C/g_{m,INV}$.

Further defining a parameter V_{eff}, we can write $g_{m,INV} = I_D/V_{eff}$ [31]. Assuming that the regeneration is finished when $V_{O,diff}$ becomes V_{DD}. It results in the following expression of t_{reg}

$$t_{reg} = \frac{V_{eff}C_C}{I_D}ln\frac{V_{DD}}{A_kV_{I,diff}} \tag{3.6}$$

Using Eq. (3.6), we can rewrite the expression of the regenerative charge for one conversion step as

$$Q_{C,reg-s} = 2V_{eff}C_Cln\frac{V_{DD}}{A_kV_{I,diff}} \tag{3.7}$$

Since an N-bit SAR ADC needs N steps to complete one conversion, the input voltage difference of the comparator for the ith-step can be expressed as

$$V_{I,diff}(i) = |-V_{IN} + D_{N-1}\frac{V_{REF}}{2} + \cdots + \frac{V_{REF}}{2^i}|, 1 \leq i \leq N \tag{3.8}$$

where V_{IN} is the input voltage, D_{N-1} is the decision of MSB.

We assume that V_{IN} is evenly distributed between 0 and V_{REF}. This further indicates that $V_{I,diff}$ is also evenly distributed between 0 and a binary-weighted value of V_{REF}, which is denoted as V_m. Then, the average charge for one step can be expressed by

$$\frac{1}{V_m}\int_0^{V_m} Q_{C,reg-s}\,\mathrm{d}V_{I,diff} = 2V_{eff}C_C(ln\frac{V_{DD}}{A_k V_m} + 1) \tag{3.9}$$

Hence, the charge of a complete conversion can be derived from the sum of N-steps' charge

$$Q_{C,reg} = \sum_{k=1}^{N}(2V_{eff}C_C(ln\frac{V_{DD}}{A_k(V_{REF}/2^k)} + 1)) \tag{3.10}$$

$$= 2V_{eff}C_C(Nln\frac{V_{DD}}{A_k V_{REF}} + \frac{N(N+1)}{2}ln2 + N) \tag{3.11}$$

Moving to the reset charge, we assume that it is mainly consumed by the capacitive load at the comparator output. Consequently, the total power consumption of the comparator is equal to the reset charge at the clock frequency and the regenerative charge at the sampling frequency

$$P_C = Nf_S V_{DD} Q_{C,rst} + f_S V_{DD} Q_{C,reg} \tag{3.12}$$

We rewrite Eq. (3.12) by replacing $Q_{C,rst}$ with $C_C V_{DD}$ and $Q_{C,reg}$ with Eq. (3.11). Thus,

$$P_{COMP} = Nf_S C_C V_{DD}^2 + 2f_S V_{DD} V_{eff} C_C(Nln\frac{V_{DD}}{A_k V_{REF}} + \frac{N(N+1)}{2}ln2 + N) \tag{3.13}$$

Since the comparator offset introduces ADC offset rather than nonlinearities, the fundamental limitation on the achievable comparator resolution is noise. Based on the analysis presented in Sec. 2.3, we find that flicker noise is much smaller than thermal noise. Consequently, the comparator is constrained by thermal noise, which is derived by Eq. (2.32). Equalizing the thermal noise to the quantization noise of an

N-bit converter gives a minimum load capacitance

$$C_{C,n} = 12kT\gamma\kappa\frac{2^{2N}}{V_{FS}^2} \tag{3.14}$$

where $\kappa = 1$ and $\gamma = 1$ [31] is used in this analysis.

Considering that the effect of the process also set a lower limit to the capacitance through minimum feature size. We therefore include C_{min}, the input capacitance of a minimum-sized inverter. And C_C in Eq. (3.13) can be replaced with

$$C_C = \max(C_{C,n}, C_{min}) \tag{3.15}$$

3.3 Power Consumption Estimation of SAR Logic

A straightforward way to build a SAR logic is to use $2 \times N$ D-type Flip Flops (DFFs) for N-bit resolution, as shown in Fig. 3.3. A typical transmission-gate DFF is composed of 2 cross-coupled inverter pairs and 4 transmission gates. We therefore assume that the capacitive load of one DFF is equivalent to that of 8 inverters. Hence, the equivalent capacitive load of the SAR logic can be approximated to $16 \times N$ inverters in total.

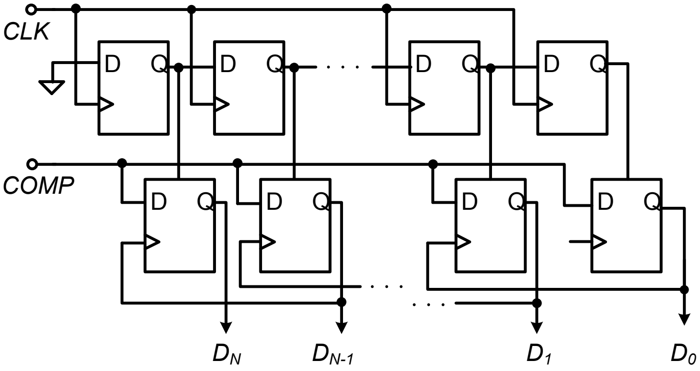


Figure 3.3: A typical design of SAR digital logic.

Leakage power consumption could be significant for a circuit designed in a high-leaky process. In this analysis, for simplicity we only consider the dynamic power consumption. Assuming a total activity of the SAR logic to be α, and then we derive the power consumption of the SAR logic as

$$P_{SAR} = 16N^2\alpha f_S C_{min} V_{DD}^2 \tag{3.16}$$

Assume that one-fourth of the transistors in the SAR logic are clocked and the activity of the rest is 0.2, we approximate α to be 0.4.

3.4 Power Consumption Estimation of a Complete SAR ADC

Adding together Eq. (3.1), Eq. (3.13), and Eq. (3.16), the earlier derived equations of block power consumption, we can express the total power consumption of a complete SAR ADC

$$\begin{aligned} P_{ADC} &= \zeta \sum_{i=1}^{N} 2^{N+1-2i}(2^i - 1)C_U V_{REF}^2 f_S \\ &+ N f_S C_C V_{DD}^2 + 2 f_S V_{DD} V_{eff} C_C (N ln \frac{V_{DD}}{A_k V_{REF}} + \frac{N(N+1)}{2} ln2 + N) \\ &+ 16 N^2 \alpha f_S C_{min} V_{DD}^2 \end{aligned} \tag{3.17}$$

In Eq. (3.17), we have included many parameters. For ease of reference, the following list summerizes the parameters used in this equation.

- ζ: normalized switching scheme-dependent parameter.
- N: resolution of the ADC.
- C_U: DAC unit capacitance, where $C_U = max(C_{U,n}, C_{U,m}, C_{min})$.
- $C_{U,n}$: thermal-noise-limited DAC unit capacitance.
- $C_{U,m}$: mismatch-limited DAC unit capacitance.
- C_{min}: input capacitance of a minimum-sized inverter in a particular technology node.
- V_{REF}: reference voltage of the ADC.
- f_S: sampling frequency of the ADC.
- C_C: capacitive load of the comparator, where $C_C = max(C_{C,n}, C_{min})$.
- $C_{C,n}$: thermal-noise-limited capacitive load of the comparator.
- V_{DD}: supply voltage of the ADC.

- V_{eff}: effective voltage, which is the ratio of drain current I_D and transconductance g_m. For classical long-channel transistors in strong inversion $V_{eff} = (V_{GS} - V_T)/2$; for weak inversion $V_{eff} = m \cdot kT/q$ [38]; for modern short-channel MOS transistors, transistors' being often biased in the transition region between weak and strong inversion makes both formulas useless [31]. In this analysis, we have tried to approximate V_{eff} from simulation, which will be discussed later.

- A_k: gain factor from the inputs to the initial imbalance of the inverter pair. In this analysis, we have tried to approximate A_k from simulation, which will be discussed later.

- α: switching activity of the SAR logic.

Approximation of A_k and V_{eff}
Equation. (3.7) can be further decomposed to

$$Q_{C,reg-s} = 2V_{eff}C_C ln\frac{V_{DD}}{A_k} - 2V_{eff}C_C lnV_{I,diff} \tag{3.18}$$

The first term in the right-hand side of Eq. (3.18) turns out to be a constant offset, and the second term is linear with the logarithm of input voltage difference. Since it is not easy to analytically derive the value of A_k and V_{eff} due to the time-varying nature of the comparator, we first simulated $Q_{C,reg-s}$ under a set of $V_{I,diff}$, and then extracted A_k and V_{eff} based on the simulation results via a least-squares fit. Figure 3.4 gives an example of curve fitting based on simulated results.

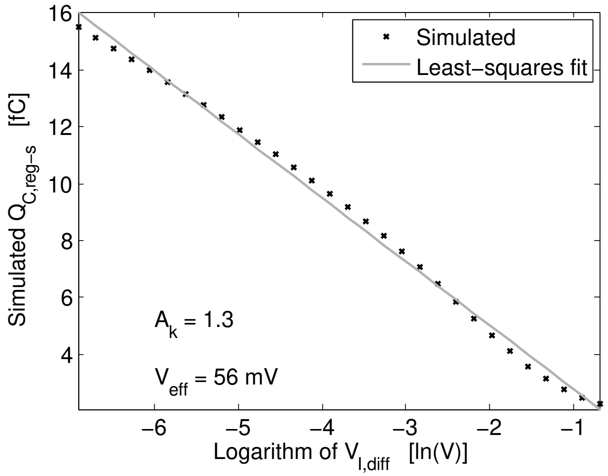


Figure 3.4: An extraction example of A_k and V_{eff} based on simulation.

We implemented a latch comparator with minimum transistor size in a 90-nm CMOS process and a capacitive load of 20 fF. We obtained $A_k = 1.3$ and $V_{eff} = 56\text{mV}$ based on the simulation results. Varying the common-mode voltage applied to the comparator input, the value of A_k and V_{eff} will change, but they are almost kept between 0.5 to 1.8 and 50 mV to 100 mV, respectively. The variations are fairly independent of scaling and apply to typical CMOS technologies from 130 nm to 65 nm. In this analysis, we use $A_k = 1.0$ and $V_{eff} = 75\text{mV}$.

Figure 3.5 shows our analyzed P/f_S of the SAR ADC together with its individual blocks. Table 3.1 shows the parameter values used in the demonstration. We plot the DAC power consumption limited by noise and mismatch, respectively. It is interesting to note that the digital logic dominates the total power when the resolution is low. However, for higher resolution, the total power is very close to the DAC power, if mismatch is the limiting factor. When mismatching is not considered, the comparator power dominates the total power.

Table 3.1: Parameter Values Used in Eq. (3.17)

$\zeta = 1$	$T = 300K$	$C_{min} = 1fF$
$V_{DD} = 1V$	$V_{REF} = 1V$	$V_{FS} = 1V$
$K_\sigma = 1\%\mu m$	$K_C = 1fF/\mu m^2$	$\kappa = 1$
$\gamma = 1$	$V_{eff} = 75mV$	$A_k = 1$
$\alpha = 0.4$		

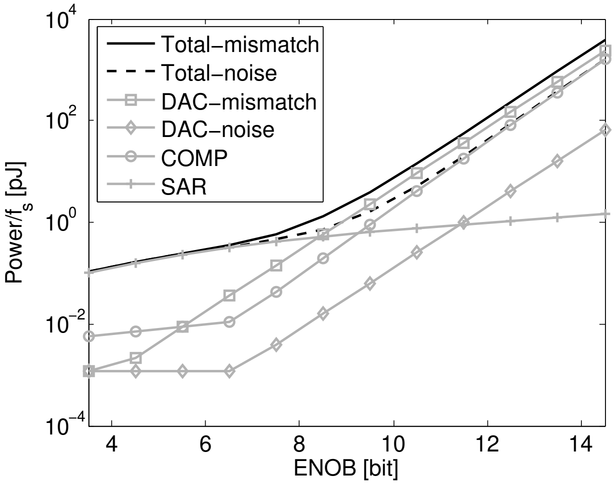


Figure 3.5: Predicted power consumption bounds for both noise-limited and mismatch-limited SAR ADCs together with their individual components.

3.5 Comparison to Experimental Data

The predicted power consumption bounds together with Nyquist SAR ADC survey data from [8] is shown in Fig. 3.6. We note that several experimental points are very close to our estimated power, indicating that our model describes reality well. The power per conversion of the SAR ADC described in [9] is very close to our estimated value. The ADC is indicated by a black circle in Fig. 3.6. This 8.75-ENOB 1-MS/s ADC was designed in a 65 nm CMOS process without any digital error correction circuit. The measured P/f_S is 1.9 pJ. Our theoretical bounds for a mismatch-limited 8.75-ENOB converter is 1.1 pJ. The ADC achieves a close value compared to our estimation by using: 1) a binary-weighted DAC with a total capacitance of 600 fF; 2) a step-wise charging for the three MSB capacitors with two intermediate steps, which further reduces the DAC power; 3) a dynamic latch comparator without static bias. With these considerations, we find a reasonable agreement between our bounds and the experimental result in [9].

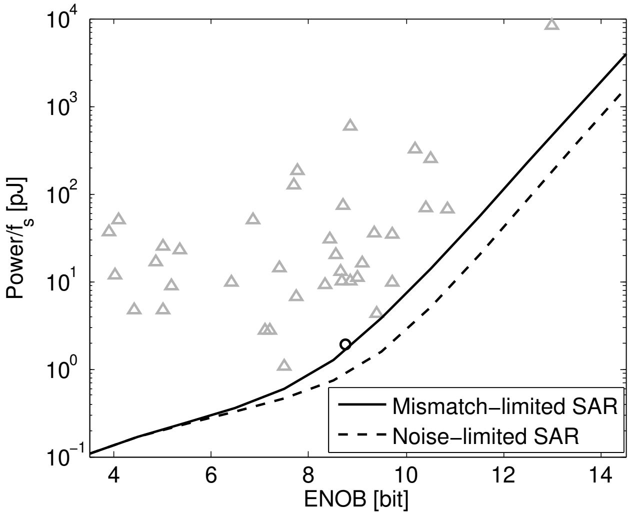


Figure 3.6: Predicted power consumption bounds (solid line for mismatch-limited and dashed line for noise-limited) together with Nyquist SAR ADC survey data.

Chapter 4

A 53-nW 9.1-ENOB SAR ADC in 0.13 μm CMOS Process

In this chapter, we will present a 53-nW 9.1-ENOB SAR ADC in 0.13 μm CMOS process. To achieve the nano-watt range power consumption, an ultra-low power design strategy has been utilized, imposing maximum simplicity on the ADC architecture, low transistor count and matched capacitive DAC with a switching scheme which results in full-range sampling without switch bootstrapping and extra reset voltage. Furthermore, a dual-supply voltage scheme allows the SAR logic to operate at 0.4 V, reducing the overall power consumption of the ADC by 15% without any loss in performance. In dual-supply mode (1.0 V for analog and 0.4 V for digital), the ADC achieves 9.1 ENOB, consumes 53 nW at 1 kS/s. The leakage power constitutes 25% of the 53-nW total power consumption.

4.1 ADC Architecture

Figure 4.1 shows the block diagram of the proposed ADC. It comprises a matched binary-weighted capacitive DAC, a low-power dynamic latch comparator, a low-leakage/low-voltage synchronous SAR digital logic, and level shifters between the digital logic and the analog blocks. In addition, a differential architecture was employed to have a good common-mode noise rejection.

In a conventional SAR ADC [37], the input voltage is sampled on the bottom-plate nodes of the capacitor array and the top-plate nodes are reset with a fixed voltage. The fixed voltage is commonly chosen to be one of the power rails in order to avoid extra voltage levels. However, this makes the DAC outputs go beyond the rails during the conversion when full-range input sampling is applied. One common way to solve this problem is to decrease the input range with the penalty of degrading the signal-to-

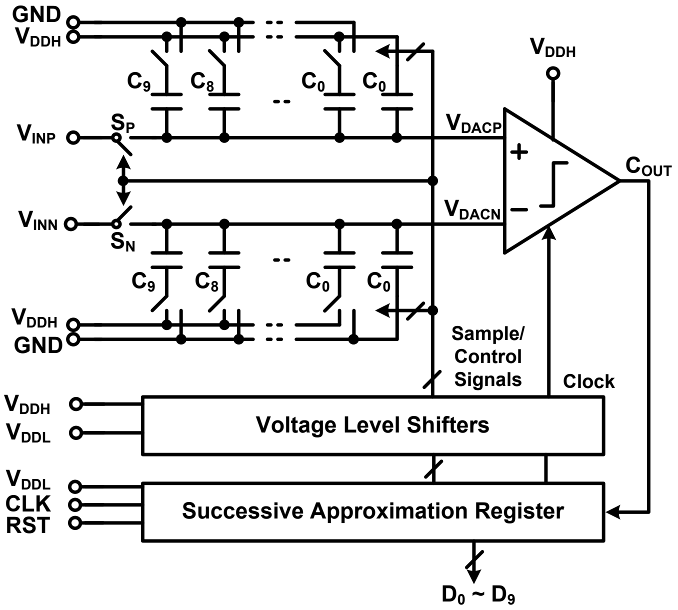

GND
V_{DDH}
C_9
C_8
C_0
C_0
V_{INP}
S_P
V_{INN}
S_N
V_{DDH}
V_{DACP}
V_{DACN}
+
−
C_{OUT}
Sample/ Control Signals
Clock
V_{DDH}
V_{DDL}
Voltage Level Shifters
V_{DDL}
CLK
RST
Successive Approximation Register
D_0 ~ D_9

Figure 4.1: Architecture of the SAR ADC.

noise ratio. Another alternative is to make the top-plate switches bootstrapped. In this work, we use top-plate sampling [9] with MSB preset to achieve full-range sampling without switch bootstrapping and extra reset voltages. As shown in Fig. 4.2, the differential inputs are initially connected to the top-plates of the capacitor array, and simultaneously the MSB is reset to high and all other bits are reset to low. Next, the top-plate sampling switch is open and the input data is sampled on the capacitor array. The comparator then performs the first comparison. If V_{DACP} is higher than V_{DACN}, the MSB remains high. Otherwise, it goes low. Then, the second approximation step starts by setting MSB-1 to high, and the comparator does the comparison again. The ADC repeats this procedure until all 10 bits are decided. During the entire conversion, the DAC outputs always remain within the rails. Moreover, the common-mode voltage of the DAC outputs is the same as that of the differential inputs, which is equal to mid-rail voltage for full-range input sampling, as shown in Fig. 4.3. The constant common-mode voltage reduces the signal-dependent offset voltage of the comparator [18].

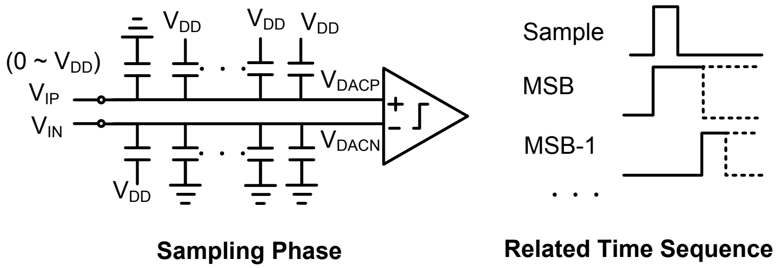

VDD
VDD VDD
(0 ~ VDD)
VIP
VIN
VDACP
VDACN
+
−
VDD
Sample
MSB
MSB-1
. . .
Sampling Phase
Related Time Sequence

Figure 4.2: The sampling phase of capacitive DAC with MSB preset.

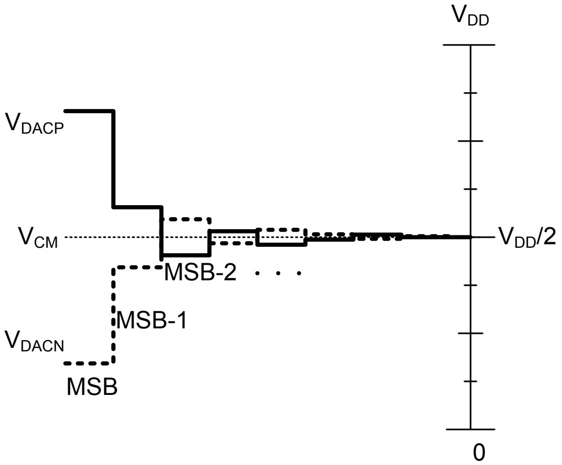

VDD
VDACP
VCM
VDD/2
MSB-2 . . .
MSB-1
VDACN
MSB
0

Figure 4.3: Waveform of the DAC switching procedure.

Lowering the supply voltage is an efficient technique to reduce both the switching and leakage power consumption. This is particularly true at low data-rates, where transistors can be slow but still meet the target speed. However, for the analog circuits operating with low supply voltages, noise and a reduced dynamic range can degrade the ADC performance. To avoid the analog performance degradation, in this design, we use a dual-supply voltage scheme, which allows the SAR logic to operate at low supply voltages. Our measurement results (in Sec. 4.3) show that this voltage scaling has reduced the overall power consumption of the ADC by 15% without any loss in performance.

4.2 Circuit Implementation

In this section, the circuit level design of the DAC, switches, comparator, and SAR digital logic are described. Since these components are critical with regards to power consumption, speed, and accuracy of the entire ADC, much of the design effort was focused on characterizing and optimizing their performance.

4.2.1 Capacitive DAC

The capacitive DAC was implemented with a binary-weighted capacitor array. In this technology, a MIM capacitor has a density of 2 fF/$\mu\mathrm{m}^2$ and a matching of $1\%\mu\mathrm{m}$. Eq. (2.16), which calculates the lower bounds for the mismatch-limited unit capacitor, leads to a minimum unit capacitance of 4 fF. Apart from the mismatch, the design rule will also set a minimum value on the MIM capacitance, which is 27 fF in this process. Consequently, the unit capacitance was set to be 13.5 fF in our work, which was implemented by two minimum process-defined MIM capacitors in series. Hence, the total array capacitance is about 14 pF.

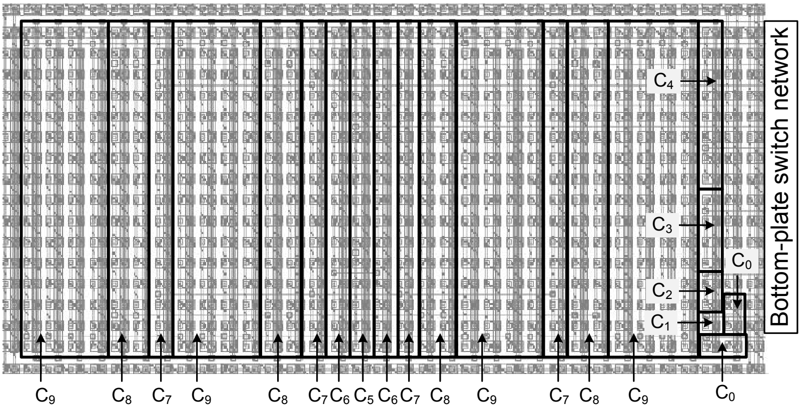


Figure 4.4: Layout of the capacitor array which follows a partial common-centroid configuration. The capacitors are indicated according to Fig. 4.1.

Besides capacitor sizing, a careful layout to avoid linearity degradation is important as well. In this work, we have utilized a partial common-centroid layout strategy for the capacitor array. Fig. 4.4 illustrates the layout floor plan. The MSB capacitors (C_9-C_5) follow a common-centroid configuration to minimize the errors from the non-uniform oxide growth in the MIM capacitors. However, the smaller LSB capacitors (C_4-C_0) have been placed close to the bottom-plate switches to simplify the routing, thereby reducing the parasitic capacitance and resistance of the interconnection. Post-layout simulations showed that the reduced parasitic of the employed partial common-centroid layout results in better DAC linearity, compared to a capacitor array with a full common-centroid layout (where the LSB capacitors were placed in the middle of the array). Based on the simulations, the DAC with the partial common-centroid layout had a peak DNL of +0.18/-0.20 LSB and INL of +0.30/-0.23 LSB, while the DAC with a full common-centroid layout had a peak DNL of +0.35/-0.16 LSB and INL of +0.40/-0.36 LSB.

4.2.2 Switch Design

The top-plate sampling switch was implemented using transmission gate, shown in Fig. 4.5, to achieve full-range input sampling. The switch together with the DAC capacitor array acts as the sample-and-hold circuit of the ADC. In Sec. 2.1.4, Eq. (2.10) derives the minimum track bandwidth of a sampling circuit. In this design, the sampling time is determined by the system clock, which is N+2 times the sampling rate. Hence, we have

$$f_{3dB} > \frac{(N+1)\cdot(N+1)\cdot ln2}{\pi} f_S \tag{4.1}$$

Based on Eq. (4.1), for a 10-bit 1-kS/s SAR ADC, the required minimum f_{3dB} is about 30 kHz. Taking account of the 14-pF sampling capacitance, the switch on-resistance (R_{ON}) should be designed to be less than 380 kΩ.

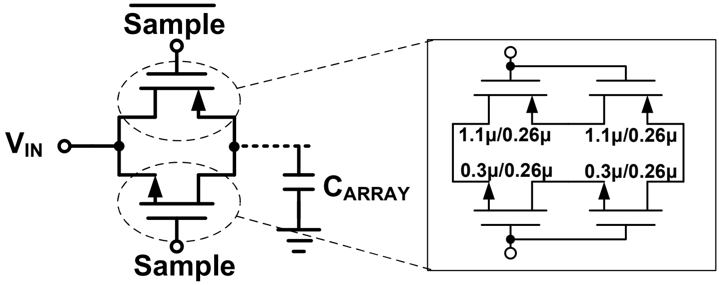
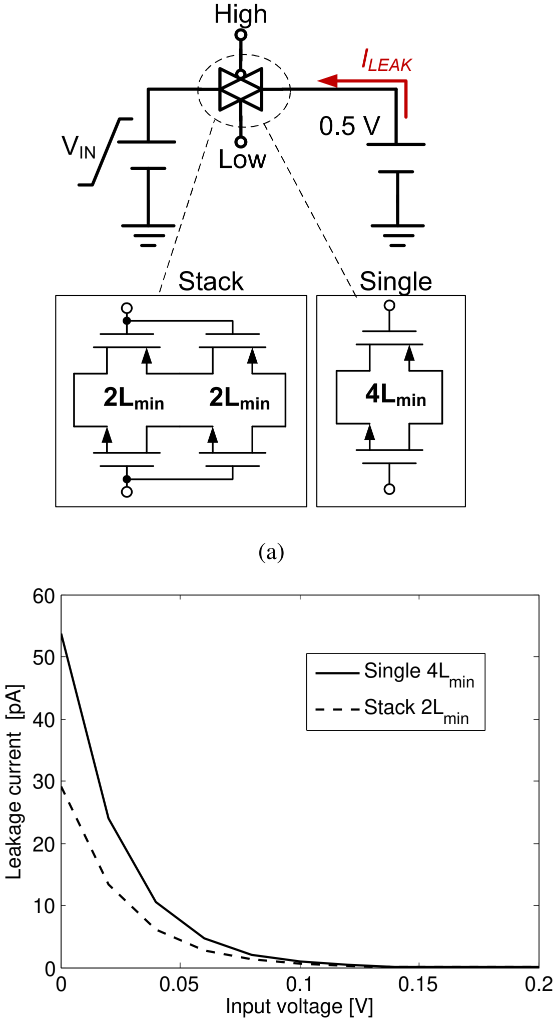


Figure 4.5: Top-plate sampling switch.

Apart from the bandwidth requirement, the voltage droop introduced by the leakage current of the switch can also degrade the sampling accuracy due to the long conversion time. The sub-threshold leakage current of the transistor is the dominant leakage contributor to the switch. In addition, the leakage current shows nonlinear dependence on the input-output voltage difference across the switch, thus introducing harmonic distortion. Increasing the channel length is an effective solution to reduce the sub-threshold leakage current. To further reduce the leakage current, we have utilized a two-transistor stack [39] (shown in Fig. 4.5). Figure 4.6 shows the simulated sub-threshold leakage currents of two different switches versus their input voltages. The figure compares the leakage current of a single transistor with a channel length of $4L_{min}$ to two transistors in series with channel lengths of $2L_{min}$. It can be seen that the stacked transistors show lower leakage for small input voltages in the range from 0 V to 0.1 V.



(a)

(b)

Figure 4.6: Simulated leakage current of the sampling switch: (a) test-bench (b) leakage current versus input voltage.

To determine the channel length of the stacked transistors, the sampling circuit was simulated at 1-kHz sampling frequency with full-range input signal for three different switch lengths (L_{min}+L_{min}, $2L_{min}$+$2L_{min}$, and $3L_{min}$+$3L_{min}$). The frequency of the input signal was swept from near-DC to near-Nyquist bandwidth. The voltage of the sampled output signal was recorded at the end of the hold phase to track the voltage droop. The simulated worst-case SNDR of the recorded voltage was found at near-Nyquist operation. The resulted SNDR for three different switch lengths were 60.9 dB, 67.4 dB, and 67.5 dB, respectively. Thus increasing the total channel length beyond $4L_{min}$ ($2L_{min}$+$2L_{min}$) did not introduce much benefit for the leakage reduction. Hence, in this work, the channel length of the stacked transistors was chosen to be $2L_{min}$ (0.26 μm).

Furthermore, we sized the transistor width and simulated the switch R_{ON} over the entire input range under -40°C at the slow process corner. The simulated maximum R_{ON} based on the chosen transistor widths (0.3 μm for NMOS and 1.1 μm for PMOS) is about 80 kΩ. With the total array capacitance of 14 pF, the f_{3dB} of the sampling circuit is then calculated to be about 140 kHz, which gives a design margin with more than four times the required minimum f_{3dB}.

At the bottom-plate sides, inverters connect the capacitors to the power rails. Ideally, minimum-size transistors can be used for all the inverters because of the low sampling rate, thus minimizing power consumption. In practice, however, special care must be taken during sizing of the MSB inverter. The NMOS top-plate sampling switch introduces parasitic PN-junction on the top-plate node. After a near-ground input voltage is sampled, during the MSB to MSB-1 transition, the voltage on the top-plate node can undershoot below ground, forward-biasing the PN-junction and causing charge loss. To avoid the undershoot voltage, the PMOS transistor in the MSB inverter was sized up to six times the minimum width.

4.2.3 Dynamic Latch Comparator

The dynamic latch comparator [40] is shown in Fig. 4.7. Buffers have been used to make the output loading identical. A succeeding SR latch stores the comparison result for the entire clock cycle.

Since the input common-mode voltage of the comparator is kept at mid-rail voltage, the total comparator offset appears as static offset, which does not affect the linearity of the ADC [18]. Though the offset of the comparator does not affect the accuracy, it will decrease the input voltage range, thus degrading the signal-to-noise ratio. Monte Carlo simulations of the comparator offset [41] showed a total offset voltage of 35.1 mV with 3-σ being considered. The simulated offset voltage decreases the SNR by 0.3 dB, thereby introducing an ENOB loss of 0.05 bit.

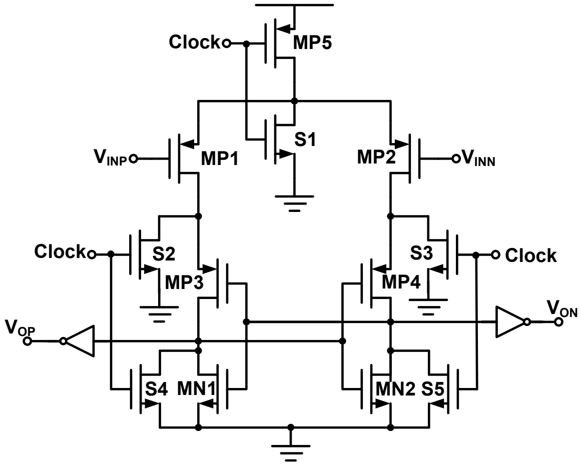


Figure 4.7: Dynamic latch comparator.

4.2.4 SAR Control Logic

For low power SAR control logic, we investigated both synchronous and asynchronous solutions. Asynchronous processing [42] has been frequently used for high-speed SAR ADCs in order to avoid a high-frequency system clock. The SAR control logic starts the conversion on the rising edge of a sampling clock, and triggers the internal comparison from MSB to LSB successively. The delay, usually generated by an inverter line [9], has a large dependency on process, voltage, and temperature variations, which makes it difficult to ensure the DAC settling. Moreover, the short-circuit current caused by the slow transition of the inverters introduce extra power consumption [9].

The proposed ADC utilizes a synchronous SAR logic, shown in Fig. 4.8. It generates the sample signal and the switch control signals for the DAC. The operation of its multiple-input 10-bit shift resister is similar to [43]. A 4-bit counter and a decoder generate the control signals for the 10-bit shift register. The entire logic uses 16 transmission-gate DFFs and the decoder has been optimized for minimum logic depth and gate count. Fig. 4.9 shows the time sequence of the SAR logic. A 12-kHz system clock has been used, and the sampling clock of 1 kHz is generated by the SAR logic.

Since the operating frequency of the SAR logic is 12 kHz, and its switching activity is not high, the leakage power dominates the total power consumption. Several techniques have been used to reduce the leakage currents, including increased channel length, minimum transistor width, and replacing the gate transistors with stacked pairs [44].

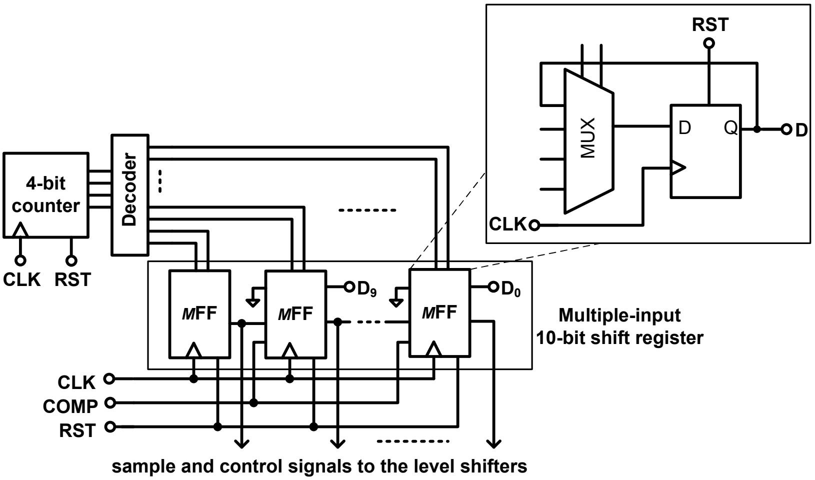

RST
MUX
D
Q
D
CLK
4-bit counter
CLK
RST
Decoder
MFF
MFF
MFF
D9
D0
Multiple-input 10-bit shift register
CLK
COMP
RST
sample and control signals to the level shifters

Figure 4.8: SAR control logic.

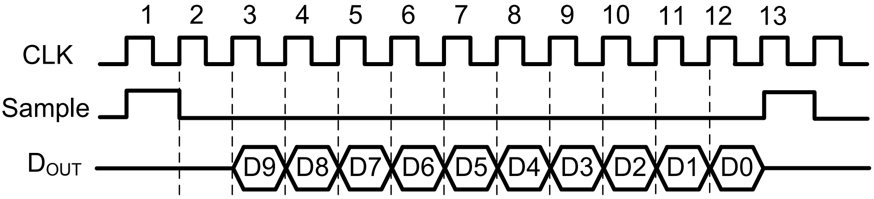

1
2
3
4
5
6
7
8
9
10
11
12
13
CLK
Sample
DOUT
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0

Figure 4.9: Time sequence of the synchronous SAR control logic.

To further reduce the switching and leakage power consumption, a dual-supply voltage scheme has been employed, allowing the SAR logic to operate at 0.4 V. A conventional level shifter, shown in Fig. 4.10, has been used to convert the logic levels between the SAR and the analog parts. In the entire ADC, twelve level shifters have been used: ten for the DAC control signals, one for the sampling signal of the top-plate switch, and one for the clock signal of the comparator.

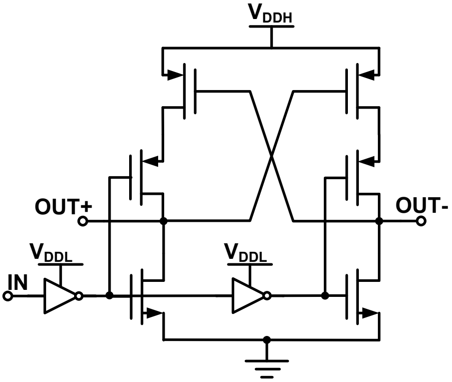


Figure 4.10: Level shifter.

4.3 Measurement Results

The prototype SAR ADC with a core area of 357×536 μm^2 was designed and fabricated in a general purpose 0.13-μm one-poly six-metal (1P6M) CMOS process. It was packaged in a 1.27 mm pitch J-Leaded Chip Carrier (JLCC) package. A photograph of the chip is shown in Fig. 4.11. The unmarked part around the ADC core includes the decoupling capacitors and the I/O buffers for the pads.

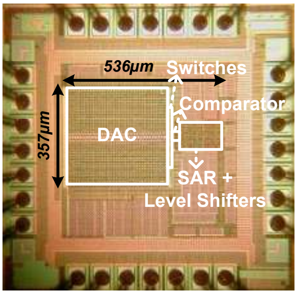


Figure 4.11: Die photograph of the ADC in 0.13-μm CMOS technology.

Histogram test [45] was conducted to measure the linearity of the ADC. A full-swing, differential sinusoidal input near DC frequency with amplitude of 1 V was applied to the 1-kS/s ADC. Fig. 4.12 shows the measured DNL and INL error with respect to the output code. The peak DNL error is +0.54/-0.61 LSB, and the peak INL error is +0.45/-0.46 LSB.

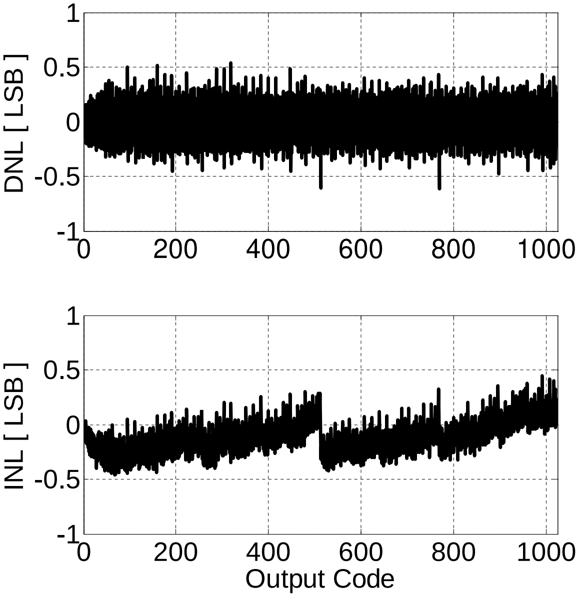


Figure 4.12: Measured DNL and INL errors.

The SNDR of the ADC was measured using tone testing. A fast Fourier transform (FFT) of the 1-kS/s ADC at near-Nyquist operation is shown in Fig. 4.13. The amplitude of the test stimulus was set to -0.5 dBFS. The measured SNDR is 56.7 dB, providing 9.1 ENOB. Fig. 4.14 shows the ENOB of this ADC with respect to the input frequency, where the ENOB remains almost constant over the entire bandwidth. Hence, the effective resolution bandwidth (ERBW) is higher than the Nyquist bandwidth.

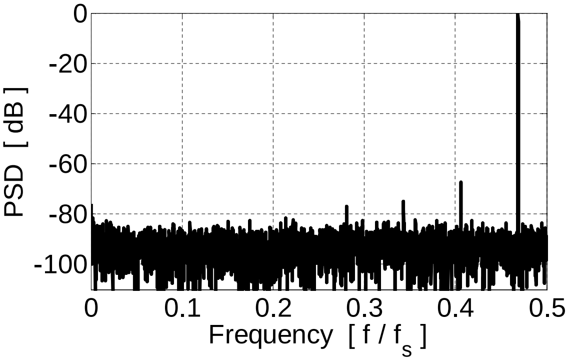


Figure 4.13: Measured 8,192-point FFT spectrum at 1 kS/s.

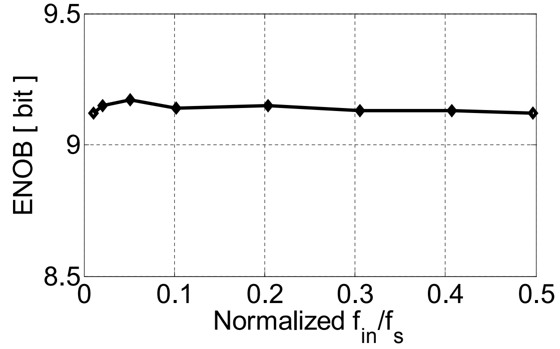
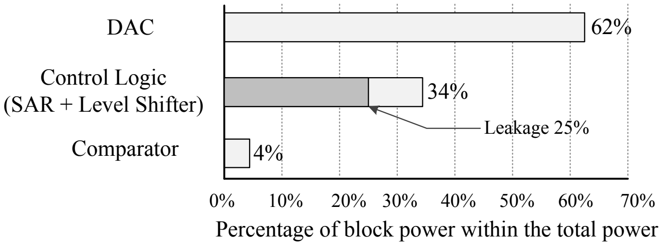


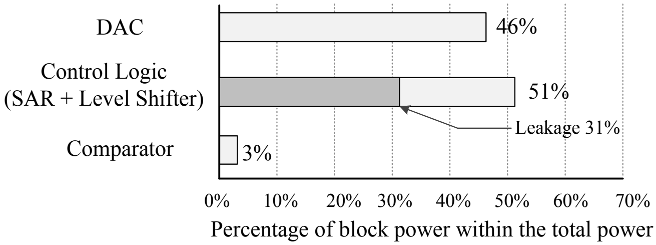
Figure 4.14: ENOB of the ADC versus input frequency.

Multiple supply voltage domains were utilized, allowing detailed measurement of the power consumption in the DAC, comparator, and SAR control logic, respectively. The total measured power consumption of the 1-kS/s ADC is 53 nW in dual-supply mode (V_{DDH} of 1.0 V for DAC and comparator, and V_{DDL} of 0.4 V for SAR logic) and 72 nW in 1-V single-supply mode. The measured leakage power of the digital part is 13 nW in dual-supply mode and 22 nW in 1-V single-supply mode, which constitutes 25% and 31% of the total power consumption, respectively. It implies that the digital leakage power consumption is a major contributor to the total power consumption.

The power of the level shifters was simulated based on post-layout extraction. In dual-supply mode, the level shifters consume 12 nW; in 1-V single-supply mode, they consume 10 nW. Excluding the 10-nW power consumption of level shifters from the total 72 nW would result in a total ADC power consumption of 62 nW in the single-supply mode. This indicates that the voltage scaling has reduced the overall power consumption of the ADC by 15% without any loss in performance. Fig. 4.15 shows the power breakdown of the ADC in the two modes. Table 4.1 summarizes the measured performance of the ADC.



(a) Dual-supply mode V_{DDH} = 1.0V and V_{DDL} = 0.4V



(b) Single-supply mode V_{DDH} = V_{DDL} = 1.0V

Figure 4.15: The ADC power breakdown in dual and single supply modes, where the percentage of digital leakage power is indicated by dark color.

The power and dynamic performance of the 1-kS/s ADC under different supply settings were measured. The figure-of-merit (FOM) which has been used to compare the ADC performance is defined as

$$FOM = \frac{Power}{\min\{f_S, 2 \times ERBW\} \times 2^{ENOB}} \tag{4.2}$$

Table 4.2 shows the measurement results together with the corresponding FOM. The ADC achieves the optimal performance at V_{DDH} = 1.0 V and V_{DDL} = 0.4 V with the lowest FOM of 94.5 fJ/Conversion.

As demonstrated in this work, at such low-sampling rates, leakage power becomes a significant portion of the total power, degrading the FOM as compared to ADCs for higher sampling rates. Therefore, Table 4.3 compares the measurement results of this work to previously published SAR ADCs with comparable sampling rates [46][47][48]. As the table shows, this ADC achieves the lowest power and FOM.

Table 4.1: ADC Measurement Summary

ADC Performance		
Technology	standard 0.13-μm CMOS	
Core area [mm^2]	0.19	
Resolution [bits]	10	
Input range	0 - V_{DD}	
Sampling rate [kS/s]	1	
DNL [LSB]	+0.54/-0.61	
INL [LSB]	+0.45/-0.46	
SNDR (at Nyquist) [dB]	56.7	
SFDR (at Nyquist) [dB]	67.6	
ADC Power Breakdown		
Supply voltage [V]		
Comparator, DAC	1.0	1.0
SAR	0.4	1.0
Comparator [nW]	2	2
Capacitive DAC [nW]	33	33
Control Logic (SAR+Level Shifter) [nW]	18	37
Total Power [nW]	53	72

Table 4.2: ADC Performance Under Different Supply Settings

$V_{DDH}/V_{DDL}[V]$	*0.8/0.4*	*1.0/0.4*	*1.0/1.0*	*1.2/1.2*
Power [nW]	45	53	72	94
ENOB (at Nyquist) [bit]	8.7	9.1	9.1	9.2
FOM [fJ/Conv.]	108.1	94.5	129.4	159.8

Table 4.3: ADC Comparison

	[46]	[47]	[48]	This Work
Technology	0.8 μm	0.35 μm	0.18 μm	0.13 μm
Sampling rate [kS/s]	0.8	1	4.1	1
Power [nW]	3000	230	850	53
ENOB [bit]	9	10.2	6.9	9.1
FOM [fJ/Conv.]	7300	195	1700	94.5

A comparison of the implemented ADC with our mismatch-limited power consumption bounds is shown in Fig. 4.16. The ADC is a bit far from the bounds because leakage power consumption, which is neglected in our power analysis for simplicity, does take a significant portion of the total ADC power consumption, thereby degrading the energy efficiency.

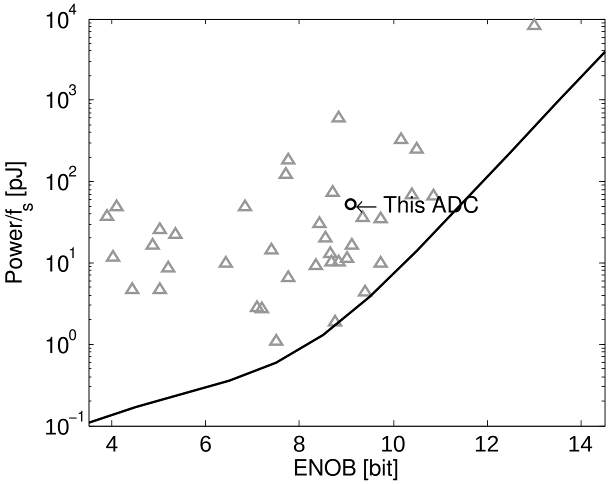


Figure 4.16: Predicted mismatch-limited SAR ADC power consumption bounds (solid line) together with Nyquist SAR ADC survey data (Δ) and the implemented ADC (o).

Chapter 5

A 3-nW 9.1-ENOB SAR ADC in 65 nm CMOS Process

In Chapter 4, we presented a 53-nW 9.1-ENOB SAR ADC at 1 kS/s in 0.13 μm CMOS process. Following a design strategy with maximum simplicity in the architecture, the ADC achieved the ultra-low-power consumption by using a binary-weighted capacitive DAC with a top-plate sampling technique, a dual-supply voltage scheme allowing the SAR control logic to operate at 0.4 V, as well as low-leakage circuit techniques and considerable design optimizations.

Based on the understanding from our previous work, in this chapter we present a single-supply-voltage 10-bit (9.1-ENOB) 1-kS/s SAR ADC in 65 nm CMOS process, with a substantial (94%) improvement in power consumption, resulting in 3-nW total power consumption.

Taking advantage of the smaller feature size and the availability of standard- and high-$\mathrm{V_T}$ devices in 65 nm process, the ultra-low-power consumption is achieved by: 1) a split-array capacitive DAC, which substantially reduces the DAC capacitance while still ensuring sufficient linearity; 2) a bottom-plate sampling approach reducing the charge injection error due to use of small DAC capacitance, while enabling full-range input sampling without extra voltage sources; 3) a multi-$\mathrm{V_T}$ design, allowing the ADC to meet the target performance with a single supply voltage of 0.7 V, thereby reducing both the switching and leakage power consumption; and 4) a latch-based SAR control logic resulting in reduced power consumption and low transistor count.

5.1 Comparison in Leakage between 0.13 μm and 65 nm CMOS Processes

The previous design in 0.13 μm CMOS process has shown that leakage is the issue. Fig. 5.1 shows the simulated transistor sub-threshold leakage current versus channel length in the standard 0.13 μm CMOS process, and Fig. 5.2 in the low-power 65 nm CMOS process. It can be seen that the leakage performance is much better in the low-power 65 nm process than that in the standard 0.13 μm process. Moreover, high-V_T devices are the primary choice in this design where leakage is the major concern.

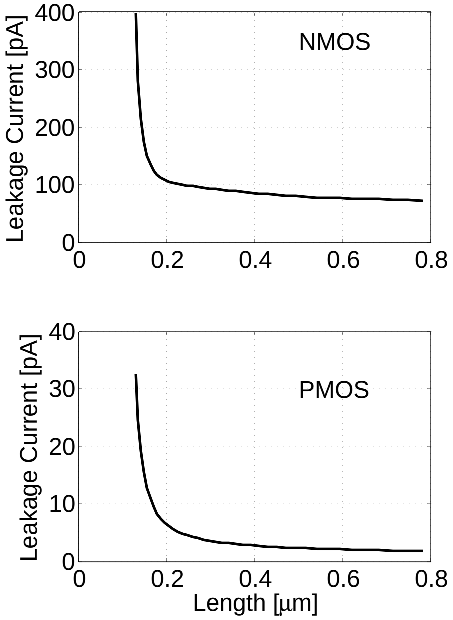
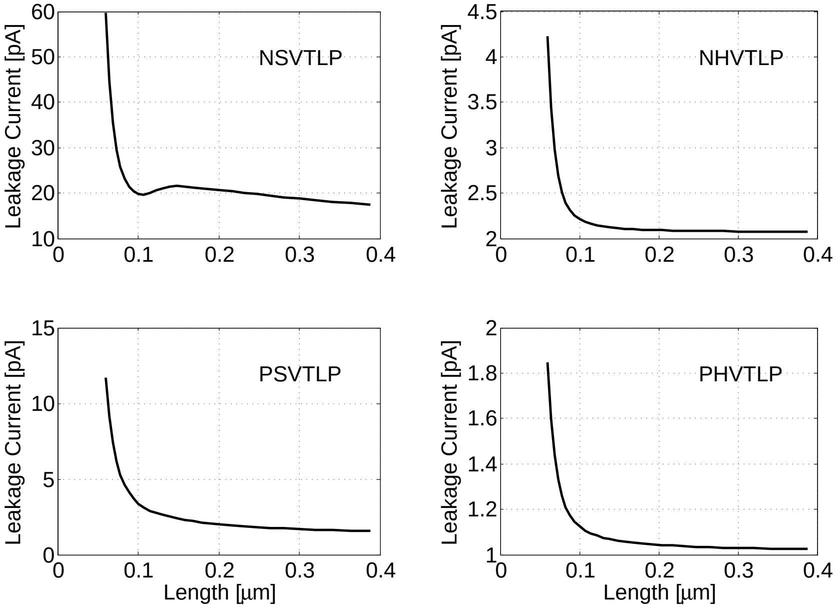


Figure 5.1: Simulated transistor sub-threshold leakage current versus channel length in standard 0.13 μm process at 0.15-μm W_{min}, 1-V supply, typical corner, and 27°C.

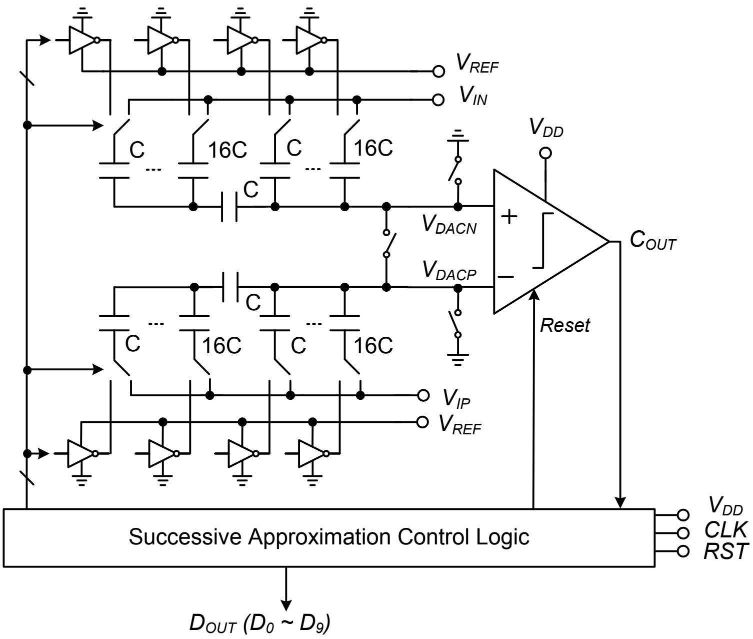


(a) (b)

Figure 5.2: Simulated transistor sub-threshold leakage current versus channel length in low-power 65 nm process at 0.135-μm W_{min}, 1-V supply, typical corner, and 27°C: (a) standard-V_T devices (b) high-V_T devices.

5.2 ADC Architecture

The architecture of the proposed SAR ADC is shown in Fig. 5.3. It comprises a differential capacitive DAC, a dynamic latch comparator, and a synchronous SAR control logic.



V_{REF}
V_{IN}
C
16C
C
16C
C
V_{DD}
+
−
V_{DACN}
V_{DACP}
C_{OUT}
Reset
C
16C
C
16C
V_{IP}
V_{REF}
Successive Approximation Control Logic
V_{DD}
CLK
RST
D_{OUT} (D_0 ~ D_9)

Figure 5.3: SAR ADC architecture.

5.2.1 Split-Array DAC

The metal capacitor in 65 nm CMOS process has good matching properties. It has a matching of 0.5 $\%\mu\mathrm{m}$ and a density of 0.4 fF/$\mu\mathrm{m}^2$. For a 10-bit binary-weighted capacitive array, it leads to a minimum unit capacitance of 0.2 fF based on Eq. (2.31). While the minimum metal capacitance defined by the design-kit is 10 fF, which is much larger than necessary to meet the linearity requirements, thereby resulting in considerably large array capacitors and high switching power consumption.

Hence, we implemented a split binary-weighted capacitive array with 5-bit sub-DAC and 5-bit main-DAC. Based on Eq. (2.31), it requires a larger unit capacitor of 6 fF compared to that in a single-array DAC. Further considering the design margin, a 15-fF unit capacitance is chosen, which still arrives at a smaller total array capacitance of 945 fF.

5.2.2 Bottom-Plate Sampling

Since the array capacitance is significantly reduced, the charge injection during sampling will degrade the conversion accuracy, and therefore bottom-plate sampling technique is used to minimize the error.

When a full-range input voltage is sampled on the bottom-plates, the top-plate nodes are usually reset to the input common-mode. Otherwise, the DAC outputs will go beyond the rails for certain input range. In this work, we use a sampling approach to avoid introducing the extra reset voltage source, and at the same time the approach still ensures full-range input sampling without degrading the signal-to-noise ratio.

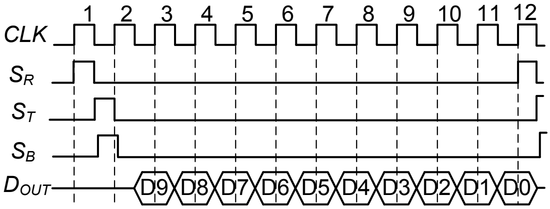
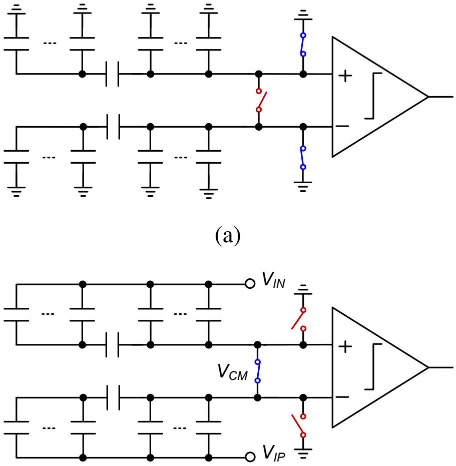


Figure 5.4: Time sequence of SAR ADC.



(b)

Figure 5.5: DAC arrays during (a) reset phase (b) sampling phase.

Figure 5.4 illustrates the time sequence of the SAR ADC, which takes 11 clock cycles in total to complete one conversion. The first clock cycle is divided into reset phase and sampling phase. Fig. 5.5 depicts the switching status of DAC arrays during the two phases. In reset phase (Fig. 5.5(a)), the control signal, indicated as S_R in Fig. 5.4, becomes high. The capacitors are discharged to ground. When it comes to the sampling phase (Fig. 5.5(b)), the control signals, driving the bottom-plate switches and the top-plate connection switch, turn to high, which are indicated as S_T and S_B in Fig. 5.4, respectively. The bottom-plates of the differential capacitor arrays are then connected to the differential input. The top-plates are shorted, and their voltage becomes the input common-mode. Consequently, only the differential-mode input is sampled on the array, which makes the DAC outputs always remain within the rails.

To minimize the charge injection error, the top-plate connection switch is turned off before the bottom-plate switches. As shown in Fig. 5.4, the signal S_B is delayed by a series of weak inverters compared to the signal S_T.

5.2.3 Low-Voltage Single Supply

Lowering the supply voltage is an efficient technique to reduce both the switching and leakage power. This is particularly true for digital circuits, where transistors can be substantially slow but still meet the target data-rates. For the analog circuits, however, low voltages will introduce sampling distortions and comparator decision error. In our previous work, a dual-supply voltage scheme was utilized. The additional supply and level shifters increase the design complexity and consume extra power.

In this work we chose a single supply for simplicity. In addition, a combination of high-$\mathrm{V_T}$ and standard-$\mathrm{V_T}$ transistors is utilized to minimize the leakage while still ensuring sufficient speed at low voltages (down to 0.6 V), thereby achieving the optimal energy efficiency. Our measurement results (in Sec. 5.4) show that the ADC achieves 4.5 fJ/conversion-step with 8.8 ENOB at 0.6 V and 1 kS/s.

5.3 Circuit and Chip Implementation

5.3.1 Capacitive DAC

As aforementioned, the DAC with split-array, shown in Fig. 5.3, is composed of two binary-weighted capacitive arrays with an attenuation capacitor in the middle. The attenuation capacitor is set to be the unit capacitance instead of a fractional value for ease of layout and good matching. Removing a dummy unit capacitor at the end of the sub-DAC introduces gain error about 1 LSB. If necessary, the gain error can be calibrated in the digital domain.

A careful layout to avoid linearity degradation is important as well. Fig. 5.6 illustrates the DAC layout floor plan for one differential branch. Both the main-DAC ($\mathrm{C_9}$-$\mathrm{C_5}$) and sub-DAC ($\mathrm{C_4}$-$\mathrm{C_0}$) use a partial common-centroid strategy. The MSB capacitors follow a common-centroid configuration to minimize the errors from

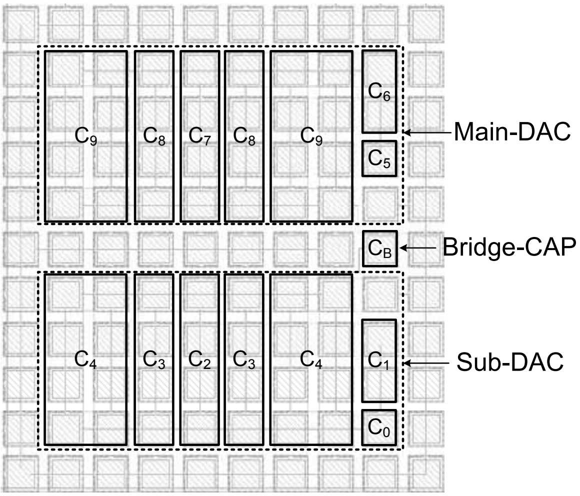


Figure 5.6: Layout floor plan of the capacitor array. The capacitors, not indicated in the figure, are dummies.

the non-uniform oxide growth in the metal capacitors. The smaller LSB capacitors are placed close to the switch network to simplify the interconnection.

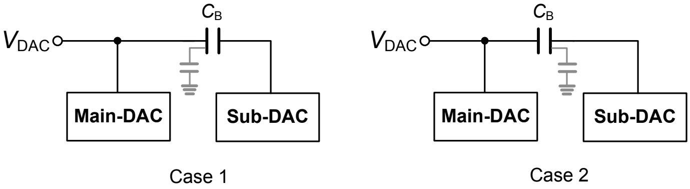


Figure 5.7: The parasitic capacitance of the bridge capacitor: 1) connected to the main-DAC (Case 1); 2) connected to the sub-DAC (Case 2).

The parasitic capacitance associated with the bridge capacitor degrades the ADC performance. Fig. 5.7 shows two connection cases of the parasitic capacitor. Intuitively, the capacitor plate which contributes the major parasitic capacitance should be connected to the main-DAC, which is 'Case 1' in Fig. 5.7. Since the sub-DAC interpolates between transition voltages generated by the main-DAC, if the parasitic capacitor is connected to the sub-DAC, it will introduce more step variations to the transfer curve. To verify the effect by simulation, the capacitive DAC was implemented under three cases: 1) parasitic capacitance of 10 fF connected to the main-DAC; 2) parasitic capacitance of 10 fF connected to the sub-DAC; and 3) ideal bridge capacitor without parasitics. The ADC dynamic performance at near-DC input frequency of the three cases based on transistor-level simulations are given in Table 5.1. Compared to the ideal case, the parasitic capacitor degrades the ADC performance. Moreover, the worst case happens when the parasitic capacitor is connected to the sub-DAC. Therefore, in the DAC layout, the plate of the bridge capacitor which contributes the major parasitic capacitance is deliberately connected to the main-DAC.

Table 5.1: ADC Dynamic Performance With Respect to Bridge Capacitor Connection

	SNR	SNDR	THD	Unit
Case 1 (to Main-DAC)	60.77	60.39	-71.13	dB
Case 2 (to Sub-DAC)	60.24	59.77	-69.64	dB
Case 3 (Ideal)	60.84	60.45	-71.14	dB

5.3.2 Switch Design

The switches of the capacitor array are shown in Fig. 5.8. Multi-$\mathrm{V_T}$ design approach has been used. Three types of transistors are provided by the process: high-$\mathrm{V_T}$, standard-$\mathrm{V_T}$, and low-$\mathrm{V_T}$. Because low-$\mathrm{V_T}$ transistors have high leakage current, they are not suitable for this design. Hence, only high-$\mathrm{V_T}$ and standard-$\mathrm{V_T}$ transistors are used, and they are indicated by HVT and SVT in the figure, respectively.

Since the conversion time is long and the top-plate nodes are floating during the conversion, to minimize the voltage droop caused by leakage current, the top-plate switches are all using high-$\mathrm{V_T}$ NMOS. Moreover, in order to further reduce the leakage current, the reset-switches utilize a two-transistor stack and long channel length ($1\mu m$), and the connection-switch uses four times the minimum channel length.

At the bottom-plates of the capacitive array, transmission gates with standard-$\mathrm{V_T}$ devices are used to speed up the DAC settling when V_{IN} is near mid-range. However, the inverters, switching the bottom-plate nodes between ground and V_{REF}, are implemented with high-$\mathrm{V_T}$ transistors to reduce the leakage current from V_{REF}.

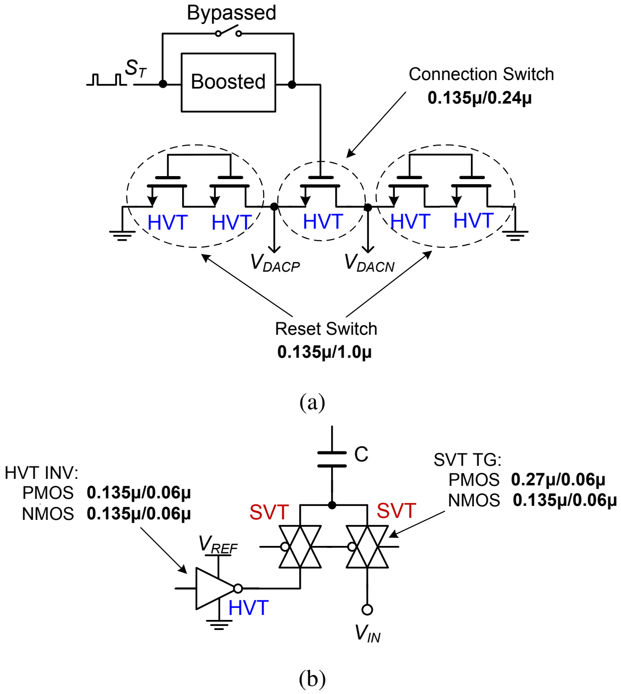

Bypassed
S_T
Boosted
Connection Switch
0.135μ/0.24μ
HVT
HVT
HVT
HVT
HVT
V_{DACP}
V_{DACN}
Reset Switch
0.135μ/1.0μ
(a)
C
HVT INV:
PMOS 0.135μ/0.06μ
NMOS 0.135μ/0.06μ
SVT
SVT
SVT TG:
PMOS 0.27μ/0.06μ
NMOS 0.135μ/0.06μ
V_{REF}
HVT
V_{IN}
(b)

Figure 5.8: (a) Top-plate switches. (b) Bottom-plate switches.

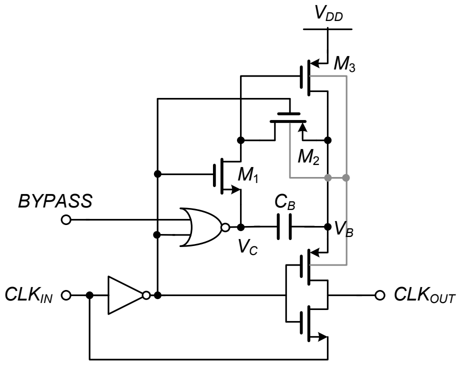

V_{DD}
M_3
M_2
M_1
BYPASS
C_B
V_B
V_C
CLK_{IN}
CLK_{OUT}

Figure 5.9: Voltage boosting circuit with bypass function.

Though the top-plate connection-switch with high-$\mathrm{V_T}$ devices effectively reduces the sub-threshold leakage current, its high on-resistance will introduce severe distortions at low supplies when it passes midrail voltages. In view of this, a voltage boosting circuit, similar to [49], is used to drive the connection-switch at low supply voltages. As depicted in Fig. 5.9, when the input clock goes low, M_1 and M_3 turn on, M_2 turns off, V_C goes to ground, V_B connects to V_{DD}, and the output clock goes low; when the input clock goes high, M_1 and M_3 turn off, M_2 turns on, V_C connects to V_{DD}, V_B is then boosted to $2V_{DD}$, and the output clock goes high with $2V_{DD}$. In practice, due to charge sharing between $\mathrm{C_B}$ and the parasitic capacitance associated to node V_B, the boosted output is less than $2V_{DD}$.

The boosting circuit can be disabled by setting the *BYPASS* signal to high. The output of the NOR gate is then kept at ground, and the output logic high always equal to V_{DD}.

5.3.3 Dynamic Latch Comparator

The dynamic latch comparator [50] is shown in Fig. 5.10. It has no static biasing. Buffers are connected successively to make the output loading identical. A followed cross-coupled NAND gates store the comparison result for an entire clock cycle. The reset signal is synchronous with the clock of the SAR control logic.

Similarly, the comparator utilizes a combination of high-$\mathrm{V_T}$ and standard-$\mathrm{V_T}$ transistors to minimize the leakage while ensuring the target speed at low voltages. Standard-$\mathrm{V_T}$ devices are used for the differential input transistors and the cross-coupled inverters to enhance the comparison speed. A high-$\mathrm{V_T}$ PMOS is implemented for the bias transistor to reduce the leakage current from the supply.

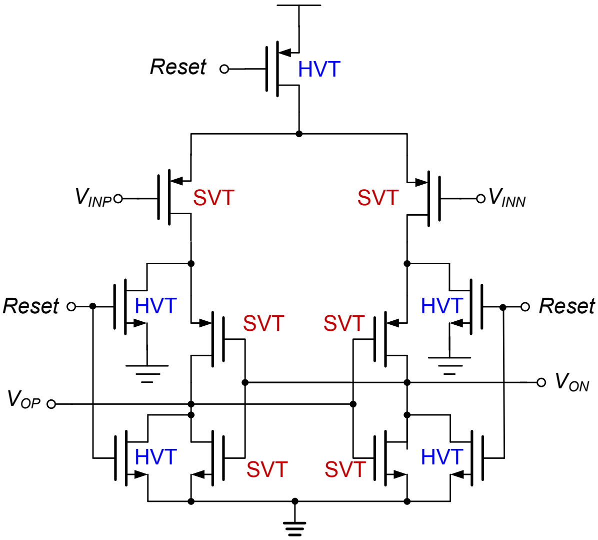


Figure 5.10: Dynamic latch comparator with high- and standard-$\mathrm{V_T}$ transistors.

Since the input common-mode voltage of the comparator is kept at mid-rail voltage, the comparator offset appears as static offset, which does not affect the ADC linearity [18]. However, the offset decreases the input voltage range, thus degrading the signal-to-noise ratio. Monte Carlo simulations of the comparator offset showed a standard deviation of 17 mV. Assuming 3σ is considered, it results in a total offset voltage of 51 mV, decreasing the SNR by 0.7 dB. The decreased SNR introduces an ENOB loss of 0.1 bit.

5.3.4 SAR Control Logic

The SAR control logic is shown in Fig. 5.11. It consists of a shift register, a set of bit latches, a sample signal generator, and a combinational switching logic. Due to the low sampling rate, static logic instead of dynamic one is used for the register and latches to avoid charge leakage. On the other hand, since speed is not a major concern, the logic circuits are designed with minimum size.

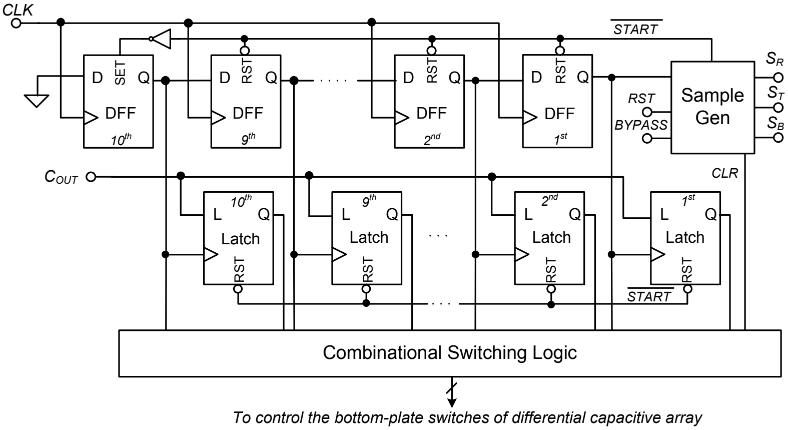

CLK
START
D SET Q
DFF
10th
D RST Q
DFF
9th
DFF
2nd
DFF
1st
RST
BYPASS
Sample Gen
S_R
S_T
S_B
CLR
C_{OUT}
L Q
Latch
RST
10th
9th
2nd
1st
START
Combinational Switching Logic
To control the bottom-plate switches of differential capacitive array

Figure 5.11: SAR digital control logic.

A latch instead of a DFF, shown in Fig. 5.12, is used to store the comparator decision, thus reducing the transistor count and lowering the power consumption. However, special care must be taken during generating the latch signal. The latch may miss the current comparator result and record the successive one due to an improper latch signal. In this design, the output signal from the corresponding-order DFF of the shift register, indicated in Fig. 5.11, is used to clock the latch.

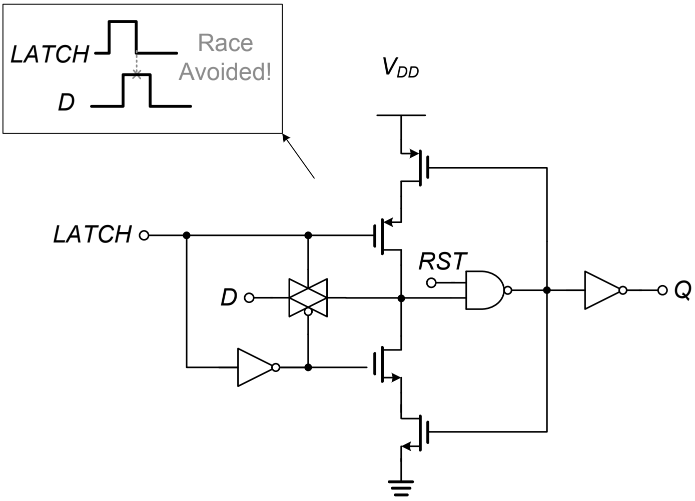


Figure 5.12: Latch circuit.

5.3.5 Chip Implementation

A micrograph of the entire ADC in 65 nm CMOS process is shown in Fig. 5.13. The core occupies 0.037 mm^2, while the remaining area in the figure is used for supply decoupling. For clarity, the right part of Fig. 5.13 shows the ADC layout including the differential capacitive DAC, the comparator, and the SAR digital logic.

Table 5.2 shows the power breakdown of the ADC at 0.7 V and 1 kS/s according to simulations. By subtracting the schematic-based total power consumption from the post-layout-based one, the power consumption of parasitics is approximated to be 1.24 nW, which constitutes a large portion of the total power (44%). This can be improved by optimizing the layout, but it also demenstrates that the interconnection becomes more significant for such a low-speed design with small transistor dimensions in deep-submicron technology. In addition, according to the schematic-level simulation, the total leakage power is 0.67 nW, which contributes 43% of the total power consumption.

Table 5.2: Simulated Power Consumption

	Schematic [nW]	Post-layout [nW]
Comparator	0.09 (6%)	0.25 (9%)
DAC	0.75 (48%)	1.10 (39%)
SAR logic	0.73 (46%)	1.46 (52%)
Total	1.57 (100%)	2.81 (100%)

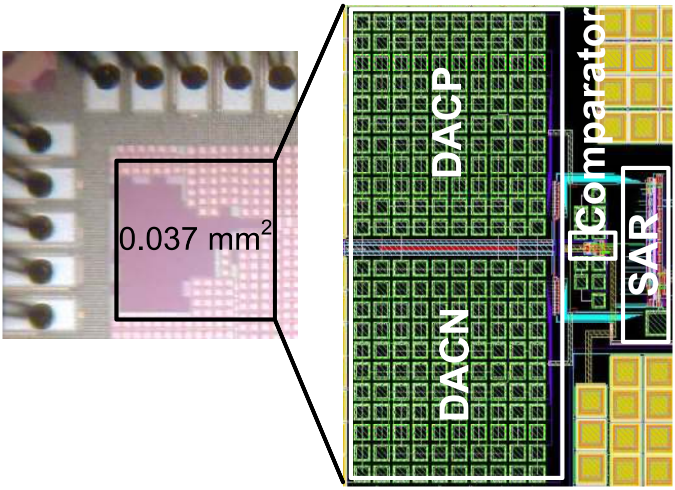


Figure 5.13: Die photo and layout view of the ADC in 65 nm CMOS process.

5.4 Measurement Results

Histogram and tone test were conducted to measure the static and dynamic performance of the 1-kS/s ADC, respectively. At V_{DD} of 0.7 V, the measured peak DNL error is +0.48/-0.55 LSB, and the peak INL error is +0.52/-0.61 LSB, as shown in Fig. 5.14.

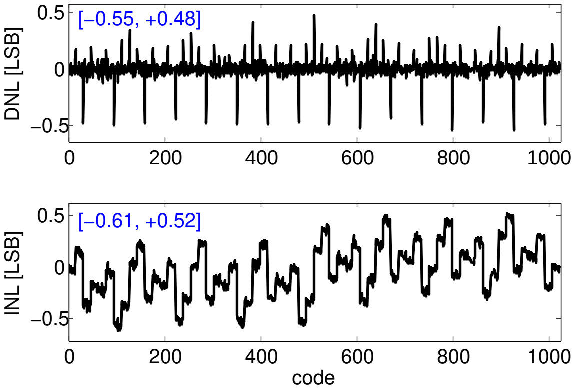


Figure 5.14: Measured DNL and INL errors of 1-kS/s 0.7-V ADC.

At the same supply, the measured FFT spectrums of the ADC at both near-DC and near-Nyquist operations are depicted in Fig. 5.15. The amplitude of the test stimulus was set to -0.65 dBFS. At near-DC operation, the measured SNDR is 57.1 dB, providing 9.2 ENOB. When the input frequency increases to near-Nyquist bandwidth, the measured SNDR becomes 56.6 dB, resulting in 9.1 ENOB.

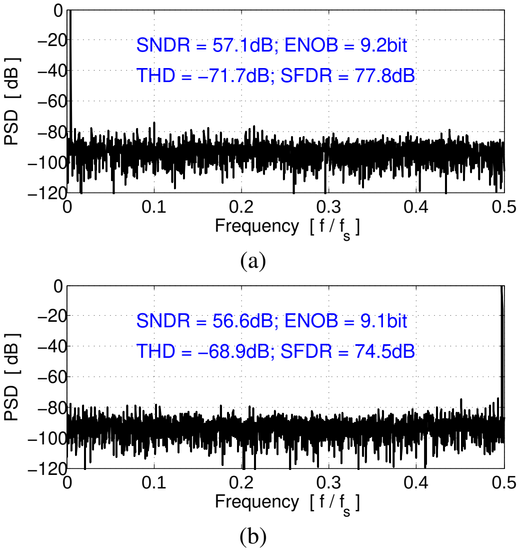


Figure 5.15: Measured 8,192-point FFT spectrums of 1-kS/s 0.7-V ADC: (a) near DC (b) near Nyquist.

The measured total power of the 1-kS/s ADC at 0.7 V is 3 nW, leading to a FOM of 5.5 fJ/conversion-step. Table 5.3 summarizes the measured performance of the ADC.

The power and ENOB of the 1-kS/s ADC under different supply voltages were also measured, and the results are shown in Table 5.4. At V_{DD} from 0.6 V to 1.0 V, the sampling switch is boosted; At V_{DD} of 1.2 V, the boosted circuit is bypassed. The ADC achieves the minimum FOM of 4.5 fJ/conversion-step at 0.6 V.

Table 5.5 compares the measurement results of this work to previously published SAR ADCs with comparable sampling rates. As the table shows, this ADC achieves the lowest power and FOM.

Table 5.3: ADC Measurement Summary

Technology	low-power 65-nm CMOS
Core area [mm^2]	0.037
Resolution [bit]	10
Input range [V]	0 - V_{DD}
Sampling rate [kS/s]	1
Supply voltage [V]	0.7
DNL [LSB]	+0.48/-0.55
INL [LSB]	+0.52/-0.61
SNDR (near Nyquist) [dB]	56.6
SFDR (near Nyquist) [dB]	74.5
THD (near Nyquist) [dB]	-68.9
ENOB [bit]	9.1
Total power [nW]	3
FOM [fJ/Conv.]	5.5

Table 5.4: Measured ADC Performance Under Different Supply Voltages

V_{DD} [V]	Power [nW]	ENOB [bits]	FOM [fJ/Conv.]
0.6	2	8.8	4.5
0.7	**3**	**9.1**	**5.5**
0.8	4	9.1	7.3
0.9	5	9.2	8.5
1.0	6	9.2	10.2
1.2	8	9.0	15.6

*N*ote: For V_{DD} = 0.6 V - 1.0 V, the sampling switch is boosted; for V_{DD} = 1.2 V, the sampling switch is not boosted.

Table 5.5: ADC Comparison

	[47]	[48]	[22]	[51]	This Work
Technology	0.35 μm	0.18 μm	0.13 μm	65 nm	65 nm
Sampling rate	1 kS/s	4.1 kS/s	1 kS/s	20 kS/s	1 kS/s
Area [mm^2]	N/A	0.11	0.19	0.212	0.037
Supply voltage [V]	1.0	0.5	1.0/0.4	0.55	0.7
Power [nW]	230	850	53	206	3
ENOB [bit]	10.2	6.9	9.1	8.84	9.1
FOM [fJ/Conv.]	195	1700	94.5	22.3	5.5

A comparison of the implemented ADC with our mismatch-limited power consumption bounds is shown in Fig. 5.16. Compared to the previous ADC, this ADC is quite close to the bounds. The leakage power consumption is significantly reduced due to the less-leaky low-power 65 nm CMOS process, thus improving the energy efficiency.

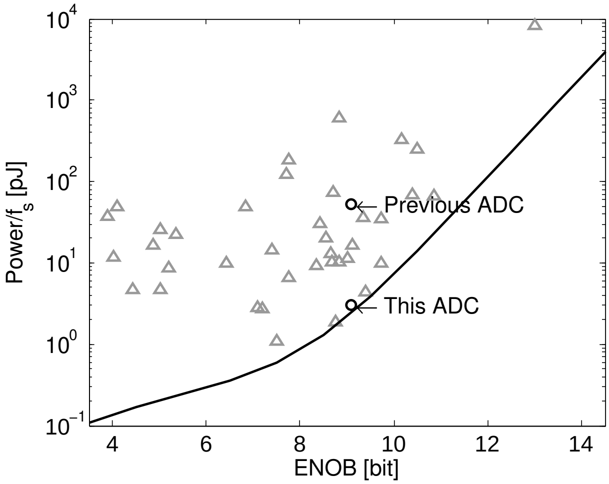


Figure 5.16: Predicted mismatch-limited SAR ADC power consumption bounds (solid line) together with Nyquist SAR ADC survey data (Δ) and the implemented ADCs (o).

Chapter 6

Conclusions

Implantable medical electronics require low-speed, medium-resolution ADCs with ultra-low-power operation. Among prevalent ADC architectures, SAR ADCs are favored due to their high energy efficiency. The error sources as well as the power consumption bounds of the SAR ADC have been analyzed. At low resolution, the power consumption of SAR ADC is bounded by digital switching power. At medium-to-high resolution, the power consumption is bounded by thermal noise if digital assisted techniques are used to alleviate mismatch issues; otherwise it is bounded by capacitor mismatch.

Two 10-bit 1-kS/s SAR ADCs have been implemented. Following the design strategy with maximum simplicity in the architecture, the first ADC, implemented in a standard 0.13 μm CMOS process, achieves 9.1 ENOB with 53-nW power consumption by using a binary-weighted capacitive DAC with a top-plate sampling technique, a dual-supply voltage scheme allowing the SAR control logic to operate at 0.4 V, as well as low-leakage circuit techniques and considerable design optimizations. The leakage power constitutes 25% of the total power consumption.

Based on the understanding from the first chip, the second ADC, implemented in a low-power 65 nm CMOS process, achieves 9.1 ENOB and makes a substantial (94%) improvement in power consumption, resulting in 3-nW total power consumption. The ultra-low-power consumption is achieved by using an architecture with maximal simplicity, a small split-array capacitive DAC, a bottom-plate sampling approach reducing charge injection error and allowing full-range input sampling without extra voltage sources, and a latch-based SAR control logic resulting in reduced power and low transistor count. Furthermore, a multi-V_T circuit design approach allows the ADC to meet the target performance with a single supply voltage of 0.7 V. The ADC can even operate down to a supply voltage of 0.6 V, achieving an optimal energy efficiency of 4.5 fJ/conversion-step with 8.8 ENOB at 1 kS/s.

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