Design of UWB Transceiver SiP for Short Range Communication

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***Abstract*—Since UWB system uses a wide frequency range from 3.1GHz to 5.1GHz, package parasitic effects have been a hot issue which affects system malfunction. To prevent such malfunction, SiP technology is adjusted considering not only a circuit performance but various design issues in a package from viewpoints of signal integrity and power integrity. Furthermore, UWB band-pass filter is embedded into a package to reduce a complexity of transmitter circuit and the power consumption. Designed UWB SiP performance is verified by the measurement in time domain.**

Keywords- UWB; SiP; signal integrity; power integriy; embedded filter

I. INTRODUCTION

Since a permission of Ultra-Wideband (UWB) from 3.1GHz to 10.6GHz as commercial use by Federal Communication Committee (FCC) in 2002 [1], UWB system has become one of the most expected technologies in Wireless Personal Area Networking (WPAN). FCC defined UWB system clearly as wireless system whose fractional bandwidth is more than 20% [2].

However, such a high and wide frequency can bring a serious problem that degrades system performance and reduce a success rate. Even if a circuit operation is verified on chip, a package with whole circuit system may have a trouble. Because a package environment includes many noise sources, it is not appropriate to transmit high frequency signal [3]. Many interconnections between active components such as wire-bonding, transmission line and via behave like a low pass filter which consists of capacitor and inductor. UWB signal with such a high and wide frequency is sensitive to the interconnection between a circuit and package. Moreover, the power for circuit operating comes from a package plane whose dimension is fixed, which can be another noise source that degrades system performance. Hence, not only active circuits but also package environment should be considered simultaneously in design process of high frequency system. In System-in-Package (SiP) technology, the role of a package is to integrate two chips and any other passive components as well as to protect from outside [4].

Proposed UWB transceiver System-in-Package (SiP) uses broad-band range from 3.1GHz to 5.1GHz known as low range of UWB. To makes UWB signal, transmitter system needs two parts, the impulse generator on chip and band-pass filter on package [7]. This transmitter scheme has many merits such as low power consumption and small circuit area. Moreover, in this research, passive band-pass filter, which is another part to make UWB signal, is embedded into a UWB package. Therefore we can achieve smaller UWB transmitter system than previous work [5][7]. On the other hand, the receiver part to recover digital signal from UWB signal is mainly designed on chip. In addition, to increase the success rate and receiver sensitivity, the external environment of package such as minimum wire-bonding effect, output load modeling for accurate buffer size on chip, optimized via size for transmitting signal and plane dimension for avoiding resonance frequency should be also considered simultaneously. Considering above factors, we have manufactured UWB transceiver SiP, then verified in time domain by the measurement.

II. TRANSMITTER AND RECEIVER CIRCUITS

The whole system mainly composed of chip and package as shown in Figure 1. The modulation scheme in this system is on-off keying which means that only one UWB signal is generated when data is one. The target date rate of UWB system is over 100Mbps which is higher than WLAN.

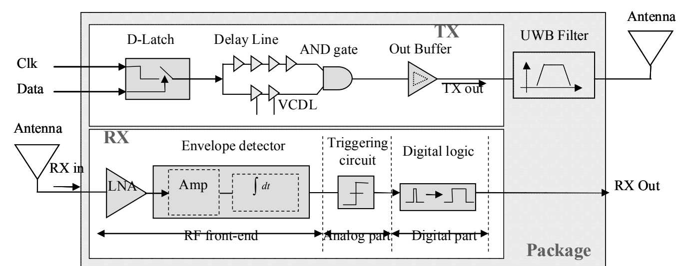

Figure 1 Transmitter consists of only digital blocks on chip and band-pass filter on package. The receiver system is mainly designed on chip.

A. *Two Parts of UWB Transmitter : Impulse Generator on Chip and Band-Pass Filter on Package*

To generate UWB signal, clock and data signal are needed at transmitter circuit. Using these digital signals, transmitter circuit on chip produces sharp impulse signal which has many frequency components from low frequency to over-10GHz.

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The band-pass filter in package is needed to shape the impulse signal from 3.1GHz to 5.1GHz to satisfy the target specification. Furthermore, stop-band region less than 3.1GHz or more than 5.1GHz should have large insertion loss to satisfy UWB regulation mask from FCC [1]. The generated UWB signal from the band-pass filter heads to the broad band antenna to radiate UWB signal to the outside.

B. *UWB Receiver Circuit*

The receiver circuit on chip only recovers digital signal from UWB signal. To minimize the complexity of circuit and increase the success rate, receiver circuit is composed of simple blocks and uses non-coherent scheme without PLL or VCO [8]. Furthermore, the bias voltage for analog or RF circuit comes from a package directly without any bias circuit on chip.

Figure 2 shows a fabricated transmitter circuit and receiver circuit using TSMC 0.18um process. Total transmitter dimension is about 0.25x0.22mm^2 and receiver circuit also has small dimension about 1.75x0.74mm^2.

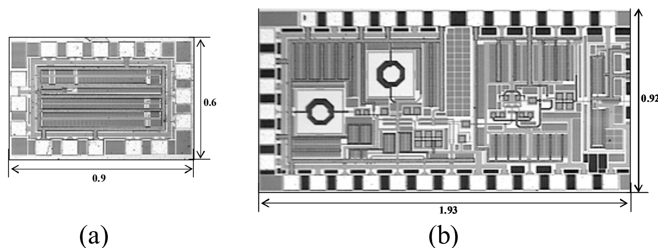


Figure 2 Photograph of (a) transmitter circuit and (b) receiver circuit

III. UWB PACKAGE

There are many considerable issues when designing UWB transceiver package to avoid a critical hazard and minimize parasitic components. The main issue is how to embed band-pass filter into package and minimize via effect to occur an impedance mismatching. Interconnections such as wire-bonding and transmission line between chip and package should be considered to verify the transmission capability of UWB signal and the impulse signal. Furthermore, plane size which is related with whole package size and generates certain noise also should be considered.

A. *Minimization of Bonding Effect to Reduce the Impedance Mismatching*

Wire-bonding which is used to connect chip and package has high impedance at high frequency range such as UWB and it causes impedance mismatching. Moreover its value is proportional to the length of wire-bonding. Therefore, to reduce the reflection at wire-bonding, we use minimum pad size and arranged as close to the chip pad as possible. However, this approach has small trouble that the minimum pad size causes different impedance mismatching with transmission line. To solve this problem, only I/O pads have different pad size to satisfy 50ohm [6]. Figure 3 shows an attached receiver circuit using wire-bonding and designed pads shape. The I/O pad size for UWB signal has larger size than power/ground pads size.

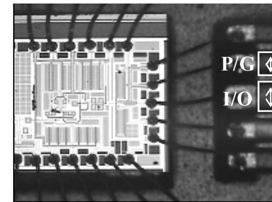


Figure 3 Photograph of wire-bonding between chip pad and bonding pads on package. Bonding pads have different size depending on its function.

B. *Output Load Modeling for Output Buffer Size on Chip*

The exact modeling of I/O load needed in advance to design circuits correctly and increase the success rate. The output load where the impulse signal heads to from transmitter circuit should be modeled accurately to determine a size of output buffer on chip. There are many mismatching factors outside such as wire-bonding, transmission line, and so on. They can be modeled as combination of resistor, capacitor and inductor as shown in Figure 4.

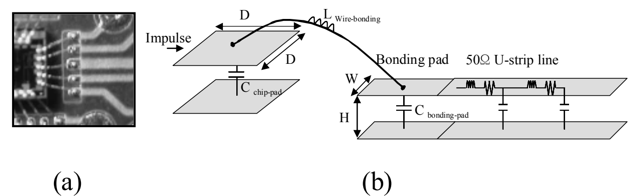


Figure 4 (a) Photograph shows output load of the package and (b) it can be modeled as lumped elements such as resistor, capacitor and inductor.

A few assumptions should be made before modeling. A package material, the characteristic impedance of u-strip, the rising time of the signal from the chip, and the length of transmission line should be determined. Chip pad and bonding pad can be modeled as a capacitor using equation (1) [6]. Wire bonding can be modeled as an inductor using rule of thumb which indicates 1nH per 1mm. The time delay in transmission line is obtained using equation (2) [6].

$$C = \varepsilon_o \varepsilon_r \frac{A}{d} \tag{1}$$

$$TD = \frac{Length}{c / \sqrt{\varepsilon_r}} \tag{2}$$

The transmission line can be represented by the combination of resistor, inductor and capacitor. Total capacitance and inductance can be simply given using equation (3) and (4) [6]. The number of segment is obtained using equation (5) [6]. The rising time in this case assumed about 50ps whose bandwidth is 6.3GHz.

$$L_{total} = (TD)(Z_o) \tag{3}$$

$$C_{total} = \frac{TD}{Z_o} \tag{4}$$

$$Segment \geq 10\left(\frac{Length}{T_r c / \sqrt{\varepsilon_r}}\right) \quad (5)$$

The total inductance and capacitance are divided according to the segments. The resistance per segment is obtained by the equation (6).

$$R = 2\sqrt{\frac{\pi f \mu}{\sigma}} \quad (6)$$

Following above steps, the output load shown in Figure 5 (a) can be modeled like Figure 5 (b). The black line in Figure 5(c) shows a measurement result and the gray line represents a simulation result. Two results show a fine correlation. Hence, we can obtain a suitable output buffer size in CMOS about 240um/80um.

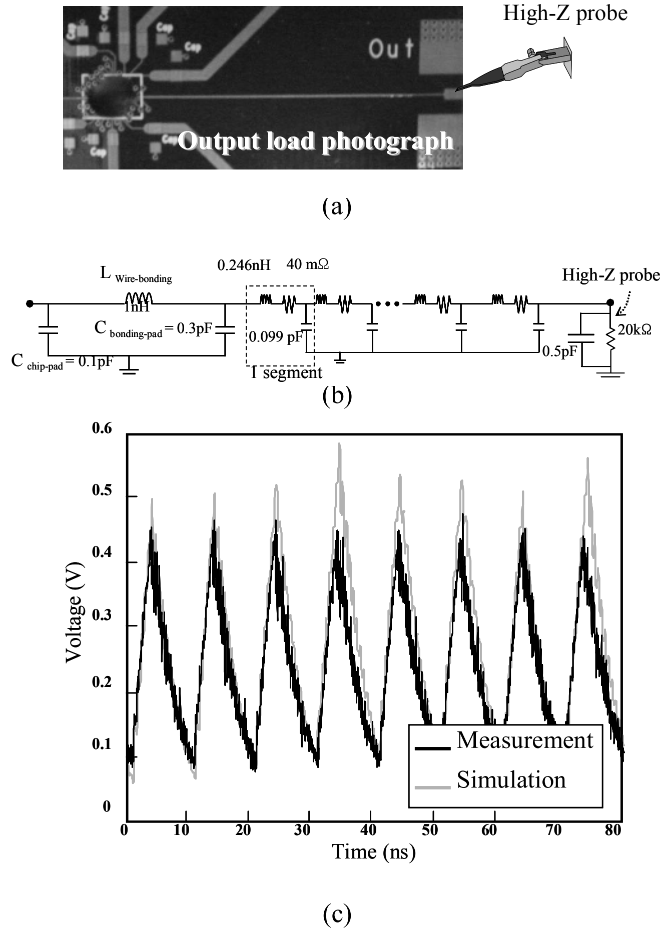


Figure 5 (a) Photograph of output load (b) The model has various lumped components. (c) The measurement result and simulation result from model have a good correlation.

C. Signal Transmission with Minimization of Via Effect

Impulse signal or received signal from the antenna can not avoid 'via effect' which acts as a low-pass filter to go from circuit to the test board. Therefore, it is need to consider this effect and try to minimize it in advance before the real package design. Especially, signal via which cause a reference change in package degrade rising time or make a impedance reflection whenever signal goes down from top layer to bottom layer. Signal via can be modeled using capacitor (C_{via}) from the anti-pad and inductor (L_{via}) from the length of via as shown in Figure 6 (a). It looks like a simple low-pass filter, so there arise so much insertion loss whenever high frequency signal transmitted. While, inductance has fixed value from fixed stack-up, the capacitance can change using a size of anti-pad. In our search, we have found optimized via size that has the highest transmission capability in advance using 3D full wave simulator. However there is always a tolerance error when manufacturing a package. So, dummy packages which considered tolerance error factor are designed and verified the simulation result using measurement. The photograph in Figure 6 (b) shows measurement setup using microprobe, dummy packages and board, and the left graph represents simulation and measured S-parameter results depending on the via clearance. Impulse or UWB signal will go down from port1 to port2 in real package. The gray dot line shows a 3D simulation result which has maximum insertion loss between 3.1GHz and 5.1GHz is about -1.06dB. The black dot, dash and solid line shows a measurement result depending on dummy package that has different via clearance. From this result, the optimized via clearance about 0.1mm to avoid a reflection is obtained. By these pre-simulation and measurement, more fine and exact design becomes possible and they help the package to have high transmission capability.

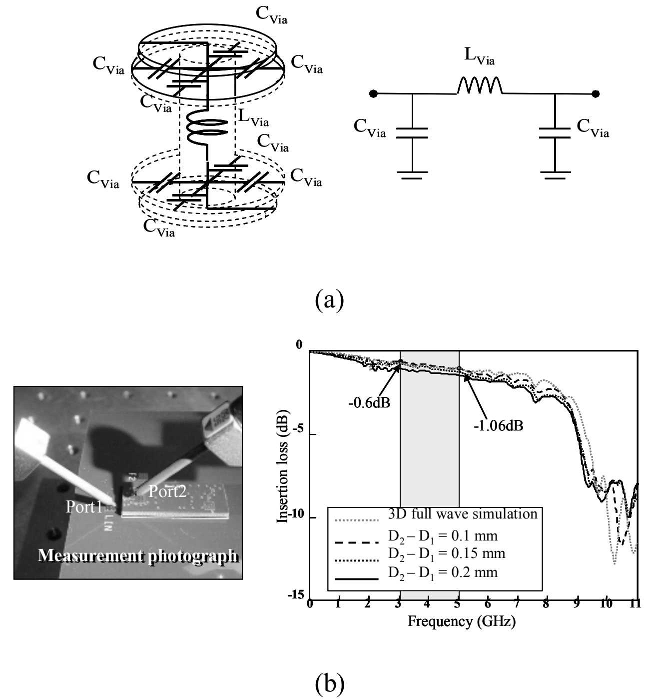
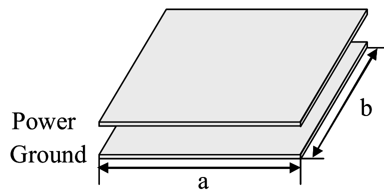


Figure 6 (a) 3D full-wave simulation setup has two ports at the end of via. (b) Photograph of measurement setup using microprobe on the dummy package and board (c) Simulated and measured S-parameter depending on the via clearance

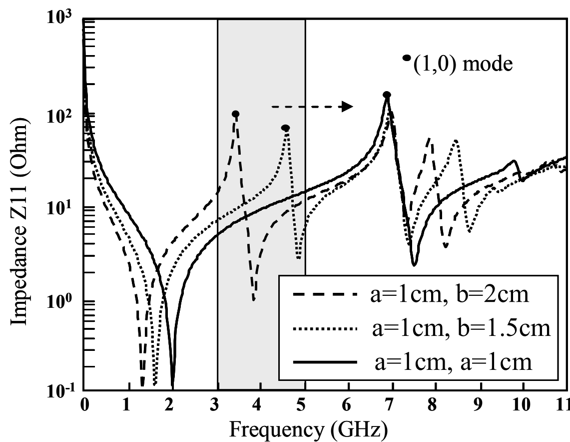
D. Optimized Plane Size for Avoding Resonance

Two planes that face each other make plane resonance according to equation (7) [9] and the impedance (Z_{11}) of power distribution network (PDN) at this resonance frequency becomes very large. Due to this high impedance, a large power/ground noise called as simultaneous switching noise (SSN) will be generated significantly. Moreover, if signal go through these planes using via, this generated noise will be coupled to the signal [10]. This means that the plane size is decisive to degrade or improve system performance. In our research, to avoid the first resonance frequency within target frequency, pre-simulation is performed in advance as shown in Figure 7 (a). From 3D simulation, we can obtain a small and suitable size about 10mm by 10mm. In this case, the first resonance frequency is about 7GHz which is larger than 5GHz. If any edge is larger than 10mm, the first resonance frequency occurred below 5GHz as shown in Figure 7 (b).

$$f_{mn} = \frac{c}{2\pi\sqrt{\varepsilon_r}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \quad (7)$$



(a)

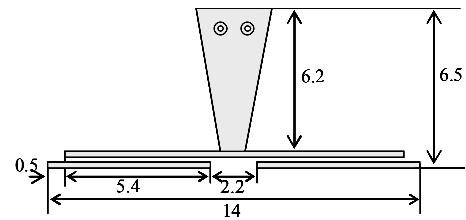


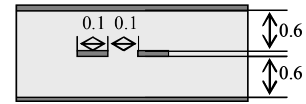
(b)

Figure 7 (a) Power and ground plane has a rectangular shape for UWB package. (b) The first resonance point is dependent of the plane size.

E. Embedded Band-pass Filter in Package

To make UWB transceiver SiP, it is needed to insert embedded passive band-pass filter into a small package. As explained previous chapter, band-pass filter plays an important role to generate UWB signal. While band-pass filter should have pass-band region between 3.1GHz and 5.1GHz, this broad bandwidth feature has a limitation in implementation on chip. To solve above problem, a passive coupled line filter with stub [5] in package is used to shape the impulse signal from the transmitter as shown in Figure 8 (a). Total dimension is about 14mm by 6.5mm and signal feeding line is a strip type which can be inserted easily between planes.

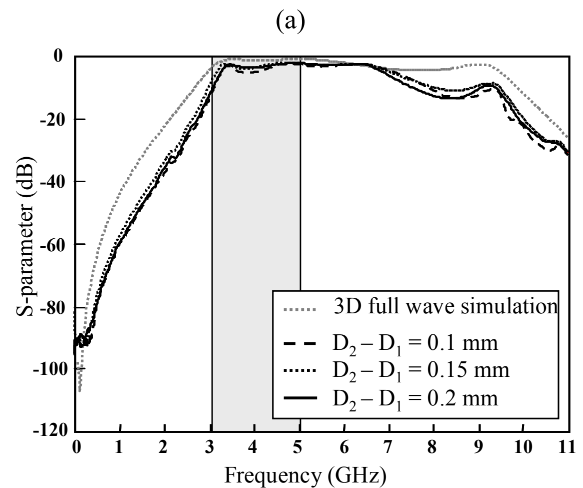




Cross section view.

(Unit : mm)

(a)



(b)

Figure 8 (a) Band-pass filter consists of two coupled line and short stub. (b) A simulated and measured S-parameter show that the pass-band region is from 3.1GHz to 5GHz.

The gray dot line in Figure 8 (b) shows simulation result using CST MWS. The insertion loss within pass-band region is about -1dB and bandwidth is from 3GHz to 7GHz. Moreover, the insertion loss in stop-band region is less than -30dB at 1.6GHz. However, due to via at the end of filter, the signal propagation capability within pass-band region will be degraded. The impedance mismatching is a main reason that reduces the filter performance. Therefore, via clearance is controlled to minimize mismatching between via and filter. The black dot, dash and solid line in Figure 8 (b) shows a simulation result changing via clearance. Therefore, we have obtained the optimized size about 0.2mm of via clearance at embedded filter.

F. *Fabricated UWB Transceiver Package*

Proposed transceiver package is ball grid array (BGA) type and consists of five layers whose stack-up is signal-ground-power-ground-signal as shown in Figure 9 (a). Transmitter and receiver circuit is placed on top layer using wire-bonding. Two chips share the same ground planes, the second and forth layer, to guarantee the return current path. Band-pass filter is embedded in third layer. Second and forth ground plane are reference planes for strip line of band-pass filter's feeding line. Furthermore, power plane for transmitter and receiver is separated to prevent noise transmission. On the bottom layer, there are 42 ball pads for a soldering with test vehicle. Whole dimension is 25mm by 10mm which is much less than 100 won coin as shown in Figure 9 (b).

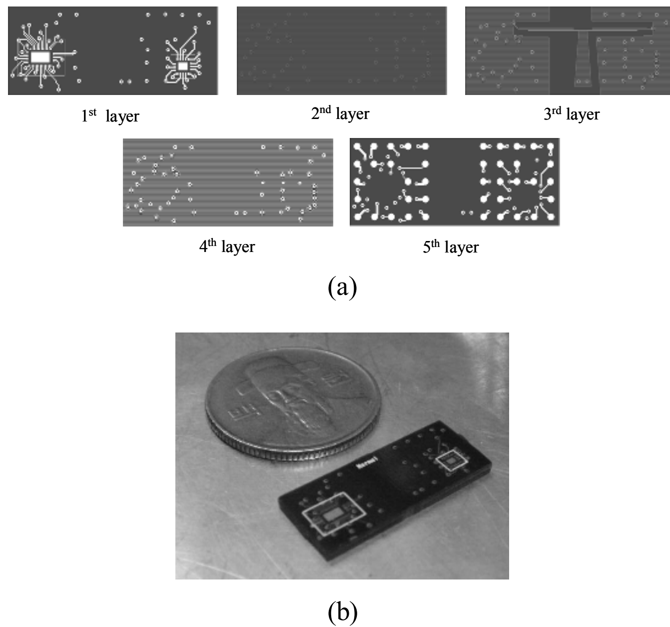


Figure 9 (a) The layout of UWB package for each layer (b) The fabricated UWB package is less than 100 won coin.

IV. EXPERIMENTAL VERIFICATION

The experimental measurement is performed to verify the designed UWB transceiver SiP. First of all, the transmitter is verified with time domain measurement of UWB signal. To do this, the impulse signal from transmitter circuit is measured directly in advance using real time oscilloscope as shown in Figure 10. The impulse signal has 77ps of rising time and 67ps of falling time which include many high frequency components. Peak-to-peak voltage of the impulse signal is about 1.073V. This impulse signal goes to the band-pass filter in a package. After band-pass filter, UWB signal is generated as shown in Figure 11. This UWB signal has about 450mV of amplitude and 1.4ns of pulse duration which is less than 2ns of UWB specification.

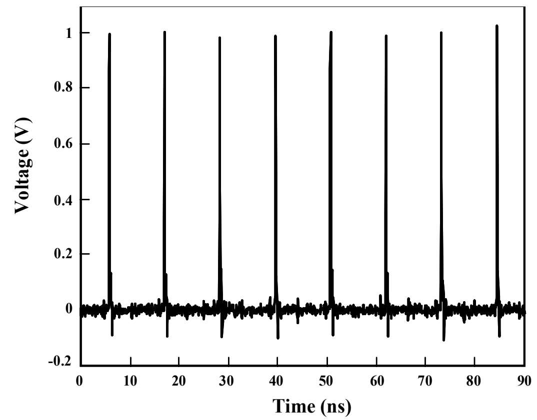


Figure 10 The measurement result of the impulse signal from transmitter circuit

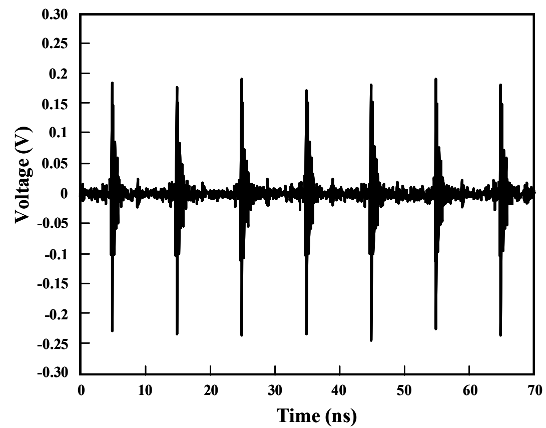


Figure 11 The UWB signal shape from band-pass filter

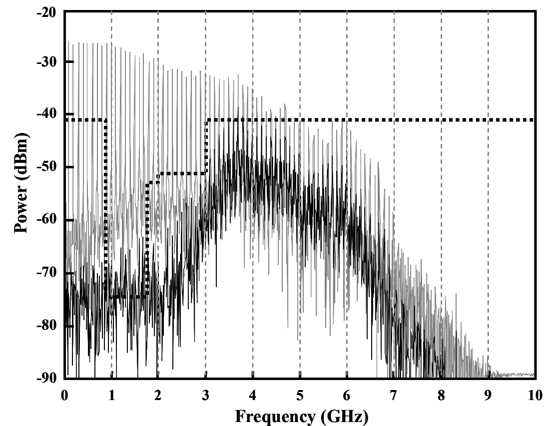


Figure 12 The impulse signal has many frequency components from 100MHz to over 10GHz while UWB signal mainly has from 3.1GHz to 5.1GHz.

The analysis of UWB signal should be done to know whether this signal satisfy UWB regulation mask or not. Figure 12 shows frequency components of the impulse signal and UWB signal in frequency domain. The black dot line represents a regulation mask at indoor system. The gray line of the impulse signal has many frequency components from 100MHz to over 10GHz. After band-pass filter, many other

frequency components except target frequency range are diminished. Hence, generated UWB signal can be used in wireless network system.

The receiver system is verified using real time oscilloscope to see recovered digital data from UWB signal. Broad band antenna is used to radiate or receive UWB signal. Figure 13 shows measured data from receiver system. The detectible range is about 1.35m which is longer than previous research. It is confirmed that UWB receiver system operates correctly.

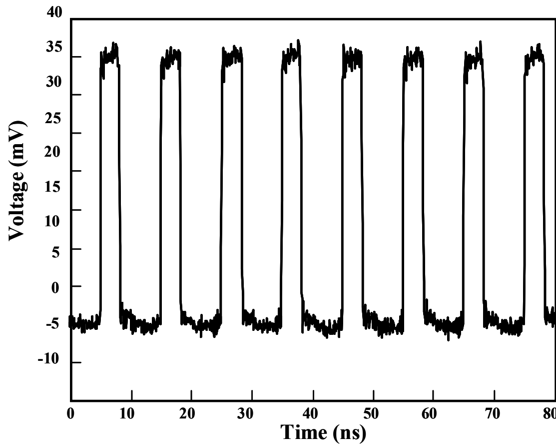


Figure 13 The graph shows recovered data signal when data patter is "11111111"

V. CONCLUSION

UWB transceiver SiP has been designed and manufactured. When designing a package, various factors are considered such as pad size, output load modeling, plane size and embedded band-pass filter in order to increase the system performance. We have verified UWB transceiver SiP by measurement in time domain. The fine UWB signal depending on data is generated successfully and data signal is successfully recovered in the designed system as well.

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