IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received November 29, 2019, accepted December 21, 2019, date of publication December 30, 2019,
date of current version January 8, 2020.

Digital Object Identifier 10.1109/ACCESS.2019.2962905

Design of Wideband Microstrip to SICL Transition for Millimeter-Wave Applications

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This work was supported by the INSPIRE Faculty Award, Department of Science and Technology (DST), Government of India, under Grant DST/INSPIRE/04/2016/001549.

ABSTRACT In this communication, the design and working principle of a wideband microstrip to substrate integrated coaxial line (SICL) planar transition for millimeter-wave applications is presented. In the proposed work, along with tapering of microstrip line, two triangular slots in the top ground plane are utilised to compensate for the discontinuity arising at the microstrip-SICL junction & minimize reflections over a wide bandwidth. To confirm the theoretical claims, the proposed microstrip to SICL transition is fabricated using standard multilayer PCB process. The measured results of the prototype indicate return loss better than 14 dB with a maximum insertion loss of 1.78 dB for DC to 40 GHz band (19 dB bandwidth up to 20 GHz with insertion loss less than 0.71 dB). The modeling of proposed transition is presented & versatility of the design is illustrated for different dielectric constant & thickness. Effortless integration of SICL with the widely used microstrip transmission line simplifies the feeding process of SICL based broadband antennas & microwave circuits.

INDEX TERMS Millimeter-wave, planar, substrate integrated coaxial line (SICL), wideband transition.

I. INTRODUCTION

The fifth generation (5G) communication exhibits potential to support diverse services owing to its high data rate. For enhanced functionality of the system, hybrid integration of various transmission lines is often necessary [1]. The stringent requirements of 5G would be testing the designers to produce planar components to accommodate its FR-1 (Sub-6 GHz) & FR-2 (28 GHz) band simultaneously [2]. Novel technologies in planar form have emerged for efficient design of microwave/millimeter-wave circuits [3]–[5]. In [3], planar counterpart of waveguide has been extensively utilized to develop various microwave circuits and antennas. A novel methodology to interconnect substrate integrated suspended line with coplanar waveguide is shown in [4]. A newer technology to synthesize the traditional coaxial line in planar form was devised in [5], namely substrate integrate coaxial line (SICL). This structure also referred as fenced stripline [7], [8] supports low loss at millimeter-wave frequency and prohibits propagation of undesired parallel plate mode. The wideband TEM mode of wave propagation in SICL can simultaneously support the operating bands of upcoming 5G communication and also provide backward compatibility to 3G/4G. In [9] and [10], a coaxial to SICL transition has been reported. A novel rectangular waveguide to SICL transition is proposed in [11] to act as a four way power divider to feed a circularly polarized antenna array in E-band. One of the most popular transition currently used in SICL technology is the coplanar waveguide (CPW) transition [12], [13] in which a plated via connects the central conductor of SICL to signal line of CPW. In [12], SICL to CPW transition fabricated in low temperature co-fired ceramic (LTCC) technology is shown to operate up to 40 GHz with insertion loss less than 2 dB in the entire 10 dB return loss bandwidth. A SICL to conductor backed CPW transition (CBCPW) [13] devised in standard PCB technology demonstrated better than 10 dB return loss & 1.72 dB insertion loss in DC-13 GHz band. Design and working of an SIW to SICL transition has been verified in [14] for 6.7 to 7.42 GHz band. In [15], integration of substrate integrated waveguide (SIW) filter with a non-resonant SICL node is experimentally validated. The usage of CBCPW to SICL transition is discouraged for ultra-thin substrates as the width

The associate editor coordinating the review of this manuscript and approving it for publication was Vittorio Camarchia.

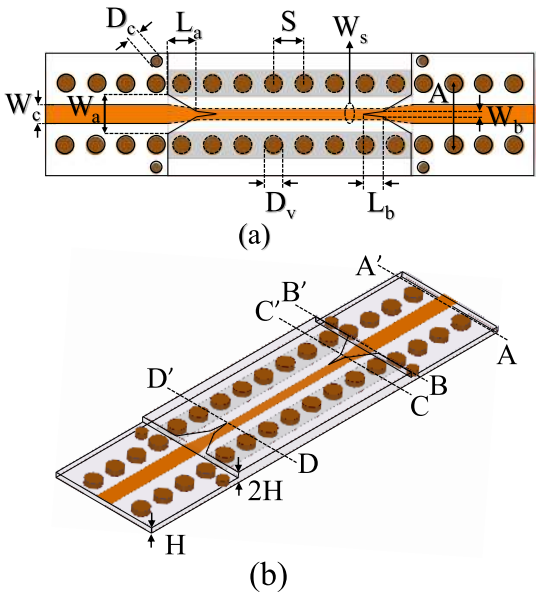

FIGURE 1. Geometrical model of the proposed microstrip to SICL transition (a) Top-view (b) Isometric view.

of the CBCPW signal line is considerably small & soldering the coax connector becomes challenging without shorting it to the adjacent ground plane.

In this work, a back to back microstrip to SICL transition is developed to operate till 40 GHz with return loss better 14 dB and insertion loss less than 1.78 dB (19 dB bandwidth up to 20 GHz with insertion loss less than 0.71 dB). The proposed transition simplifies the feeding process of SICL section by eliminating need for vertical transitioning blind via. The proposed tapered slot in the top ground plane facilitates wideband transition from microstrip to SICL without any abrupt phase variation. Integration of SICL with the ubiquitous microstrip transmission line will help in exploiting the advantages of SICL.

II. DESIGN OF MICROSTRIP TO SICL TRANSITION

The 50 Ω SICL section is fabricated by sandwiching a conducting strip between a pair of low loss Taconic TLY-5 ($\epsilon_r = 2.2, \tan\delta = 0.0009$) substrate each of thickness $H = 0.25$ mm. This configuration is bounded by two rows of metallic vias connecting the top and bottom plane with a metallic sheet enforced through the vias to enhance the coaxial nature of SICL section as shown in Fig. 1(a). The characteristic impedance of the SICL is a function of substrate thickness to width of inner conductor ($2H/W_s$) ratio. Here the substrate thickness is fixed and width of SICL inner conductor is optimized to obtain 50 Ω characteristic impedance. The diameter of via $D_v = 0.75$mm and pitch between them $S = 1.25$mm are selected so as to minimize electromagnetic wave leakage from the designed SICL section. The parameters S & D_v also play a crucial role in determining the TEM mode bandwidth of SICL. The TEM mode propagation is ensured by controlling the operating frequency of next higher order

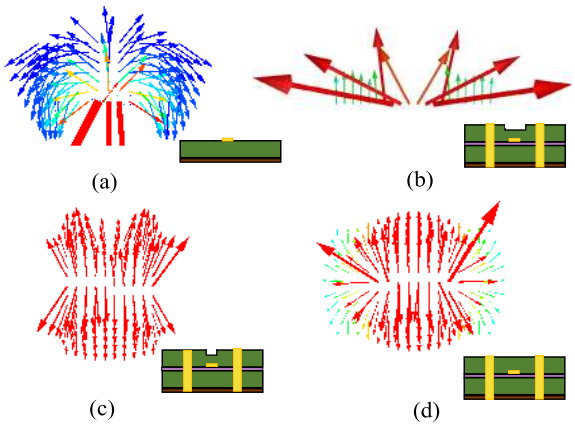

FIGURE 2. Vector E-field across planes (a) AA′ (b) BB′ (c) CC′ and (d) DD′.

mode TE_{10} which is shown below $f_{TE_{10}}$ [5].

$$f_{TE_{10}} = \frac{c}{2\sqrt{\varepsilon_r}}\left(A - \frac{D^2}{0.95S}\right)^{-1} \quad (1)$$

In the designed SICL line, distance between the parallel delimiting via rows A is chosen as 2.5mm in order to keep the higher order mode near to 50 GHz.

A. WIDEBAND MECHANISM OF THE PROPOSED MICROSTRIP TO SICL TRANSITION

At the microstrip−SICL juction two triangular slots of length L_a and L_b with widths W_a and W_b respectively are etched on the top ground plane as shown in Fig. 1(a) and 1(b). These two triangular slots of unequal length and width aid in mitigating abrupt variation in electric field caused at the junction of transition. The E-field along cross section AA' of microstrip line is shown in Fig. 2(a). As expected there exists E-field from top microstrip line to bottom ground plane along with fringing fields. The proposed transition is devised by connecting a SICL section to a substrate truncated microstrip line. Due to the introduction of top conductor of SICL at the junction of transition, horizontal component of E-field ceases to exist, therefore a mismatch in field configuration before and after the transition degrades the performance. To mitigate that, a small slot in the top conductor is introduced which helps to orient the field from middle layer to either half of the top conductor as shown in Fig. 2(b). As the slot is gradually tapered inwards, it is observed in Fig. 2(c) the E-field smoothly transitions in to a radially outward configuration. Finally, electric field with radially outward orientation similar to conventional coaxial line is observed across the cross-section DD' of second triangular slot in Fig. 2(d). Further, the microstrip line is gradually tapered inwards over length L_a in a linear fashion to facilitate broadband matching. The tapering of the line along with slots on the top plane of microstrip-SICL junction compensates for any discontinuity arised and minimizes reflections over a wide bandwidth. The copper plated via holes along the microstrip line prevent excitation of spurious parallel plate waveguide mode between

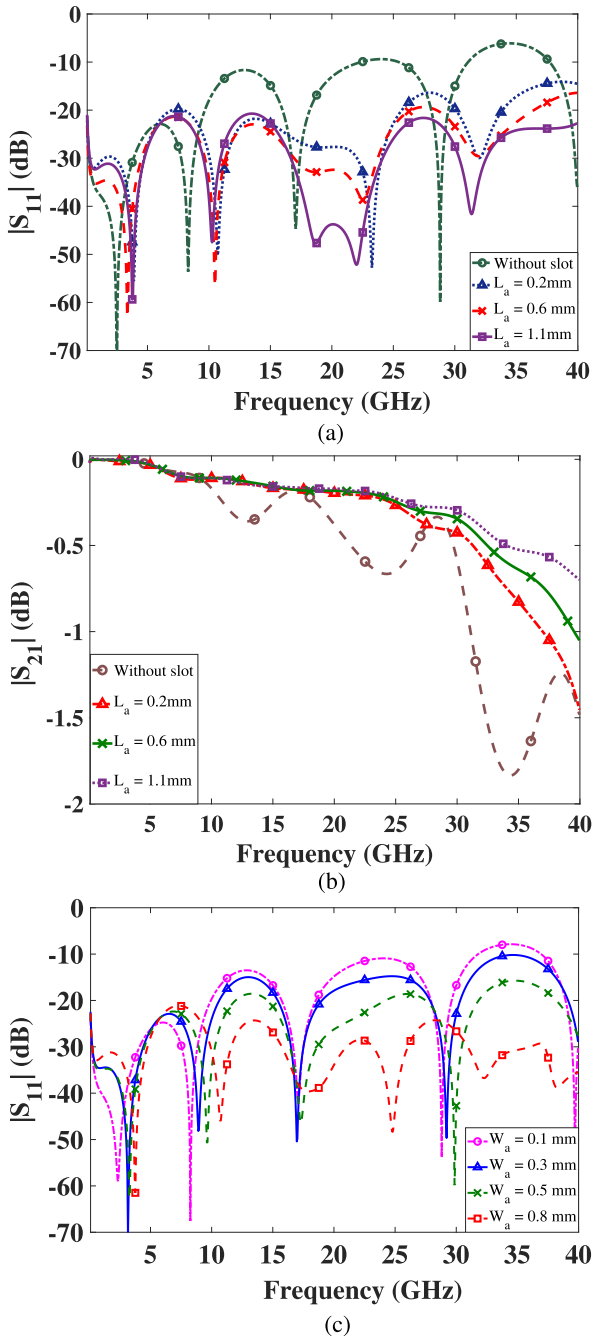

FIGURE 3. Study on performance of proposed microstrip to SICL transition with: Variation in slot length L_a (a) Reflection coefficient (b) Insertion loss and, (c) Slot width W_a.

the ground and top conducting line. Further, metallic vias of diameter $D_c = 0.5$mm are placed at the microstrip and SICL boundary to mitigate wave leakage. The performance of microstrip to SICL transition with variation of slot length L_a is studied in Fig 3(a) and (b). The total length of slot in top conductor is kept approximately at $\lambda_g/4$. It is observed that the return loss and insertion loss at higher frequencies improve significantly with inclusion of proposed slot in top ground plane. In Fig. 3(c), the performance of proposed transition with variation in width of slot in top conductor is

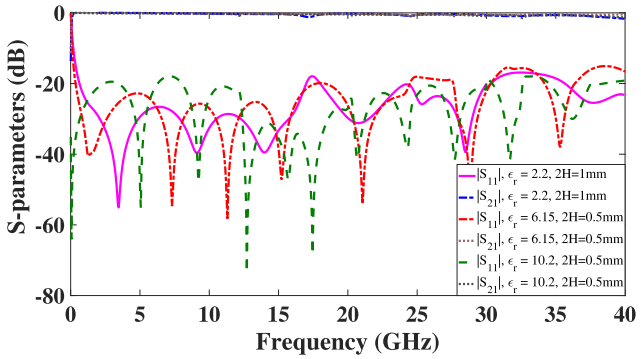

FIGURE 4. Full-wave simulated S-parameters of proposed microstrip to SICL transition with change in dielectric constant and thickness.

TABLE 1. Dimensions of the proposed 50 Ω microstrip to SICL transiton.

	L_a (mm)	L_b (mm)	W_a (mm)	W_b (mm)	W_c (mm)	W_s (mm)
$\epsilon_r = 2.2^*$ 2H = 0.5mm	1.2	0.8	0.8	0.1	0.75	0.43
$\epsilon_r = 6.15$ 2H = 0.5mm	1.4	0.4	1	0.14	0.36	0.18
$\epsilon_r = 10.2$ 2H = 0.5mm	0.4	0.8	0.42	0.27	0.22	0.12
$\epsilon_r = 2.2$ 2H = 1.0mm	1.8	1.2	1.1	0.3	1.58	0.9

*: Fabricated prototype

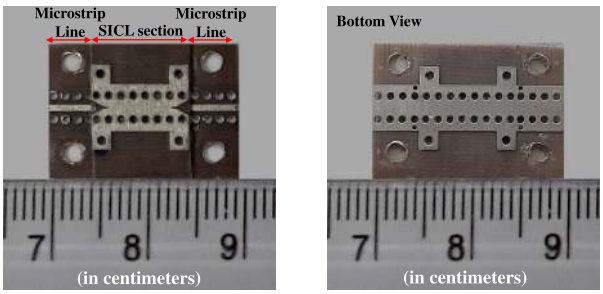

FIGURE 5. Photograph of the proposed wideband microstrip to SICL transition (a) Top View (b) Bottom view.

investigated. The slot opening from the center of microstrip line ($W_a/2$) is estimated to $\lambda_g/20$ ($\pm 0.03\lambda_g$) for the electric field to progressively adapt to SICL based TEM configuration along the tapered section. The robustness of the proposed transition is confirmed by modeling it for different dielectric constant and thickness. The simulated results in Fig. 4 indicate a return loss of at least 18 dB in the operating band 0.51 GHz to 40 GHz with insertion loss less than 1.4 dB. Dimensions of the proposed transition for different dielectric constant and thickness is listed in Table 1.

III. RESULTS AND DISCUSSION

The proposed back to back microstrip to SICL transition is tested with the help of a K-Type (2.4mm) end-launcher using Agilent E8361C PNA. Photograph of the fabricated prototype is depicted in Fig. 5 and the dimensions of proposed transition

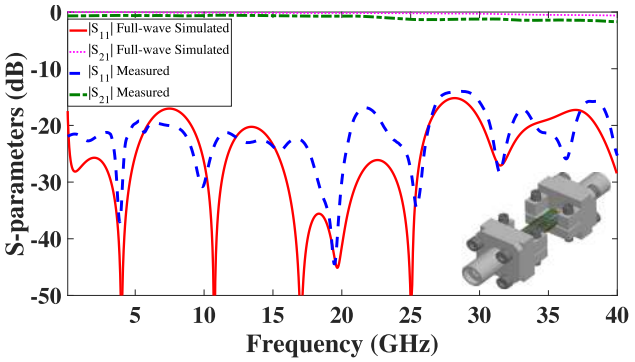

FIGURE 6. Simulated and measured S-parameters of the proposed wideband microstrip to SICL transition.

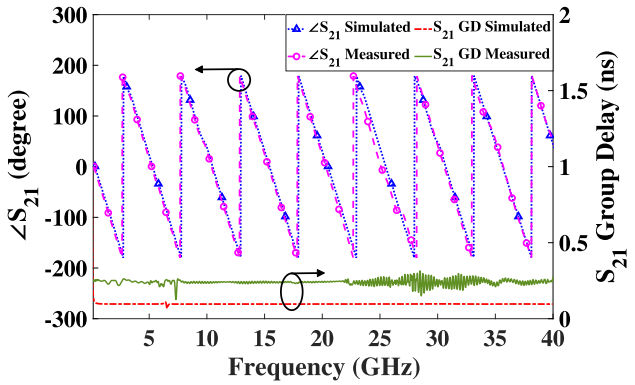

FIGURE 7. Measured phase and group delay (GD) characteristics of the proposed microstrip to SICL transition.

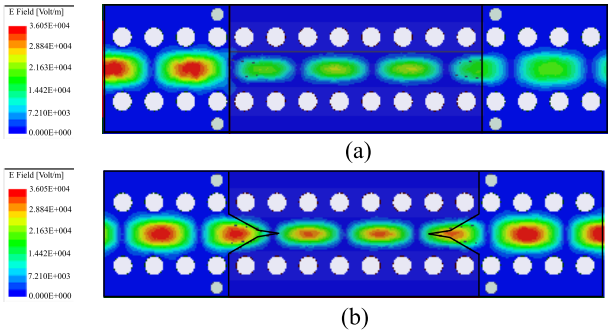

FIGURE 8. Magnitude of electric field in bottom ground plane at 35 GHz (a) Without proposed slots etched in top ground (b) With proposed slots etched in top ground.

are mentioned in Table 1. The back to back microstrip to SICL transition is simulated using Ansys HFSS and the simulation model is depicted in inset of Fig. 6. The measured results demonstrate wideband impedance matching with better than 14 dB return loss and less than 1.78 dB insertion loss up to 40 GHz (19 dB bandwidth up to 20 GHz with insertion loss less than 0.71 dB) as illustrated in Fig. 6. It is to be noted the measured insertion loss takes in to account the two K-type connectors used to facilitate the testing of the proposed prototype. The discrepancy between measured and simulated

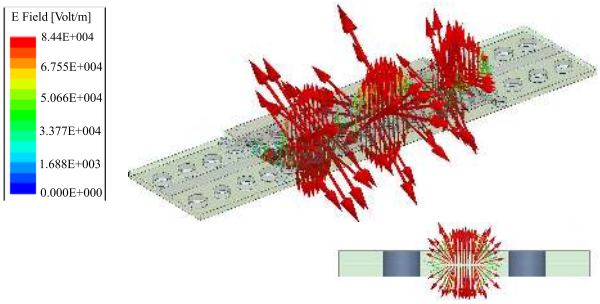

FIGURE 9. Vector electric field plot along the length of SICL section of the proposed back to back transition at 28 GHz.

TABLE 2. Comparison of the proposed microstrip to SICL transition with previously reported works.

Ref.	Technique	Frequency Range	Max. $\|S_{21}\|$ (dB)	Blind Via
[9]	SICL to Coaxial	DC to 32.7 GHz	$\leq$0.1*	Yes
[10]	SICL to Coaxial	12 to 14 GHz	N.M	Yes
[11]	SICL to Waveguide	71 to 78 GHz	N.M	Yes
[12]	SICL to CPW	DC to 40 GHz	$\leq$2	Yes
[13]	SICL to CBCPW	DC to 13 GHz	$\leq$1.72	Yes
[14]	SICL to SIW	6.7 to 7.42 GHz	$\leq$1.4	Yes
This work	SICL to Microstrip	DC to 40 GHz	$\leq$0.71 dB up to 20 GHz $\leq$1.78 dB up to 40 GHz	No

*: Simulated Data, NM: Not Mentioned

results can be attributed to fabrication tolerances and air gap in bonding the two substrate layers. From Fig. 7 it is observed the proposed slot in top conductor does not cause any abrupt variation in phase and supports wave propagation with a low peak to peak group delay variation of 0.16 ns. The variation of E-field at microstrip-SICL junction at higher frequencies can be analyzed through Fig. 8. The magnitude of electric field without slots on the top ground plane as depicted in Fig. 8(a) causes reflections due to abrupt variation of impedance at microstrip-SICL junction. Whereas, the proposed slot in top ground plane as portrayed in Fig. 8(b) helps to transform the E-field uniformly from quasi-TEM mode of microstrip to broadband TEM mode of SICL minimizing mismatch between these two transmission lines. Further, in Fig. 9 the similarity of the radially outward electric field vector in the SICL section with its non-planar counterpart affirms coaxial nature of SICL in planar form. The performance of designed back to back microstrip to SICL transition is compared with previously reported SICL transitions in Table 2.

IV. CONCLUSION

The design and analysis of wideband microstrip to SICL transition is presented in this work. In the proposed transition, a SICL section is fed by a substrate truncated microstrip line. The effect of tapered line along with double triangular etched slot in top ground plane to reduce reflection at microstrip - SICL junction is investigated. A wideband 14 dB

impedance bandwidth from DC to 40 GHz is achieved with insertion loss less than 1.78 dB (19 dB bandwidth up to 20 GHz with insertion loss better than 0.71 dB) using the proposed methodology. Further, the adaptability of transition for different dielectric constant and thickness is evaluated. Utilization of substrate truncated microstrip line eliminates the need of blind via thereby reducing the fabrication complexity. The superior integration capability of planar microstrip line with electromagnetically robust broadband monomode TEM operating SICL promotes the utilization of SICL for various practical applications.

ACKNOWLEDGMENT

The authors would like to thank Prof. A. R. Harish and Prof. M. J. Akhtar of IIT Kanpur, India, for providing their measurement facilities.

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